

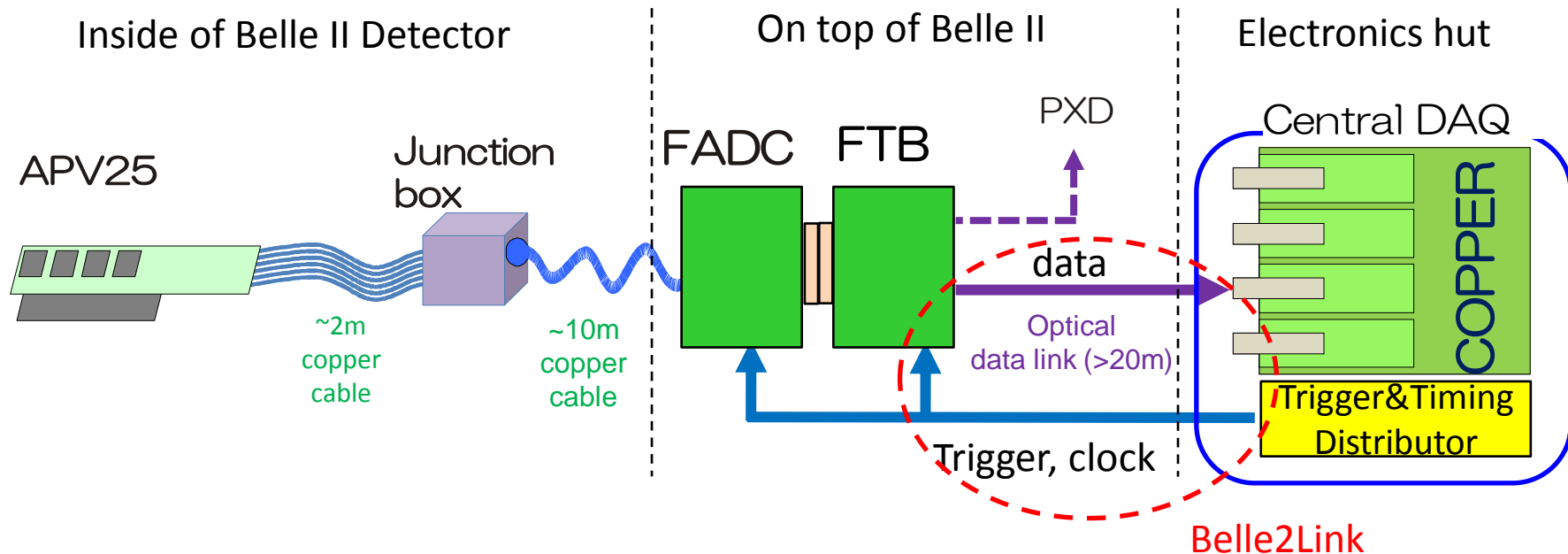
FTB Status and Outlook

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Apr. 9, 2013

Telescope test Gemba Meeting

SVD DAQ System



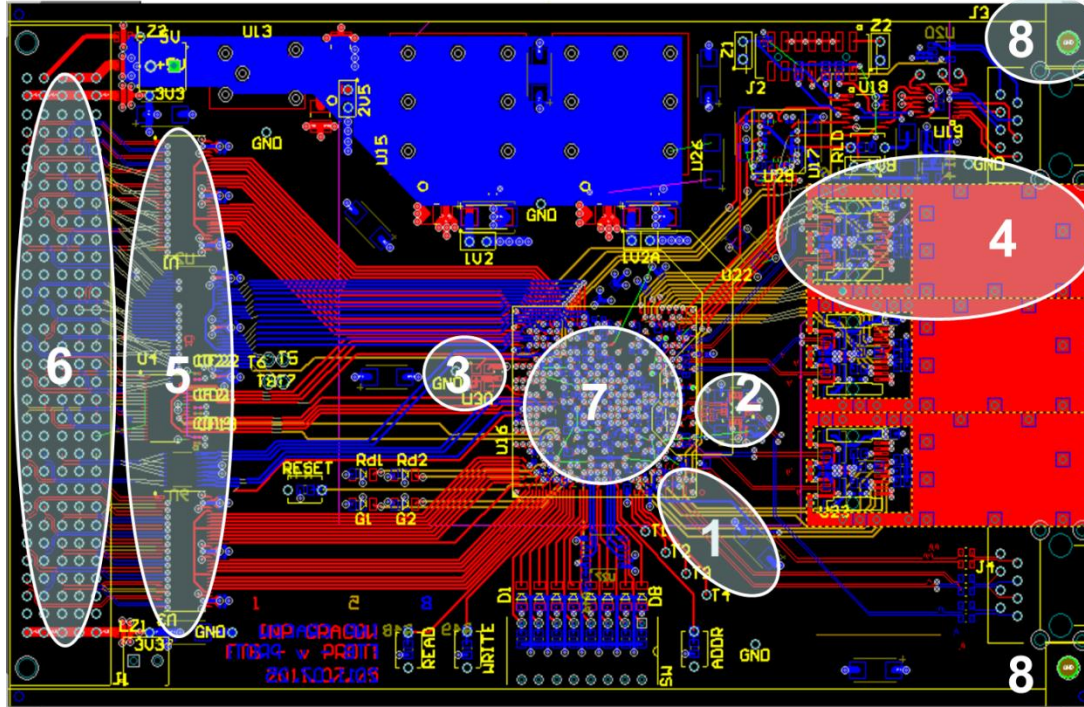
Belle2link test have been done with the FTB ver.1 prototype board

- Dummy data transferred via Belle2link to copper
- Using Trigger and clock data from FTSW

Several improvement + connection to the FADC → Ver.2

- Improved clock distribution etc.

FTB Prototype Ver.2



Changes from ver.1

1. Output to TTD moved to Bank2
2. 127MHz Oscillator + DS25CP152 chip.
3. TTD Clk to GTP RefClk pins.
4. 32MHz Oscillator on board
5. Third OptoLink
6. Different drivers
7. Changed pin-out
8. XC6SLX75T -> XC6SLX100T
9. Module equipped with Front Plate

5 modules are being produced by Wacek (Krakow)

1 module to KEK

1 module to PXD

2 modules remain in Krakow (will be used for DESY test)

1 spare module

FTB Prototype ver.2 production

- PCB boards are ready
- Parts from one of the Distributors are not delivered yet.
→ will arrive by this Thursday
- Paper of the official order by the administration ready in this week
- Parts and assembly work documents will be sent to the company by the end of this week
 - Assembly work will take ~10 working days

→ Assembly will finish ~end of Apr.

(1 month delay from the original plan (March))

FTB Firmware

- Being prepared for FTB ver.2
- Need to fix “Common interface” between subdetector core and Belle2link core → need to discuss in Belle2link group
- More test of the Belle2link on FTB
 - Only confirmed with simple dummy data with single trigger
 - Need to confirm realistic data size and trigger rate up to ~30MB/s/COPPER (not in DESY test but in BelleII condition)

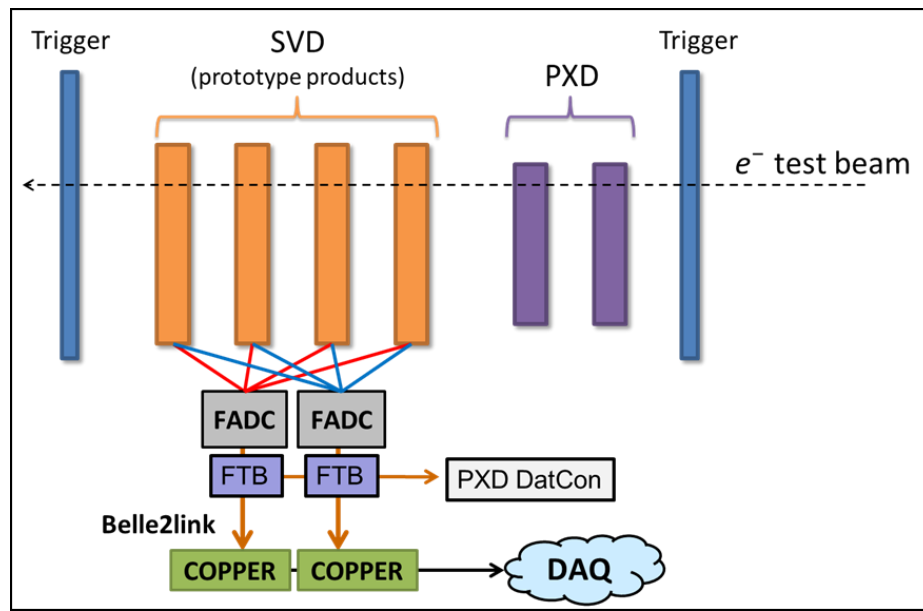
	#ch	occ [%]	#link	/link [MB/s]	#CPR	ch sz [B]	ev sz [kB]	total [MB/s]	/CPR [MB/s]
SVD	223744	1.7(5.5)	48	8.9(33.8)	48	4	14.9	428	8.9(33.8)

avg. occ. larger occ. in L3

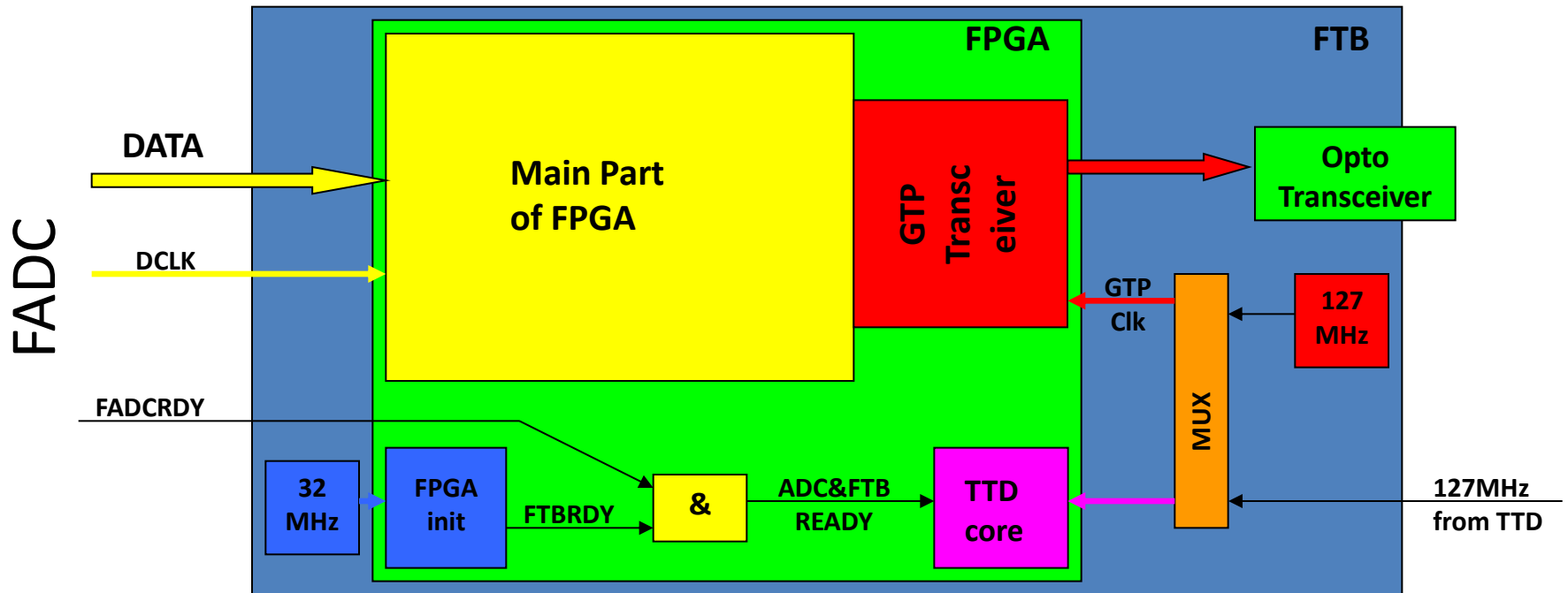
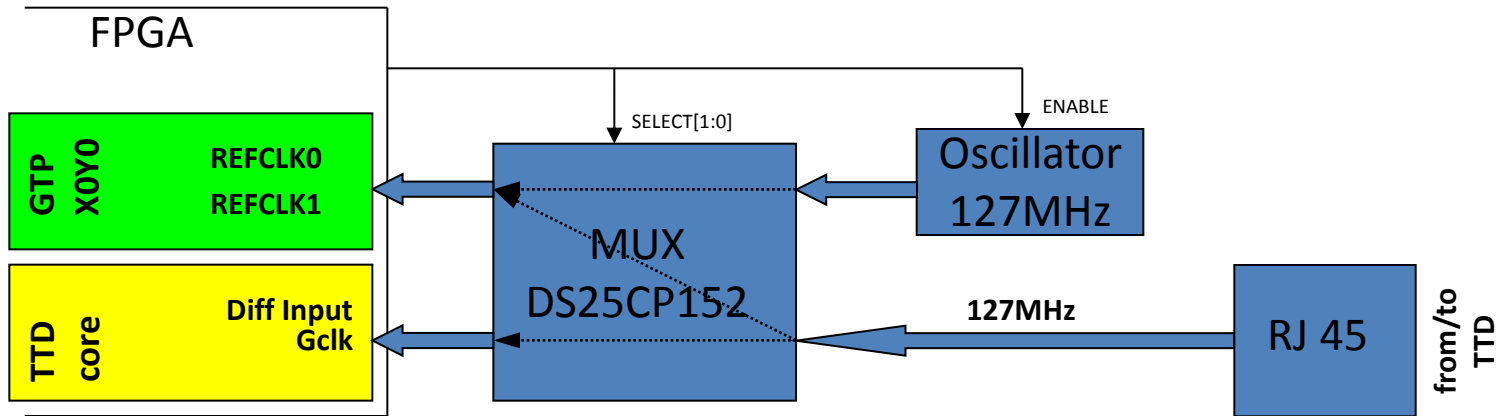
The diagram shows two annotations below the table. 'avg. occ.' has a blue arrow pointing to the 'occ' column (1.7(5.5)) and a red arrow pointing to the '/link' column (8.9(33.8)). 'larger occ. in L3' has a red arrow pointing to the '/link' column (8.9(33.8)).

2013 Milestones

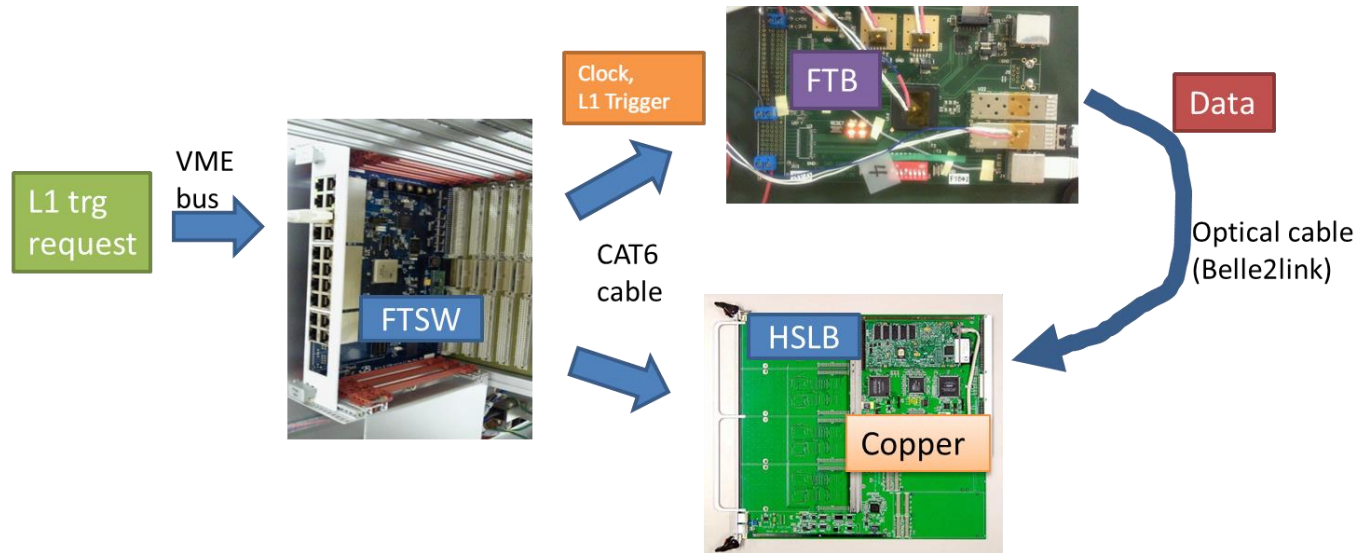
- Prototype FADC and FTB hardware and firmware preparation :
release by 2013 April → May ?
→ FTB ver.2 - Copper connection test @ KEK
- Readout chain communication test : by 2013 June → to be discussed
→ FADC – FTB – copper
– DatCon @ Vienna
- System test incl. central DAQ and PXD
 - Dry run test @ KEK: FTB-COPPER-DAQ
 - Full chain test @ DESY before telescope test: SVD ladder - APV - FADC - FTB – Copper



TTD and GTP Clock distribution. Clock Domains.



FTB+Belle2link Performance Test



Check the data rate (data size , trigger rate) is enough for SVD

SVD data size:

Avg data size/event/link ~ 320 bytes (occ.=1.7%, 14.9KB/event)

Higher occ. for L3 ~ 1200 bytes (x3.5)

Maximum trigger rate is 30kHz

Performance Test Preliminary result

- Trigger sent from FTSW by request via VME bus
- Dummy data sent from FTB via Belle2link
- The received data COPPER is checked by CPU on COPPER
 - Data checked on memory. No recording to disk.
- Result
 - 256 bytes @ 50 kHz (fixed interval) : No error for 500×10^6 events (100sec)
 - 1024 byte a @ 30 kHz
 - Error detected... Data received COPPER does not match with the data sent from FTB
 - Need detailed check
 - Validity and speed of my data checker on COPPER
 - my FTB test firmware performance
 - Next trigger may come before my dummy data generator finishes? etc.
 - Belle2link core status
 - Status of Belle2link core's FIFO, intrinsic data transfer performance