TTD plan for telescope test

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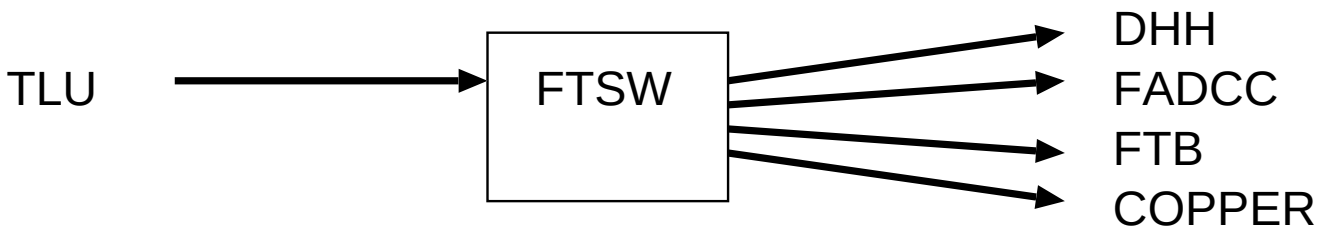
現場 (Gemba) meeting

at DESY

Task of TT at telescope-test

- **Receive trigger from EUDET / TLU**
- **Trigger-Timing (TT) control of Belle II subsytems**
  - Target: 1x DHH, 1x SVD-FADC-master, ?x SVD-FTB, 1x(?) COPPER
  - Generate self-running 127 MHz system clock from FTSW oscillator
  - Distribute trigger and related info in Belle II TT format
  - Trigger flow control



- **Busy return to EUDET / TLU**
- **Run number / event number / timestamp**

Hardware list

- **Minimum list from KEK**
  - 1x FTSW board (version 3.1, any type)
  - VME CPU
  - CAT7 cables (10m, 5m, 3m, 1m)
- **Shared/optional items**
  - VME crate (4 free 6U slots in COPPER crate?)
  - PC to boot VME CPU (shared with COPPER boot host)
  - Network switch, LAN cables
  - JTAG program cable
  - TT-IO board to accept NIM/LEMO signals
  - Spares (FTSW, VME CPU)

Connection between TLU and FTSW

(based on TLU v0.2c document)

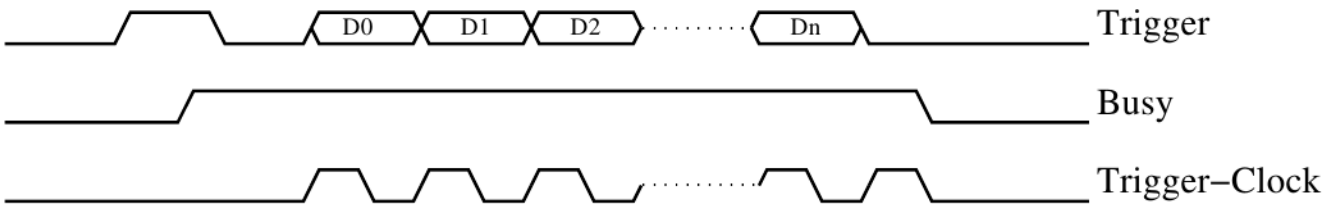
- TLU uses 4-pair LVDS on Ethernet standard RJ-45 pin assignments, **fully compatible with FTSW**
- CAT7 cable ($\leq$15 m?) to be used (shielded cable is needed)
- Pin assignment:
  - **1-2:** data-clock to TLU, **3-6:** busy to TLU,
    5-4: reset from TLU, **7-8:** trigger from TLU
  - polarity of data/busy/trigger is **opposite** of FTSW (no problem)
    polarity of reset is **same** as FTSW
- On FTSW side, **AUX port** will be used
- **System clock:** TLU has no clock input, and FTSW can't use TLU's clock output (40 MHz? 48 MHz?) as the system clock
- By the way, who will be in charge of operating TLU?

Trigger timing from TLU to FTSW

- **Trigger timing** from TLU is **asynchronous** to any clock
- Trigger timing as 31ps RMS-jitter
- FTSW will quantize it to
  - **8ns LSB coarse trigger-timing** (if nobody complains)
  - or to 2ns LSB fine trigger-timing if necessary
- **Time stamp** is attached at TLU in unit of 40/8=5 MHz clock,
  another time stamp is attached at FTSW in unit of 127 MHz clock,
  + 2-bit fine trigger timing info if needed
- FTSW would like to receive TLU clock output for TLU time-stamp
  - **TLU's LVDS LEMO 0B** output connector to RJ-45?
    Easy if such a cable already exists
  - **TLU's TTL LEMO 00** output: Add a LEMO 00 connector on FTSW?
    Easy if 3.3V LVTTL, but need a level-shifter if 5V TTL
- Do we measure the trigger time with a better precision?

Timing signals between TLU and FTSW

- **Busy handshake**
  - FTSW asserts a BUSY signal (dedicated LVDS pair)
  - FTSW drives data-clock to get 16-bit trigger counter



  - 8 MHz Trigger-Clock (127M/16) to be used (has to be ~10 MHz)
  - Minimum deadtime ~2 μs
- **Trigger timing:**
- **Trigger latency** by TLU: 27ns. **Do we need to generate 5 μs latency?**
- **Time stamp:** no good way to synchronize TLU timestamp and FTSW timestamp

Layout and cable connection

- Is 10m cable between FTSW and DHH/FADC/FTB long enough?
  or can it be even shorter (5m)?
- Short (1m or 3m) cable from FTSW to COPPER/HSLB
  (same or neighbour crate)
- Is COPPER / FTSW area accessible during beam?
- COPPER / VME CPU host PC near the crate to connect JTAG cable

FTSW hardware status

- **FTSW 2.1** — **60** boards were produced, **34** are needed
  (∼10 were distributed, + 10x(?) boards for trigger systems)
- **FTSW 3.1** — **89** boards were produced, **95** are needed
- **FTOP** — **12** boards were produced, **12** are needed (no spare)
- **FTOR** — **2** boards were produced, **54** are needed
- **COPPER3 + TT-RX v5** — **190** boards were produced
- **TT-RX v6(?)** for COPPER2(?) — may be needed, R&D item of FY2013
- **Board test**
  - All FTSW 2.1 boards (except for -noVME) were tested at KEK
  - All FTSW 3.1 boards (including -noVME) are being tested at KEK
    (helped by Yonsei students, Cholong Lim and Kyongho Kim)
- **Final production** — **30x** FTSW3.1, **10x** FTOP, **60x** FTOR in FY2013

FTSW firmware development

- β-version protocol to be implemented (discussed in 2012 July B2GM)
- All functions should be there,
  telescope test is to identify the final step to the t_0 version
- **Status:**
  - prototype version hasn't been touched for long time
  - β-version protocol implementation has been suspended for long time
  - firmware development resumed from end-March
  - firmware for board-test was developed (with a 16-page instruction)
  - source-level unification between FTSW2.1 and FTSW3.1
- **Firmware types:**
  - $\sim$10 different firmware types
  - Relevant firmware types: Master and Frontend-emulator

Schedule

- **Dec-Mar 2012-3:** NSM alpha version development
- **Feb-Mar 2013:** FTSW version 3.1 mass production 1
- **Mar 4–14 2013:** B(2)GM PAC KEKFF
- **Mar-Apr 2013:** FTSW module test
- **Mar-Jun 2013:** FTSW beta version firmware development
- **Apr-Jun 2013:** Pocket-DAQ/FTSW/Belle2link test for CDC
- **May-Jul 2012-3:** NSM beta version development
- **anytime 2013:** FTSWx30, FTOPx19, FTORx50 final production
- **Jul 2013:** B(2)GM at VPI
- **Sep? 2013:** CDC beam-test
- **sometime 2013:** Dry run setup at DESY
- **Nov 4–15 2013:** Hadron 2013/B(2)GM
- **Jan 2014:** DESY telescope test

Backup

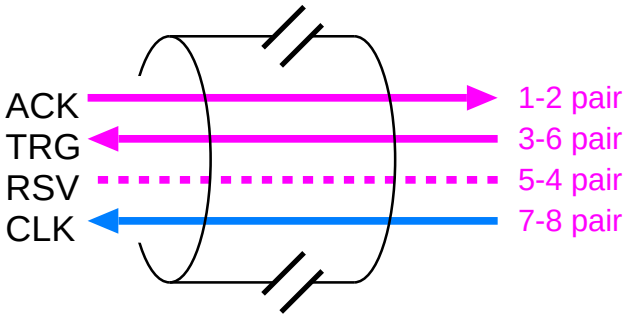
Some History

- **Jun/2011**: FTSWv2.1 was designed and made
- **Aug/2011**: used in BPID test in Nagoya, B2link test in IHEP
- **Oct/2011**: About 60 modules of FTSWv2.1 was produced
- **Feb/2012**: All 60 modules of FTSWv2.1 were tested
  (fine tuning is needed to keep the clock jitter to a tolerable level)
- **Nov/2012**: While planning for making more FTSWv2.1, decided to make version 3 to separate the clock driver with a dedicated Spartan 3AN
- **Jan/2012**: FTSWv3.0 test production (3 boards)
- **Feb/2012**: FTSWv3.1 test production (1 board)
- **Feb/2012**: FTORv1 test production 1 (2 boards)
- **Feb/2012**: FTSWv3.1 mass production 1 (88 boards)

FTSW(v3)-concept

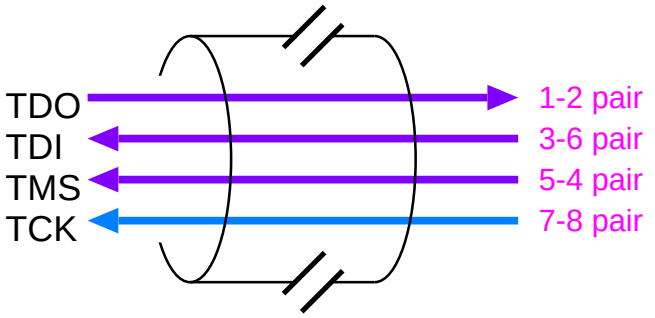
20130121 version

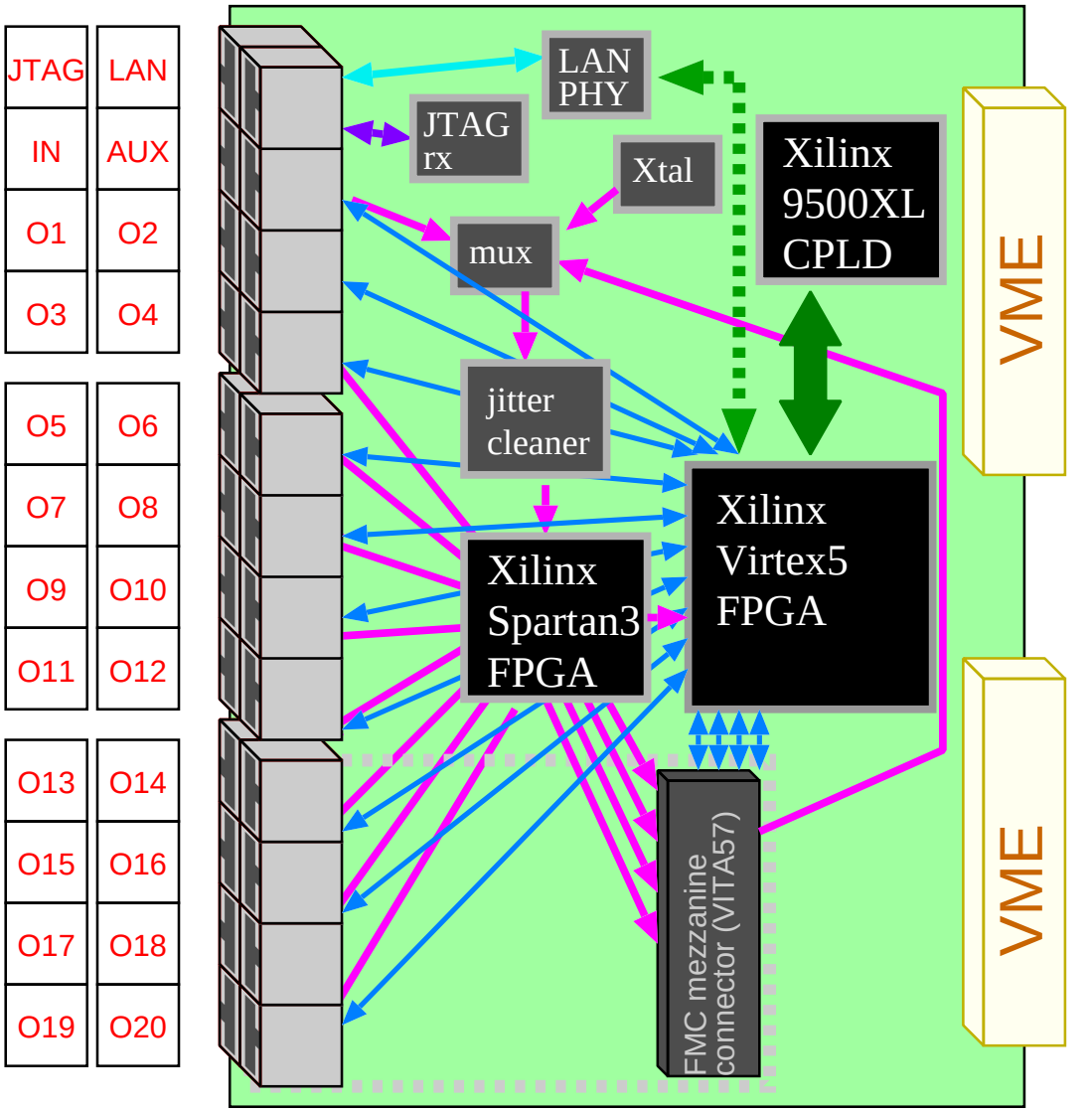
Timing signals over a LAN cable



CLK: 127 MHz (derived from 508 MHz RF clock)
TRG/ACK: serialized, 254 Mbps

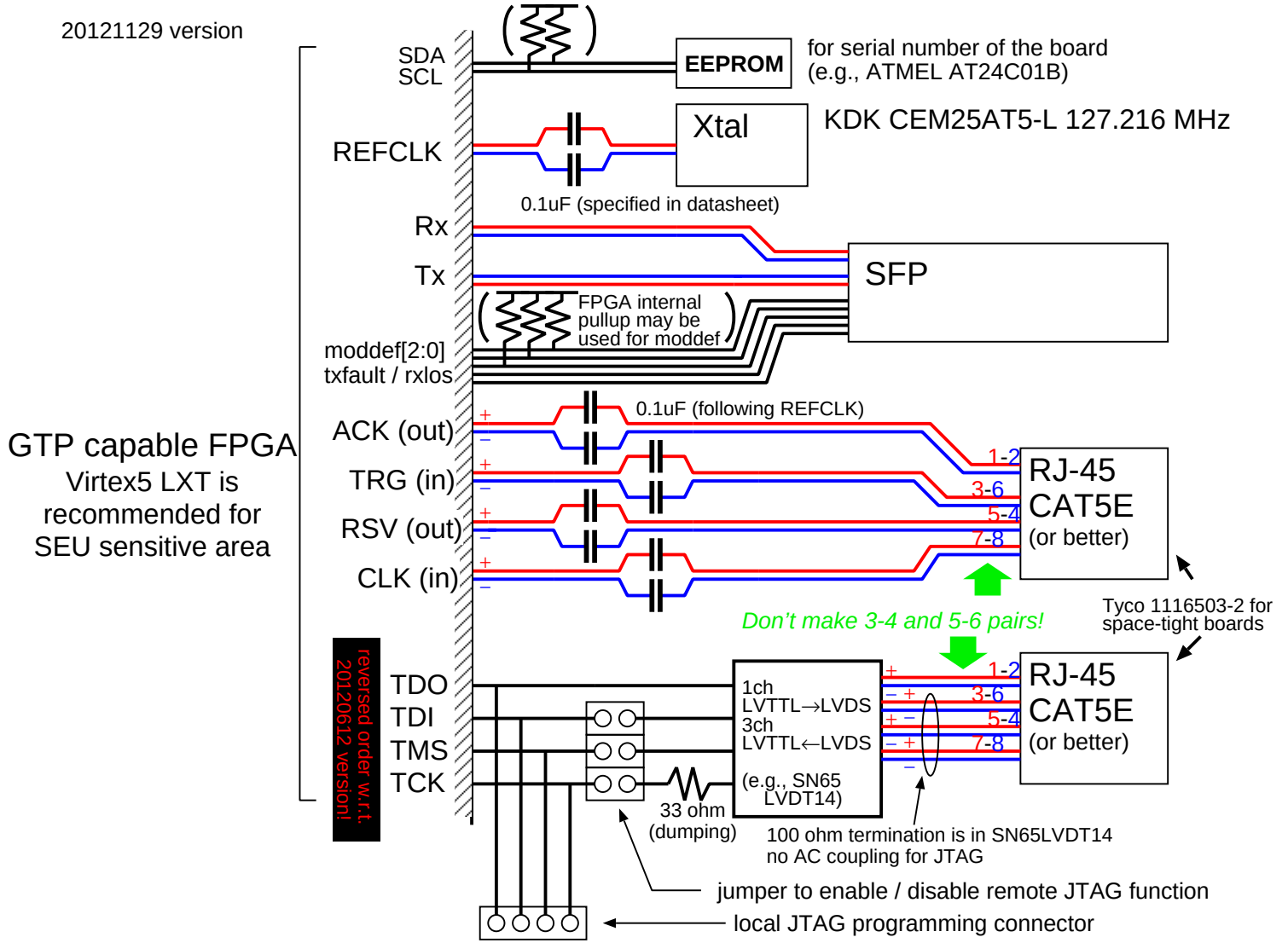
JTAG-on-LVDS over a LAN cable





CLK line and other TT lines are separated, new JTAG ordering

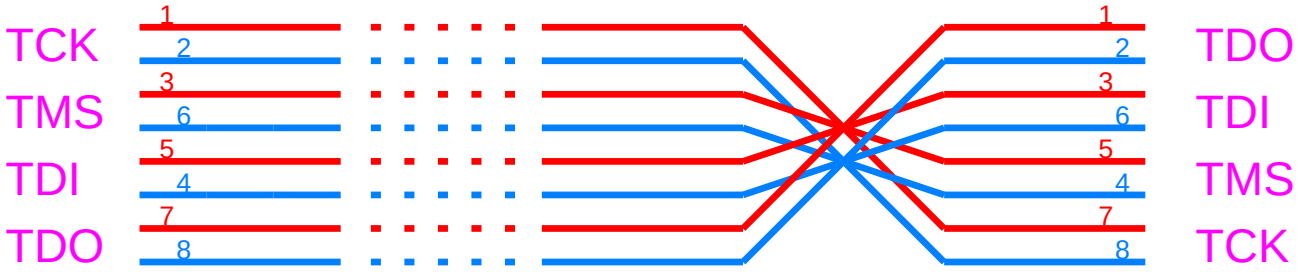
New JTAG cable definition



(TCK,TMS,TDI,TDO) ⇒ (TDO,TDI,TMS,TCK),
to unify the 7-8 pair usage to be LVDS output in FTSW

Boards with old JTAG definition?

- In principle FTSW firmware modification is possible, but. . .
- There are not many of such boards, can be just cross cables



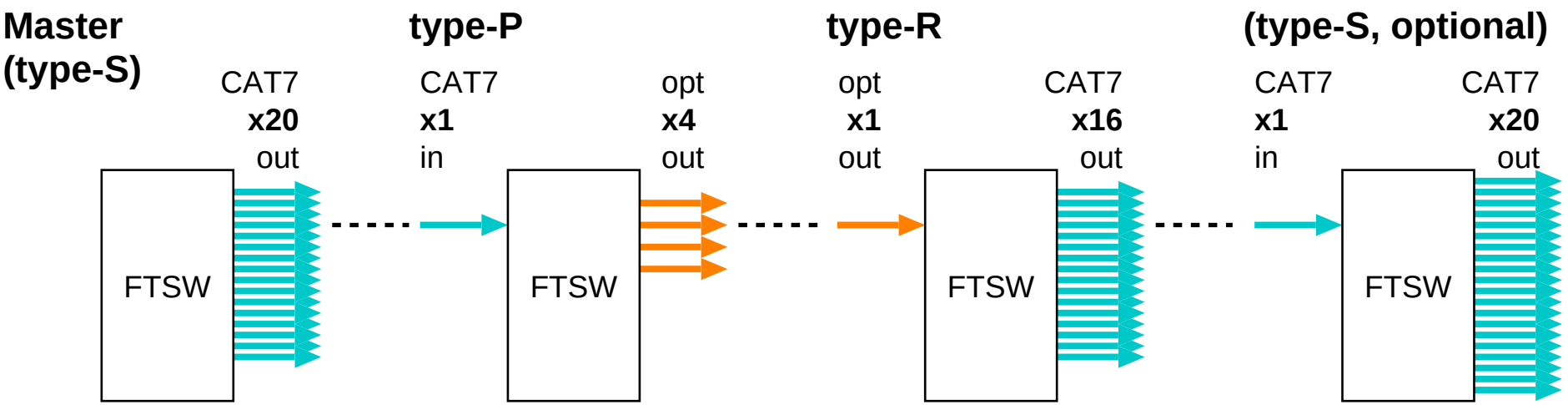
- Parts and tools are in hand for CAT5E round cable
- One cable was made and used in my FTSW2/3 mixed crate

  Is there any boards planned with the old JTAG defintion?

New CAT7 cable?

- 14% thinner flat CAT7 cable is now available from the same company
  Company: SANWA SUPPLY, Part no: KB-FLU7-10BK (for 10m black)
  `http://www.sanwa.co.jp/product/network/list/kb-flu7.html`
- 10m / 15m cables were ordered, to be tested soon

TT-network



- **single type of FTSW PC-board**
  - FMC connector for an optical add-on board
  - 2 types because of coexistence of FTSW2.1 / FTSW3.0
- **3(+2) types of FTSW**
  - type-S for 20 CAT7 ports
  - type-P for 12 CAT7 + 8 optical ports with an FTOP add-on
  - type-R for 16 CAT7 + 2 optical ports with an FTOR add-on
  - -no5V option by cutting out 5V / -noVME option by removing VME J1

FTSW-noVME option

Outcome of offline/email discussion at the Hanyang TDAQWS with G.Varner, B.Kunkler, G.Visser

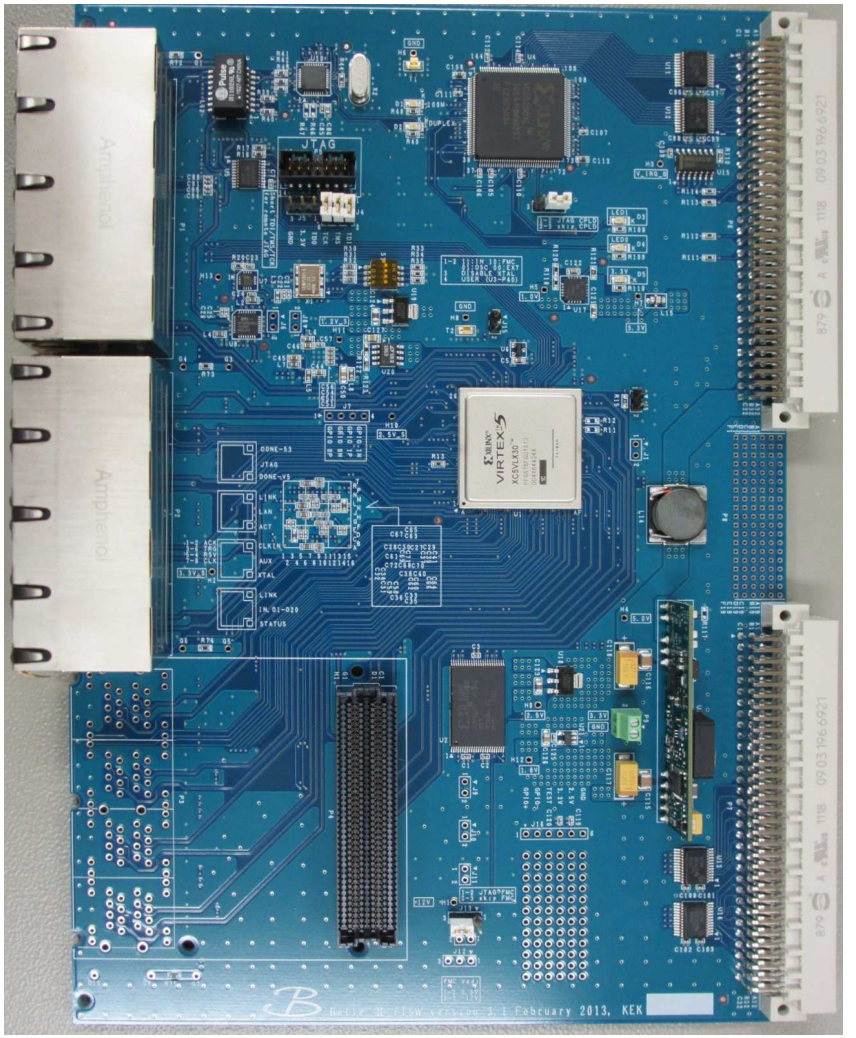
- **FTSWs for BPID and EPID are inserted in BKLM 6U crates, but...**
  - No load should be there for VME J1 connectors as they are used as custom high-speed bus
  - +5V power is VERY limited in these crates
- **FTSW-noVME option with no J1 connector as a solution**
  - +3.3V (or +5V) power (and ground) taken from the power supply lines to the front-end boards
  - Isolate the front-panel/CAT7 ground from the VME frame ground
- **Problem: less easy to test**

Things to be done

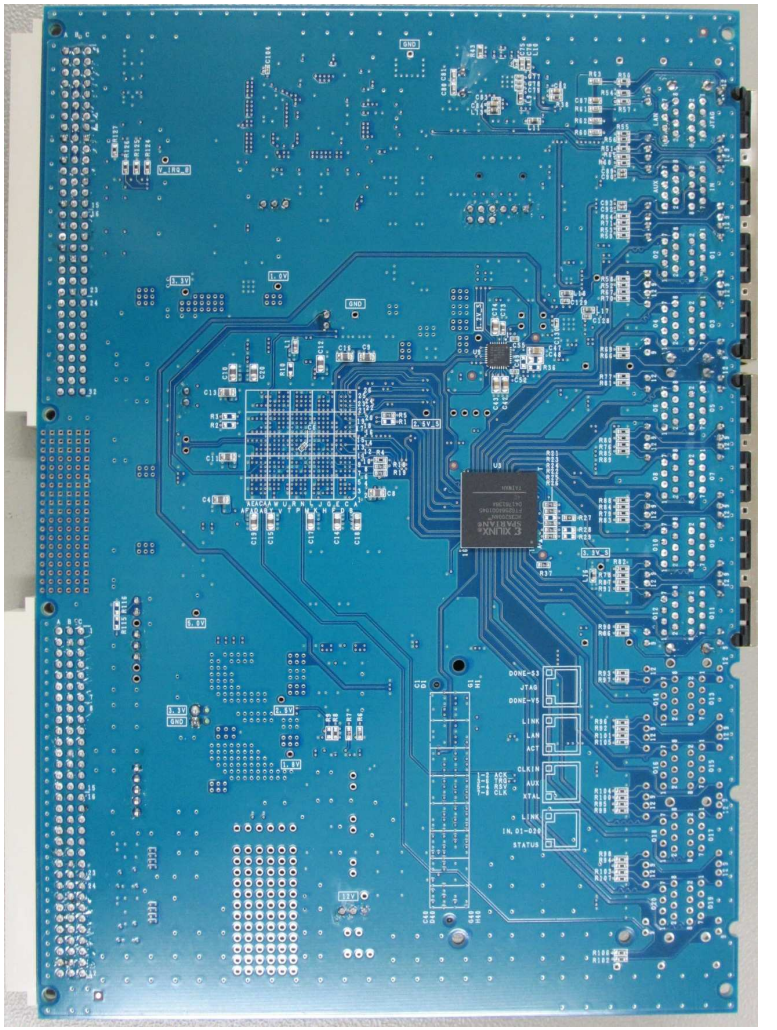
- **Hardware:**
  - FTSW module v2.1 (done, will be used)
  - FTSW module v3.1 (in mass prodcution)
  - FTOP add-on boards (done, more boards to be assembled)
  - FTOR add-on boards (test production)
  - TT-RX v5 (done, found that TT-RXv4 can't be used)
- **Protocol:** (firmware described later)
  - Cable definition (new JTAG pin assignment, sorry!)
  - Trigger distribution protocol (firmware exists)
  - Flow control protocol (some firmware exists, still a lot to be done)
  - JTAG signal embedding (not yet)
  - SEU detection (not yet)
- **Software:** (not much except for a few basic programs)
- **Documents:** (not much done)

FTSW3.1

(part layer)



(solder layer)



- FTSWv3.1 board was delivered on Feb.27

3 FTSW types

(type S)

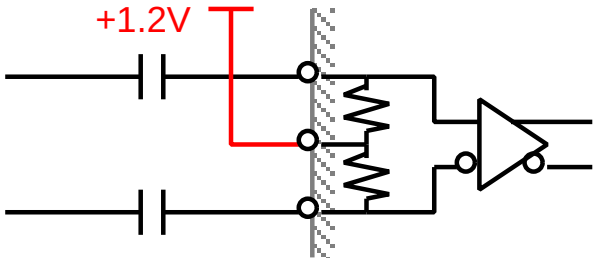
(type P)

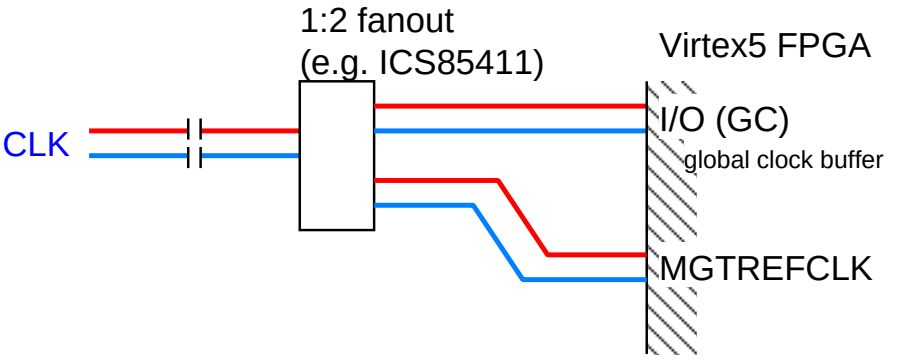
(type R)

- FTOR (two port optical receiver) boards were delivered on Feb.21

FTSW 3.0 → 3.1

- A Micrel any-level receiver chip needed a bias voltage when an AC-coupled LVDS input is used
  - No such thing was needed when AC coupled LVDS is received by an FPGA, as a bias voltage is apparently generated inside the FPGA
  - A possible bias voltage fluctuation may be the reason why the CLK jitter is affected by the phase between CLK and TRG in an FPGA
  - Adding a 1:2 fanout before FPGA to RocketIO refclk and general I/O is probably a better idea (done for CDCv4, SVDv2)





- Both of CAT7 and optical input (SFP transceiver is internally AC coupled)
- 3 FTSW 3.0 boards were hand-patched, will be still used at the test stand

FTSW 3.1 test results

- All the signal connections are tested within a very short time to meet the FY deadline
- All clock ports can deliver and receive a 127MHz clock with less than 20ps jitter, including the optical ports, without tuning the phase between CLK and TRG
- Some port and firmware dependence exists, there is room for improvement
- LAN port is not tested yet, but anyway there's no plan to use (at least LAN signal is detected by the scope)

Hardware plan

- **FTSW**
  - about 60 modules of FTSW v2.1 are there
  - 3 modules of FTSW v3.0 were
  - 89 more FTSW v3.0 modules to be produced by March 2013, if no problem is found in first 3 modules
  - 30 more FTSW v3.0 will be needed, to be produced in FY2013
- **FMC modules**
  - A few receiver connector board (FTOR) to be produced soon
  - FTOR mass production in FY2013
  - Several more FTOP modules will be needed, to be assembled soon (PC board and most of parts are in hand)
- **Crates**
  - A cheap/simple crate to be used on the detector has been ordered

Firmware and software

- No progress since last July B2GM
- Status and plan in backup (shown at TDAQWS at Hanyang in Jan)

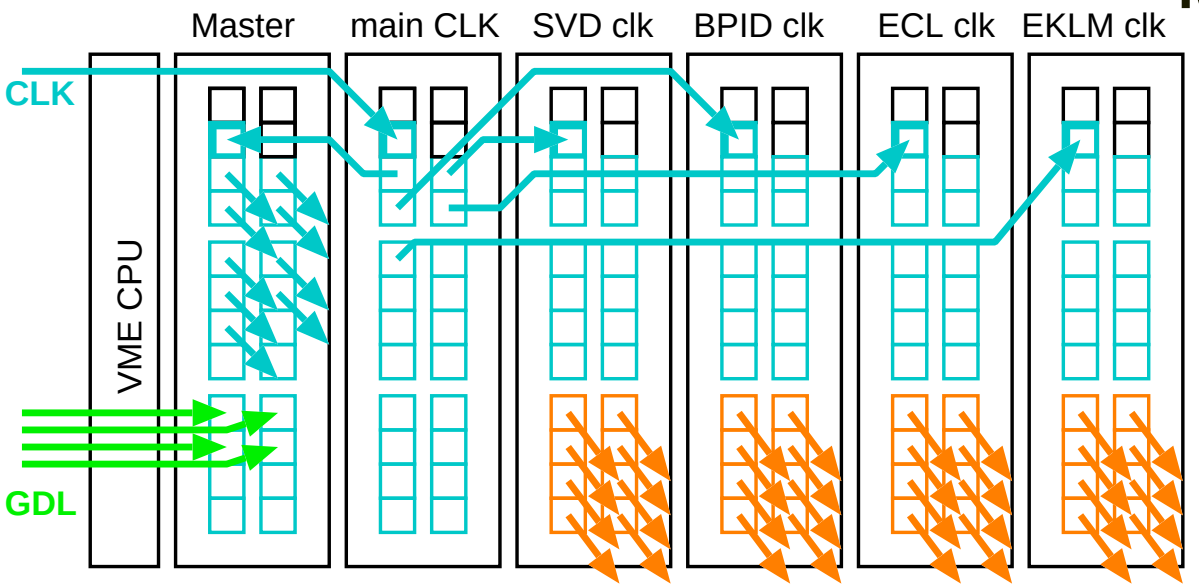
Cabling and crates

- FTSW near the detector, crates and power are needed
- Max length of 10m is prefered, 15m is the absolute maximum
  - 1m: 290mV swing, 7–8ps jitter
  - 10m: 240mV swing, 8–10ps jitter
  - 15m: 190mV swing, 10–15ps jitter
- TT cable and JTAG cable are side-by-side on FTSW
- JTAG for FTSW modules are also routed in the same way

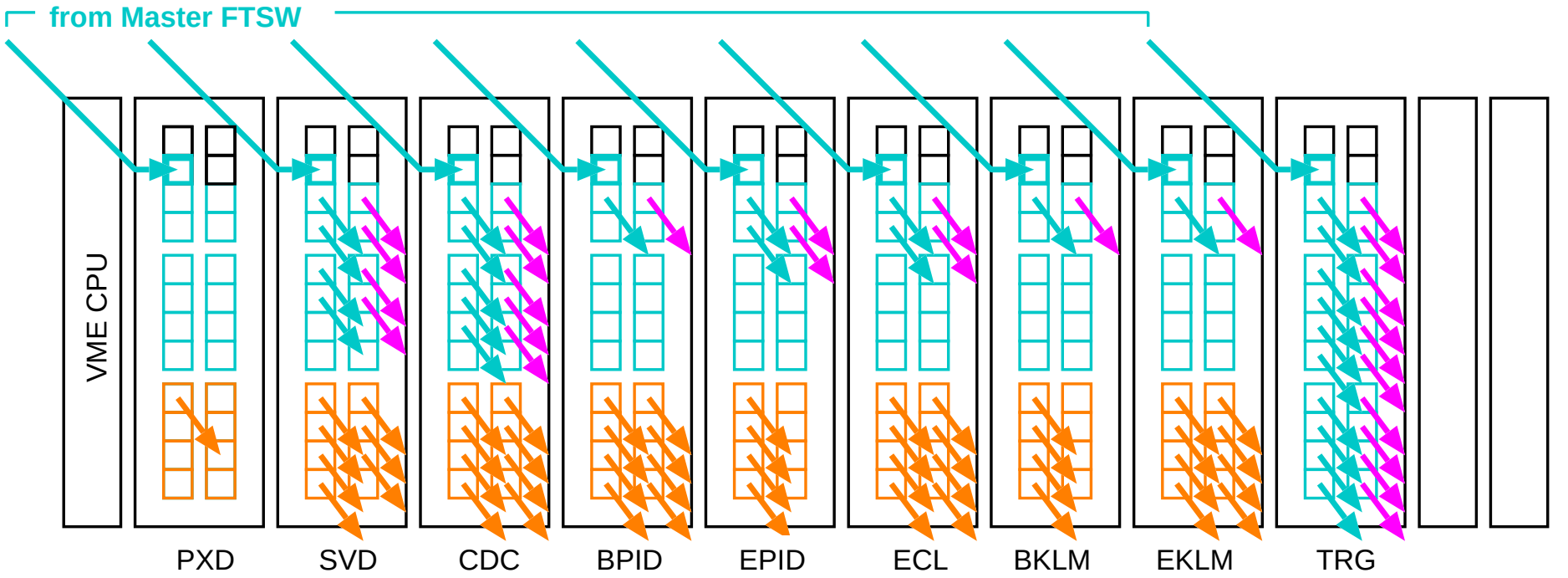
Rough cable connection layout is proposed (shown in backup)

- Connector joint for EPID is not defined yet
- Detailed cable layout (with 10m cable) has to be defined by subdetectors

Master TTD crates



- CAT7 connections of **TT** and **JTAG** to FTSW in COPPER crates and to TRG readout
- **Optical** connections to detector FTSW crates



FTSW/crate counting

- **PXD:** 8 boards (8 ports) ⇒ 1 type-R (in SVD)
- **SVD:** 48+1 boards (97 ports) ⇒ 7 type-R **(+1 crate)**
- **CDC:** 302 boards (604 ports) ⇒ 4 type-R + 32 type-S **(+4 crates)**
- **EPID:** 72 boards (144 ports) ⇒ 2 type-R-novme + 8 type-S-novme

  BPID: 64 boards (128 ports) ⇒ 8 type-R-novme (in BKLM6U)
- **ECL:** 52 boards (104 ports) ⇒ 8 type-R with no 5V (in ECL)
- **BKLM:** 16+8+32 boards (112 ports) ⇒ 8 type-R (in BKLM9U)
- **EKLM:** 112+16 boards (280 ports) ⇒ 16 type-R (in EKLM9U)

On detector: 46 type-R + 40× type-S + 8× type-R-no5V **(+5 crates)**
Grand total: 46 type-R + 60× type-S + 8× R-no5V + 15 type-P

Total: 129 boards (95 FTSW3.1 + 34 FTSW2.1)

33 type-S, 8 type-S-novme, 36 type-R, 10 type-R-novme, 8 type-R-novme 6 more FTSW3.1 is needed, 30 more to be produced including spares

Readout board id?

- Does everybody has a way to identify a board number?
- ATMEL AT24C01B EEPROM was suggested by Wacek long time ago
- FTSW v3.0 and HSLB have CPLD where such info can be stored (CPLD is not affected by different predefined register contents)
- FTSW v2.1 has no EEPROM/CPLD, but a 16-bit dip-sw can be used to store the board-id

Firmware

Minimal number of firmware types

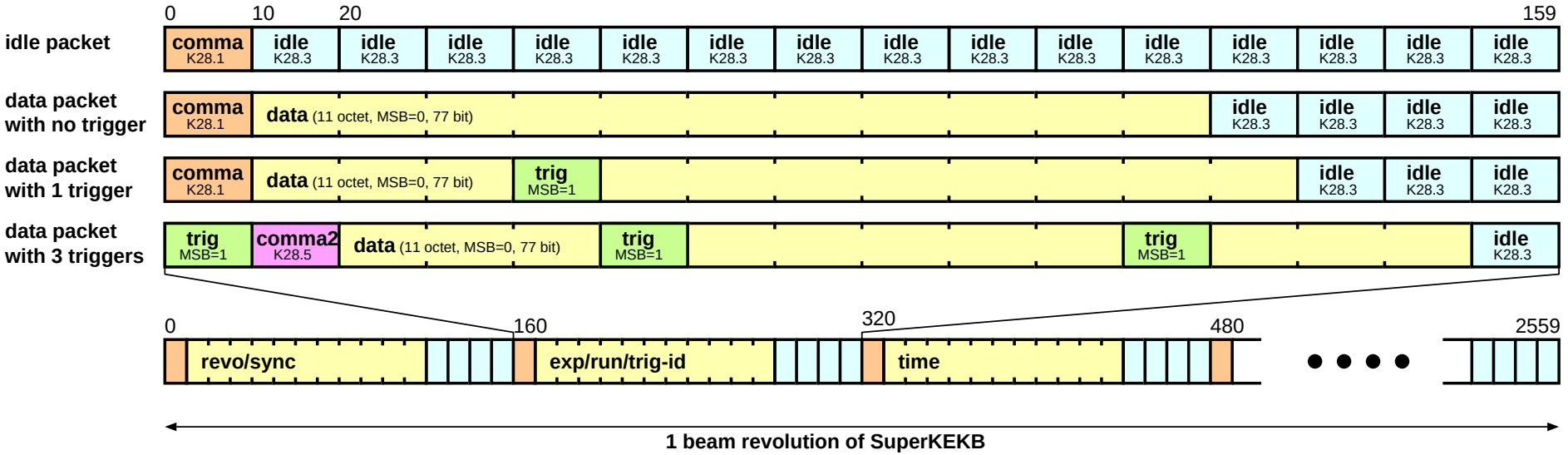
- **FTSW3.0 firmware**
  1. TT-Master
  2. 10x clock+TT+JTAG + 4x optical clock+TT distributer
  3. receiver firmware for test
- **FTSW2.1 firmware**
  4. Optical 8x TT distributer with FTOP (small mod. of 2.)
  5. Optical 8x clock distributer with FTOP (easy)
  6. COPPER handler (no JTAG)
- **Others**
  7. readout board firmware on test boards (CDC board for Virtex5, SP605 for Spartan6, ML605 for Virtex6) (mod. of 3.)
  8. TT-RXv5 firmware

TT-protocol (1)

- **Trigger-octet (8-bit, 8b10b encoded) at 5 clock (40 ns) boundary**
  - 1-bit trigger decision
  - 3-bit coarse timing within 40 ns (0..4)
  - 4-bit trigger-type/fine-timing
- **Trigger-type/fine-timing allocation (16 patterns)**
  - 4 patterns with fine-timing (BPID trigger)
    in this way, the fine-timing info (2ns LSB) is merged into trigger-type
  - 4 patterns with non-fine-timing triggers (including random)
  - 4 patterns for local triggers
  - 4 patterns for spare (can be another fine-timing trigger type)

TT-protocol (2)

- Other signals are embedded into a “frame” of 10μs long (revolution)
- Used for synchronization, control, etc
- Trigger id / time / bunch number assignment is done locally
- JTAG signals are also implemented into the frame
- Broadcast (12-bit types) or point-to-point (8-bit types + 20-bit address)
- 64-bit data (broadcast) or 48-bit data (point-to-point)



TT-protocol (3)

- Minimum trigger separation of 190 ns (24 clocks)
  generates 0.57% “deadtime” at 30 kHz trigger rate
- 1.14% deadtime if 380 ns (48 clocks),
  or 1.14% events have event pileup (and unusable in offline?)
- Anyway without fine-timing info, 380 ns gap is needed as SVD readout takes twice longer time

Software

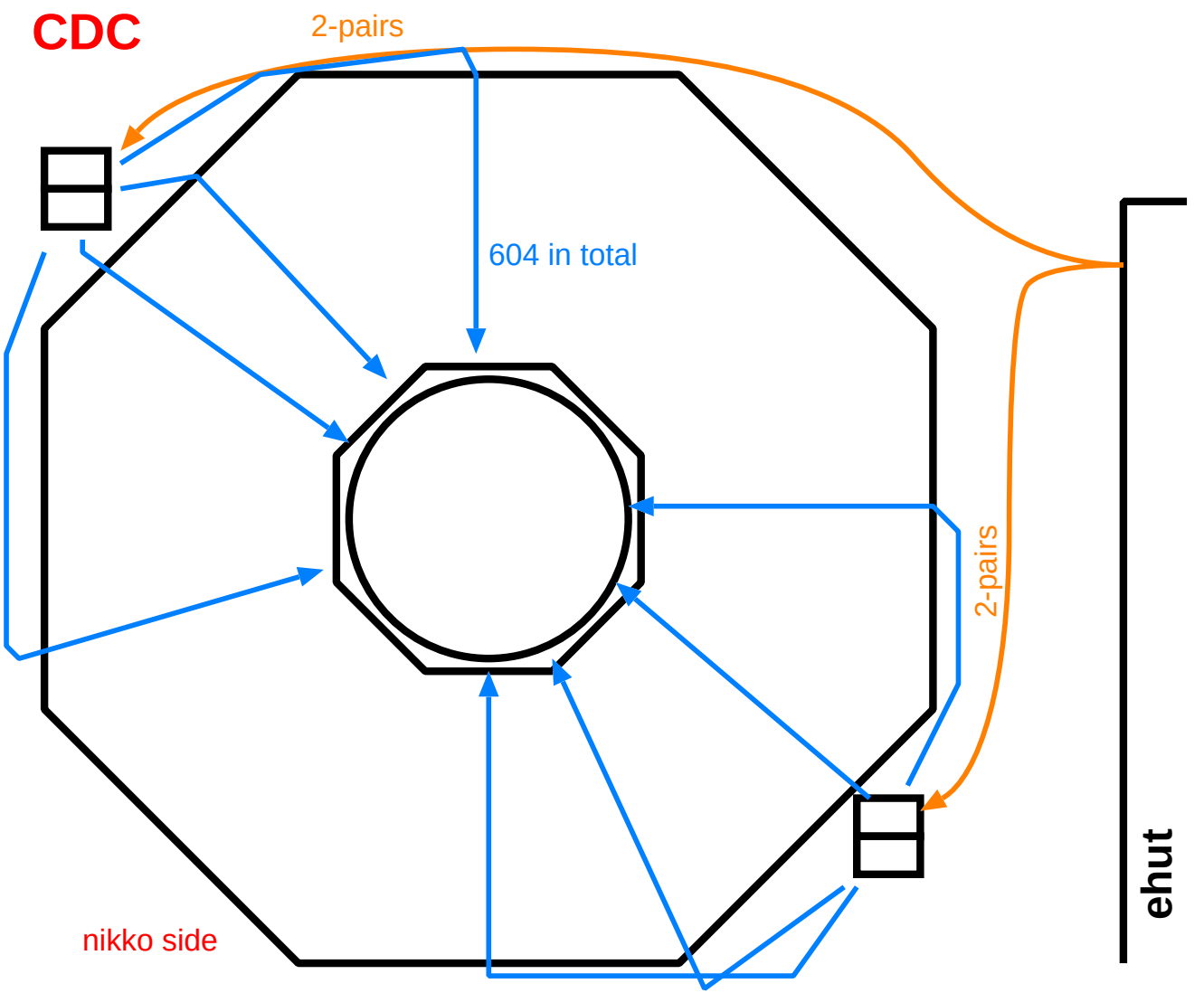
- **Master TT crate**
  - FTSW boards on the master TT crate are controled by a VME-CPU
  - No VME-CPU is planned for FTSW boards on the other crates
  - NSM program
  - JTAG programming of remote FTSW/readout boards
- **NSM program**
  - Configuration of remote FTSW boards: ports, JTAG
  - Run control through master FTSW
  - Local run control through detector-master FTSW
- **User interface**
  - Need to visualize the distribution tree
  - Monitoring of the buffer depth and other performances

Firmware status

- **Prototype firmware**
  - has no flow control and other fancy featuers
  - but has been used to distribute clock, revo signal and trigger for BPID, SVD, DHH tests
  - Available in bdaq for Virtex5 as a part of the CDC code (~nakao/work/cdc48b2link/belle2link/TT/)
  - Also available in bdaq for Spartan6 (for SP605 evaluation board) (~nakao/work/sp605tt_bpid)
  - Transplanted for Virtex6 by Igor's group for DHH (not in a public repository)
- **Beta-version firmware**
  - for telescope test, should have most of the features
  - protocol redesigned and reported in July B2GM

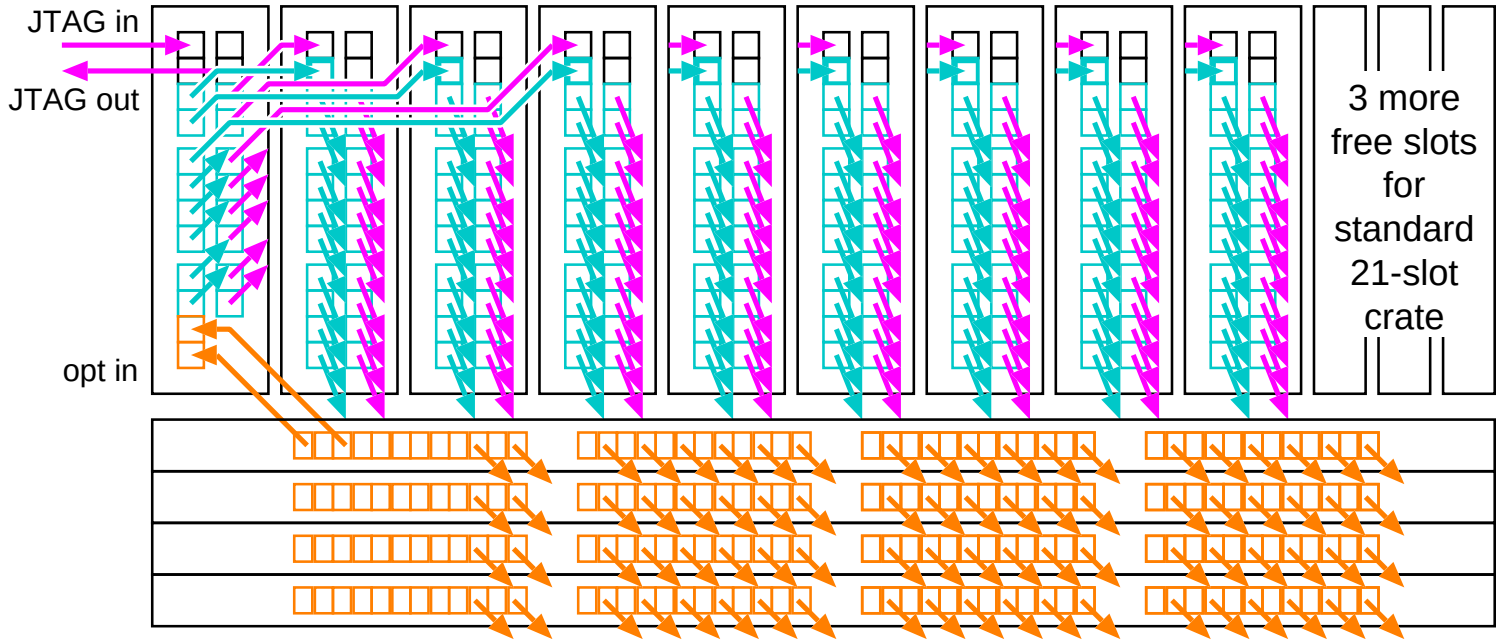
But no progress since last July B2GM

CDC



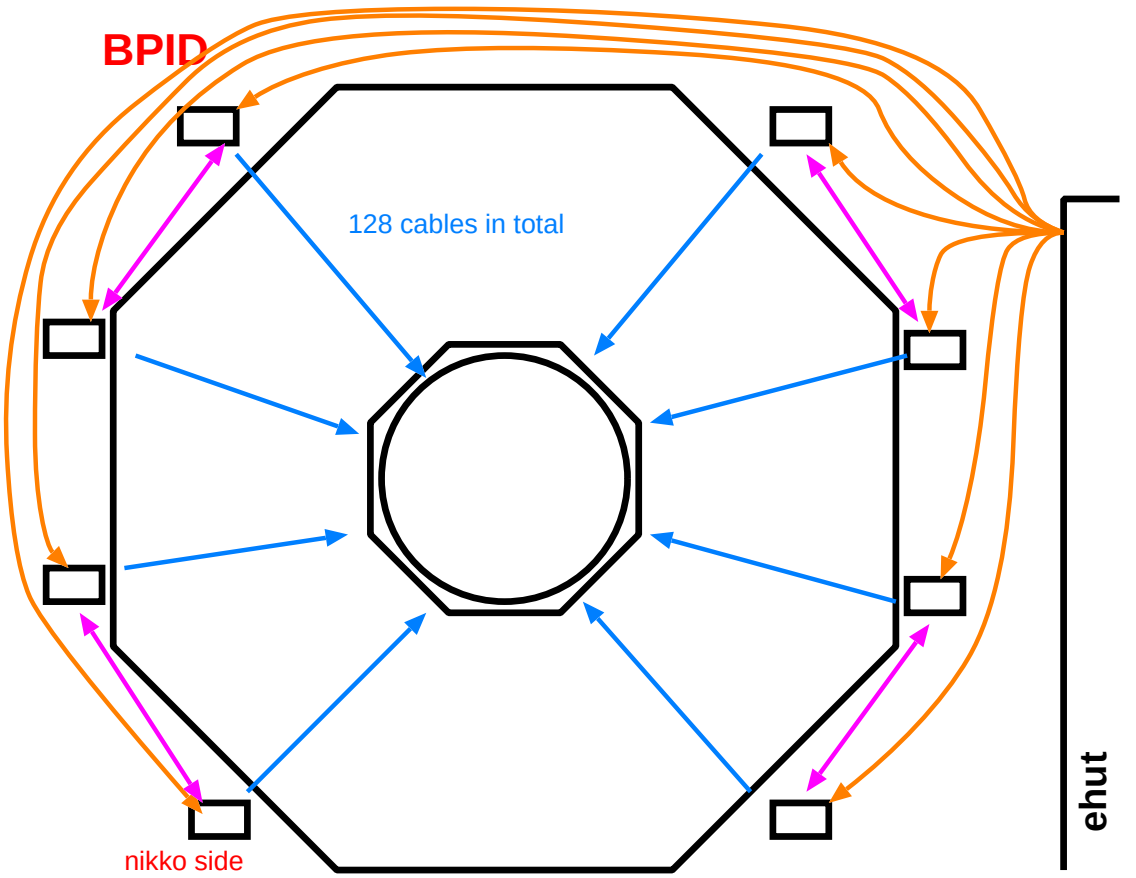
- 4 crates at 2 places, in Nikko side, using ECL racks

CDC



- 4 full FTSW crates for 302 readout boards
- Each crate: 70–80x (TTD + JTAG + Belle2link) + 1 TTD (10U)
- 2 crates in a pair to make a loop of JTAG in / JTAG out
  (left-most FTSW has no other way to reprogram) **(total 20U $\times$ 2 places)**
- Location: anywhere Nikko-side, free ECL rack space
  (inspected at 2012.Nov Gemba meeting, need to confirm with A.Kuzmin)

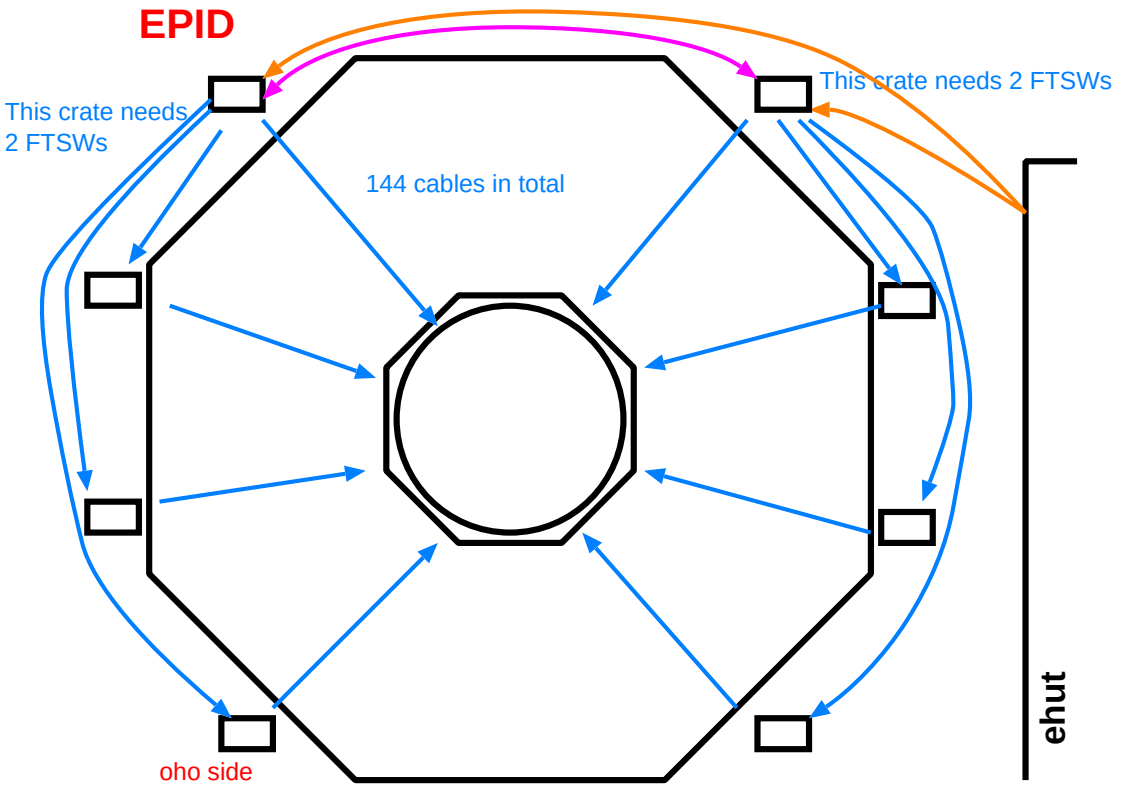
BPID



64 SCRODs in total

- One FTSW handles 8 SCRODs
- Each FTSW placed in existing BKLM 6U crate (Nikko-side)
- Need 1U more slot at each place for optical fiber patch panel

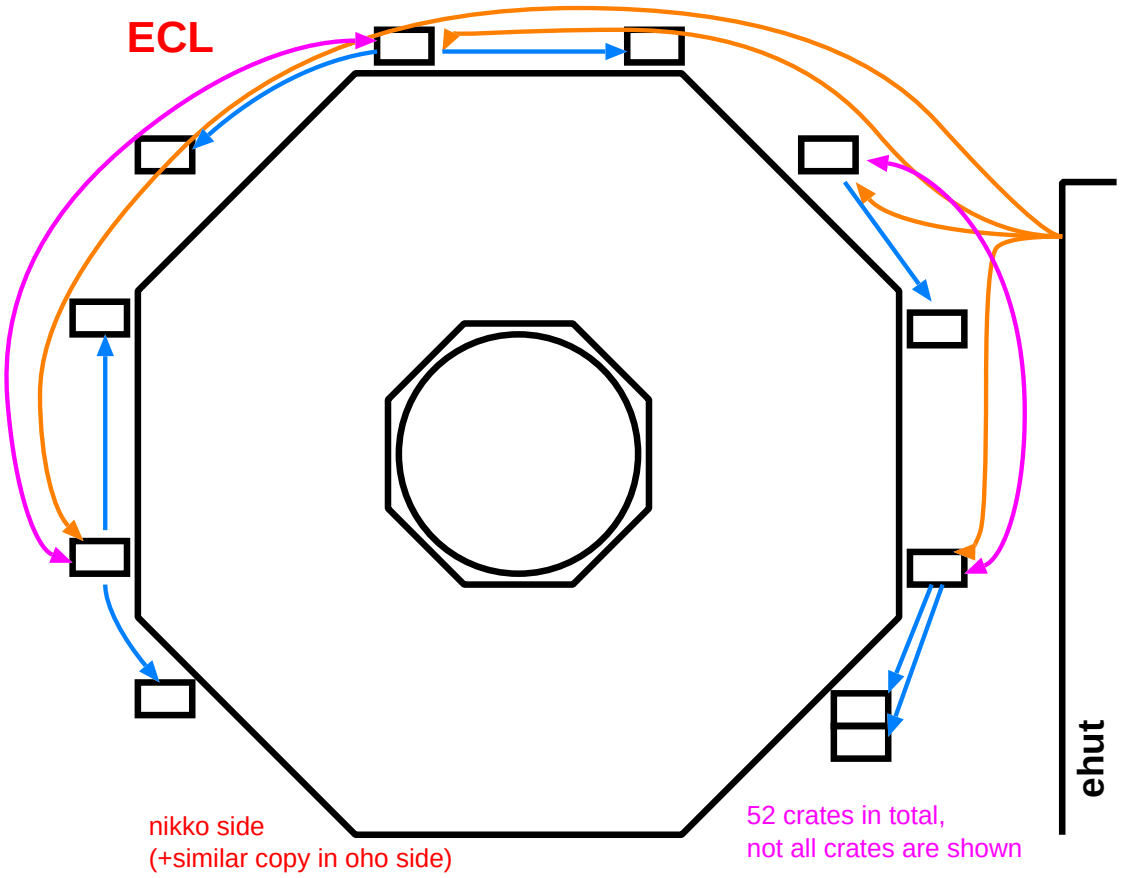
EPID



72 mergers in total

- One FTSW handles 9 mergers
- It has to be type-S, so one more step (2 type-R boards) is needed
- Each FTSW type-S placed in existing BKLM 6U crate (Oho-side)
- Two FTSW type-P also in BKLM 6U, if power supply is not limiting
- Need 1U more slot at each place for optical fiber patch panel

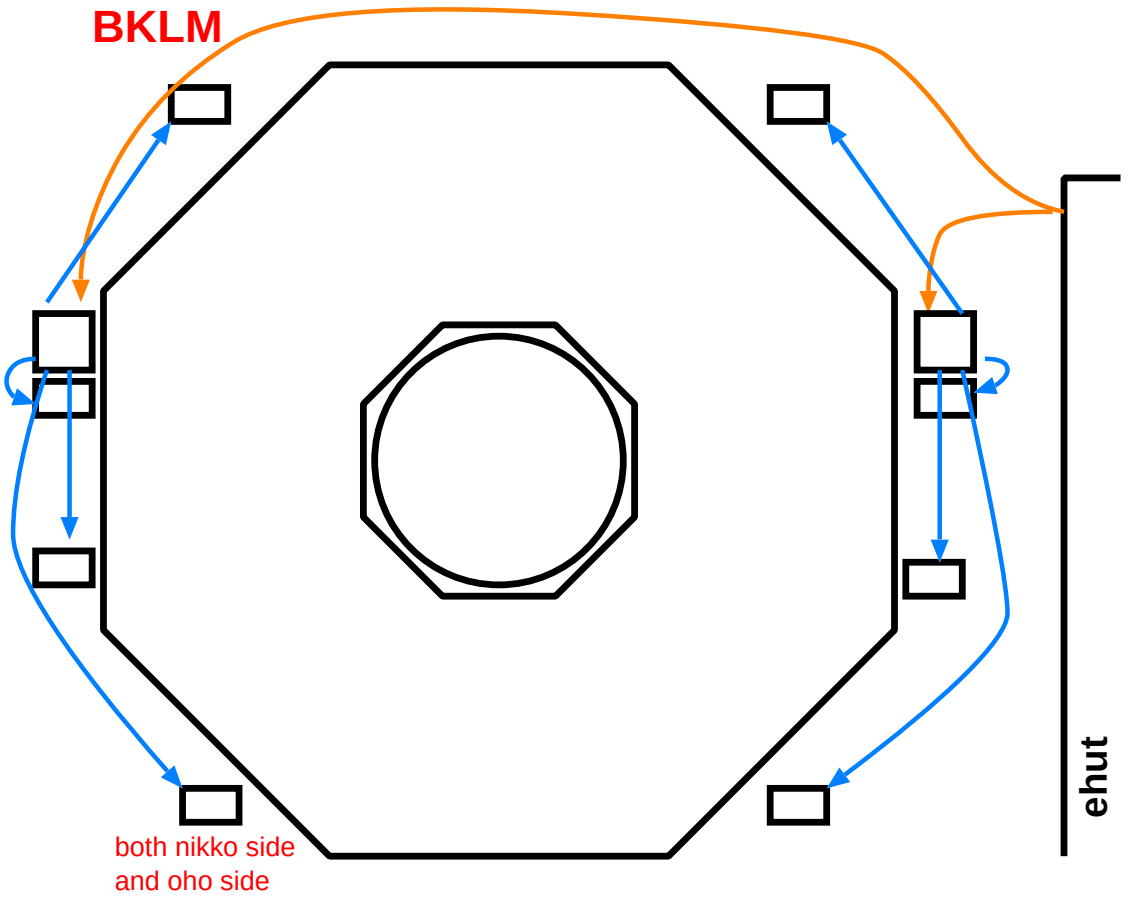
ECL



52 collectors in total

- One FTSW handles 6 or 7 collectors
- Each FTSW type-S placed in existing BKLM 6U crate (Oho-side)
- Need 1U more slot at each place for optical fiber patch panel

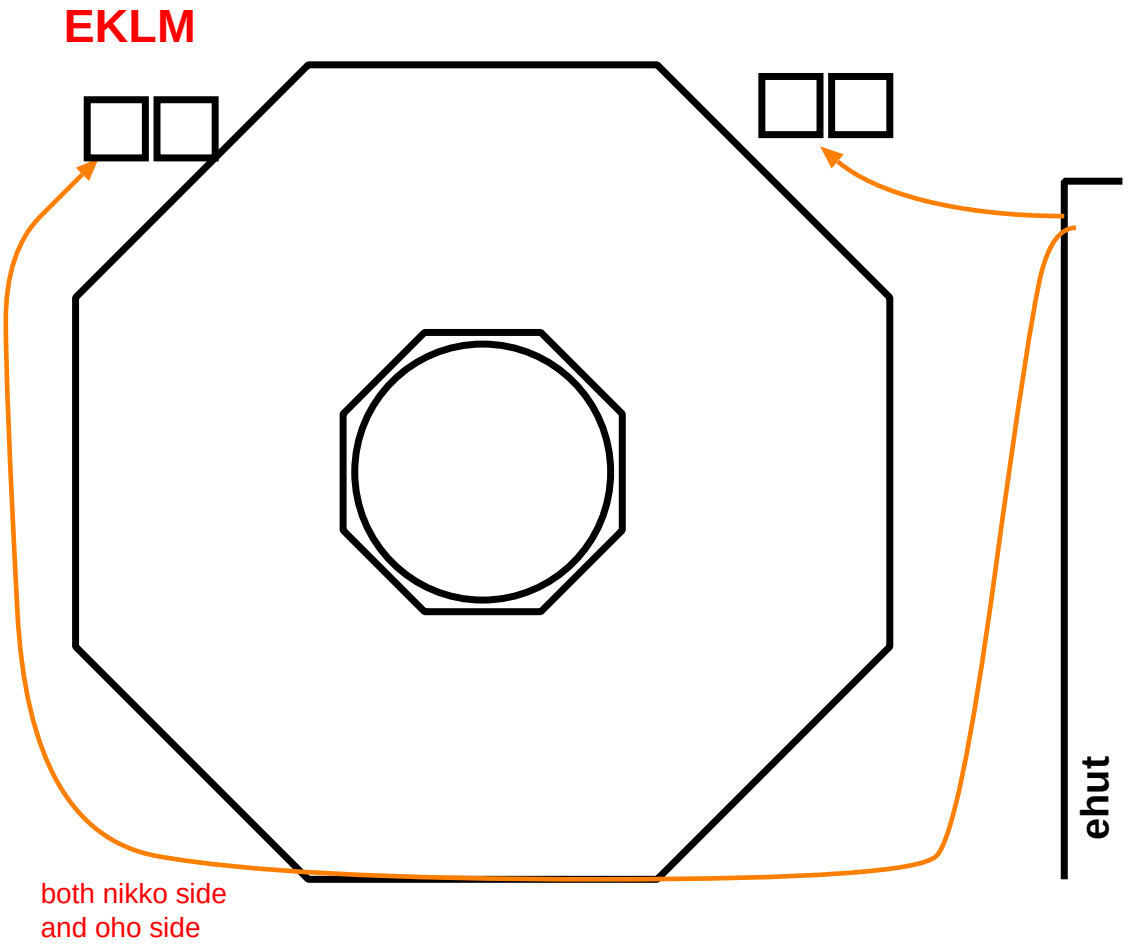
BKLM



16 concentrators(RPC)
+8 concentrators(sci)
+32 SCRODs

- Total 8 FTSW are needed at 4 crates
- 2× FTSW type-R in each crate
- Mixed 6U/9U slots in a 9U crates

EKLM



16 concentrators
+112 SCRODs

- Total 16 FTSW are needed (bad...)
- 2 FTSW per COPPER crate (forward/backward quardrants) perfectly fits
- But one of FTSW should be the next step of the other FTSW
- To put two type-R at each crate requires 2 more type-P at master-TT