Sensor

Sensor WP – general remarks

Status of the PXD-8 Production run

Future plans

(R. Richter)

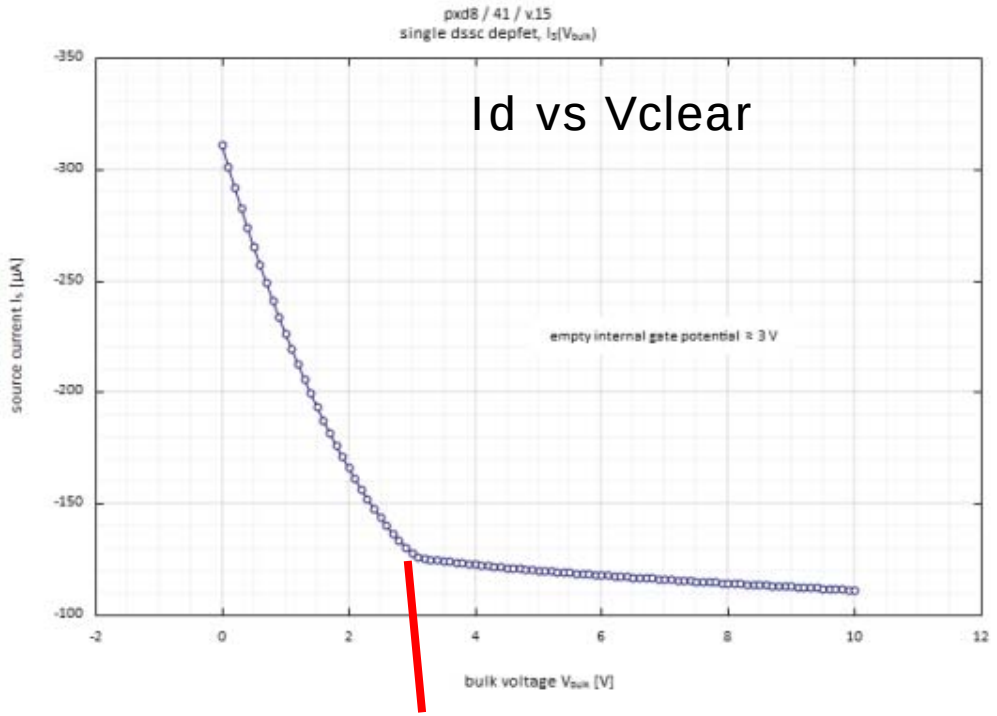
Sensor WP – general remarks

- Personal changes: Peter Lechner (WP leader) left the project (replaced by R. Richter)
- Structural changes: HLL of MPI‘s was transferred to HLL of MPG (staff 16 people + 4)
- Separation from PNSensor (personal and organization)
- Clean room activities are not affected (key persons got contracts with MPG-HLL)
- Much of processing was done by PNSensor
- 3 new technologists were hired (training on test projects)

- Lack of man power for test (see below)

PXD8 Production Status

- By end of 7. semester (Nov. 2012) 2nd Metalization finished
- Peter presented nice measurements on single DEPMOS structures
- 7 PXD8 wafers got BCB + litho (ILD for the Cu Layer)
- PXD8 left the main Clean room (hand over to the Copper Lab. HLL staff – as originally planned)
- Splitting of the batch go ahead with 2 wafers (faster and safer)



Pinch off at 3V
Potential of the empty int. Gate

Final production steps

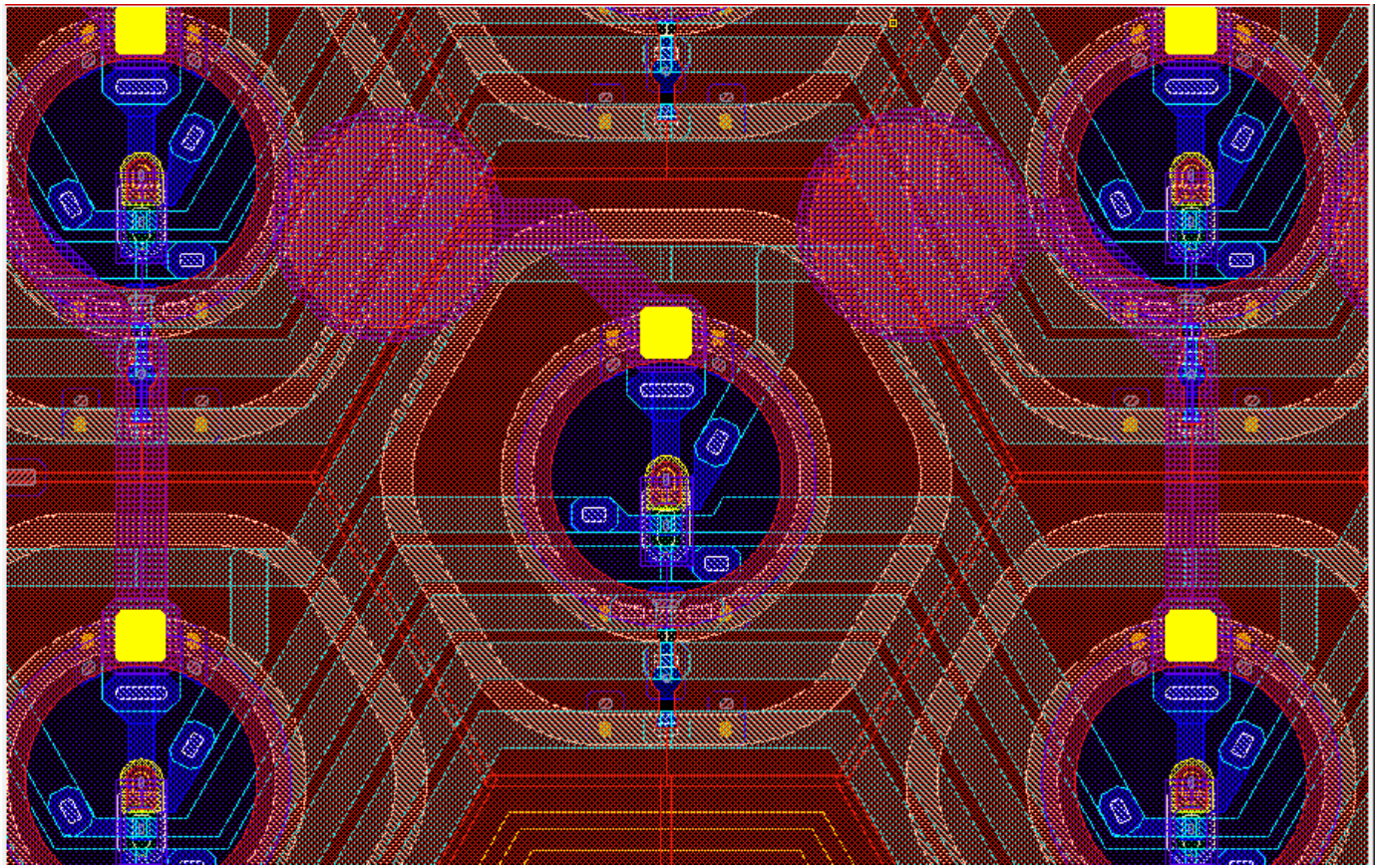
Long and intense processing comes to to an end (25 mask steps, 11 implanations)

Backend process:

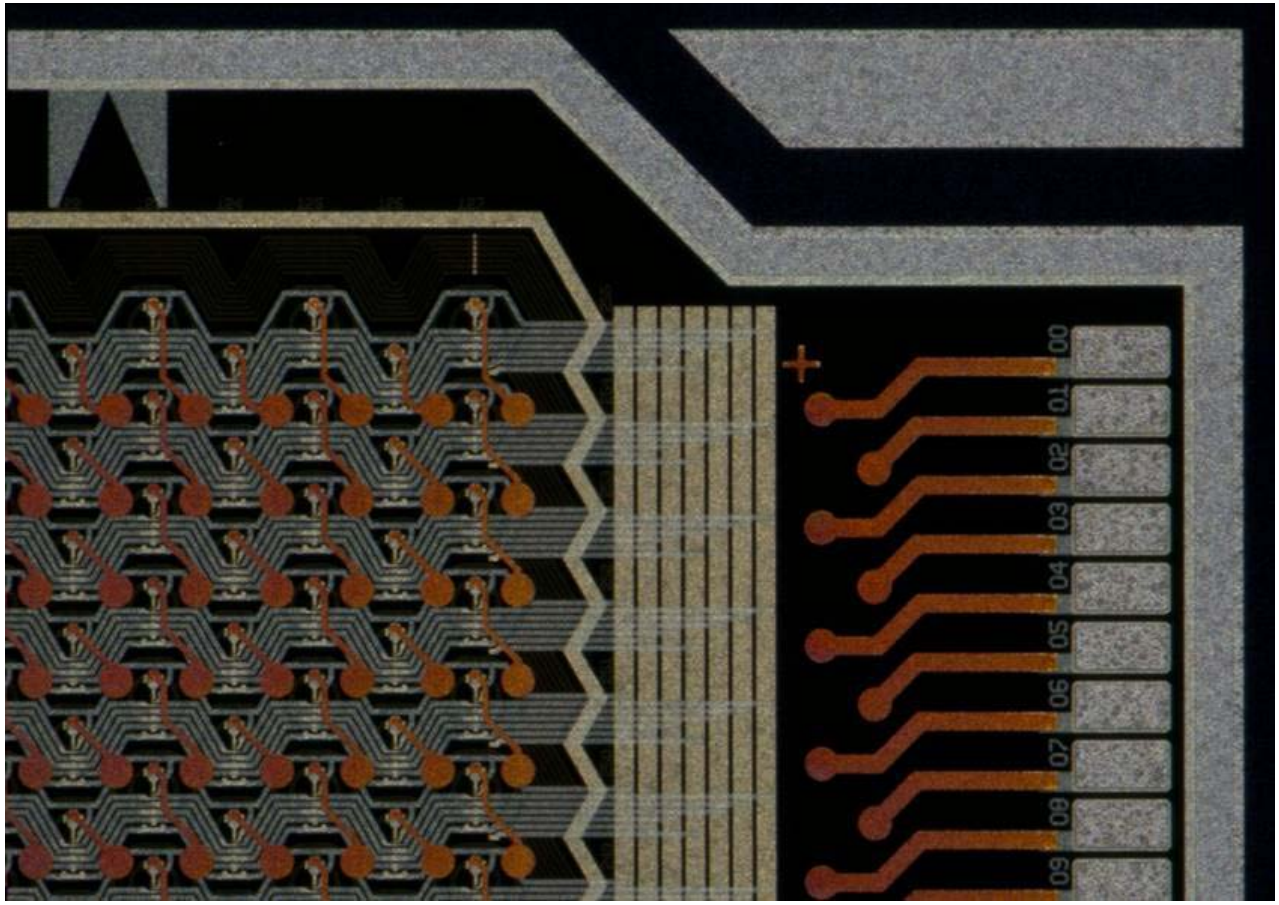
1. BCB deposition (inter-dielectric) and lithography (all wafers)
2. Descum (removal of BCB relicts by plasma etching)
3. Sputtering of Ti barrier layer and Cu seed layer (2 wafers)
4. **Lithography (3rd metal layer) and copper electro-plating**

   in line measurements
5. BCB deposition and lithography (passivation layer, solder stop)
6. Wafer dicing (1 wafer), waiting for Descum etch equipment (1 wafer)

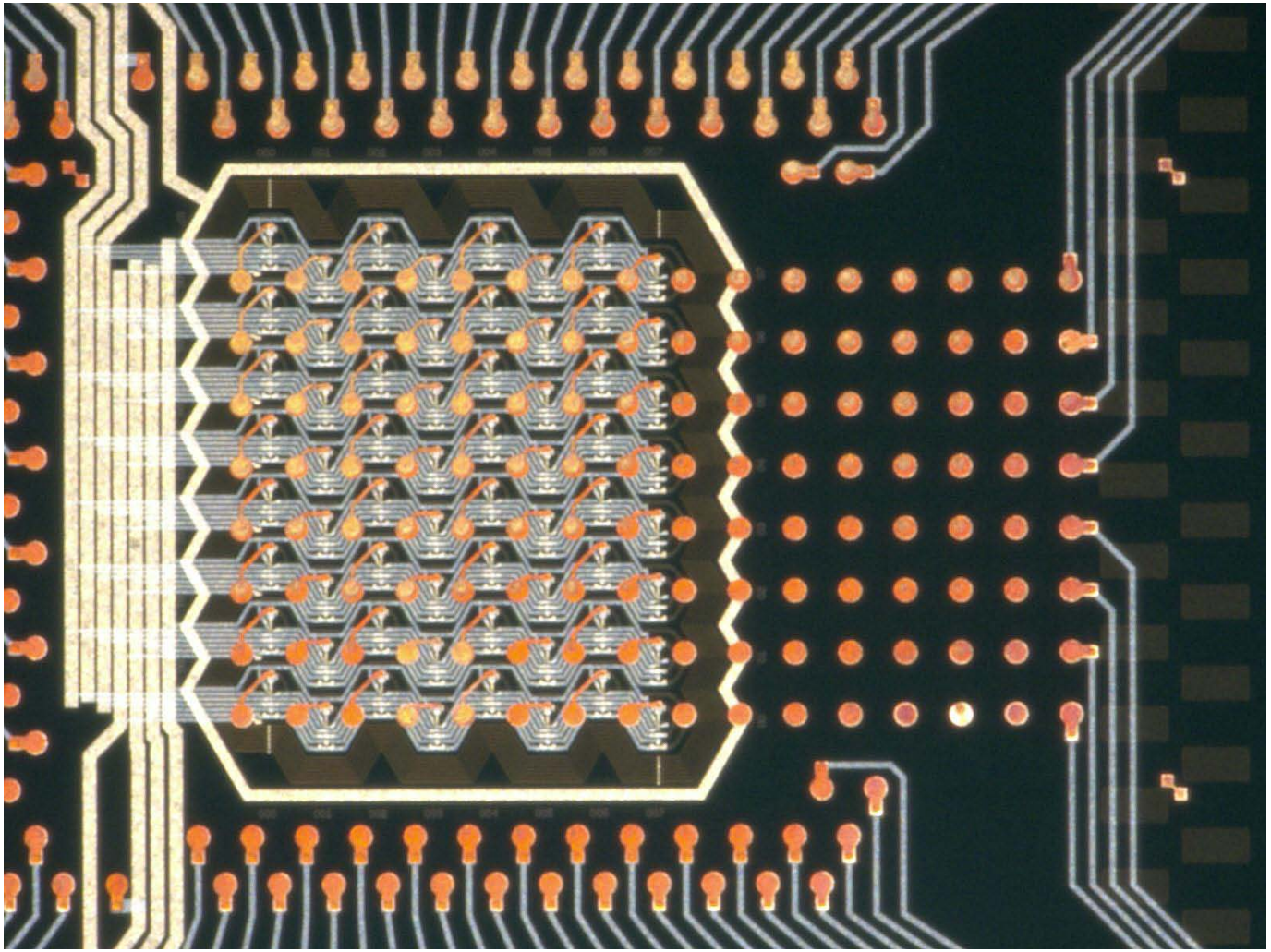
Current status: Layout view



128 x 256 Matrix



8x8 Matrix



Test activities

- One wafer will be cut (beginning of June)
  - ➢ single DEPFETs and small matrices available (wire bonded)
  - ➢ static and dynamic measurements of the different design flavors
  - ➢ determine of voltage operation windows
  - ➢ later: Dedicated pixel-wise yield test of big matrices (Input for next design and production)
- Who is doing the tests?
- PNSensor test activities are not contracted anymore; a way for continuation or alternative solutions must be found

Summary

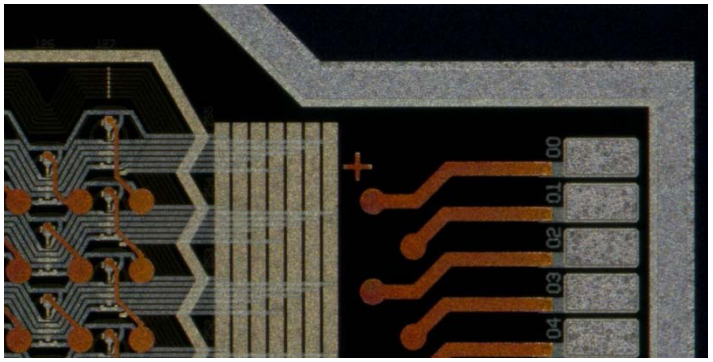
- Within the Sensor WP we have to digest changes in terms of persons and structures
- Copper processing of PXD8 will be finished by HLL staff (as planned)
- Test activities on wafer and chip level have to be reorganized

Interconnections – Sensor / ASICs

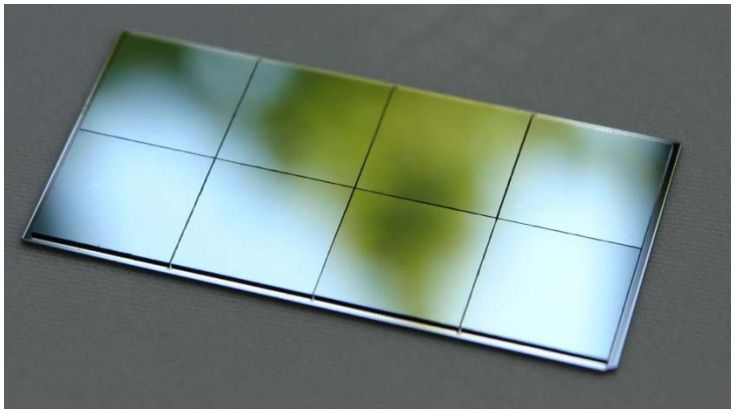
(L. Andricek)

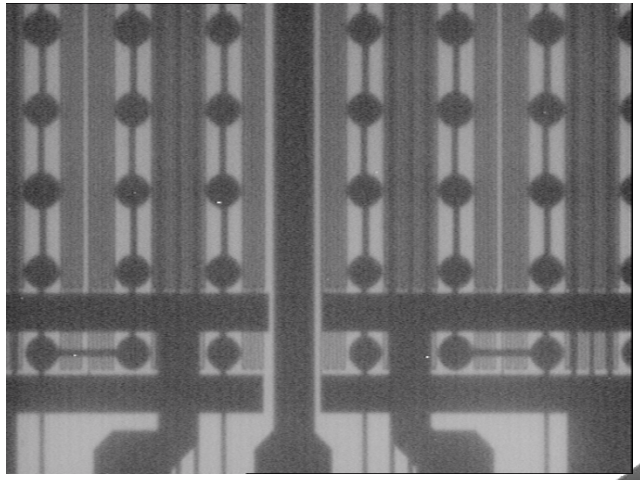
introduction

- Status at the last XDAC Meeting
  - full Cu-lithography installed at HLL
  - Tests of SF6/O2 process on diodes finished (test-xfel-3)
  - Installation and commissioning of basic FC bonder (first 128x64 modules)



- The last six months …
  - Copper on PXD 8 → sensor work package
  - Qualification of final passivation layer (solder stop)
  - Installation of remaining FC options (formic acid..)
  - Assembly of first full sized half-ladder samples
  - Options for macro-assembly on FC bonder ordered





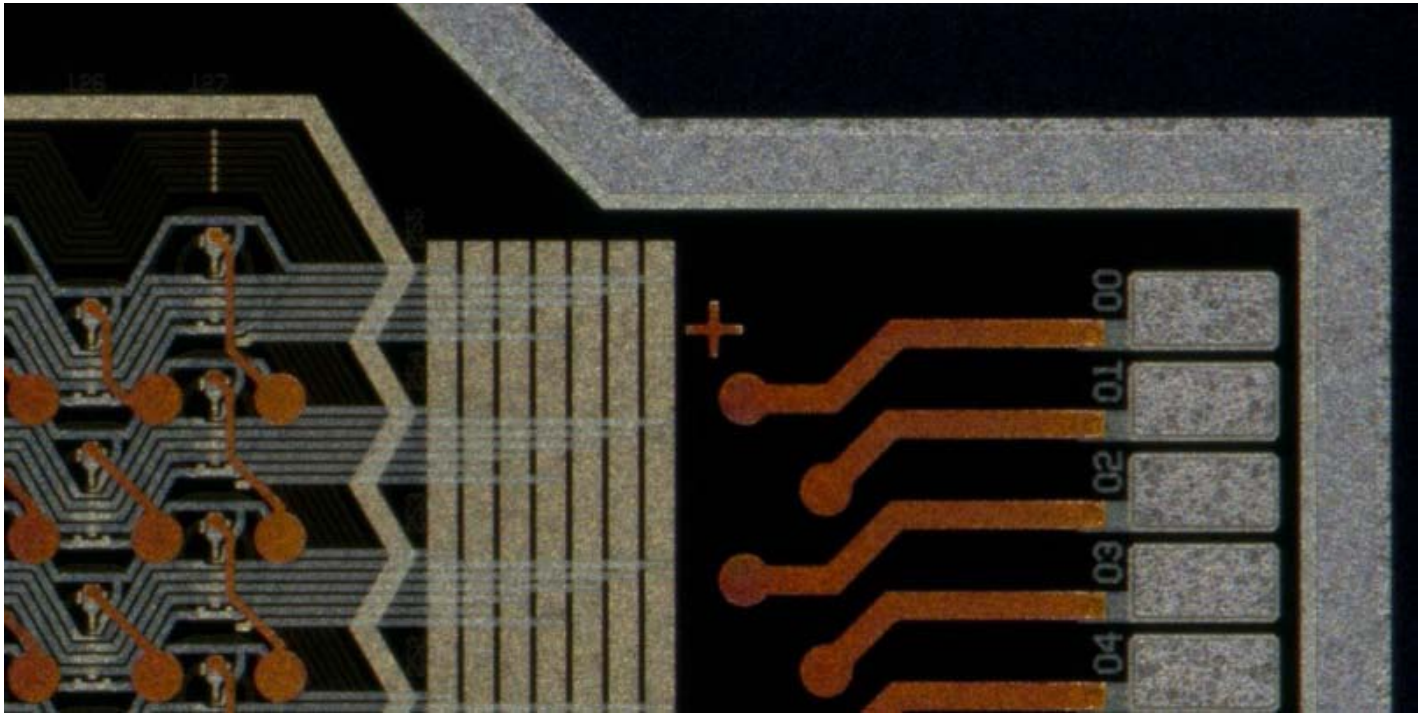
Cu process development at HLL

- Development started late 2009
  - Since then many(!) metal samples, simple test diodes, and “sensor-like” diode structures produced
  - Developments focused on back-side free processes (compatibility with low-energy entrance window)

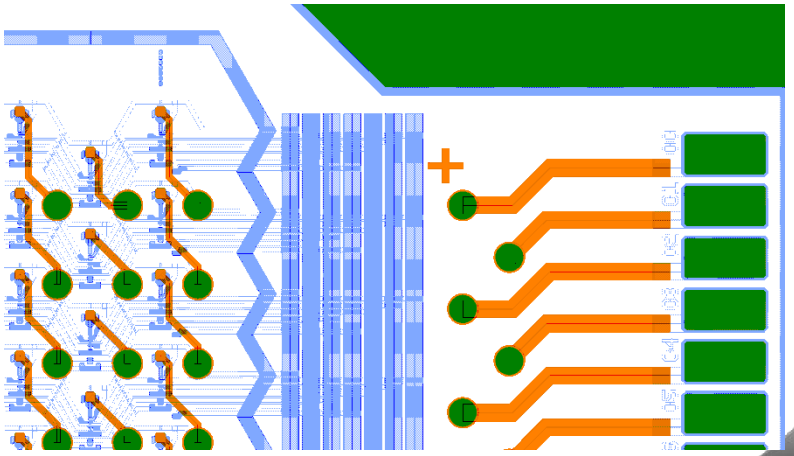
- Status: first two pxd8 wafers finished, “solder mask” final passivation still to be done

Process Step	2009	2010	2011	2012 → final
Process Up to LM (Al2) and ILD2 (BCB)	HLL	HLL	HLL	HLL
BCB SF6/O2 dry etch	n/a	n/a	IZM and Siemens CT	HLL
Ti:W/Cu seed sputtering	CNM	Siemens CT	Siemens CT	Siemens CT
Cu lithography	CNM	Siemens CT	Siemens CT	HLL
Cu ep, seed layer removal	CNM	HLL	HLL	HLL
Annealing after Cu	CNM	n/a	ATV	HLL
BCB solder mask on Cu	n/a	n/a	n/a	HLL
BCB SF6/O2 dry etch on Cu	n/a	n/a	n/a	**Siemens CT→ HLL**
Bumping (if applicable)	CNM	CNM	CNM	PacTech (→IBM)

need for solder mask



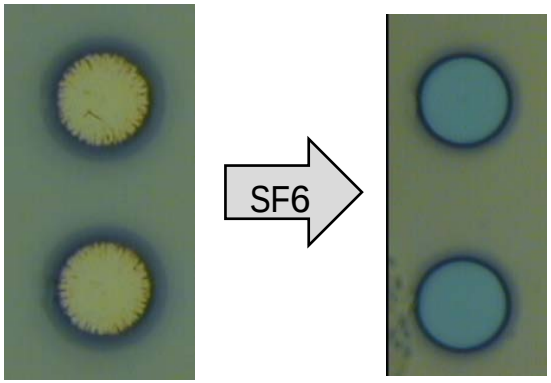
- Potential problem at pads with lateral Cu contact
  - ↳ Solder creeps along Cu trace
  - ↳ Stress on UBM!!
- need for solder mask → add BCB layer on Cu

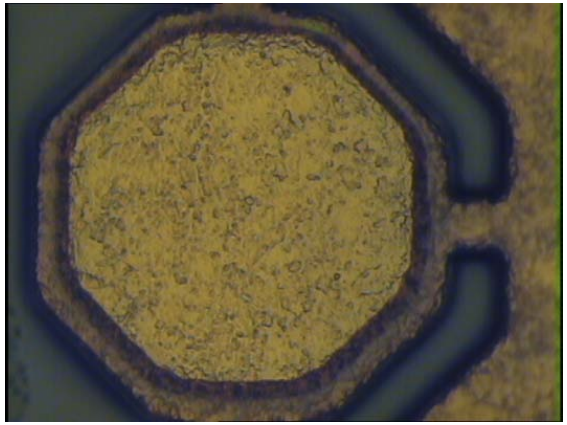


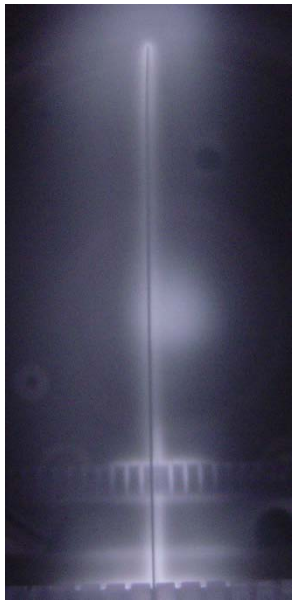
qualifying the plasma process

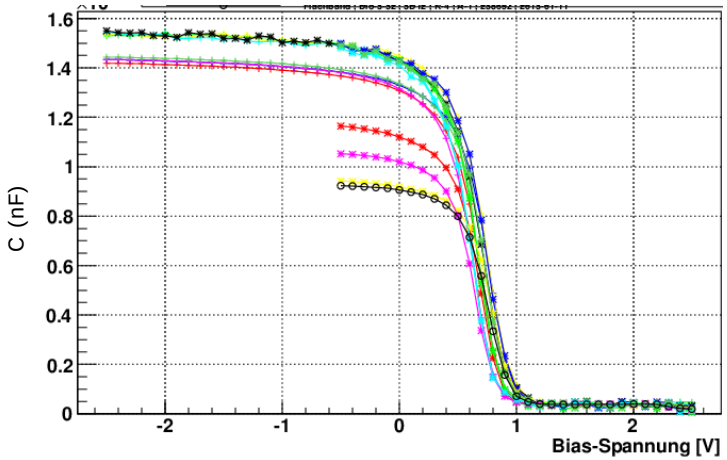
:- technological problem:

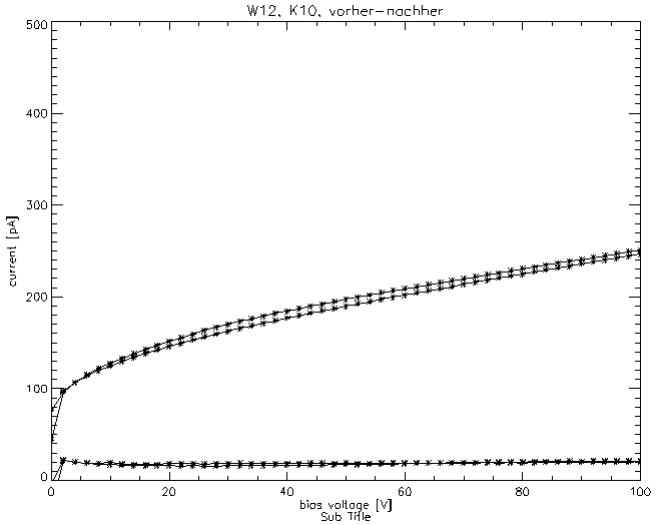
- a thin (~tens of nm) layer cannot be avoided in the BCB process → expect problems during FC











→ Tendering done, equipment ordered

FC equipment at HLL

- Semi-automated FC bonder Finetech “Fineplacer femto”, installed July 2012
- Since November 2012 in the final configuration:
  - Formic acid in the process chamber
  - Macro assembly setup (dispenser, handler..)
- ATV SRO reflow oven with formic acid, forming gas, and vacuum, installed April 2012
- Metrology & QA: IR microscope, shear tester, prep. of cross sections, X-Ray at IFIC Valencia

test vehicles

Bumped chips with daisy chains:

:- Al-BCB-Cu (~4µm) technology

:- SAC305 bumps, ~200 µm pitch, ~4000 bumps/chip

:- 1.4x1.5 cm²

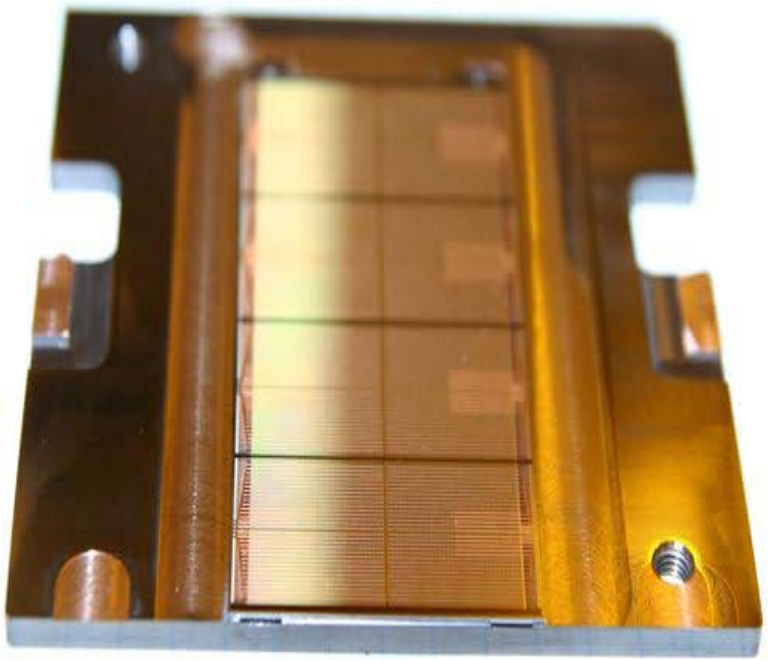
Test substrates:

:- landing pattern for chips, daisy chains

:- Al-BCB-Cu (~4µm) layer, no solder stop

:- two chips/substrate, 128x64 bumps

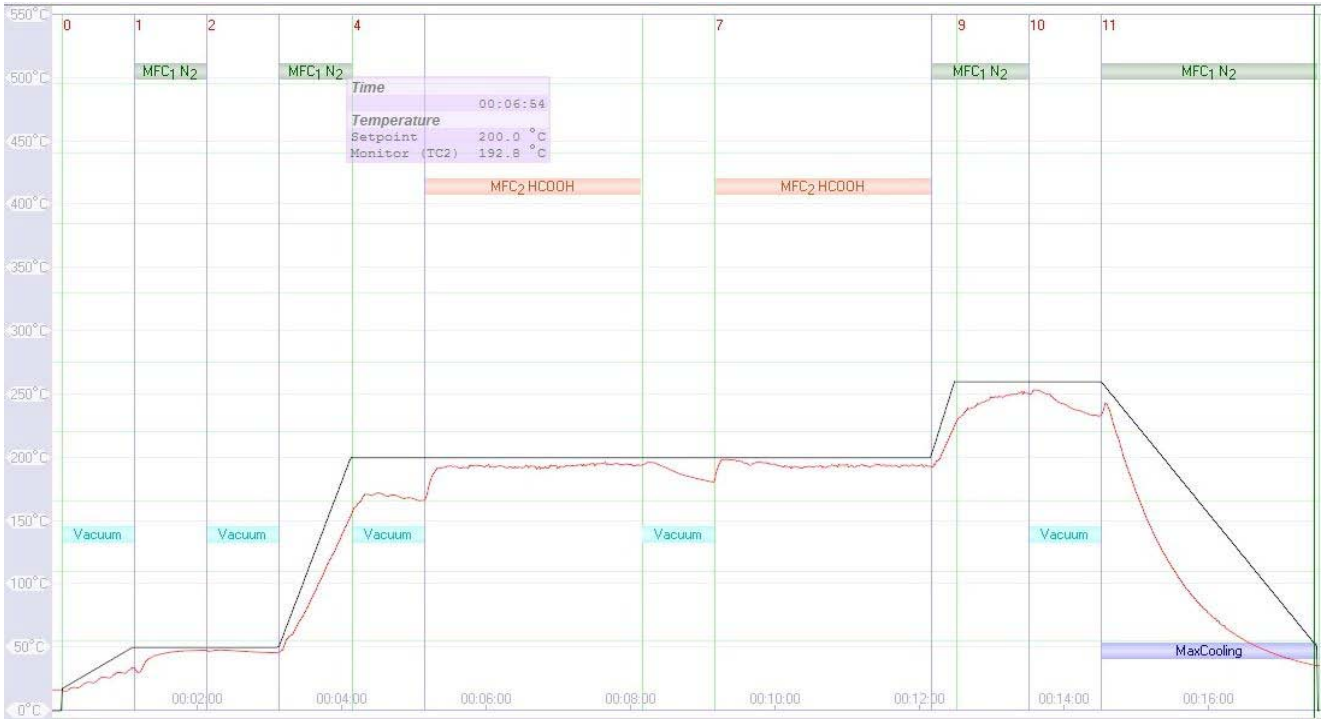
:- half ladders, 8 chips/substrate, 128x256 bumps



Substrate supported only at 1mm wide strip at the sides, in a hollow jig

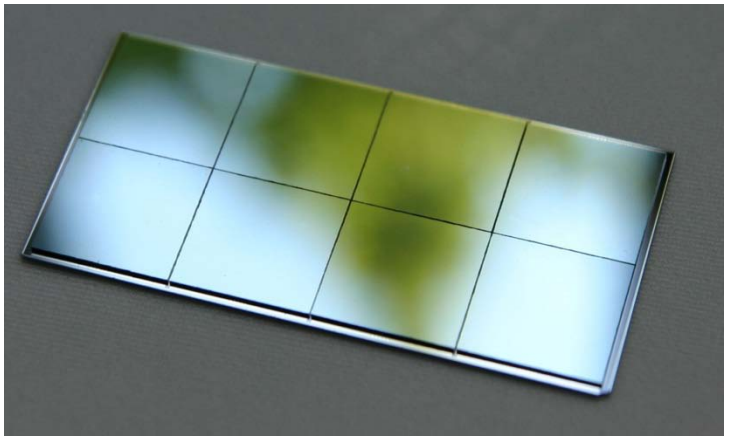
FC procedure

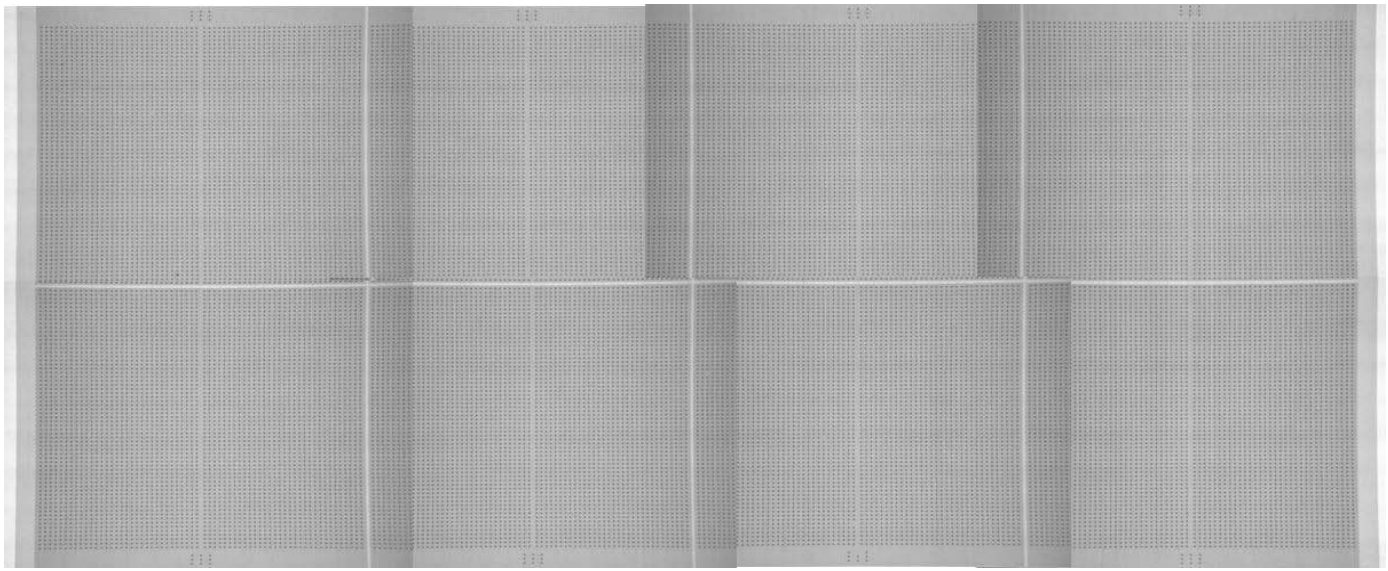
1. Clean chips and substrates in IPA/DI and formic acid vapour at 200 °C
2. Place substrate manually into jig on hotplate
3. Automatic pick-up of the 1st chip (face down)
4. Automatic alignment chip/substrate
5. Tack-bond of 1st chip (minimal pressure, 20g/chip) at 250 °C in N2/HCOOH atmosphere
6. Automatic pick-up of 2nd chip, alignment
7. Tack-bond of 2nd chip
8. Repeat 6. and 7. until all eight chips are placed
9. Manually remove substrate in jig from hotplate and place in reflow furnace
10. Run reflow profile including N2/HCOOH purge and vacuum



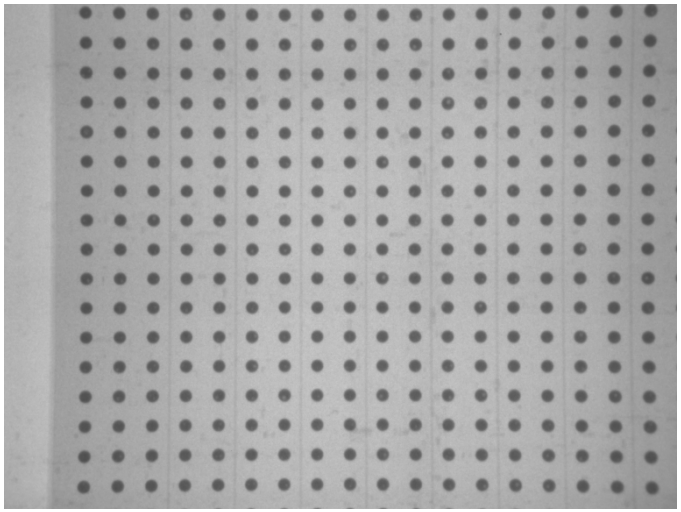
results

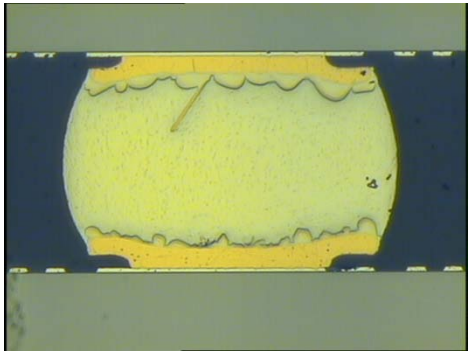
- 5 full half-ladders assembled
- Different process parameters (temp., gas flow, time ..)
- Best result, but not yet optimal .....

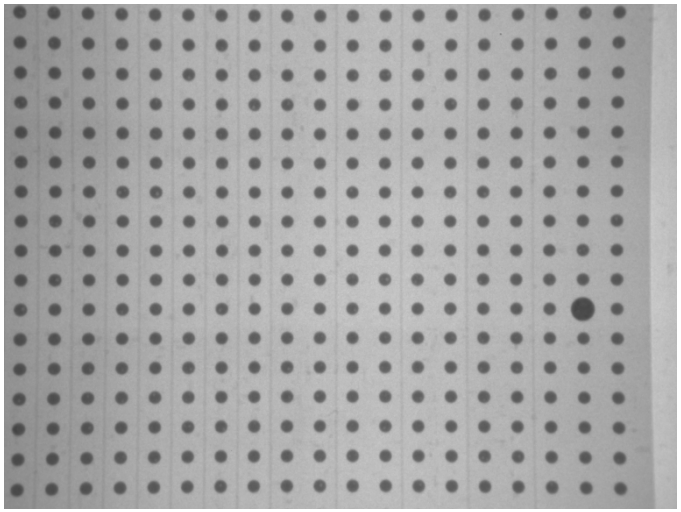


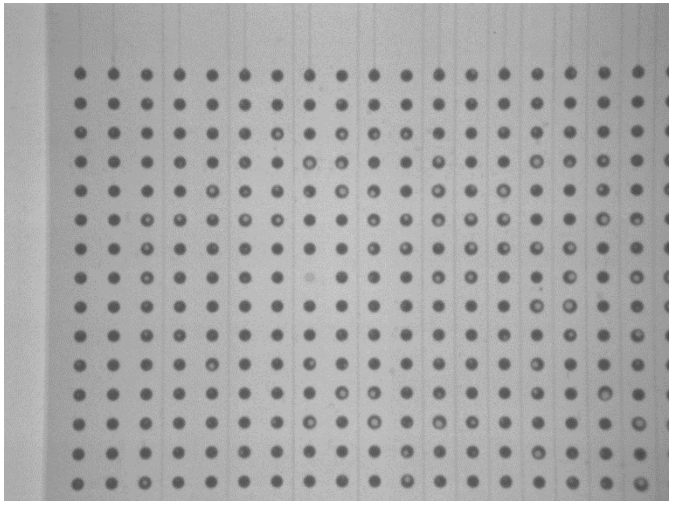


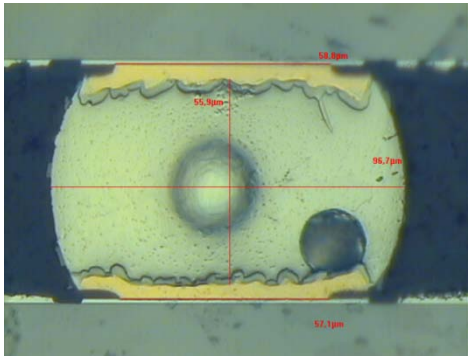
Results II

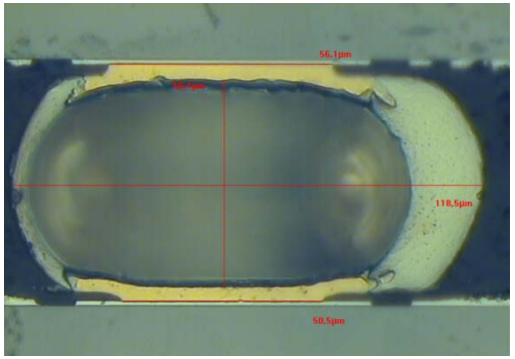






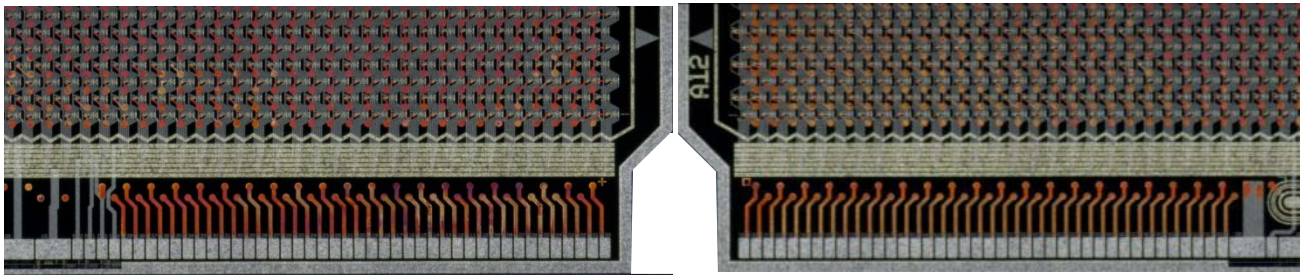


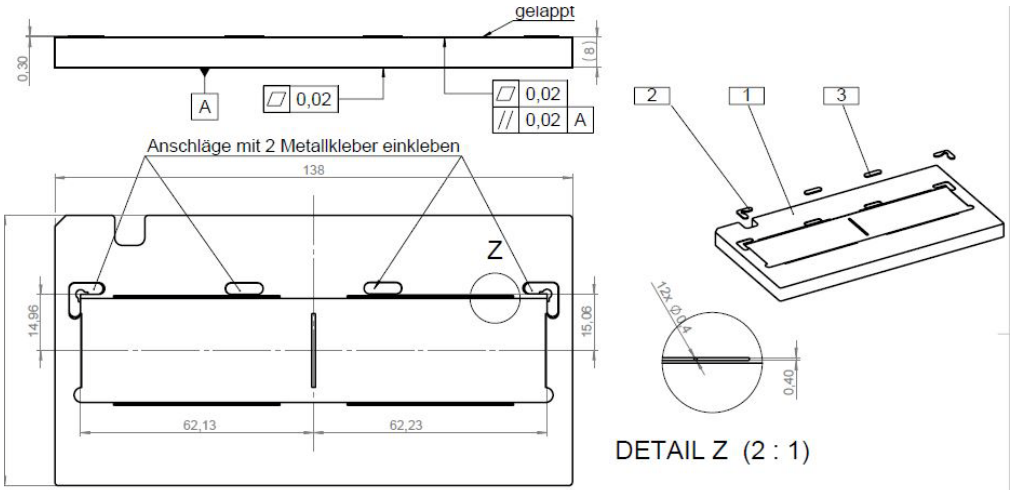


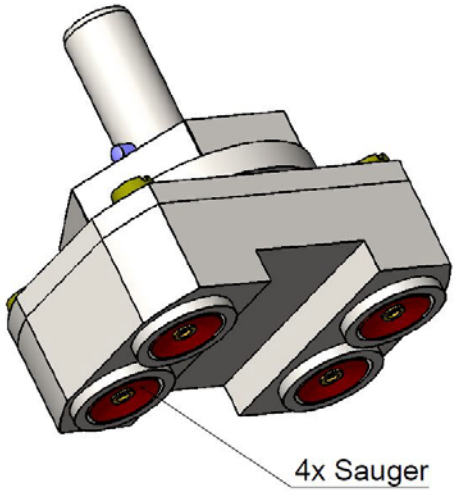


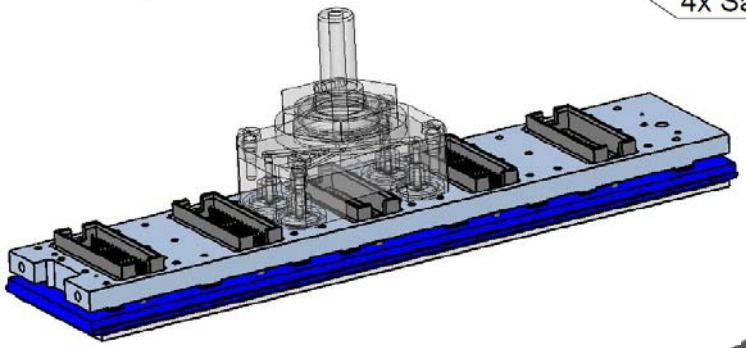
→ FC of full half-ladder works (sort off…) even with minimal pressure in hollow jig
→ We are getting closer but are not yet there
→ Optimize process and maybe process chamber of Finetech machine

macro assembly









- → Jigs and tools are ordered
- → Practice macro assembly in summer

in summary

- Cu on PXD8 done on first two wafers
  - Last process (descum) step to be installed in summer 2013
  - → see sensor work package
- FC Bonder fully installed and operational
  - Optimization of process ongoing
- Tools and jigs for macro assembly ordered
  - Work on procedure during summer

ASIC Progress

F. Erdinger for the ASIC groups

XDAC, DESY, 28.5.2013

Main Work Packages

- Further Characterization of Test Chips ADC_3 and MM3
  - ADC properties
  - Variation of Ramp current and Delay step
  - Operation of pixel-internal injection
  - Operation with PXD-7 sensor

- Preparation of F1 submission
  - Design of remaining blocks (Clock delay, Injection DAC)
  - Optimization of available blocks (ADC, Reference, Digital Part)

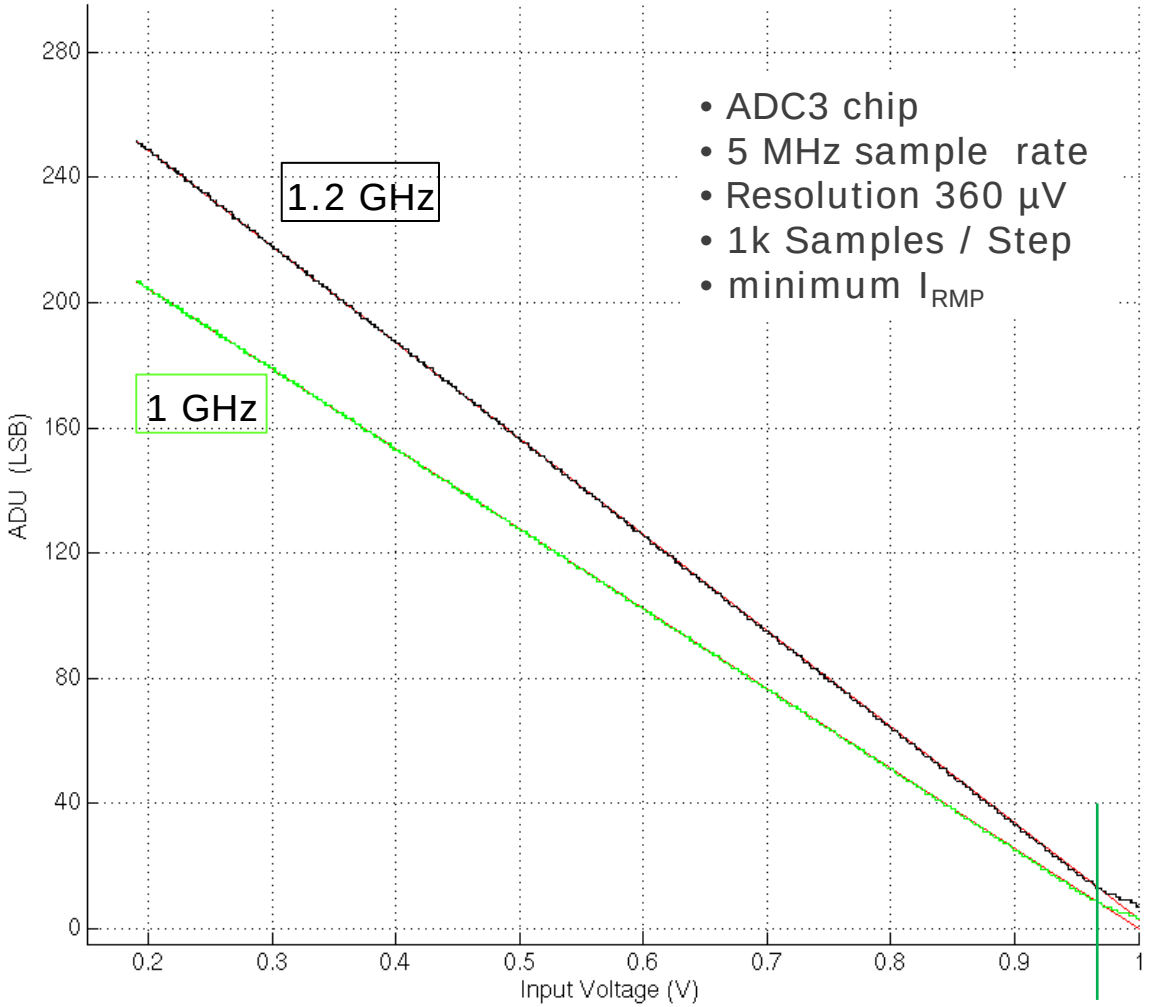
- Test Setups
  - Commissioning of ‘standard’ setup
  - Design of new setup to test full readout chain

- Time / Submission Plans

MEASUREMENTS

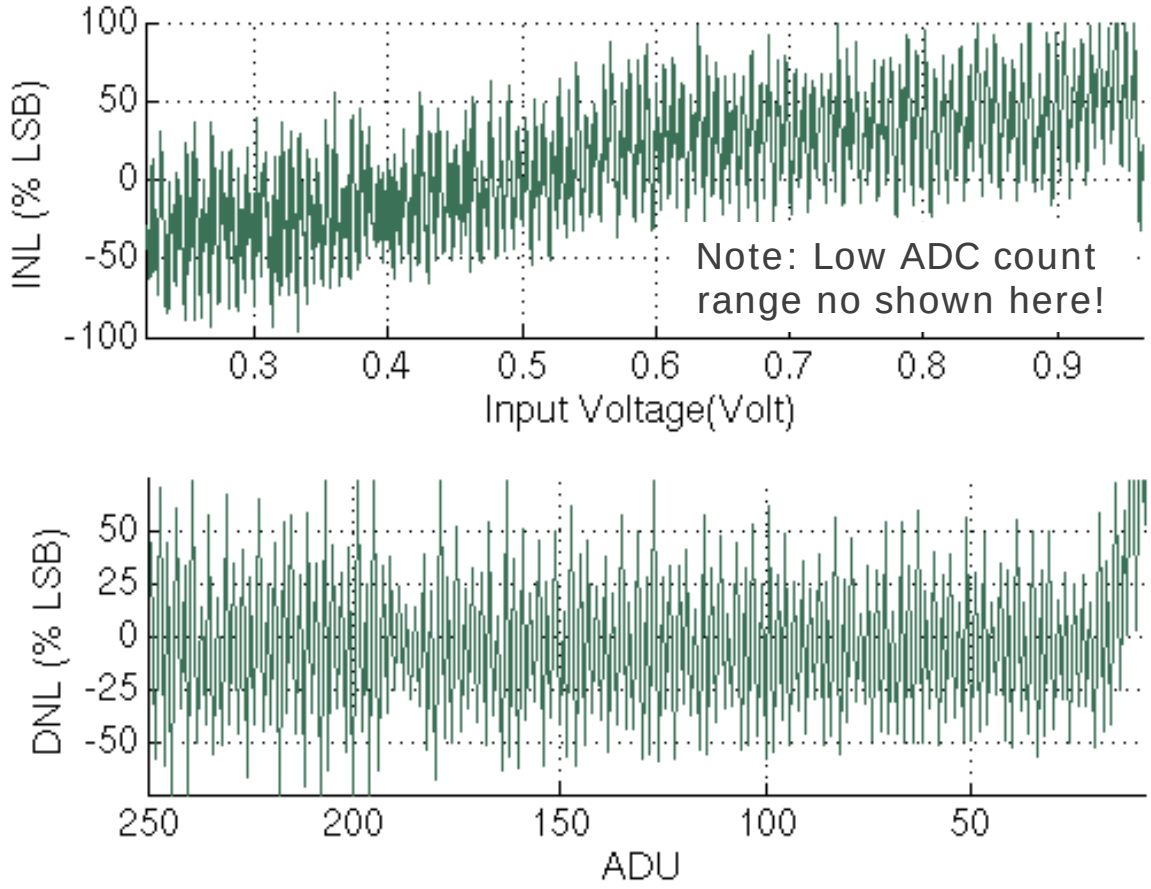
ADC at High Speed

- Increase nominal clock speed from nominal 700-800 MHz to **1 / 1.2 GHz** (!) (bin width 500/417 ps)
- GCC (standard cells) still operates
- BW of TX / CPWG / RX ok!
- Still very **nice** curves!!
  - Kink for small ADC codes not yet understood
- This is another ‘knob’ to globally change ADC gain



DNL/INL @ 1.2 GHz

- No missing codes, monotonic counting. INL < ±1 LSB, Max. DNL < ± 0.7 LSB

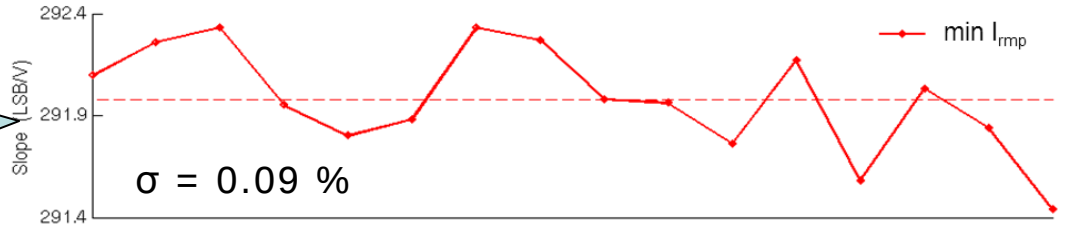


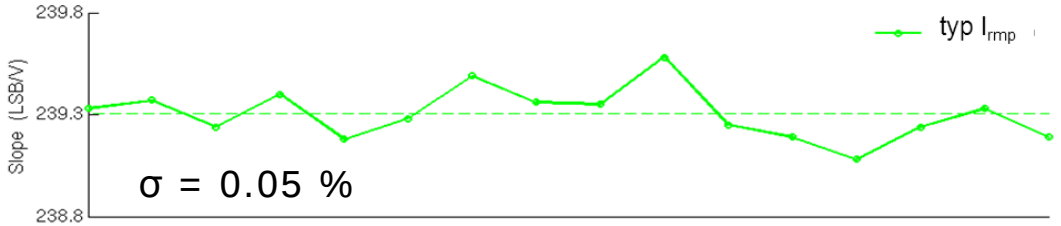
- Even faster speed probably limited by IO pads

ADC Ramp Current & Delay Step (I)

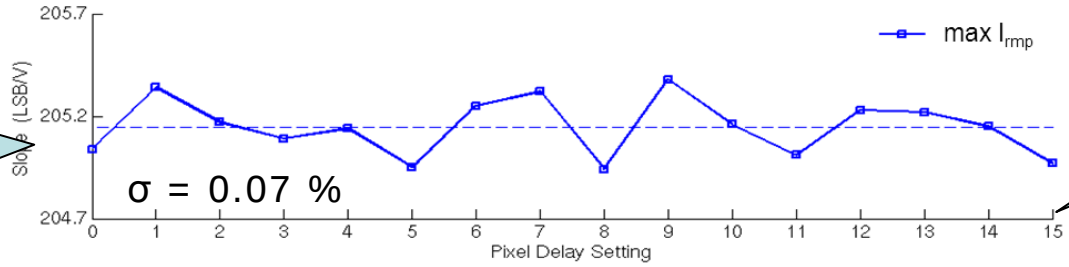
- Previous data analysis indicated a correlation between the ADC ramp current I_{rmp} and the offset setting = pixel delay
- Detailed studies on ADC3 and MM3 showed NO (significant) effect
- Example: Ramp slope (fit over full characteristic) for fixed I_{rmp} vs. Pixel Delay:

Slow discharge





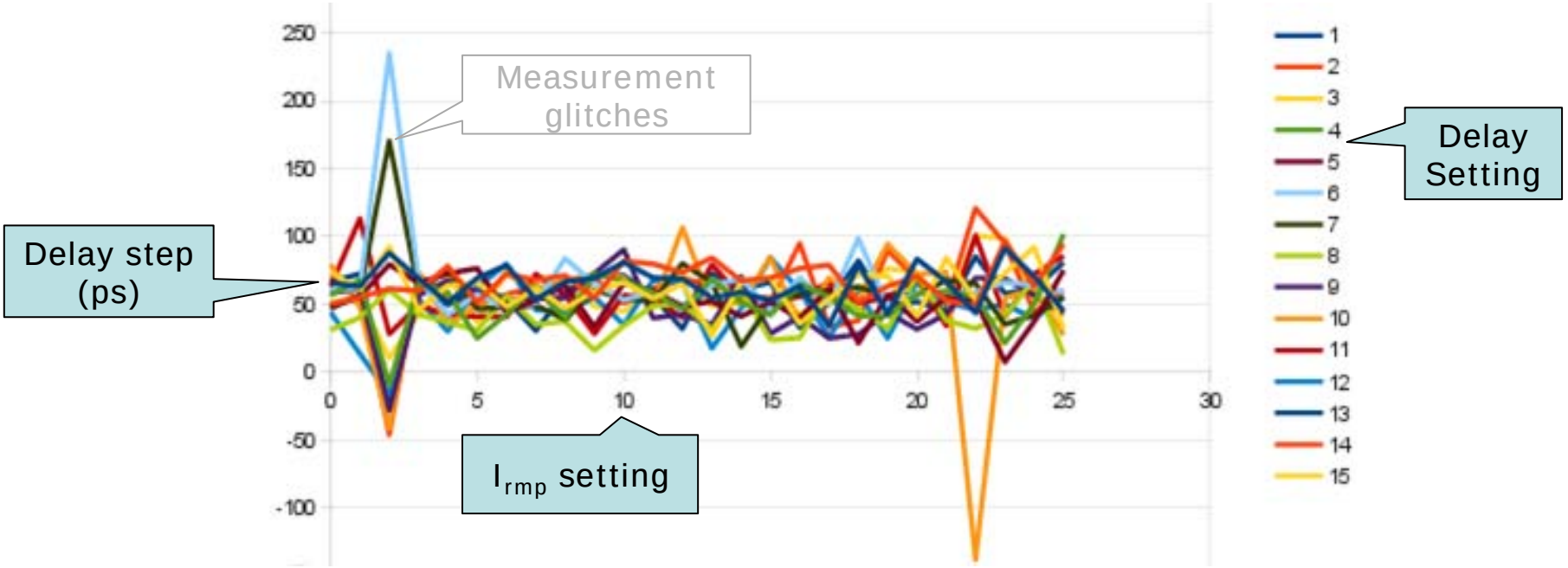
Fast discharge



Pixel Delay Step

ADC Ramp Current & Delay Step (II)

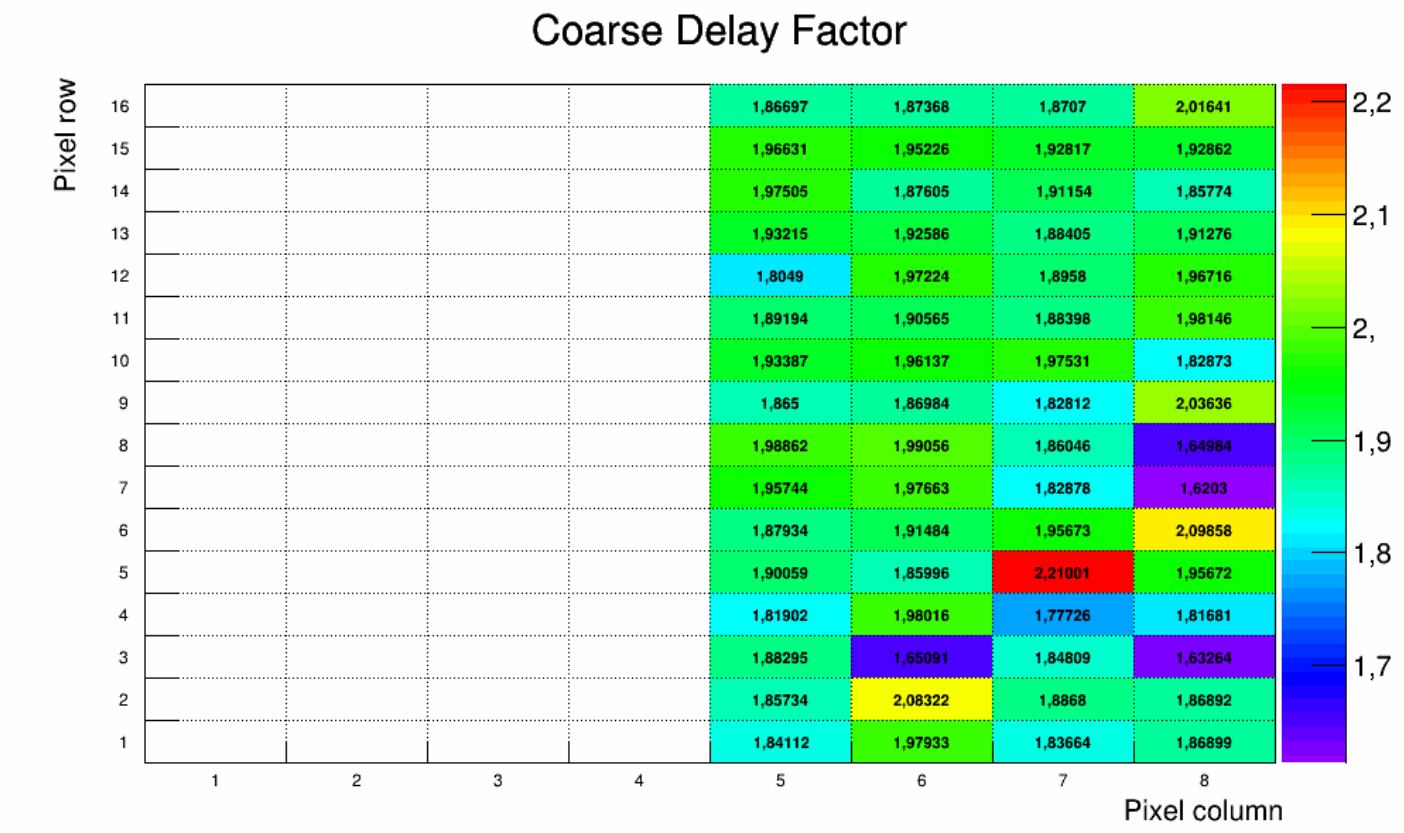
- On MM3, delay steps (1→2,..) were measured (@ Hit Out) as a function of I_{rmp}
- No systematic effect visible within measurement resolution



- There are still some correlation effects in analysis of available data. We need to find out if this are analysis artefacts, for instance from systematic effects in the determination of the bin boundaries

Delay Bin Size

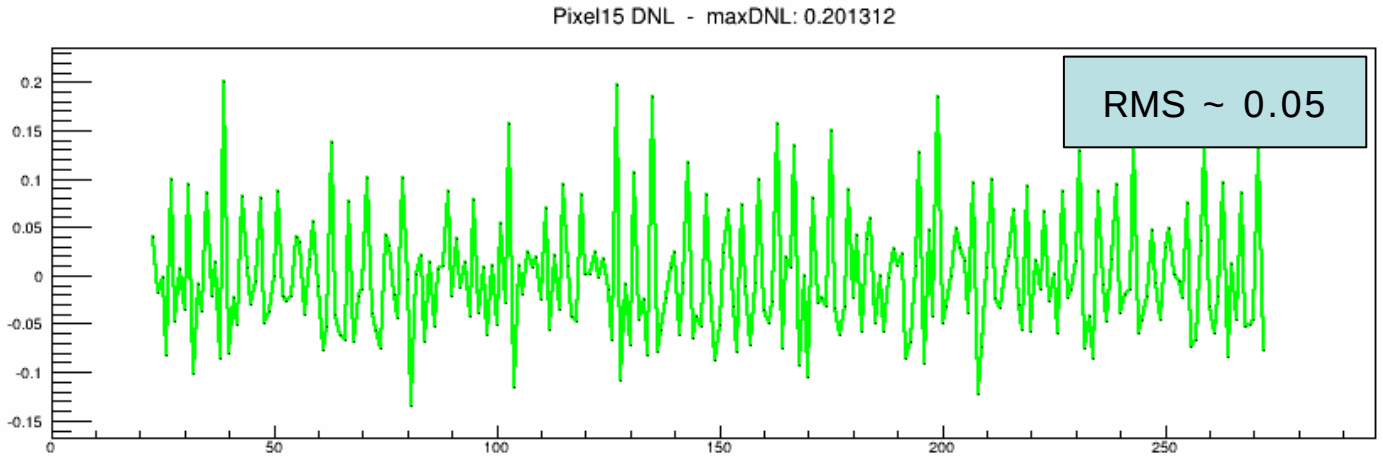
- Can set delay *step* to ‘coarse’ (~120 ps) or ‘fine’ (~60 ps) in every pixel
  - Compromise between resolution and range
- *Ratio* between coarse and fine range ~ 1.89, σ = 0.1 (design: ~2.0)

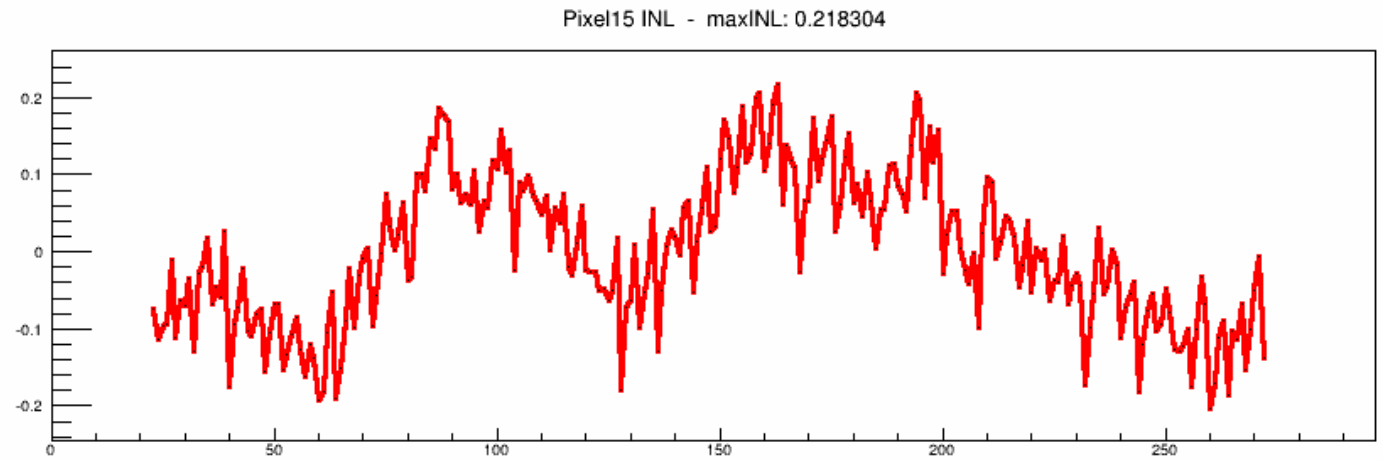


- Some outliers must be understood. Yield?

Best DNL / INL in MM3

- Measured with GCC counter via GCC start value (no ramp effect!)
- Similar to DESY results on ADC_3 chip





Difference in ADC S&H Caps

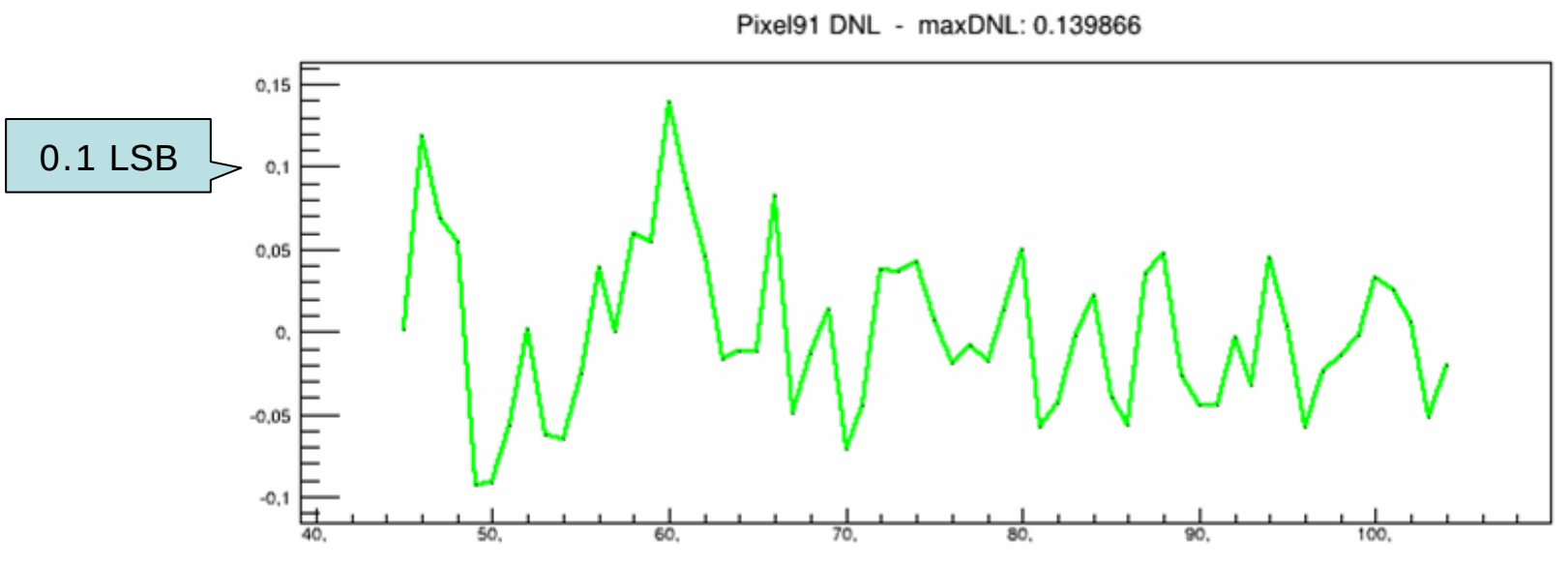
- Each pixel has two sample and hold (S&H) capacitors for double buffering.
- As only one set of trim values is available for both capacitors, their matching is important.

- By separating the ramp slope measurements into odd and even events, corresponding to C_{SH1} and C_{SH2}, the relative capacitor values can be determined.

- Measured mismatch is < 0.14 % which is negligible in this application

ADC with In-Pixel Counter (MM3)

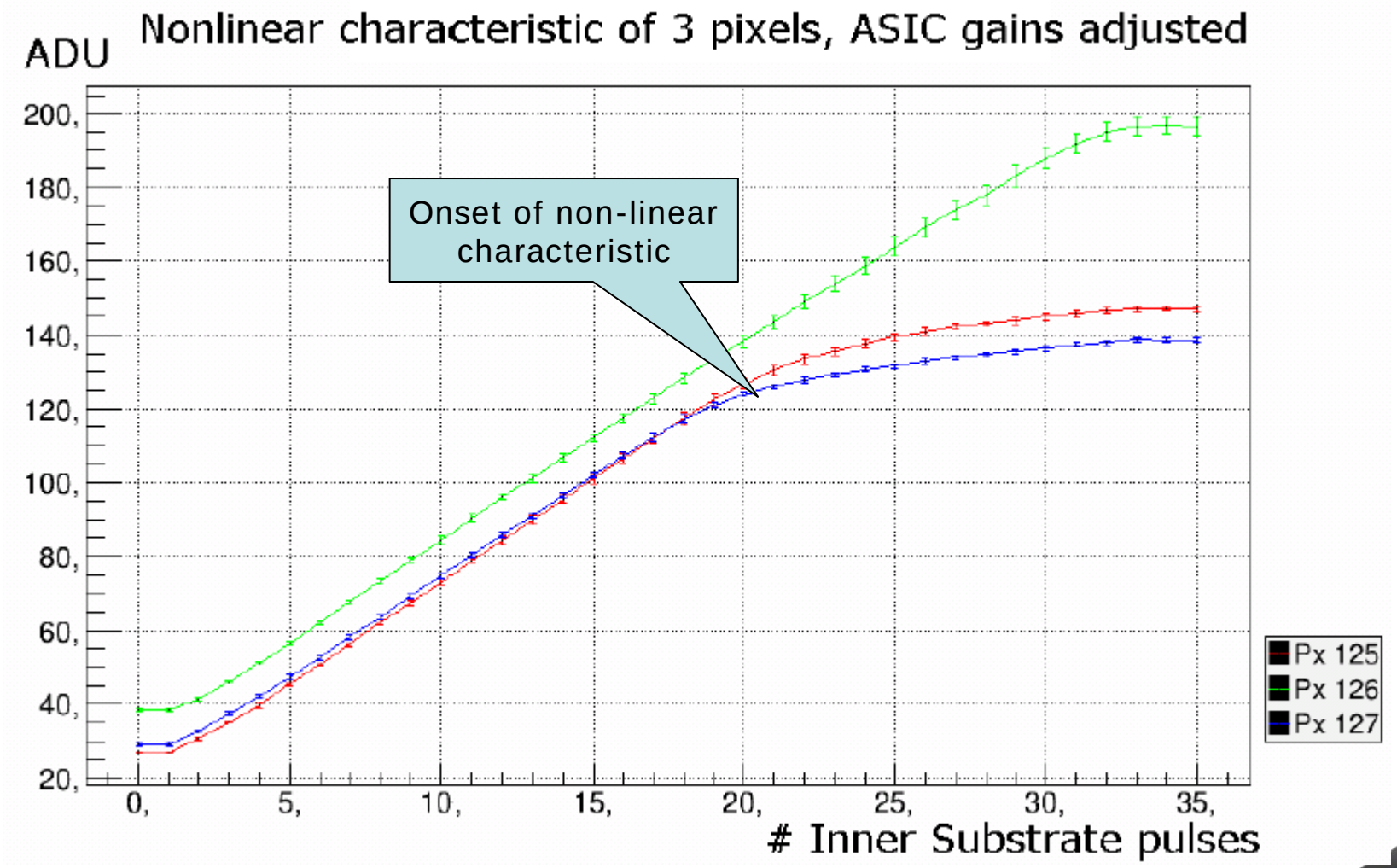
- Delicate operation (supply voltage dependence). Cause not yet understood
- Good pixels show *excellent* DNL in working range



- Will pursue this path in parallel in new test chip

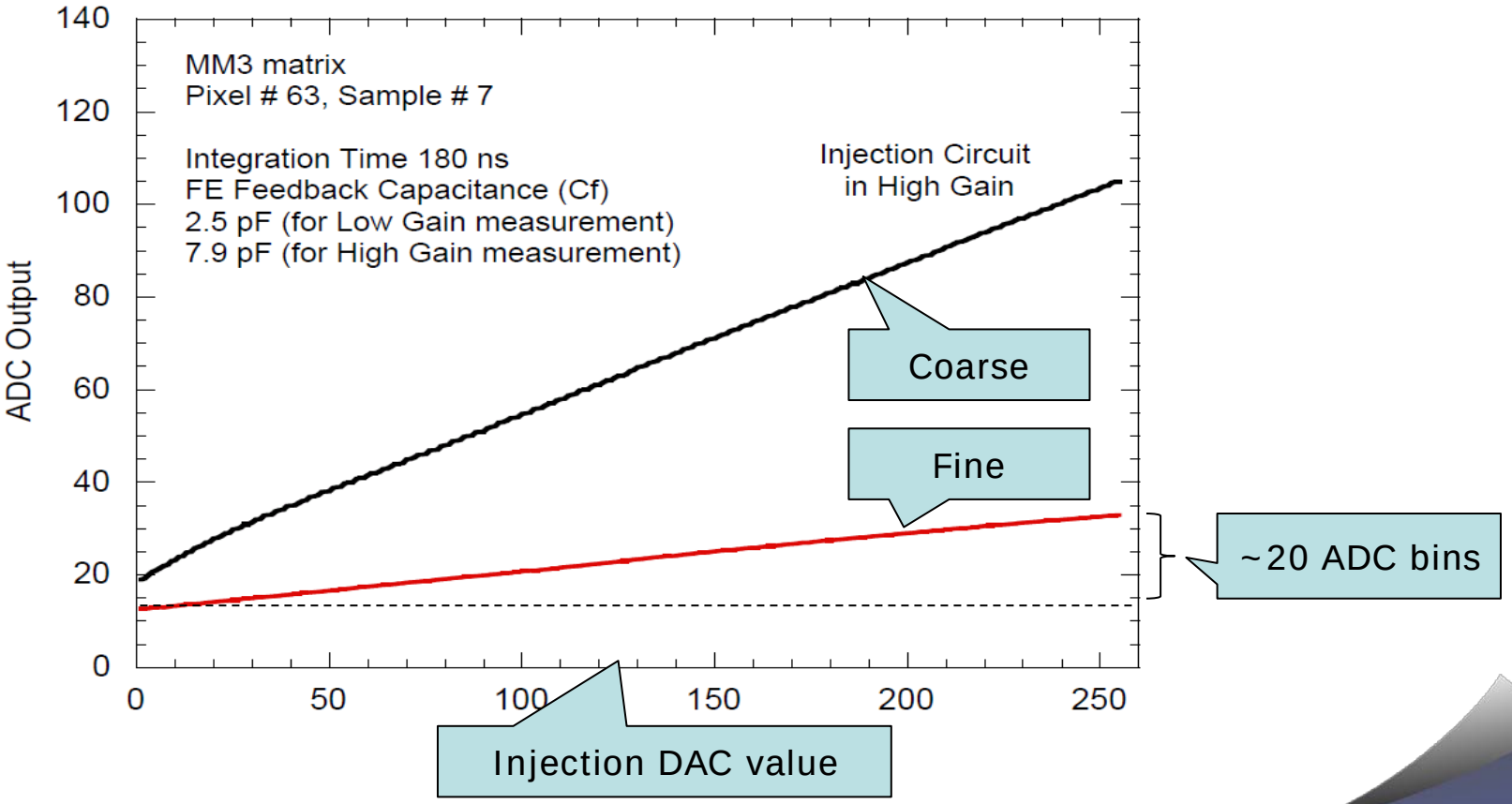
MM3 + PXD7 (Cut Gate Structure)

- A new PXD7 DEPFET is available as a Hybrid
- This is operated in MM3 setup using inner substrate pulsing



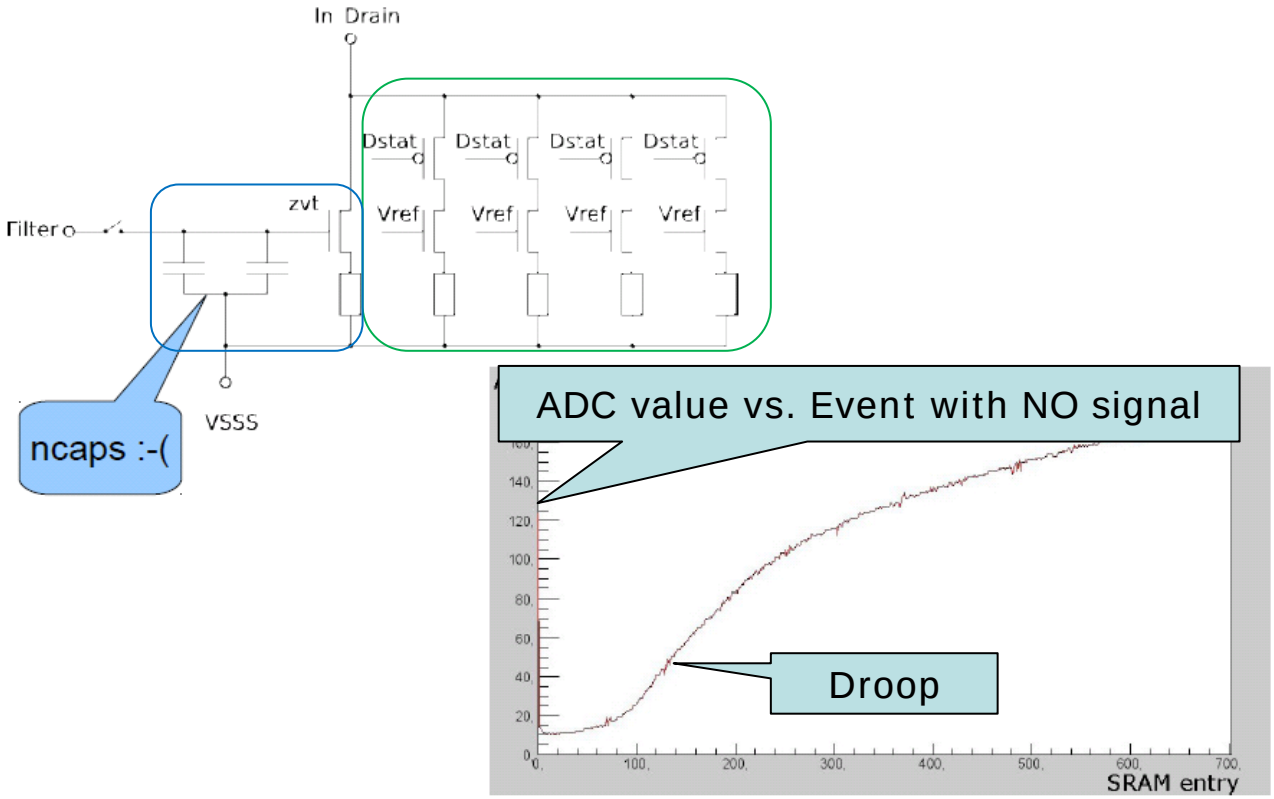
Pixel Injection

- The Pixel Injection Circuit is now integrated in every pixel and is operational
- It offers
  - a *fine* mode (~20 Injecti Bins per ADC bin) to study the linear part
  - a *coarse* injection mode (~ 10 x *fine*) to inject large signals.



Issue: Drain Current Comp. S&H

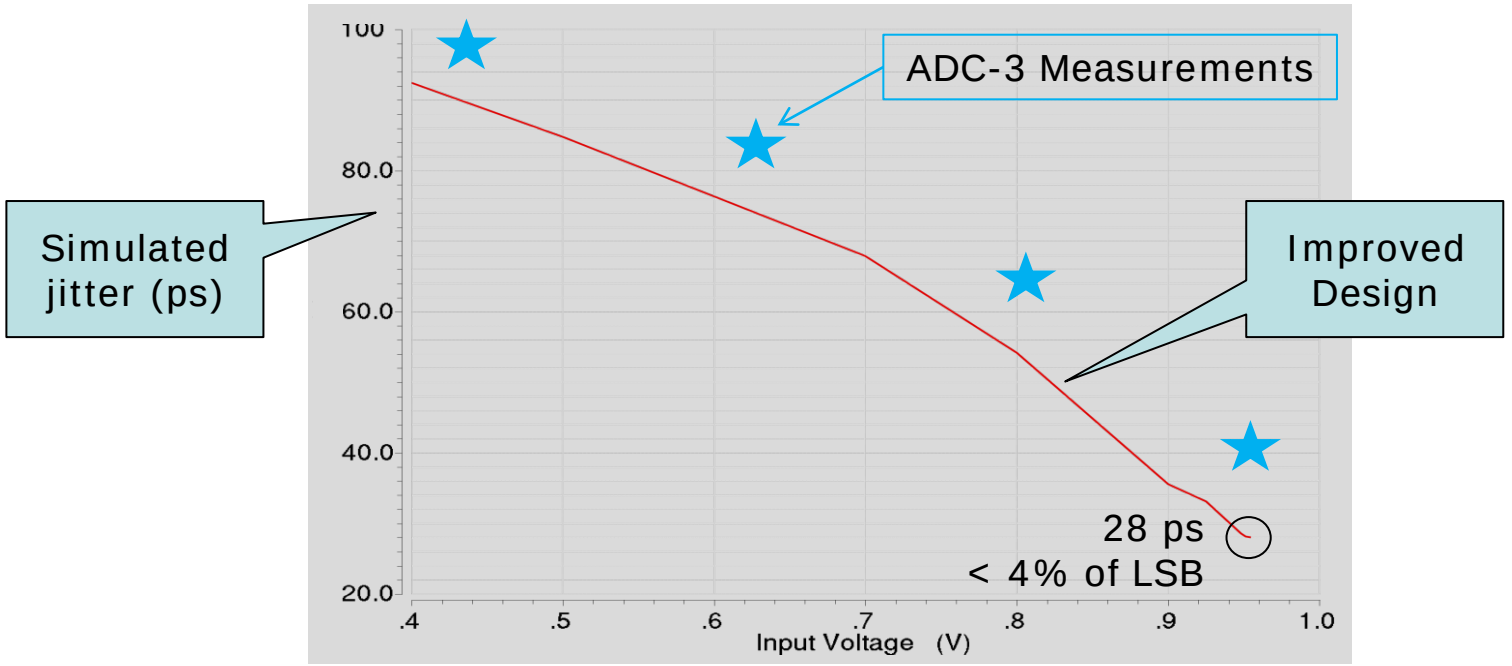
- The DEPFET Drain Current is absorbed by
  - a current DAC (coarse value)
  - A dynamically adjusted current source with Sample & Hold cap (residual)
- This cap has been changed from MiM → ncap (space reason) and is now leaky!
  - Must replace it by dgncap in next chips



Work on Building Blocks

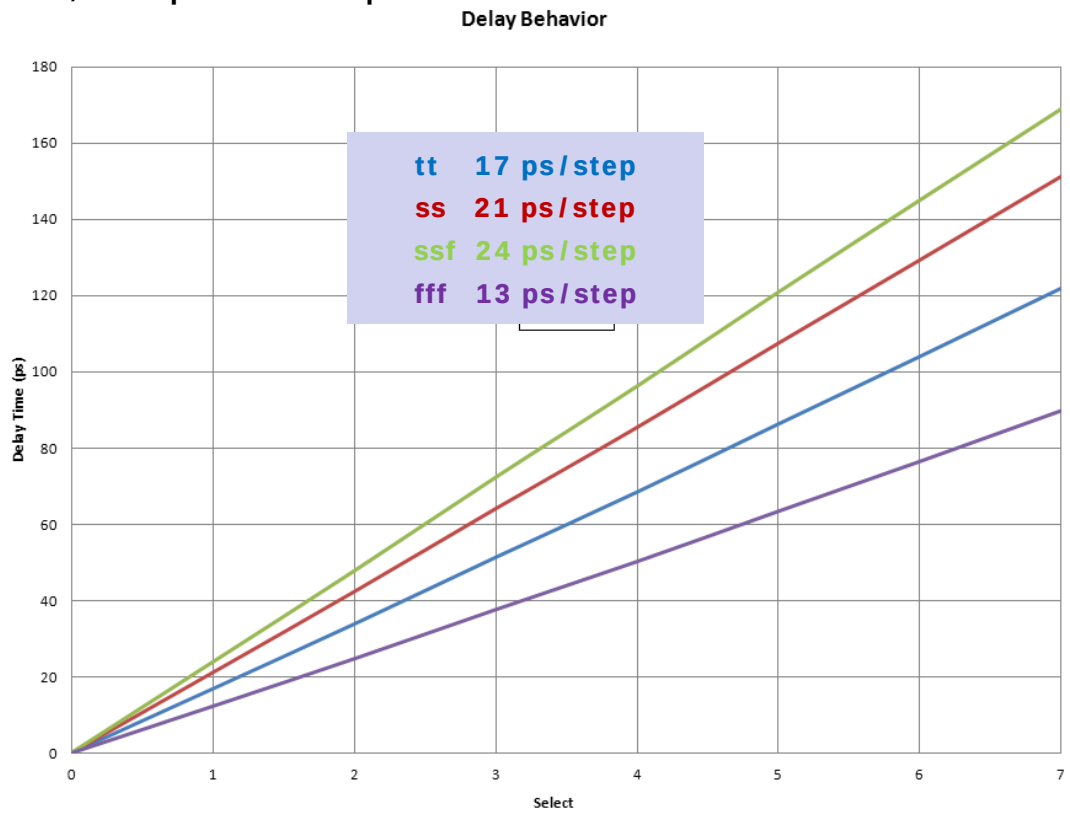
ADC Improvements

- ADC Comparator current is doubled (to 24 µA, 130µW) to reduce Jitter from 30 ps to 18 ps.
- The Full ADC has now simulated 28 ps jitter at small amplitudes.
- Bias generation is shifted to reference, design is area neutral.



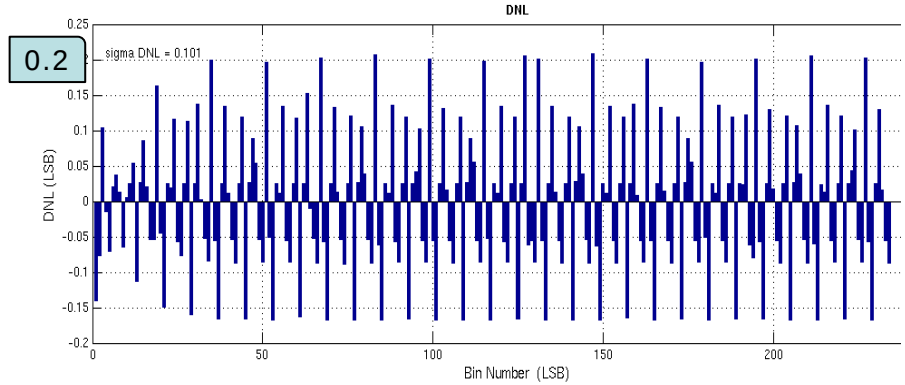
ADC Improvements

- A new *Delay Line Circuit* allow to adjust edges of clock and inverse clock going to the GCC. This can be used to minimize DNL.
- Implementation uses inverters loaded with variable # of caps
  - less variation across corners than inverters
- 3 Bits / side, Step is ~ 20ps.



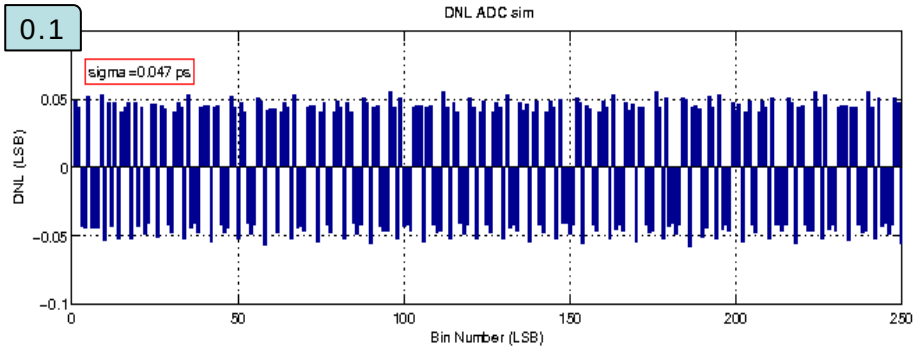
ADC Improvements

- The interface GCC → TX has been modified (two clocks are merged) to remove observed periodic DNL (of period 16).



OLD (sim)

- Now simulated DNL is 0.05 LSB:



NEW(sim)

Simulation @ ss case, last pixel

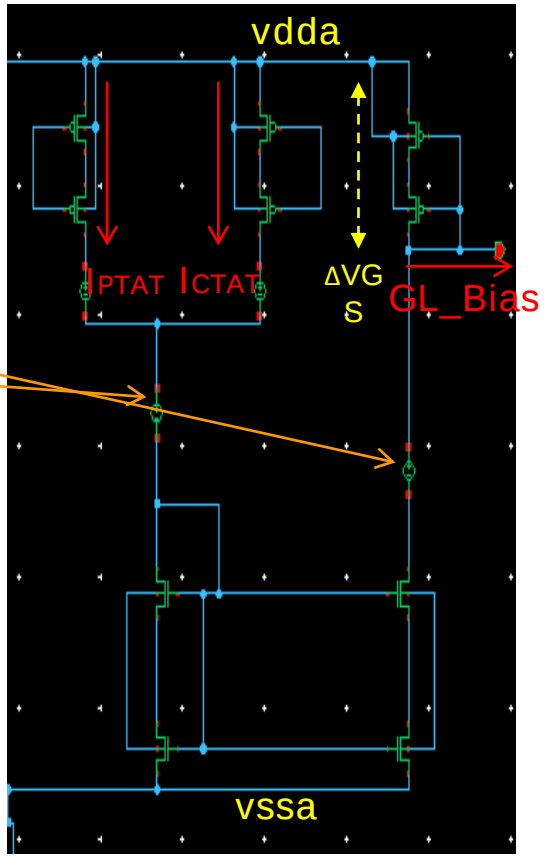
800 MHz clk, bin width 625 ps

Bias Cells

- Reference block (@ chip sides) has been simplified.

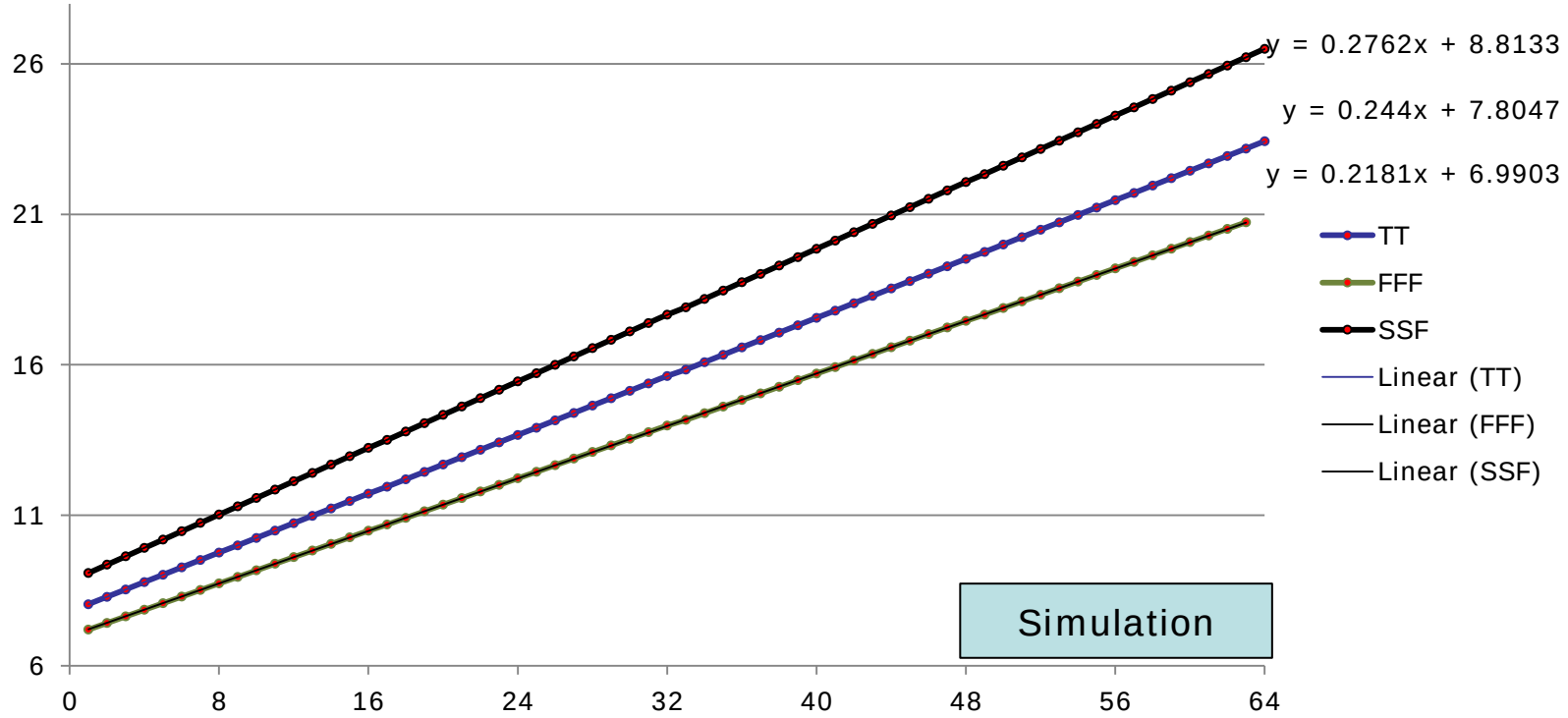
- Only one signal transported to pixels
  (PTAT and CTAT merged in periphery)
  Variation (1.1 ... 1.4V):
  0.5% in ref, 1.5% after current mirror

- No more buffer of distributed signal
  - Slightly slower turn on, but no offset



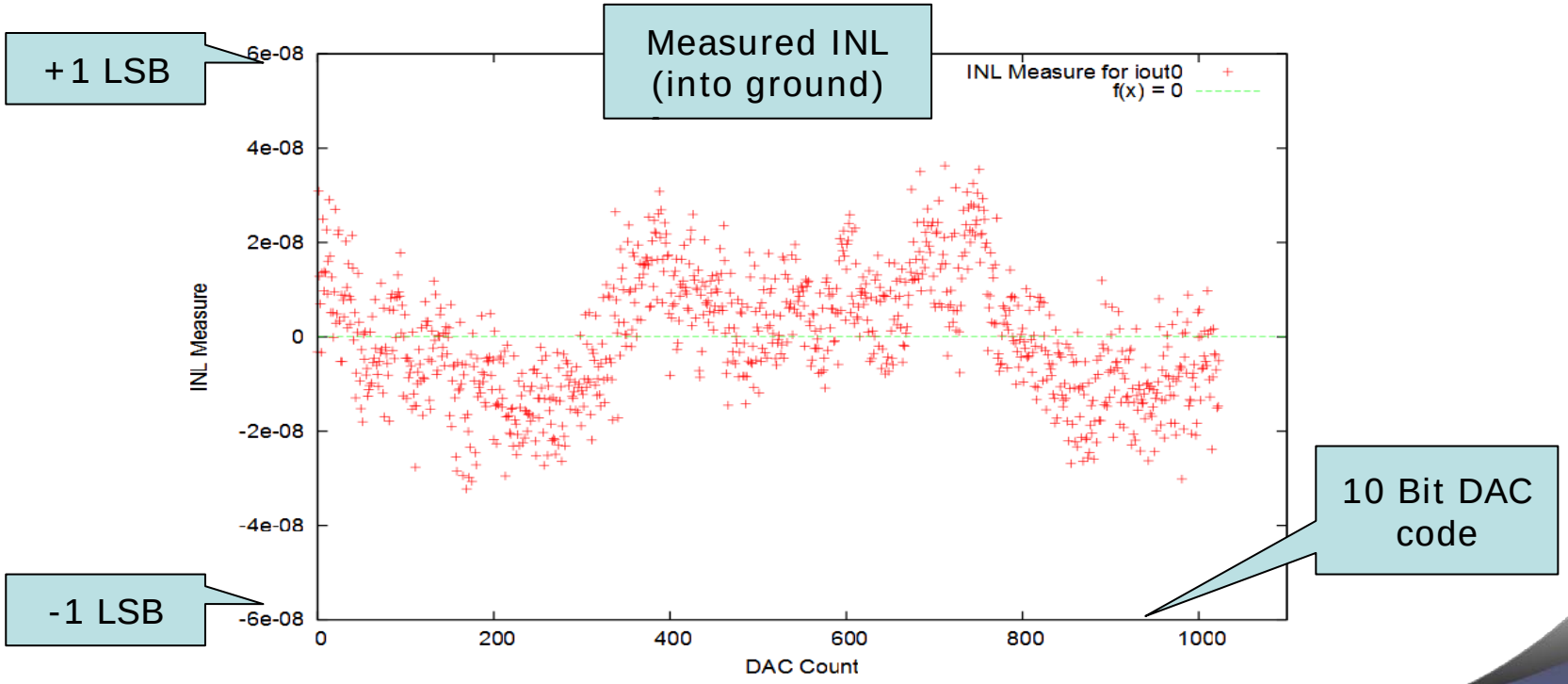
I_{ramp} DAC in pixel (for gain setting)

- Linearity has been improved
  - Use low power MOS and different scheme to add voltages



High Resolution Calibration DAC

- ADC tests in Laboratory often use a precise voltage source
- → Have decided to integrate a high resolution (static) voltage DAC on F1 and distribute signals via monitoring lines to all pixels
- DAC is based on already prototyped 10 Bit Current DAC with INL < ±0.5 LSB
  - It uses segmented unit current sources & thermometer encoder
- 4 of these DACs will drive in parallel into a resistor to provide 12 bit Voltage



Further Blocks

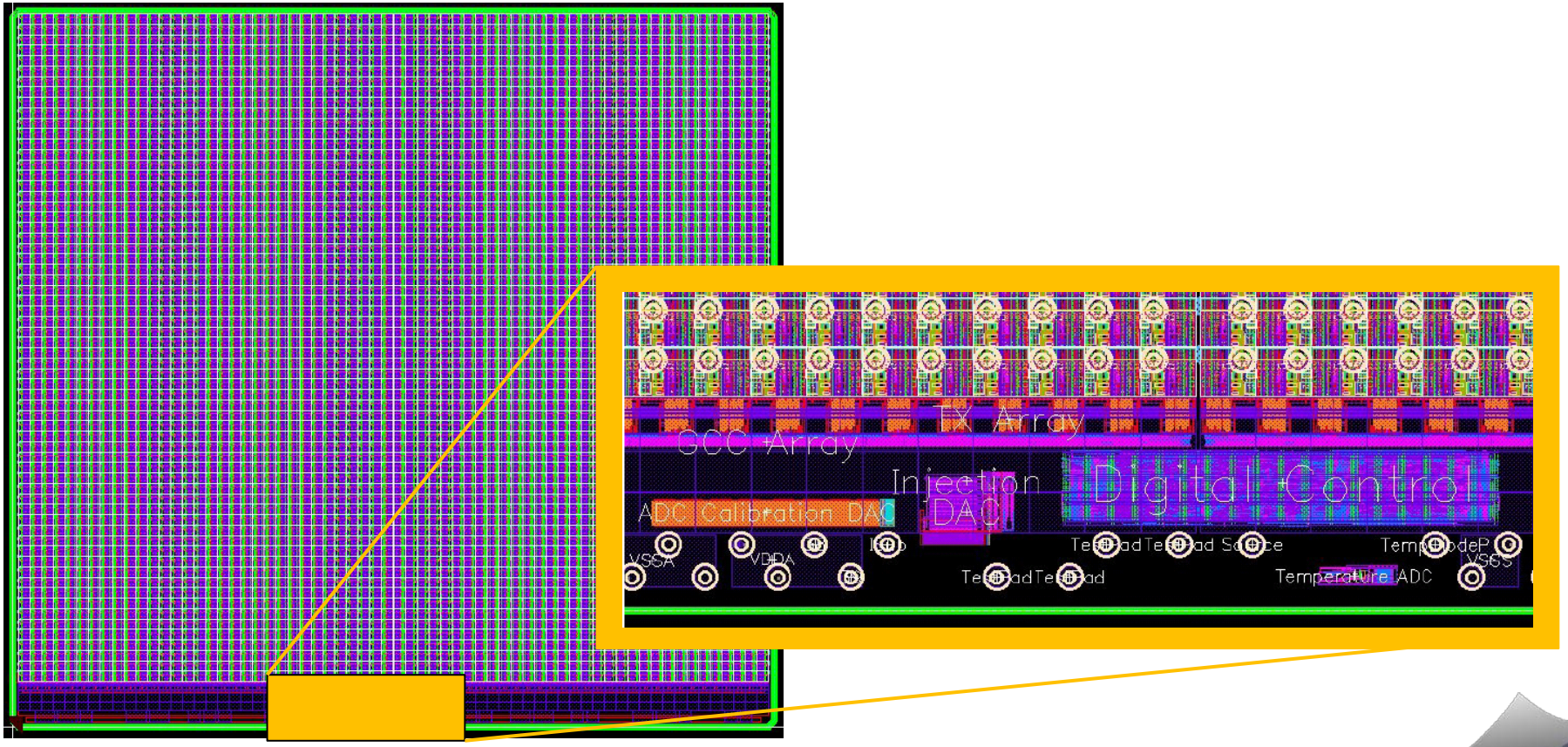
- Pixel
  - RAM size has been increased from 640 → 720
  - All new block versions will be integrated
  - Will use GCC ADC

- Digital Verilog Code (Global Part):
  - Some small bugs have been removed (sequencer, veto)
  - Additional state in Main FSM has been added to pulse reference @powerup
  - Readout is extended to full matrix
  - Some test features (check sum, ...) will be added to burst trailer

- Temp. ADC is available (voltage tests successful, temp. tests soon)

Layout

- Peripheral part is much smaller than space reserved (early on...)
- Plenty of space for power busses & decoupling caps (?)

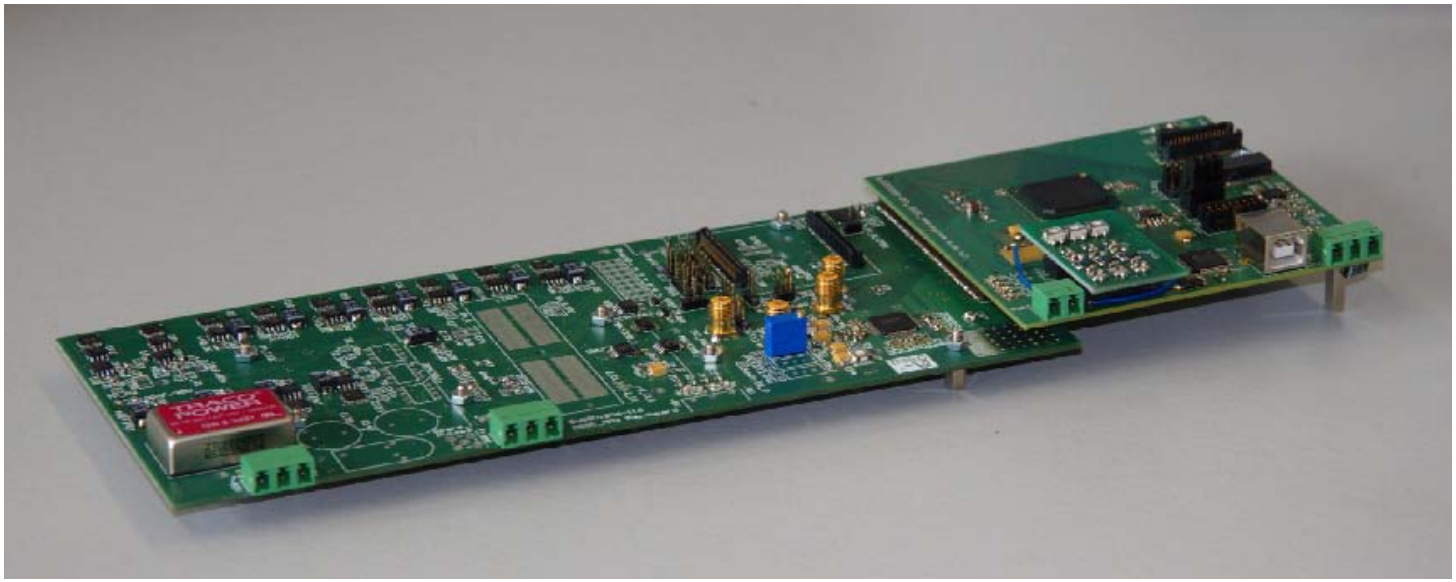


Test Setups

‘Standard’ Test Setup Installations

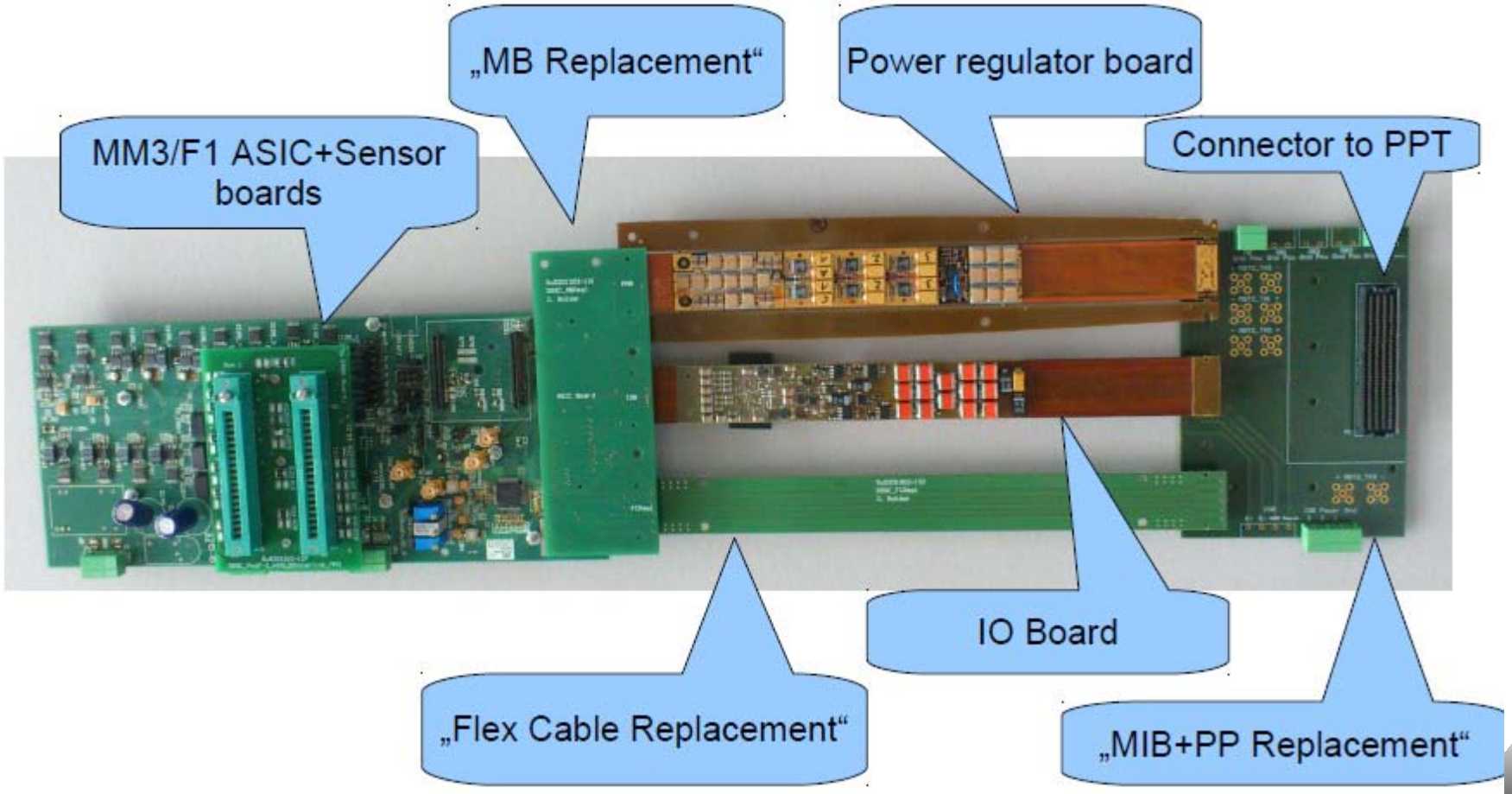
- Additional test setups are now operated in
  - Munich
  - DESY
  - Bergamo

  after (usual) initial setup problems (Linux Versions,...)
- Training workshops have been held to increase number of knowledgeable users



Putting All Components together

- New test setup replaces custom FPGA board by a collection of final components.
- IOB, Reg. Board and interface to PPT connected via multiple PCBs
- Control & data readout will be via PPT

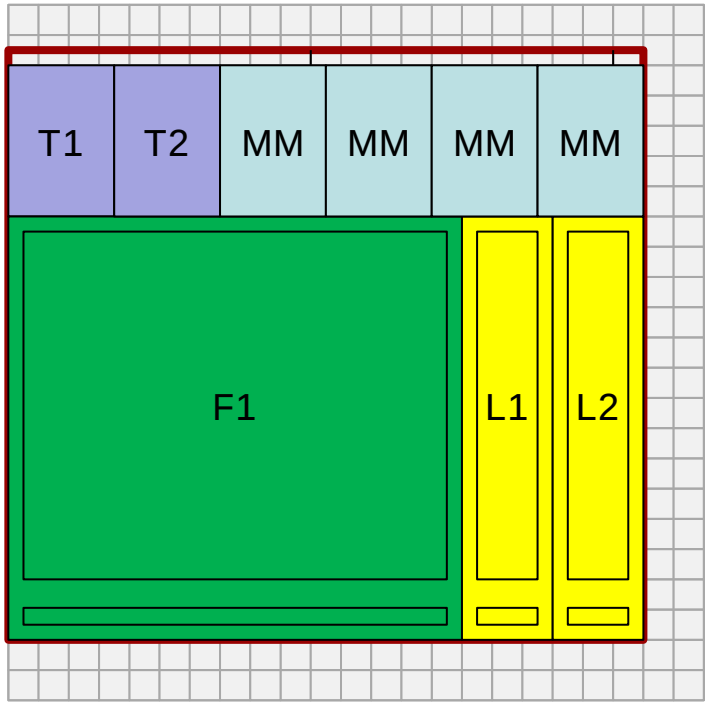


Submission Plans

Possible Reticle

- Reticle Size @ IBM: 21.0 × 19.5 mm^2
- F1 Size: 14.904 × 14.005 ~ 15.0 x 14.0 mm^2
- Mini Matrix (MMx) Size: 3.2 × 4.8 mm^2

- Reticle has space for
  - **1 x F1**
  - 'long test Chips' **Lx**
    - » ADC alternatives
  - Mini Matrix Chips **MMx**
    - » MM4 with improved power busses
    - » MMx
  - Test Chips **Tx**
    - » ADC4 (DESY)
    - » (Milano)



Time Plan

- Still not really fixed

- F1 should be back 30.8 according to present time plan
- We think it is sufficient to get the chip back *end of this year* to be ready to start full sensor size tests

- Later submission leaves more time to make ‘cost neutral’ test chips
  - ADC variations
  - Improved MM4 matrix (no power snake) for simplified sensor tests
  - Front-End Versions

- → Submission targeted *latest* End of August

THANK YOU

Module Construction

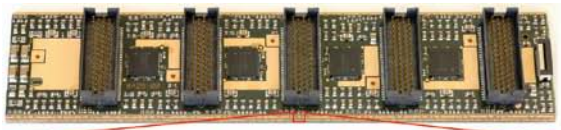
Karsten Hansen

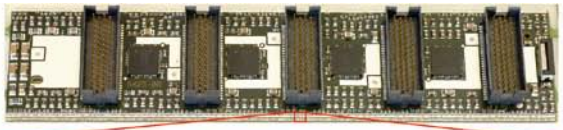
1. Main Board & Frames
2. Focal-Plane Setup
3. Electrical Tests

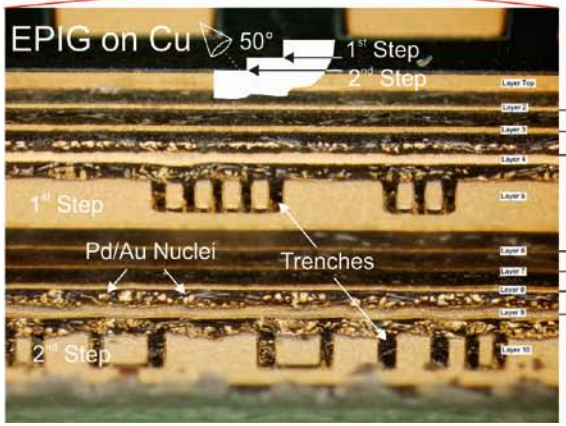
Component Status: *Main Board*

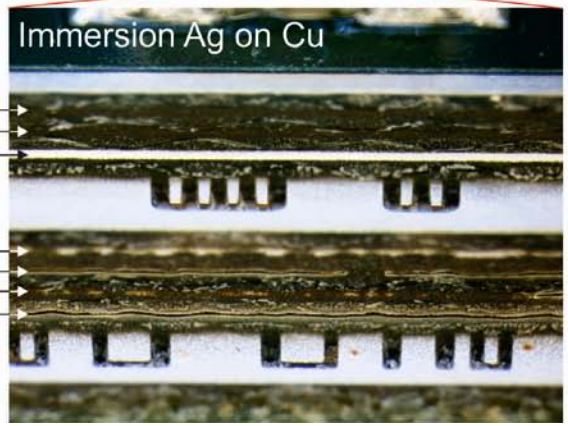
FR-4 Main Boards

LTCC-Main Board









Difficulty

- *Finishing → Pd Nuclei*
- *Laser → Trenches*
- *Cutting from Frame*
- *E-Test w/o Bond Pads*

Remedial Actions

- *Special Rinsing (tbd)*
- *Laser-Direct Structuring (tbd)*
- *Test after Assembly*

Difficulty

- *Tarnishing → Bonding*
- *Laser → Trenches*
- *Cutting from Frame*
- *E-Test w/o Bond Pads*

Remedial Actions

- *Surface Activation (tbd)*
- *Laser-Direct Structuring (tbd)*
- *Test after Assembly*

Difficulty

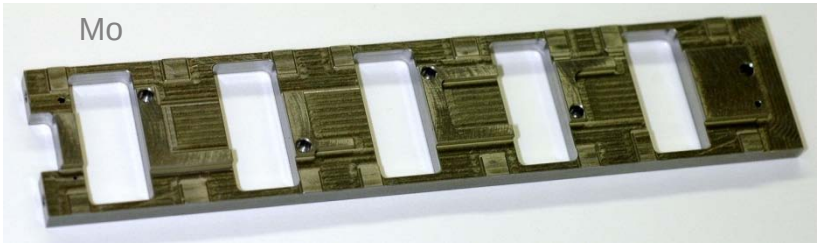
- *Clamping for Assembly*

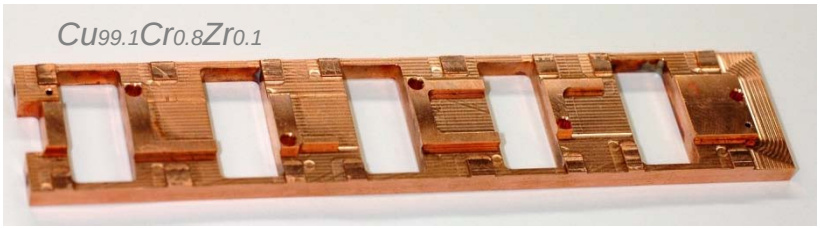
Remedial Action

- *Soft Materials*

Component Status: *Frames*

Main-Board Frames

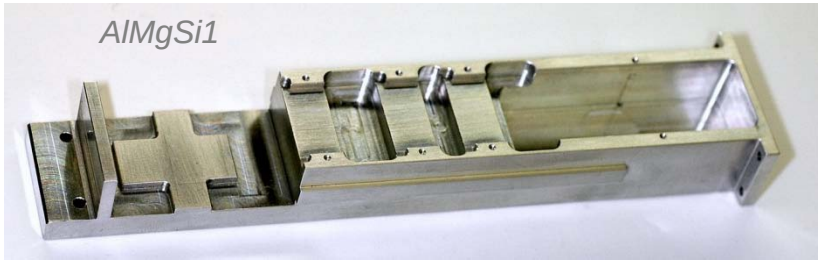


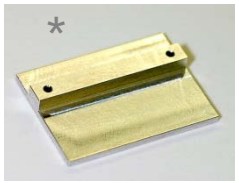


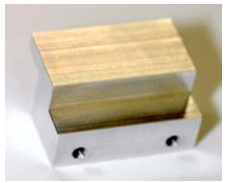
Difficulty
- *300-µm Frame-to-Device Distance too small*

Remedial Actions
- *reshape Frame*
- *increase Gap Size to 500 µm (HV Safety)*

Regulator Board





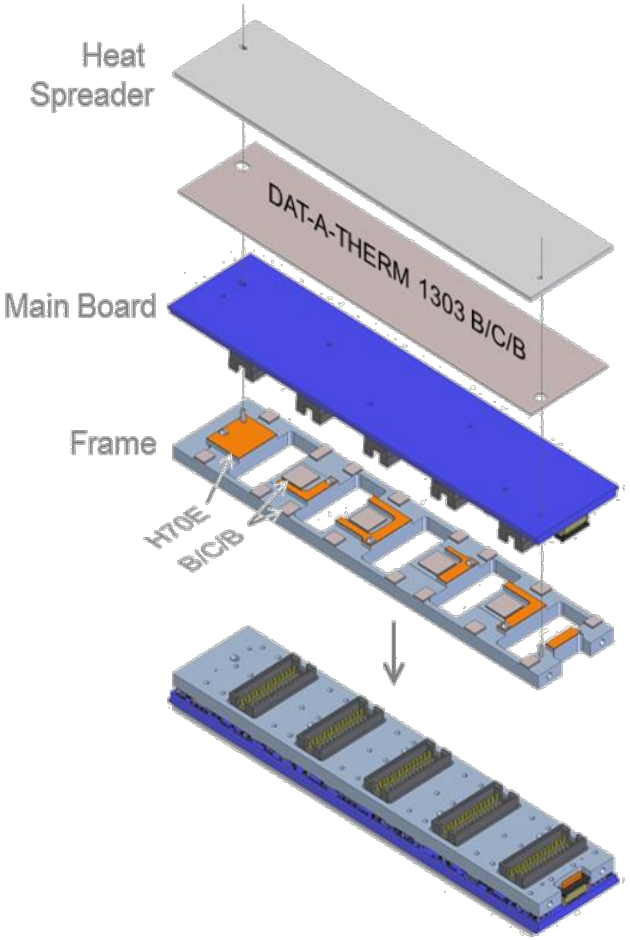


Difficulty
- *Hot Spot*

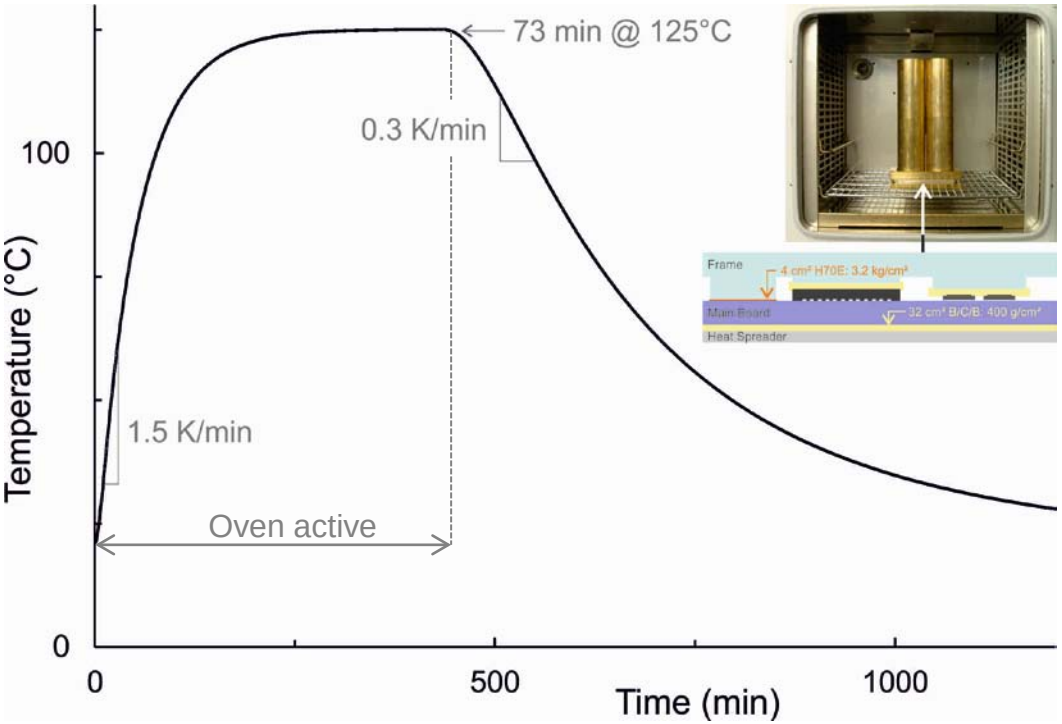
Remedial Actions
- *reshape Frame Part **

Focal-Plane Package Setup: *1st Step*

1st Setup Step



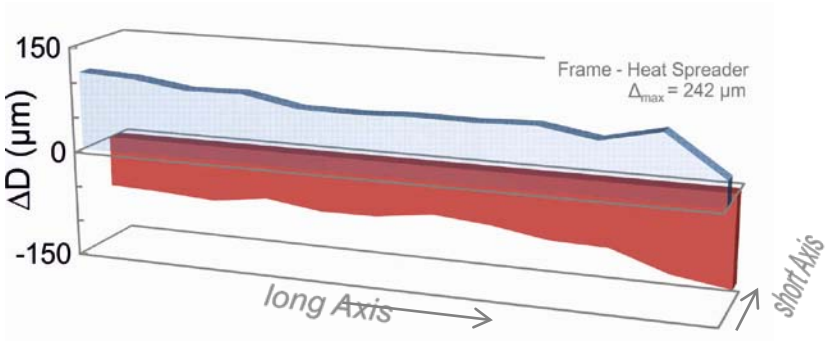
Oven Setup & measured Temperature Profile

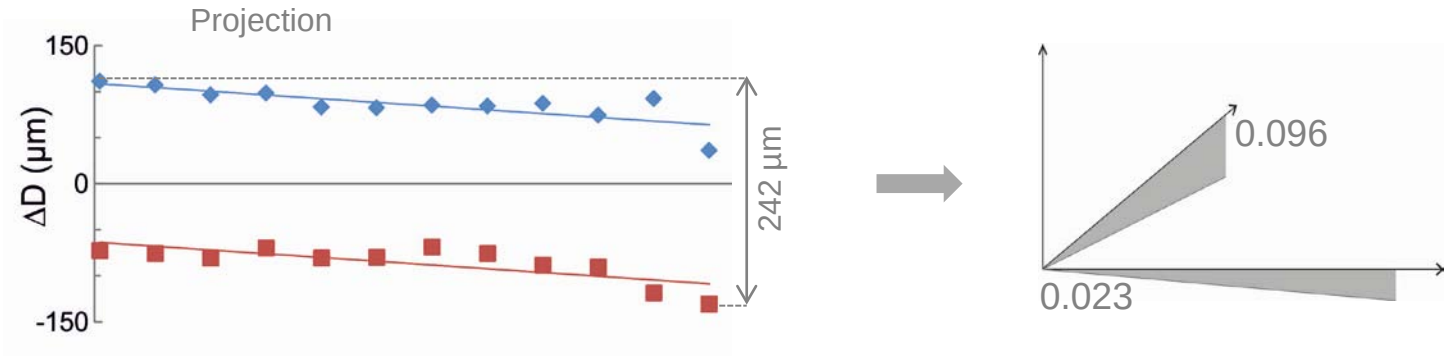


~ 1 Day per Module

Focal-Plane Package Setup: *1st Step*

Frame-to-Heat Spreader Height Profile (old Parts)





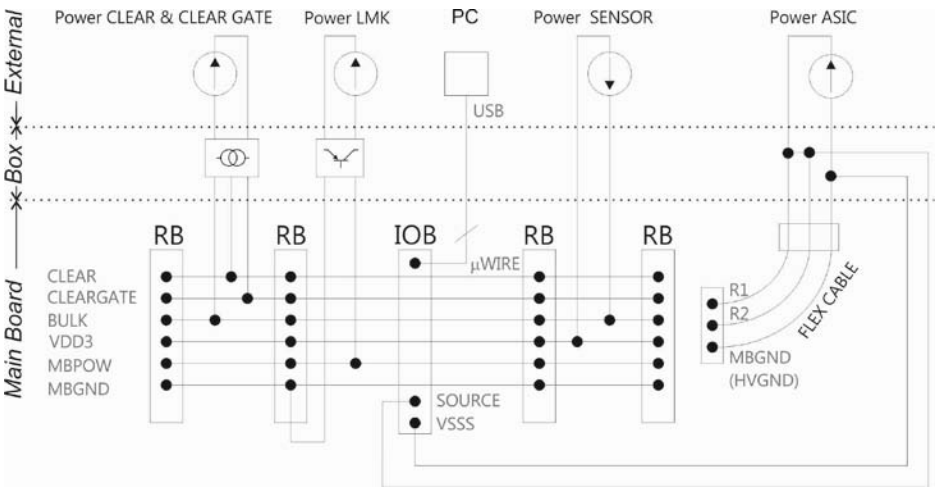
Preliminary Result

- *very small Tilt with old Parts*
- *large Height Differences between ASICs & Heat Spreader*

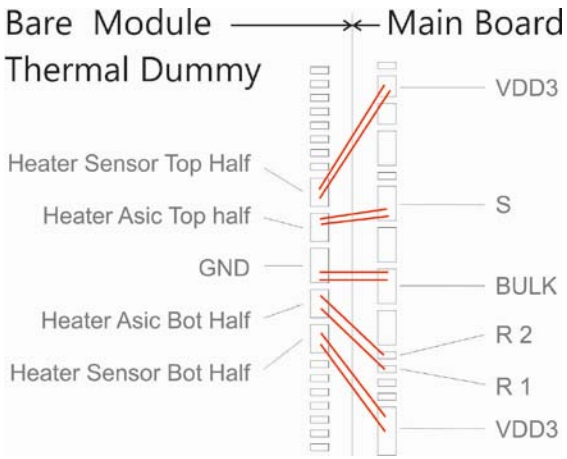
- *Therm-A-Gap 579 instead of B/C/B*
- *use Gimbal Tool or only Placement (2nd Setup Step w/ Femto)*

Thermal Imaging: *Main-Board Test Setup*

Test Setup



Wire Bonding

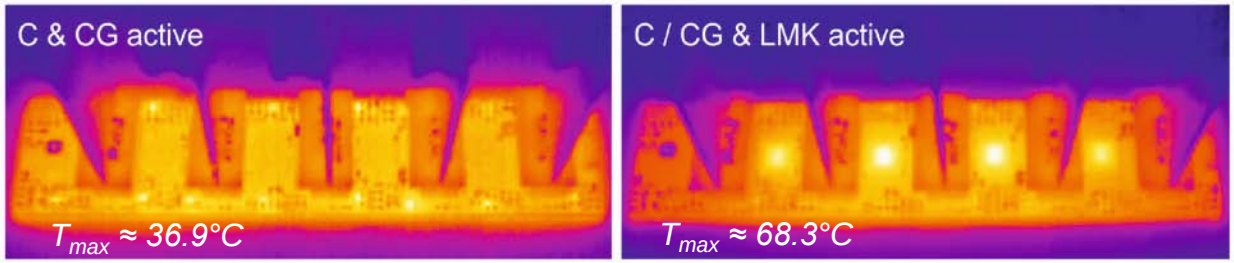


Result

- *thermal Tests with real Main Boards*
- *only PC & 4 Power Supplies needed*
- *visible Assembly Layer*

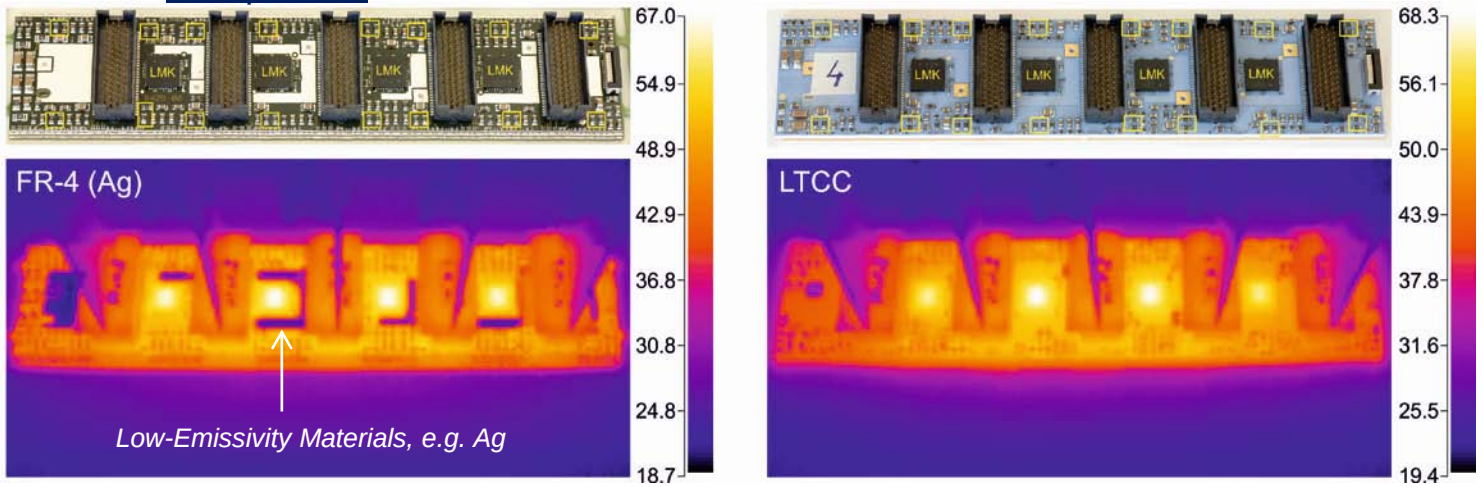
Thermal Imaging: *Results MB*

Clock Distribution & Clear-Pulse Generation (LTCC MB)



Free Convection

Comparison



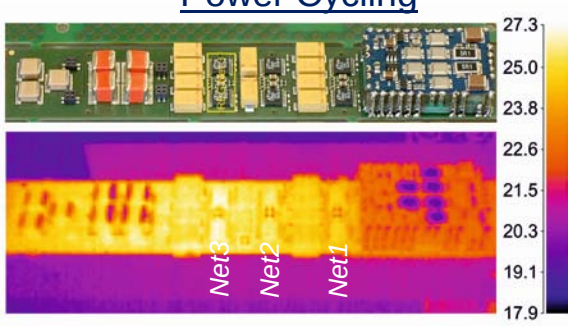
Values in °C

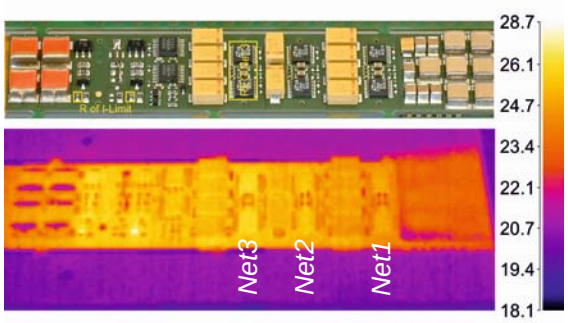
Result

- *MB shows highest Temperatures*
- *FR-4 MB behaves very similar to LTCC MB*

Thermal Imaging: *Results RB, GD & MA*

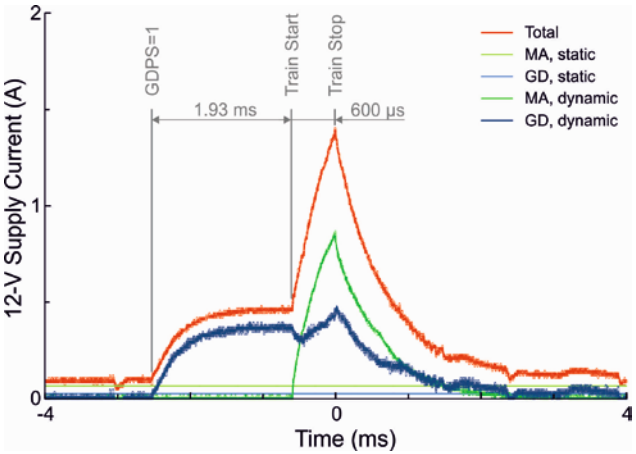
Power Cycling

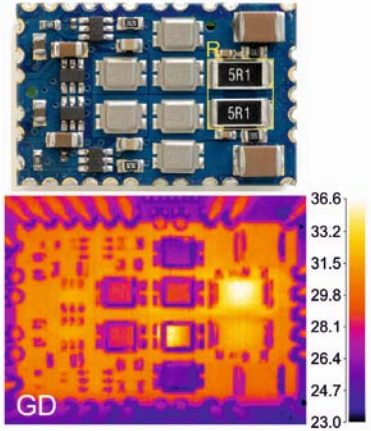


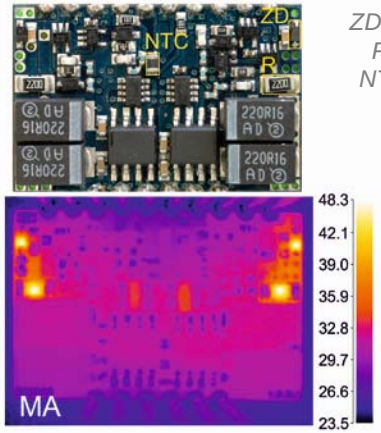


Result:
- *moderate Temperatures*
- *Hot Spots caused by Resistors of Net-3 Current Limiters*

Clear-Pulse Generation







ZD.....Zener Diode
R.....Resistor
NTC..Thermistor

Result
- *activate Resonant Converter 1.9 ms before Train Start*
- *Hot Spots on MA caused by On-Board Supply-Voltage Generation*
- *Hot Spot on GD caused by 5-Ω Clear-Output Resistor*

Thermal Imaging: *Summary*

Component		Mean Power (W)		T_{max} - $T_{Ambient}$ (K)	Device	Sensor
MB	Clock Distribution	*3.234*		*48.9*	*LMK*	*n. a.*
	Line Termination	*1.408*		*31*	R_{clear}	
RB	Power Cycling	*0.496*		*11*	R_{Limit}	*n. a.*
	GD	*0.555*		*13.6*	R_{clear}	
MIB	MA	*0.788*		*24.8*	R_{Zener}	*NTC*
IOB		*2.97*		*n. a.*	*n. a.*	*IC*
ASIC		*0.097**	*0.149***	*n. a.*	-	*n. a.*
Sensor		*0.056**	*0.228***	*n. a.*	-	*16 Ds*
Ladder		*13.1**	*16.5***	*n. a.*	-	*ICs****

*: typical-case estimation; **: worst-case estimation; ***: Cooling system incl. vacuum sensor

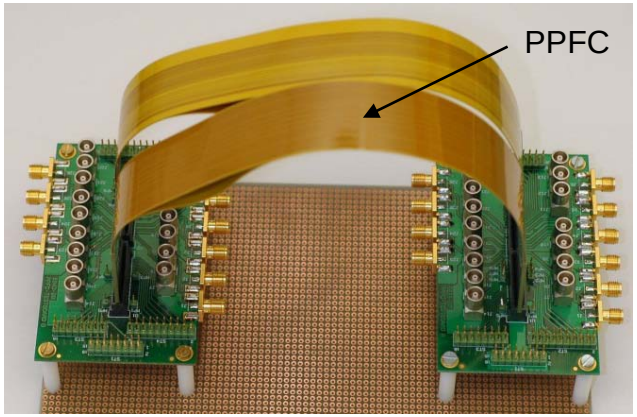
Result

- *total Camera Power well below 400 W*

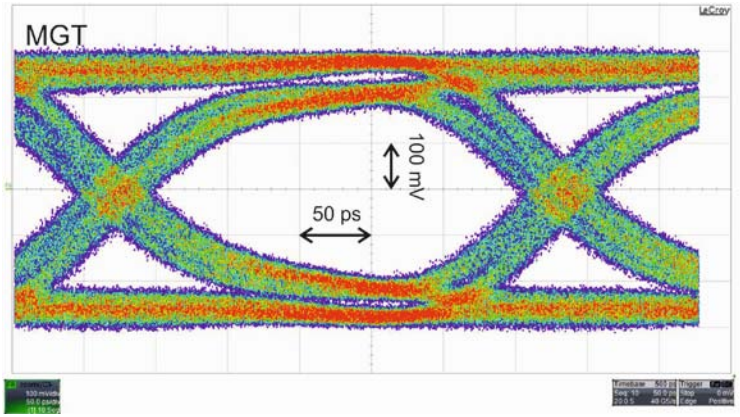
- *73 Temperature Sensors & 1 Vacuum Sensor per Quadrant*
- *To Do: Slow-Control Concept incl. Interlock for Power & Cooling*

Electrical Tests: *MGT & JTAG*

MGT-Test Setup



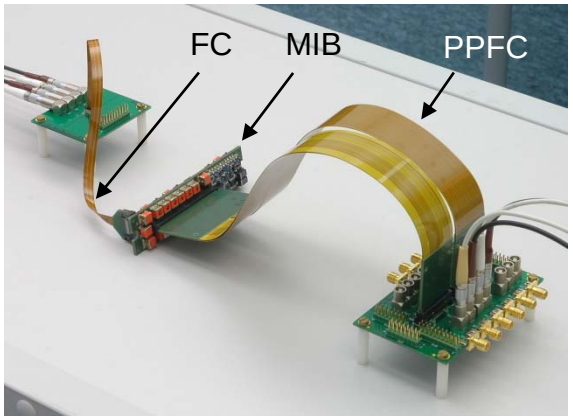
3.125 Gbps (2^7-1) PRBS (differential)



Result

- *Flexibility*
- *Bandwidth*
  (Equalization on FPGA)

JTAG-Test Setup



80-MHz CLK (single-ended)

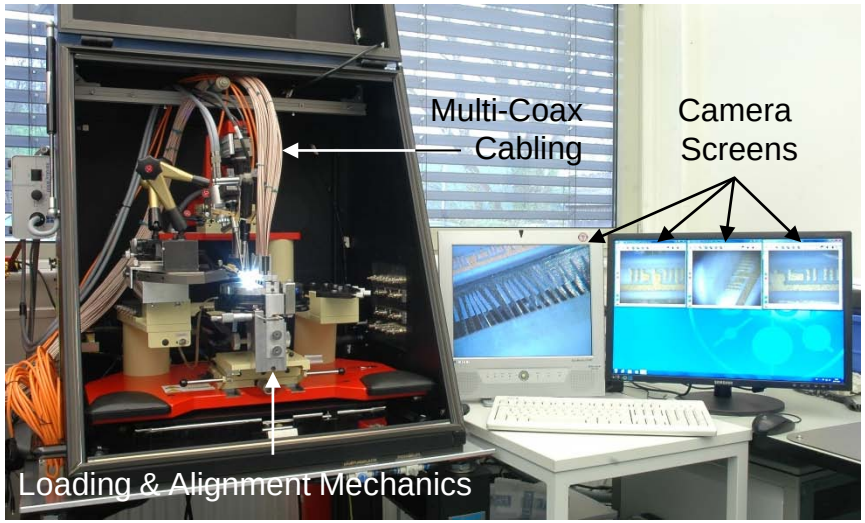
Result

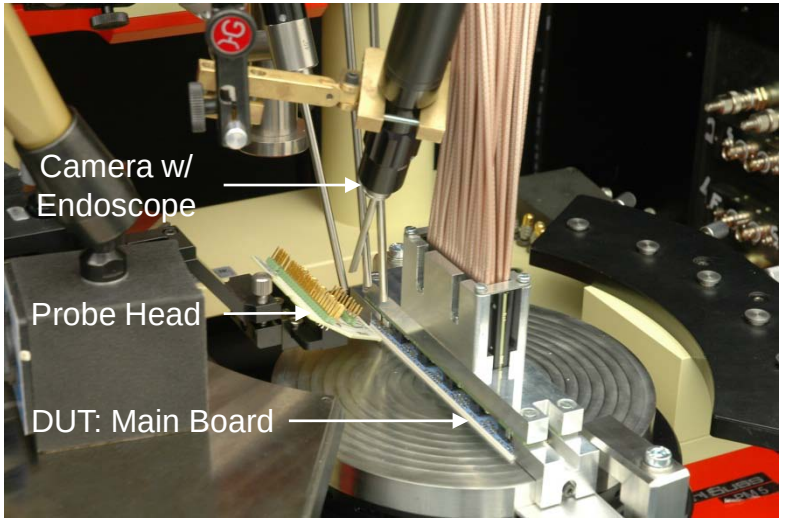
2 Mb / 99.4 ms ≈ 21 Mbps
(32 bit / Pixel x 64k Pixel / Ladder)

- *80 Mbps*
- *Train-wise Parameter Setting*

PM 5-Probe Station: *Installation Status*

Test Environment for MB & full Ladder



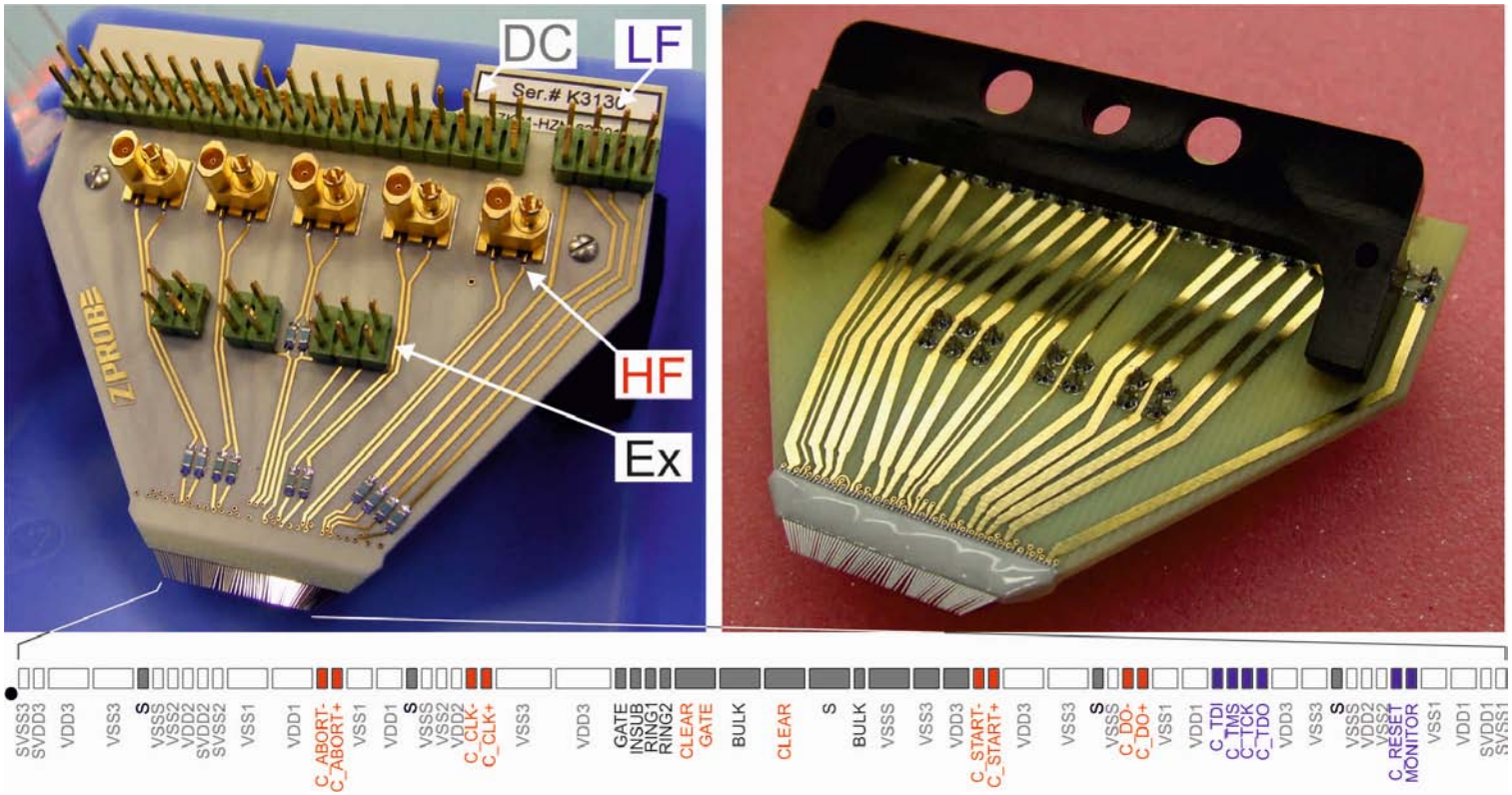


Ladder-Test Mechanics

Result

- *Cabling & Cameras* ☺
- *DUT Rotation very critical → duplicate Setup !!!*

PM 5 Probe Station: *62-pin │Z│ Probe*

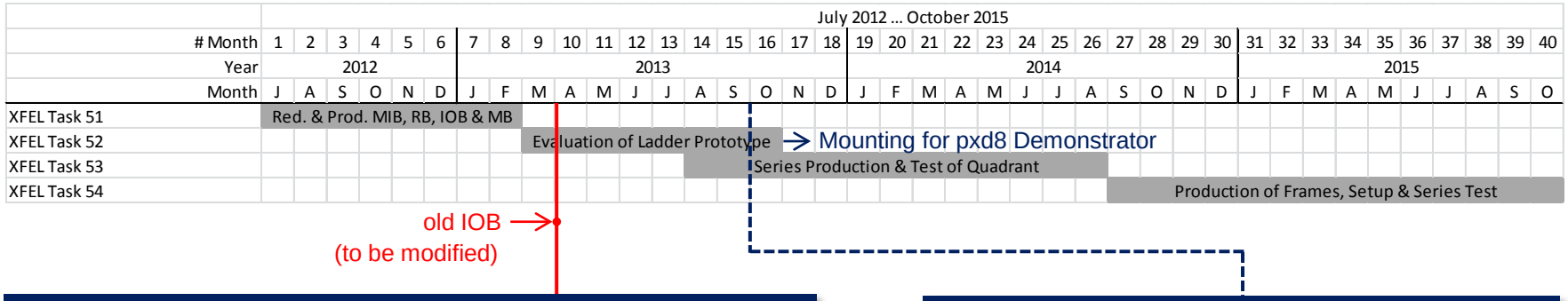


Result

- *High-Performance Connectivity of all Pads (Section of 64-I 64 Pixel)*
- *Connectivity possible for Piggy Back with*

discrete Devices & Sensor Dummies → Test Chips → F1/2 → F1/2 + Baby Sensor

Summary & Outlook



Achievements

- FR-4 Main Board available
- Flex Cables passed Performance Tests
- Patch-Panel Design started
- 62-Pin Probe available
- Main-Board & Regulator-Board Frames available
- 1st Setup Step of Focal-Plane Package passed with old parts
- Thermal Imaging completed

Future

- Finalize Probe-Station Setup
- Evaluation of Ladder Prototype
- Setup upper Focal-Plane Module Part with Frame, Main Board & Heat Spreader
- Design of Patch-Panel Prototype

providing that we can fill open Positions

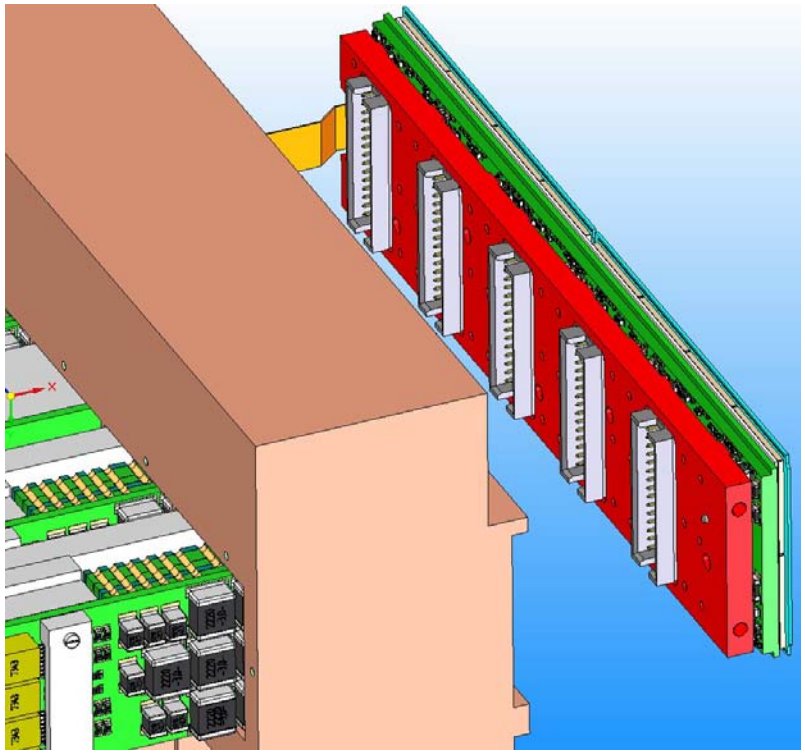
Mechanical Thermal WP

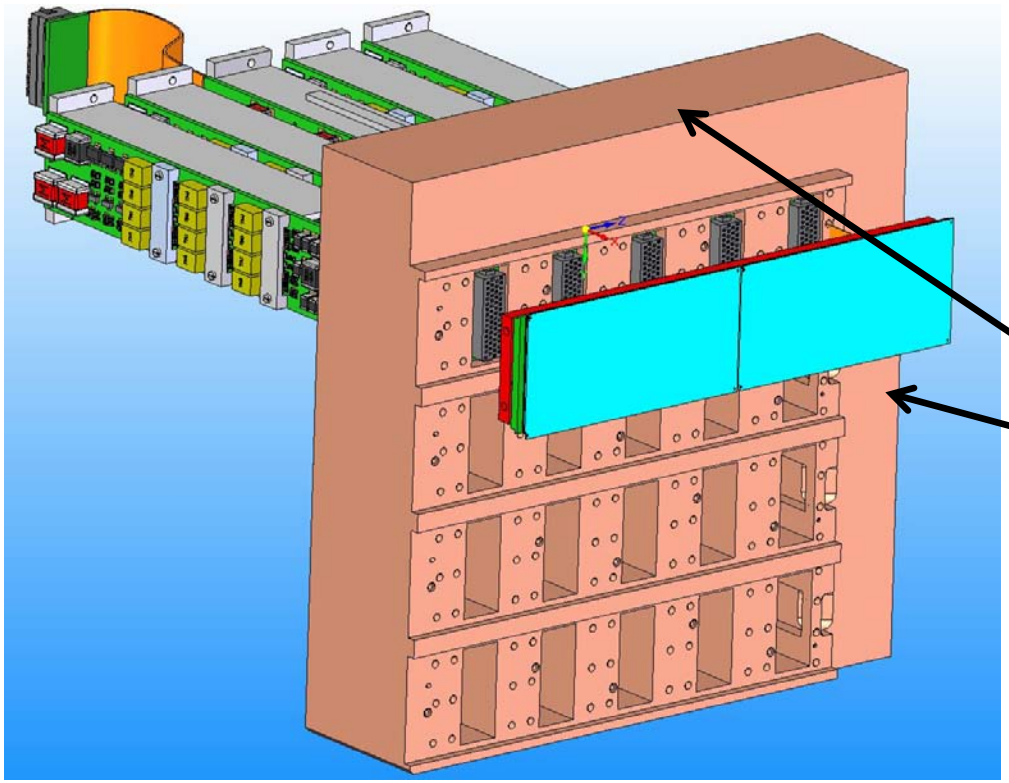
- Cooling the cooling block
- Ladder-Size Prototype System
- Approaches to movable quadrants

Cornelia Wunderer
DESY Photon Science Division
Detector Group
cornelia.wunderer@desy.de

2nd Generation Mechanics and Cooling

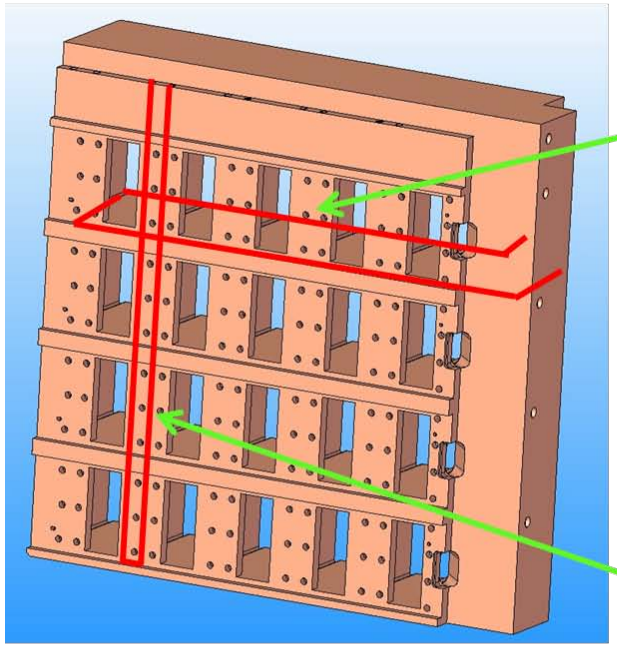
- Single “half-height” frame is narrow enough to give wire bond access
- Attachment to cooling block at “island” positions using a total of 34 screws / ladder
- Vertical boards inserted after tightening

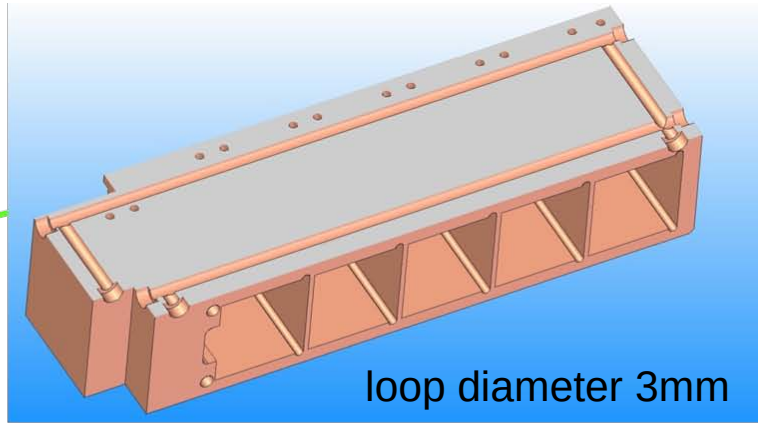


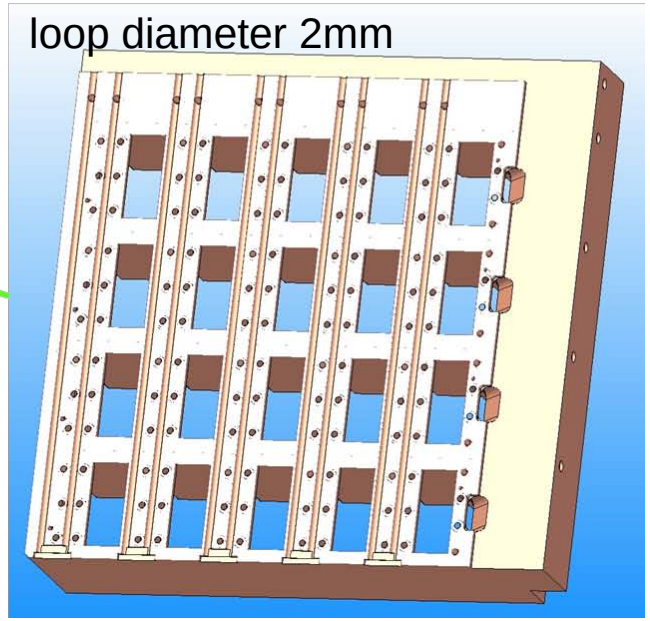


Mechanical & thermal access on 2 sides of each quadrant

Liquid Cooling Loops in Quadrant Block







Two cooling loop groups:

- through the MB frame attachment areas, and
- through the “vertical walls” of the cooling block separating the different ladders’ electronics

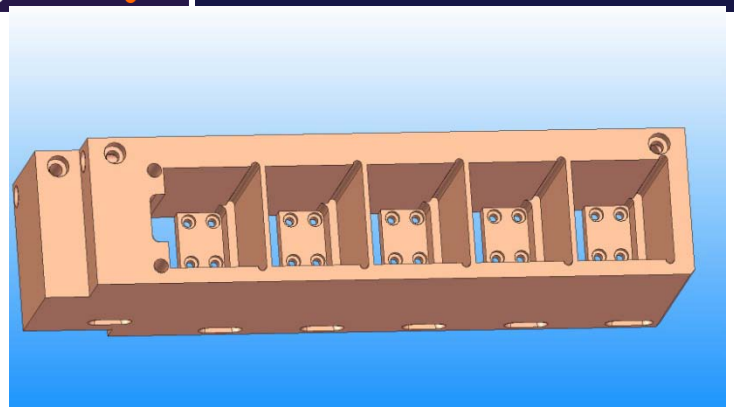
Ladder-Size Prototype

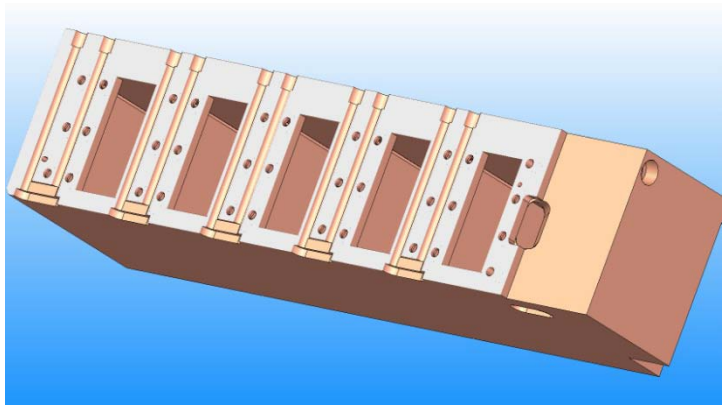
Ladder-size Prototype

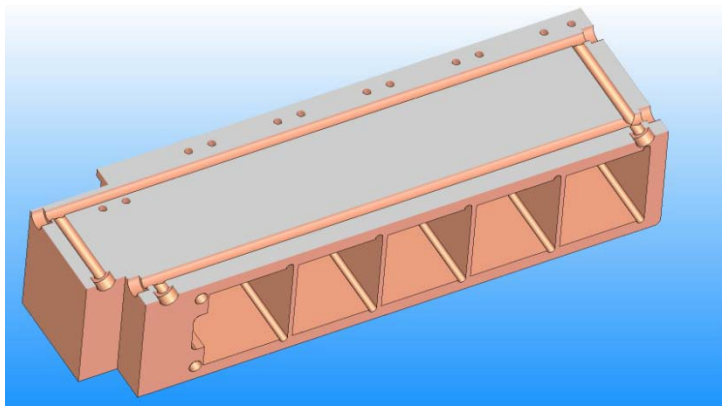
Why not immediately a full quadrant?

- Making the complicated shape of the cooling block is not cheap, and cost (almost) scales with size in this case
- A full quadrant block we'd want to be able to keep using and eventually integrate into the 1M, and therefore we would avoid the modifications needed to enable working with both liquid and "solid attachment" cooling paths
- Experiences should scale up
- Thermal mock-up tests as well as first "live" sensor tests will involve single ladders only
- Last but not least, smaller object easier to do good FSM thermal models on

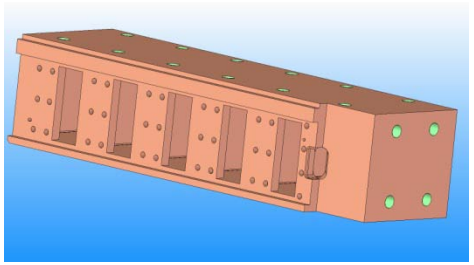
The prototype cooling block



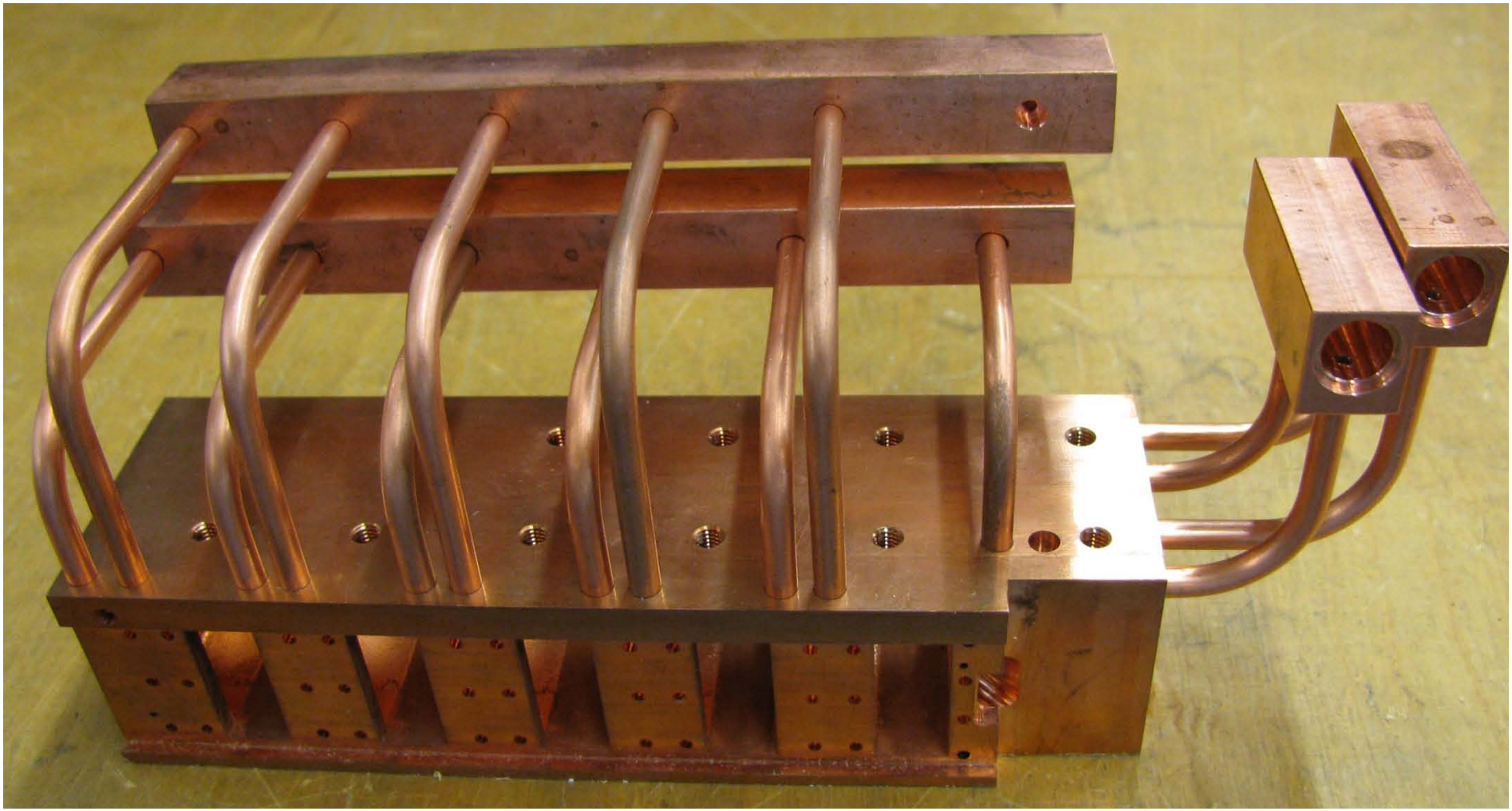




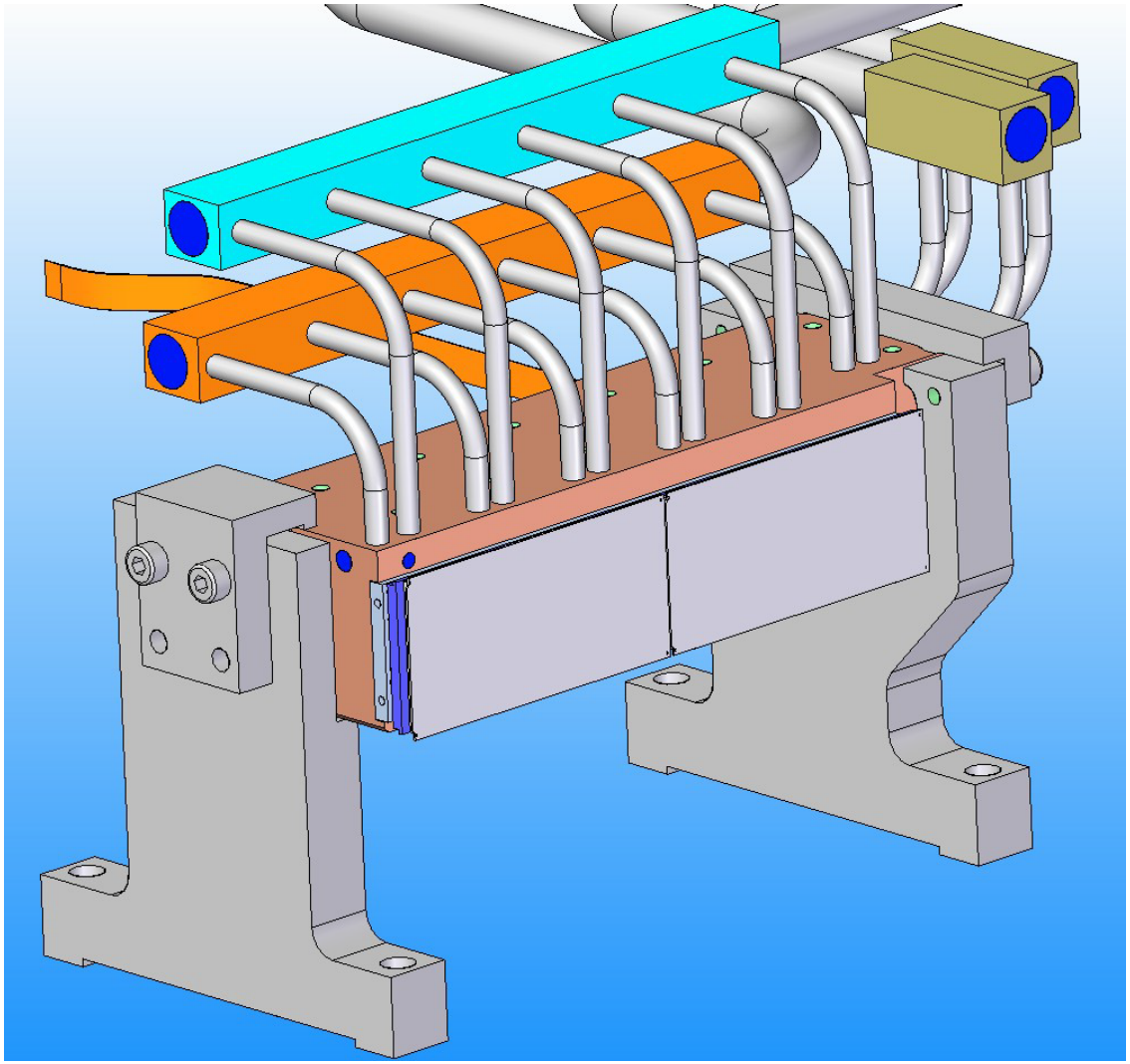
- Houses one ladder
- “tightest spots” of the full quadrant for cooling loop placement represented
- Includes drill holes for “solid” cooling attachment
- In hand



Prototype cooling block with coolant pipes

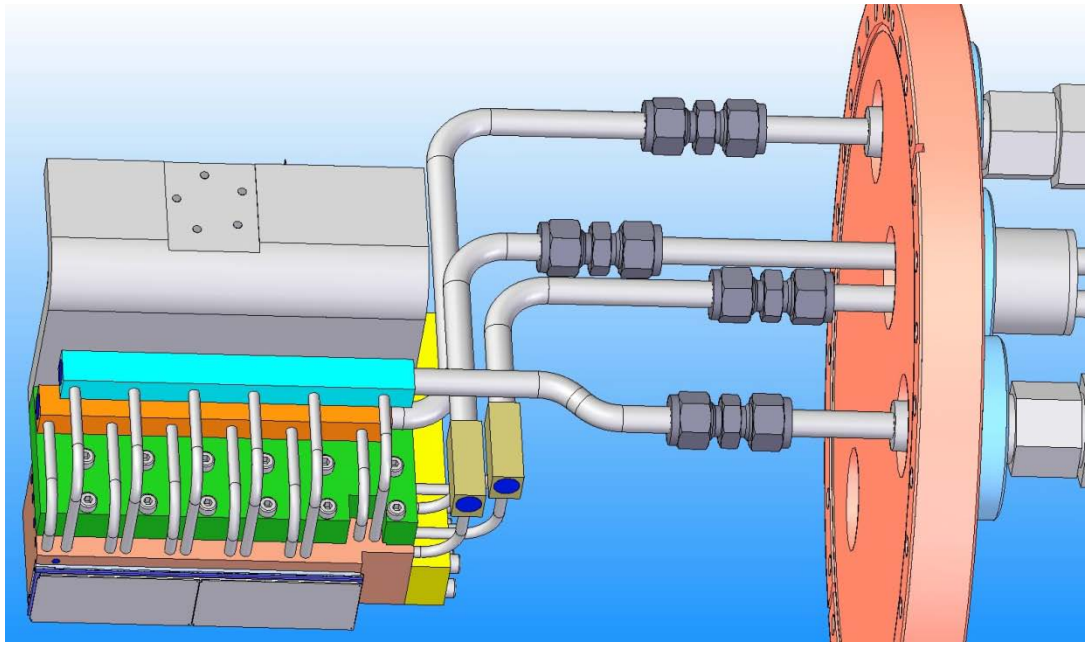


Liquid coolant operation



- The 2 coolant loops can be fed separately
- This enables testing with either one or both coolant loops
- PEEK mechanical supports
- MB Assembly with sensor shown

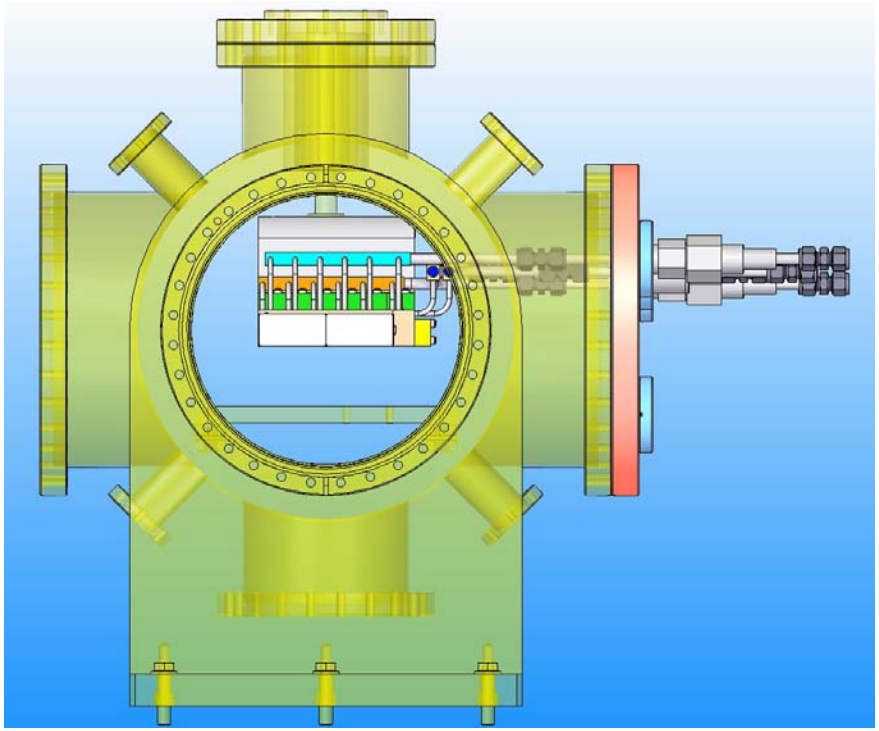
The Prototype in the Vacuum chamber

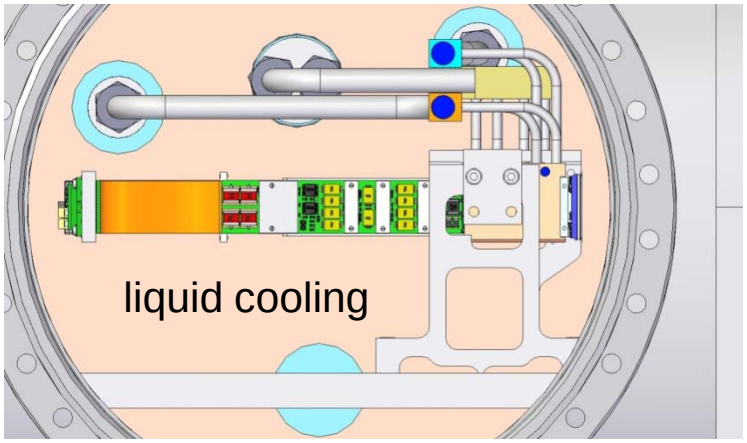


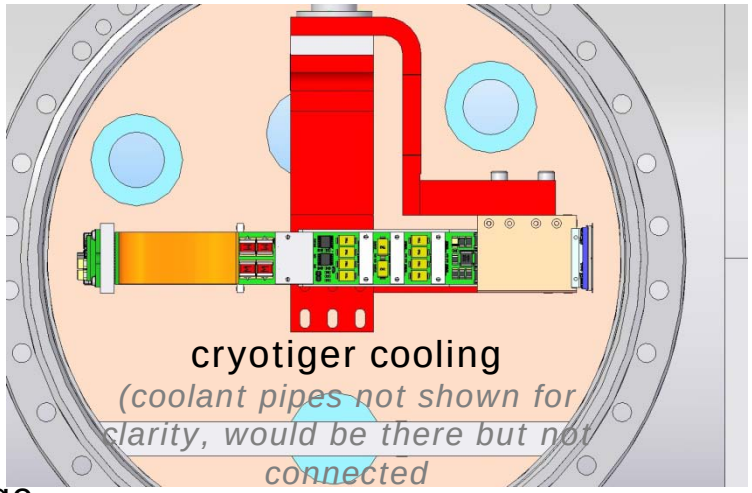
Both liquid path and cryotiger attachment (green plate and bent gray element) shown, only one would be used at a time

- We anticipate working with the liquid coolant loops
- In case of difficulties, running the coolant through a less-intricately-machined interface block, plus a “solid attachment”, would be the backup solution.
- In this test setup, we have a cryotiger for the “solid attachment” option.
  - We have one
  - For debugging/comparing with simulations, it takes out the liquid-block interface
  - “solid attachment” option implemented in the prototype setup primarily for simulation cross-checks (2 different cooling situations)
- 2 different liquid coolant feed-throughs implemented for testing on the two coolant loops

The prototype in the vacuum chamber







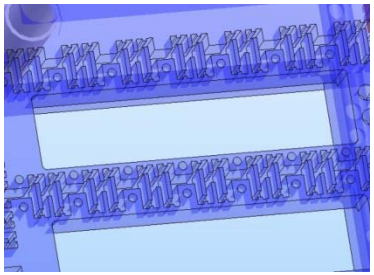
- Chamber layout made such that
  - Sensor views one large, otherwise unused flange
  - Opposing flange available for DSSC readout electronics feed-through

Most pieces already in-house, assembly in the coming weeks

A note of caution – laminar vs turbulent flow

- Turbulent flow of coolant yields much better heat exchange with the cooling block
- If one WANTS to achieve laminar flow, this is very difficult
- Simulations performed at DESY FS-DS indicate that with the slow(ish) coolant flow and high coolant viscosity we have, we might just have managed to get there … resulting in less effective cooling

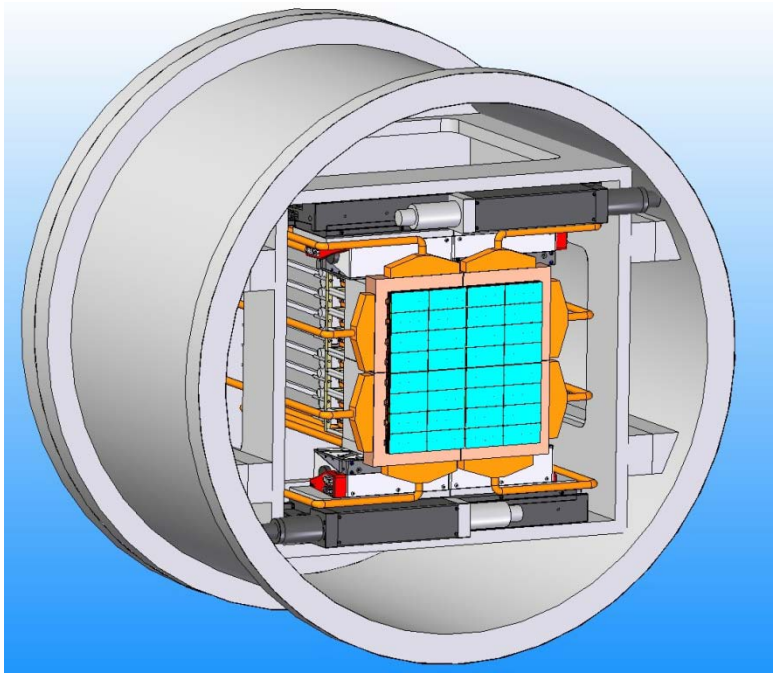
- We try out the cooling with this prototype. If we get good cooling (and thus turbulent flow) we're good
- Should the behavior of the prototype indicate laminar flow, a more elaborate design of the cooling paths (meandering route to enforce turbulence) would be required. This is doable, just more expensive.



Possible meandering coolant path: courtesy of J. Becker & S. Rah

Moving the Quadrants

Benchmarks of the rough idea outlined in 2011



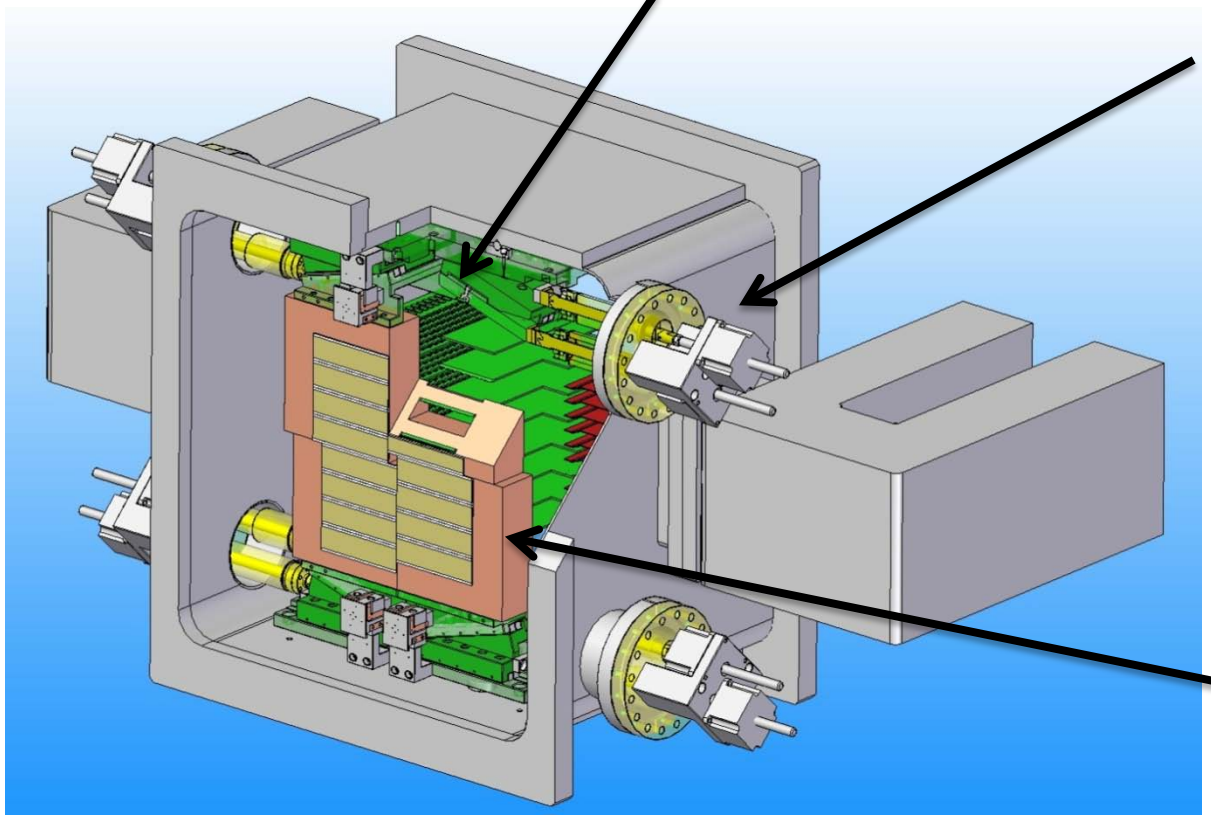
- Chamber inner diameter 80 cm
- Commercially available in-vacuum lift tables and translation stages
- This system is the basis of our mechanical accuracy (in particular: 1M planarity) infos to XFEL to date
- Completely independent X and Y stages for each quadrant
- Lift up to 1.3 cm, linear motion could be larger (but limited by flex cables anyhow)

> This would work

> It's a BIG chamber

> Lots of actively moving parts on the inside -> no fun to service

An alternate approach: outside motors



External motors ~ 6W each
Easy to service

Chamber inner dimensions shown here are 50cm x 50cm, DSSC might need a few cm more

Cooling block

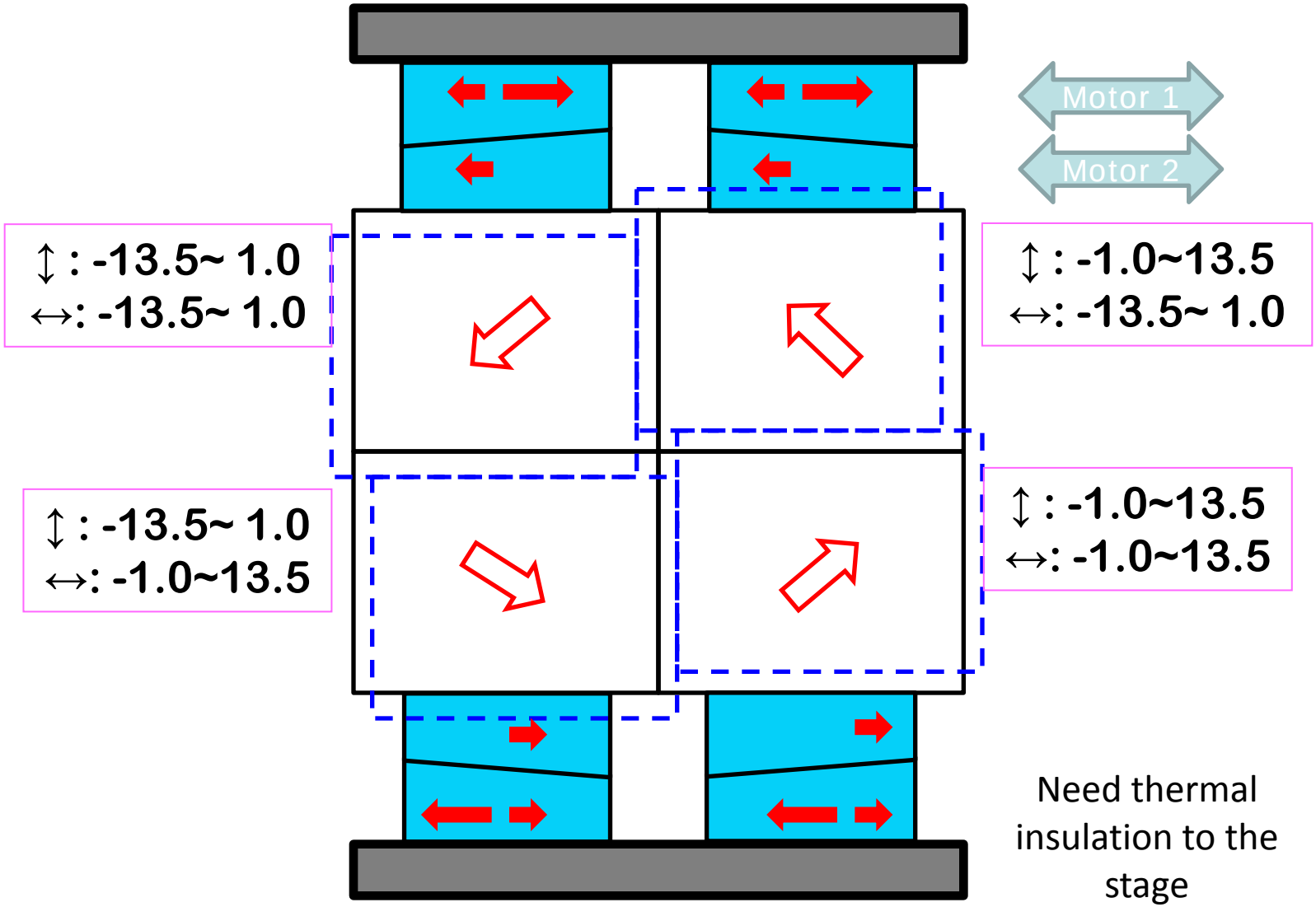
You'll have seen this before: credits to the AGIPD Mechanics Team.

Why should DSSC use the same XY translation approach as AGIPD?

- Less moving parts on the inside, and a smaller chamber, should appeal to the XFEL detector and beamline scientists
- Two detector systems using identical XY translation approaches should appeal to those at XFEL worrying about integration and maintenance
- Obvious streamlining within the mechanics teams at DESY, “all pulling on the same string” to implement and debug this approach

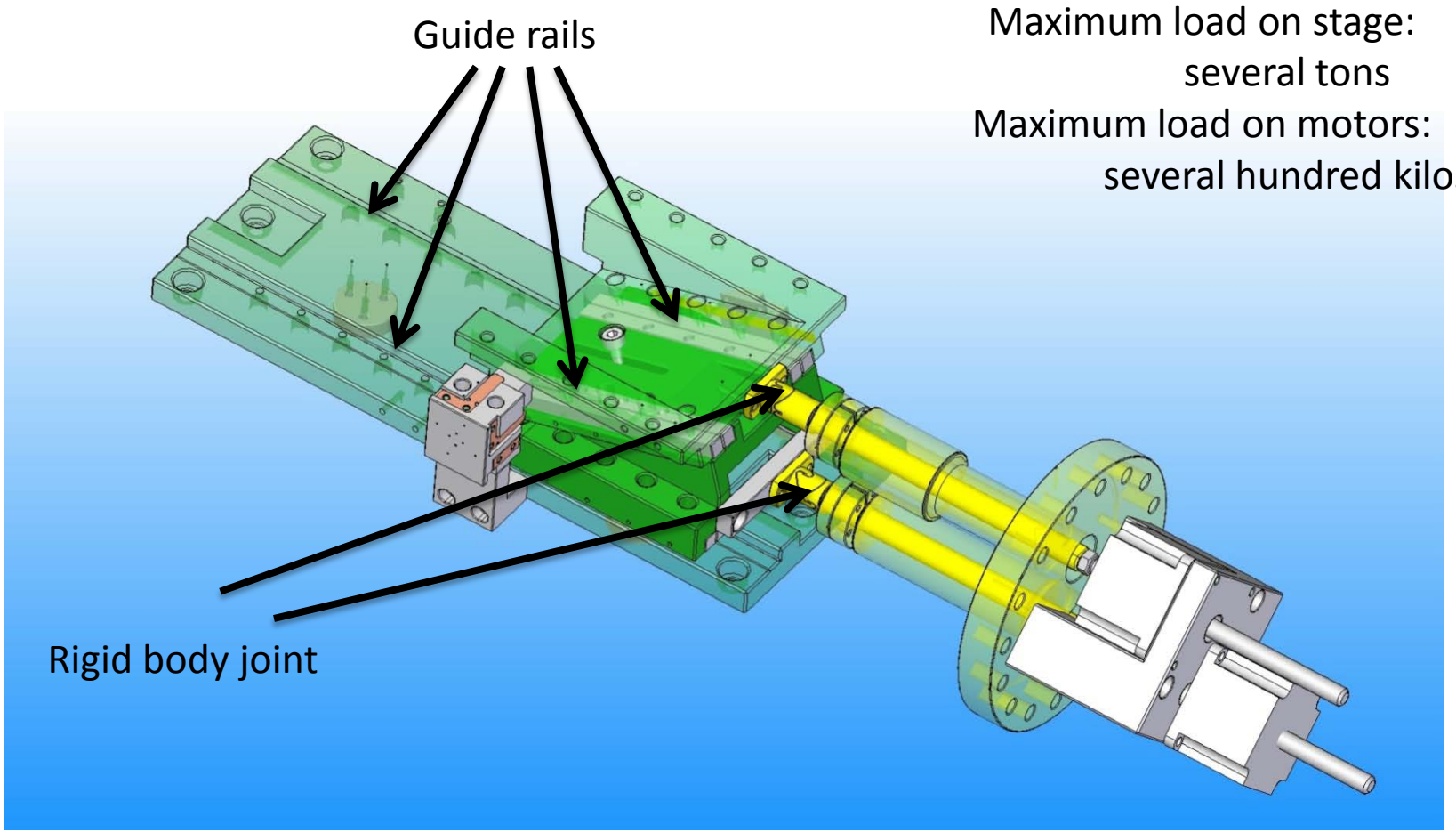
We plan to baseline using a copy / slight modification of AGIPD’s moving quadrant approach. The “old” standard-commercial-parts solution becomes a backup approach.

Image plane movement



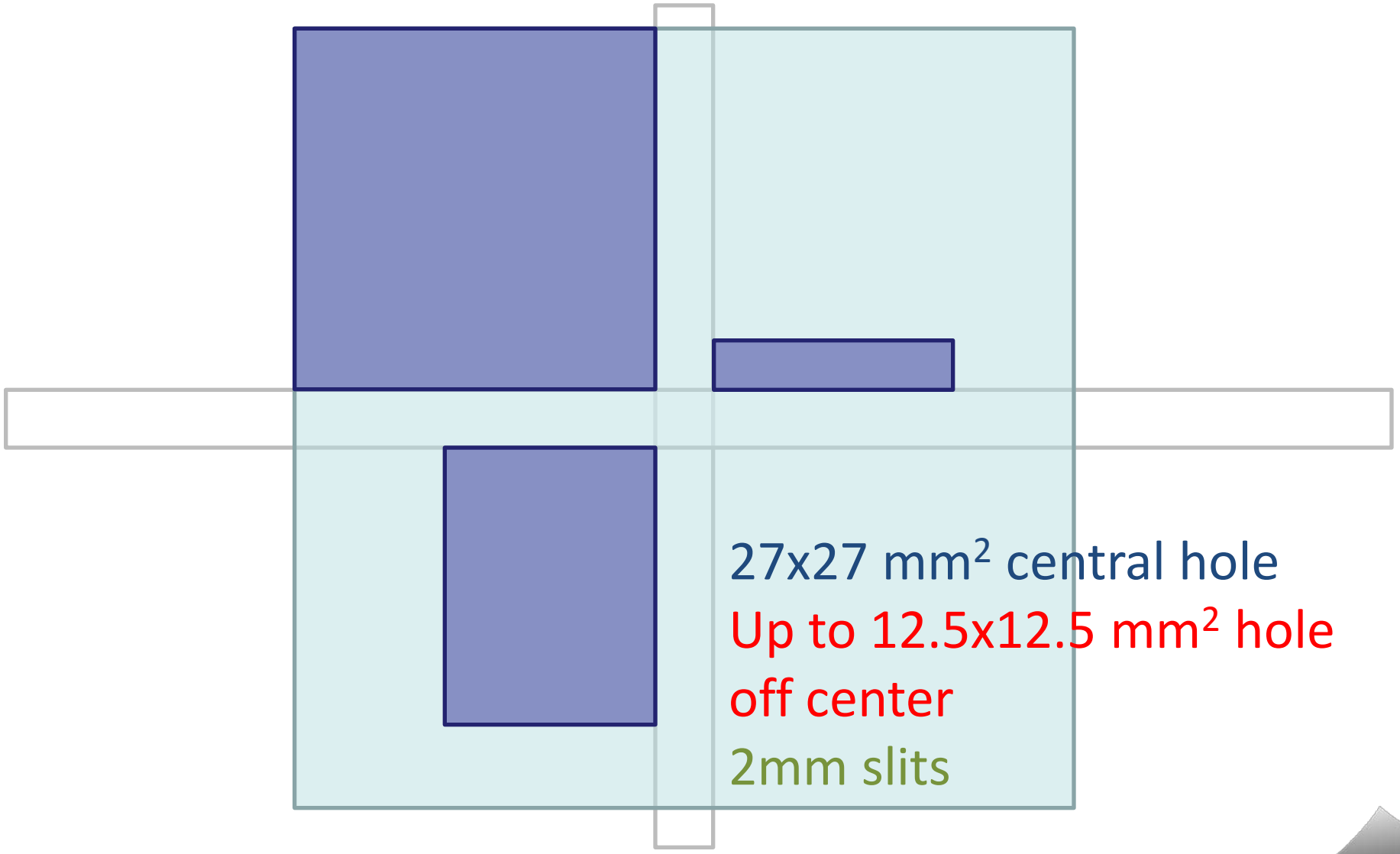
Need thermal insulation to the stage

Sliding stage



Maximum load on stage:
several tons
Maximum load on motors:
several hundred kilos

Possible holes



Next Steps

- Finish assembly of single-ladder test setup
- Thermal tests with mock-up MB assembly
  - Verification of modeling
  - Exploration of liquid cooling performance
  - (solid-state cooling for comparison of models and as back-up approach)
- Detailed XY movement design
- Settling of chamber geometry
- Detailed definition of back-end arrangement

DSSC DAQ

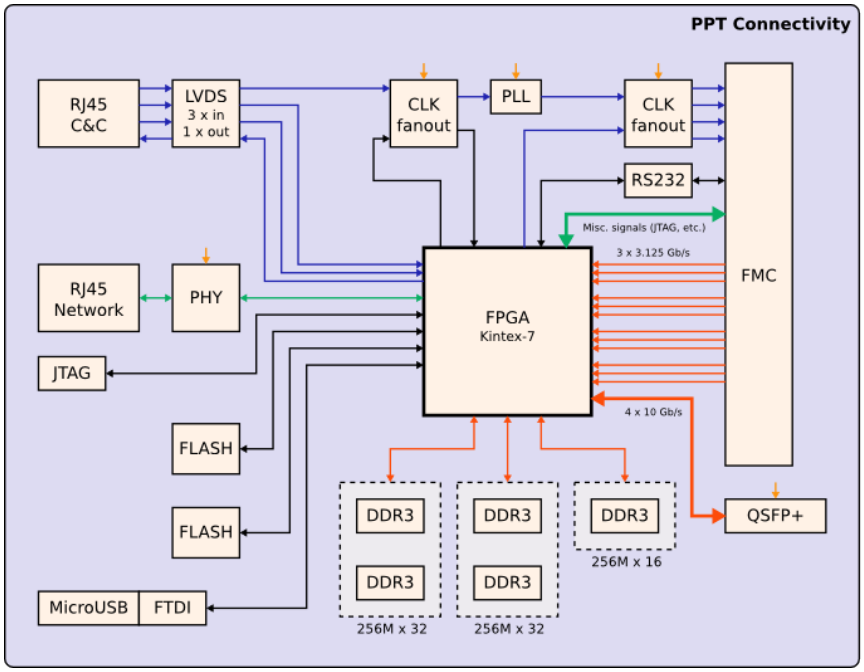
A. Kugel, M. Kirchgessner, J. Soldat, T. Gerlach*

Contents

- Design and status of patch panel transceiver PPT
  - Design process
  - Selected details
  - Implementation status
  - Initial Firmware
- Status redesign IOB
- Test Preparations

PPT Design

- Specification document started 2012-11-28
- Block diagram
- Detailed description of all functional units



- Interfaces
- Layout guidelines
- Input to schematic design
  - Started 2012-12-06
  - Finished 2013-01-30

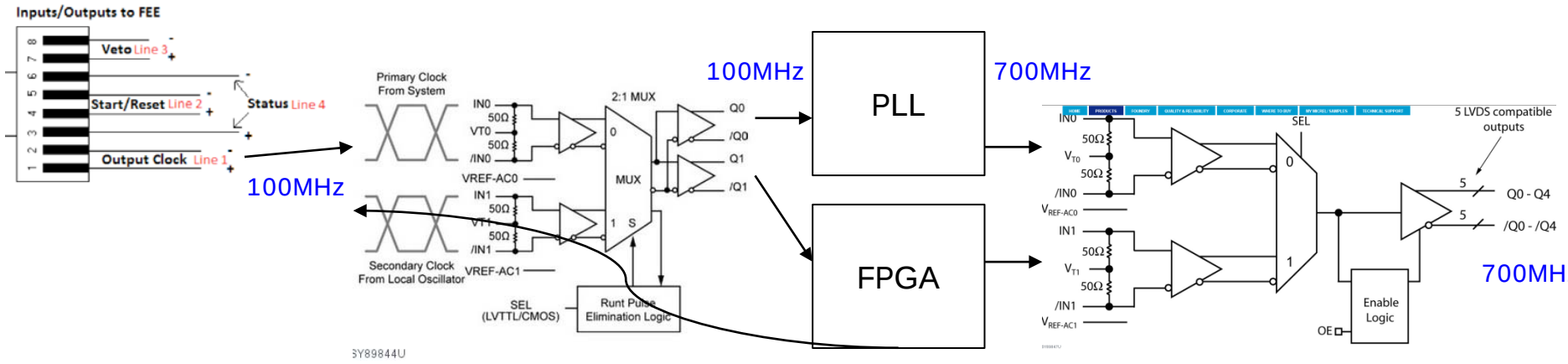
Interface Signals

- PPT serves 4 IOBs
- Interface signals run through FMC connector
- 4 groups of signals
  - JTAG (ASIC, IOB)
  - Clocks
  - IOB Control
  - Serial data
  - Spares and Power

Signal	IO_STD	Anschluss an	FMC-Pins Gruppe 1|2|3|4
		Gruppen 1 - 4	
TDO_IOB	LVCMOS_2.5V	FPGA	H7 | H10 | H13 | H16
TCK_IOB	LVCMOS_2.5V	FPGA	H8 | H11 | H14 | H17
TMS_IOB	LVCMOS_2.5V	FPGA	G6 | G9 | G12 | G15
TDI_IOB	LVCMOS_2.5V	FPGA	G7 | G10 | G13 | G16
TDO_ASIC	1.5V	FPGA, Bank 18	F31 | F28 | F25 | F22
TCK_ASIC	1.5V	FPGA, Bank 18	F32 | F29 | F26 | F23
TMS_ASIC	1.5V	FPGA, Bank 18	E30 | E27 | E24 | E21
TDI_ASIC	1.5V	FPGA, Bank 18	E31 | E28 | E25 | E22
CNTR	LVCMOS_1.5V	FPGA, via 100R	F34 | F35 | F37 | F38
RESET	LVCMOS_1.5V	FPGA, via 100R	E33 | E34 | E36 | E37
PPTCLOCK+	LVDS_2.5V	FPGA	H25 | H28 | H31 | H34
PPTCLOCK-	LVDS_2.5V	FPGA	H26 | H29 | H32 | H35
CLK+	LVDS_2.5V	Clk Fanout-Buffer	C10 | C14 | C18 | C26
CLK-	LVDS_2.5V	Clk Fanout-Buffer	C11 | C15 | C19 | C27
PPTDATA+	LVDS_2.5V	FPGA	G21 | G24 | G27 | G30
PPTDATA-	LVDS_2.5V	FPGA	G22 | G25 | G28 | G31
MGT_TX0_N	LVDS	FPGA MGT	B29 | A31 | B37 | B25
MGT_TX0_P	LVDS	FPGA MGT	B28 | A30 | B36 | B24
MGT_TX1_N	LVDS	FPGA MGT	A23 | A35 | B33 | B17
MGT_TX1_P	LVDS	FPGA MGT	A22 | A34 | B32 | B16
MGT_TX2_N	LVDS	FPGA MGT	A27 | A39 | A19 | B13
MGT_TX2_P	LVDS	FPGA MGT	A26 | A38 | A18 | B12
MGT_TX3_N	LVDS	Nicht benutzt	A3 | A7 | B5 | B9
MGT_TX3_P	LVDS	Nicht benutzt	A2 | A6 | B4 | B8
		Common	
RS232_TX	+/1 12V	FPGA	G36
RS232_RX	+/1 12V	FPGA	G37
PRSNT	Static signal	GND	H2
		Reserve	
Rsv3.3	LVCMOS_3.3V	FPGA 3.3V Bank	J6, J7, J9, J10, J12, J13, J15, J16, J18, J19
Rsv2.5_P	LVDS_2.5V	FPGA 2.5V Bank	D8 | D11 | D14 | D17 | D20
Rsv2.5_N	LVDS_2.5V	FPGA 2.5V Bank	D9 | D12 | D15 | D18 | D21
		Power/GND	
12V_main		12V	C35, C37 (über Shottky Diode)
12V_aux		12V	B1, B40 (über Shottky Diode)
Viob	1.5V	1.5V	K40, J39 (über 0R Widerstand)
GND		GND	Alle GND Pins gemäß Abbildung 14

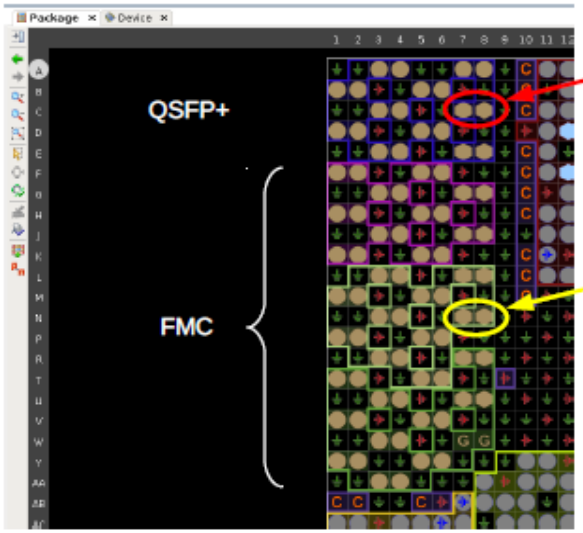
Clock Options

- 100MHz (99MHz) reference clock from C&C system via RJ45
- Drives PLL ADF4351 (upgrade from current ADF4350). Output 700MHz to IOB
- Alternative input from FPGA (100MHz)
- Alternative output from FPGA (700MHz)



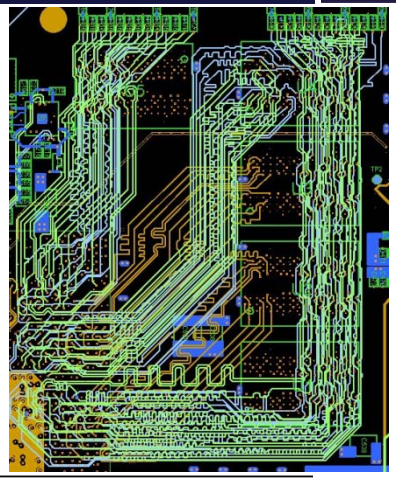
Serial Links

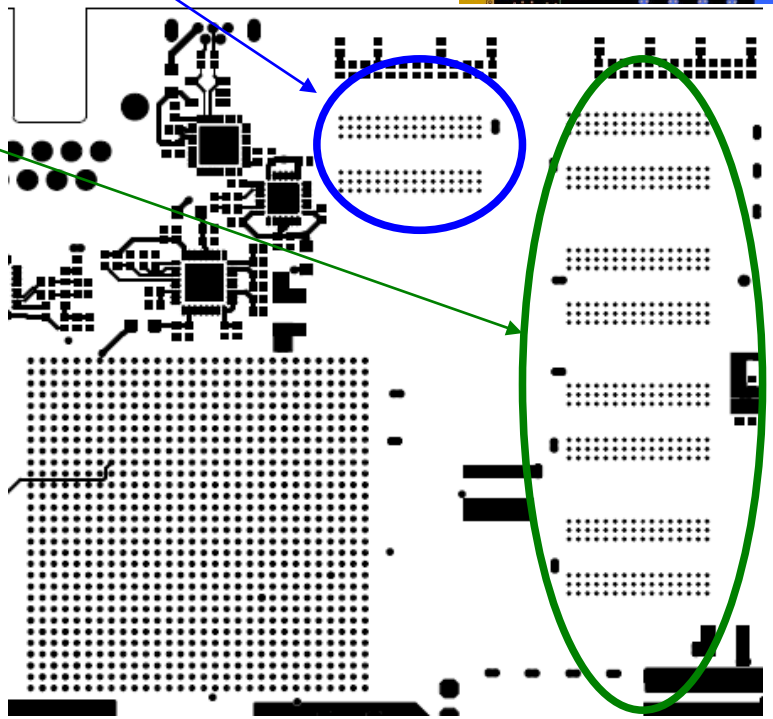
- FPGA provides 16 links up to 10Gbps
- 4 needed for QSFP+ output (10Gbps)
- 12 remaining for detector data
- 3.125Gbps/lane limited by IOB
- 3 lanes per IOB sufficient



Buffer Memory

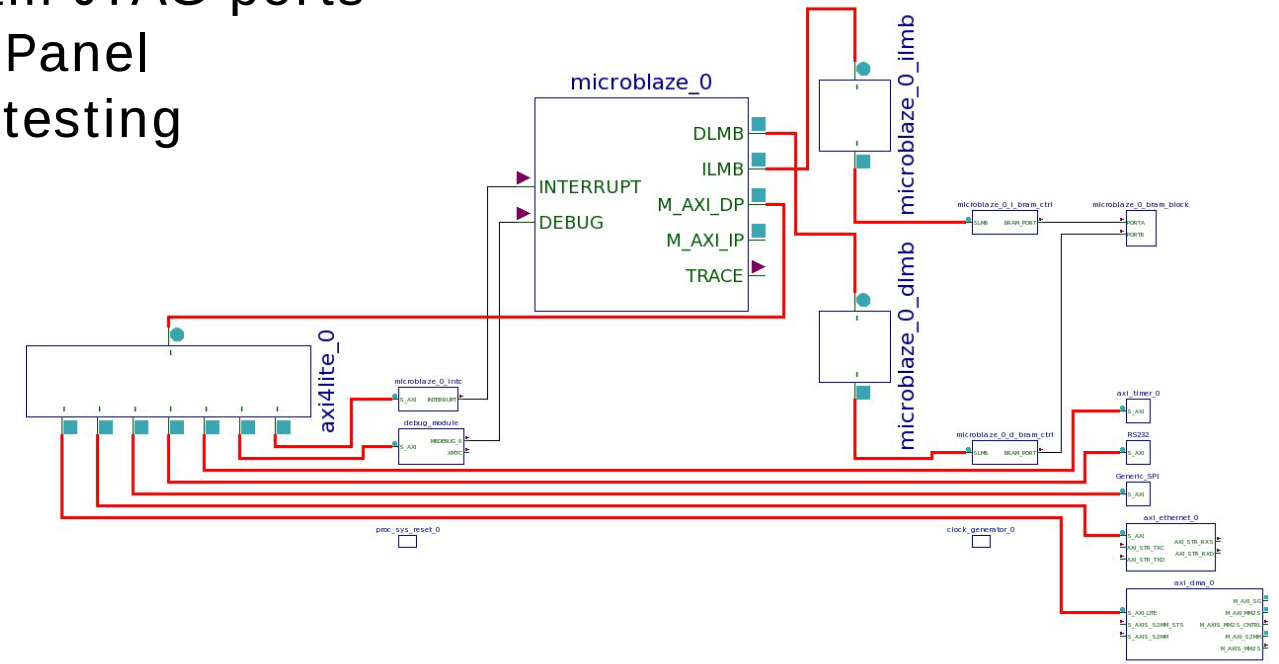
- External memory for embedded processor
  - Single chip, 2Gb, 400MHz, 16 bit
- and data buffer
  - Four chips, 2Gb, 800MHz, 64 bit
  - 100Gbps nominal bandwitdh
  - 2*40Gbps (dual-ported) required





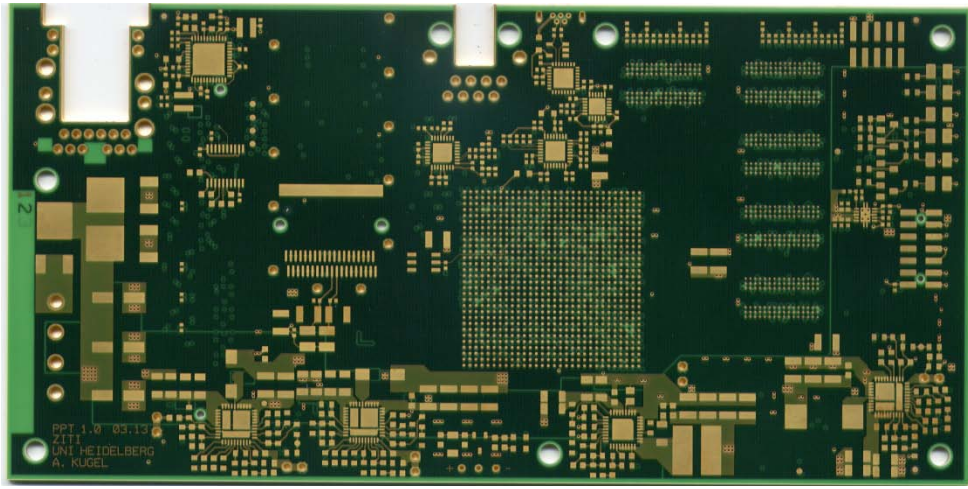
Control Architecture

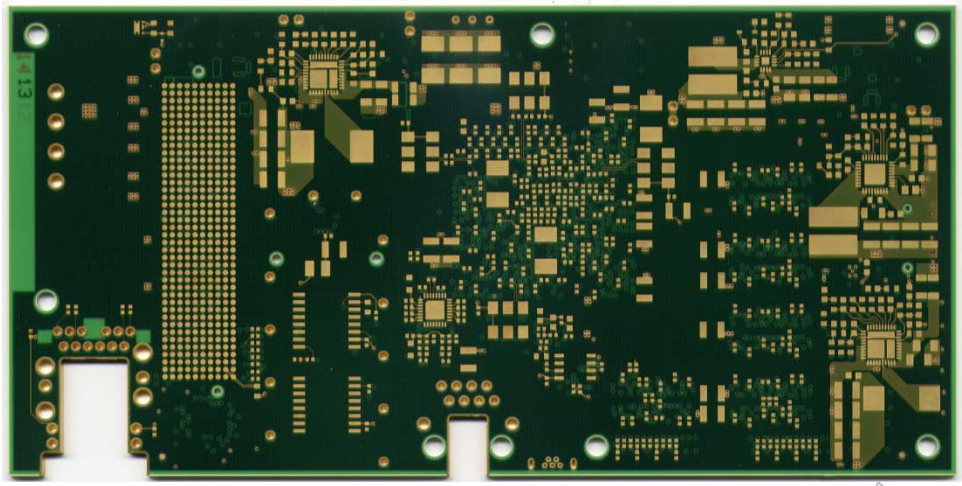
- Core control item is embedded FPGA processor (Microblaze)
- Linux-capable
- On-board configuration from FLASH
- GE port to control network
- Access to telegram encoding/decoding in FPGA
- Access to UDP DMA engines
- Access to downstram JTAG ports
- Serial port to PatchPanel
- USB serial port for testing



Implementation

- 14 layer PCB, 80*160mm, micro-vias
- Layout started (external: GED) 2012-01-22, finished 2013-03-19
- PCB finished, assembly in progress
- Prototypes expected ~2013-05-17





PPT Firmware

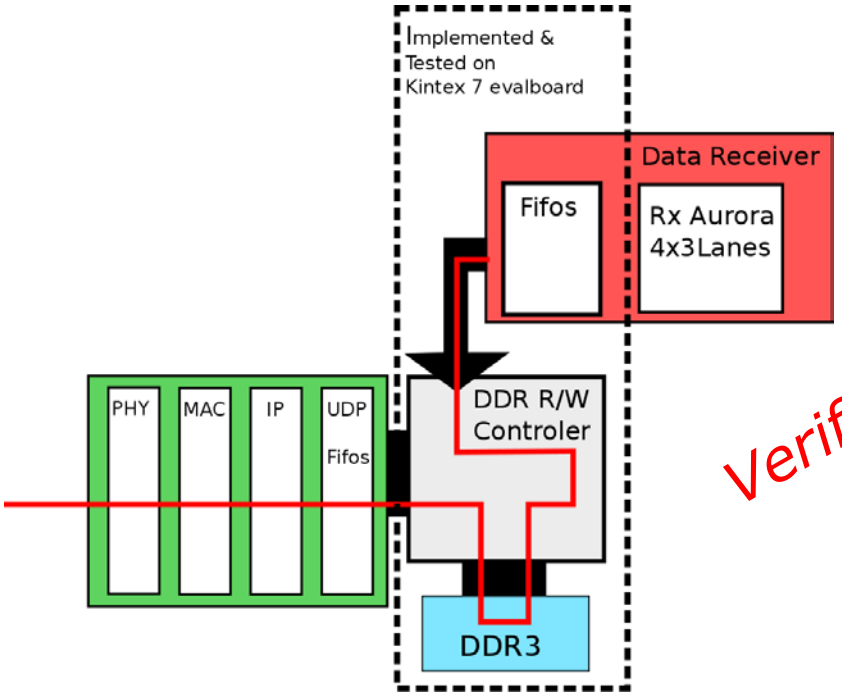
- Initial Datapath
  - Aurora-RX
  - DDR3 dual-ported
  - 10GMAC

Initial Controller

Microblaze embedded system

Linux

Simple test application

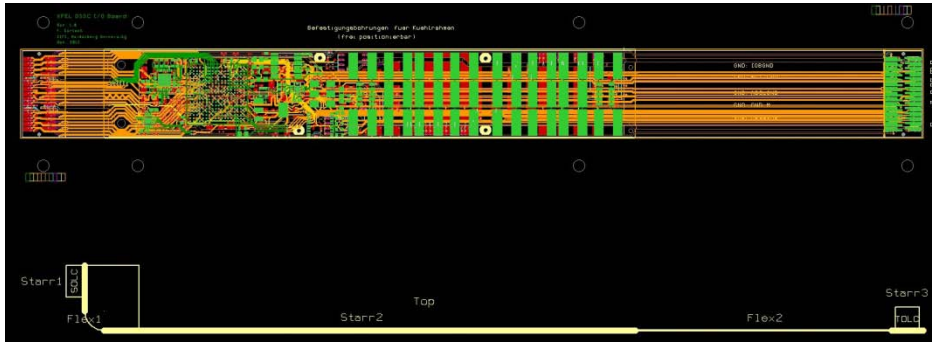


Verified on KC705 Eval Card

IOB Status

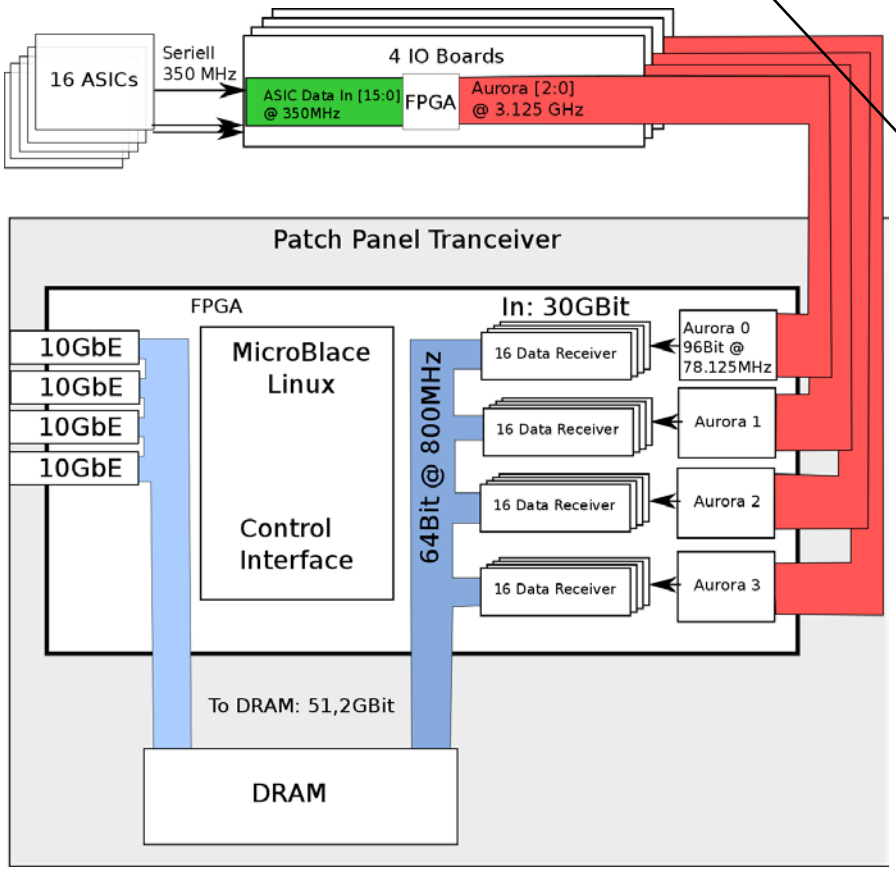
- IOB redesign/re-layout finished by Thomas Gerlach late 2012
- Production delayed due to PPT activity
- Also late (March 2013) design change: temerpatur sensor. Implemented.
- Currently under „design-for-manufacturing“ layout revision

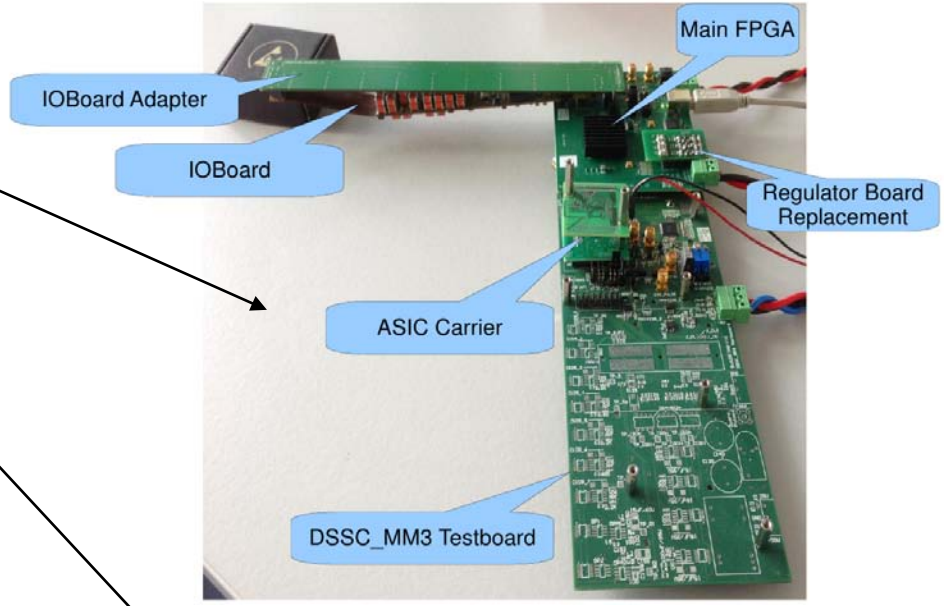
- Expect to place PCB order end of May

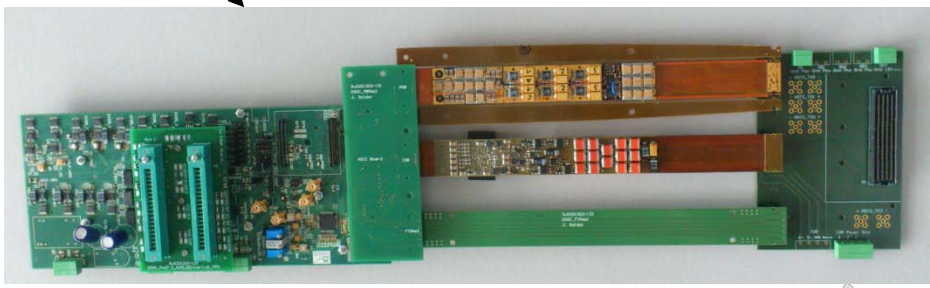


Test Preparations

- Full on-detector chain
  - ASIC focused setup
  - Global setup







CALIBRATION AND SYSTEM SIMULATION

(G. Weidenspointner)

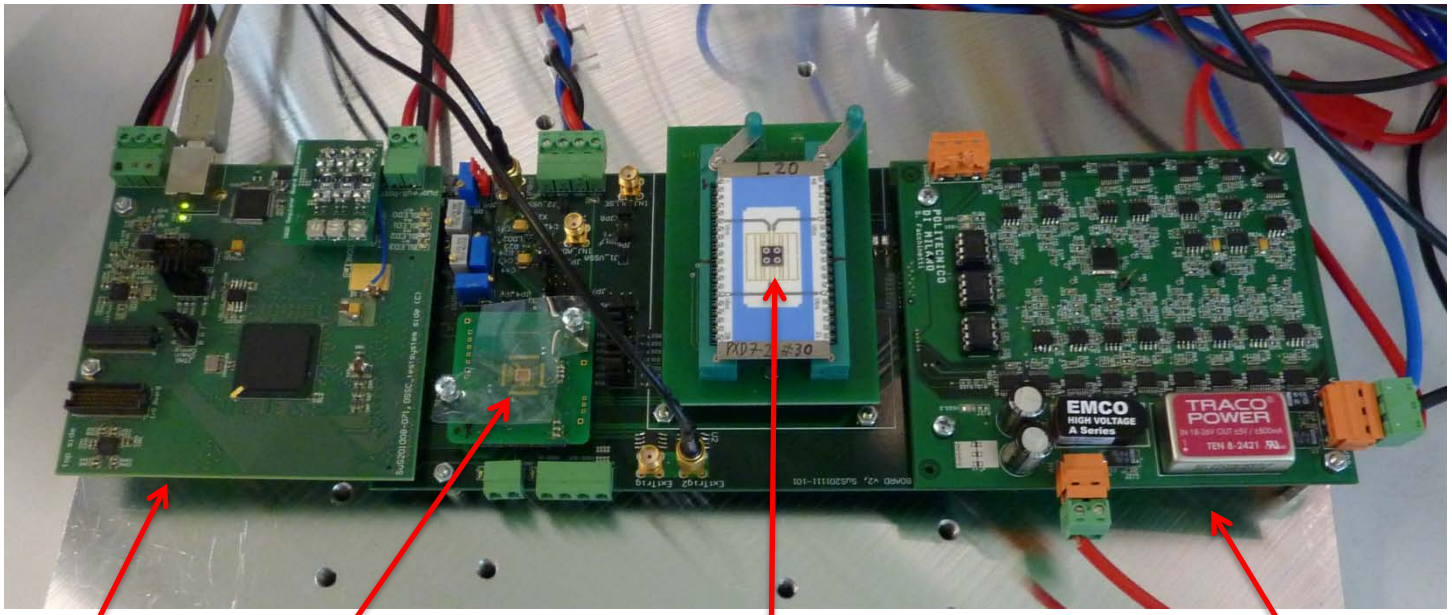
Calibration & System Simulation

Focus of recent activities:

- Experimental calibration of non-linear system response (digital output as function of charge collected in DEPFET) of prototype DSSC system (pxd-7 DEPFET and MM2 ASIC)
- Experimental study of calibration properties of new (improved) MM3 ASIC prototype

DSSC Prototype Set-up I

Definition:
DSSC prototype = pxd-7 prototype + ASIC prototype



FPGA board

MM2 ASIC

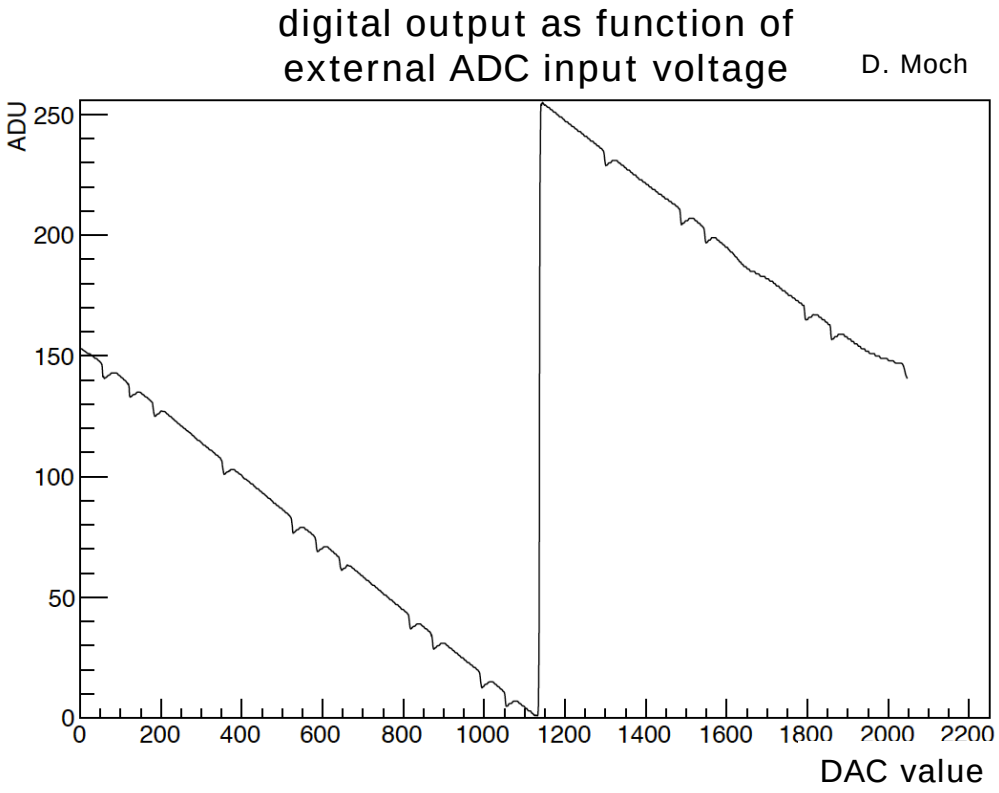
chip with 4 pxd-7 structures (only 2 can be bonded to ceramic)

bias board

DSSC Prototype Set-up II

Some MM2 ASIC caveats:

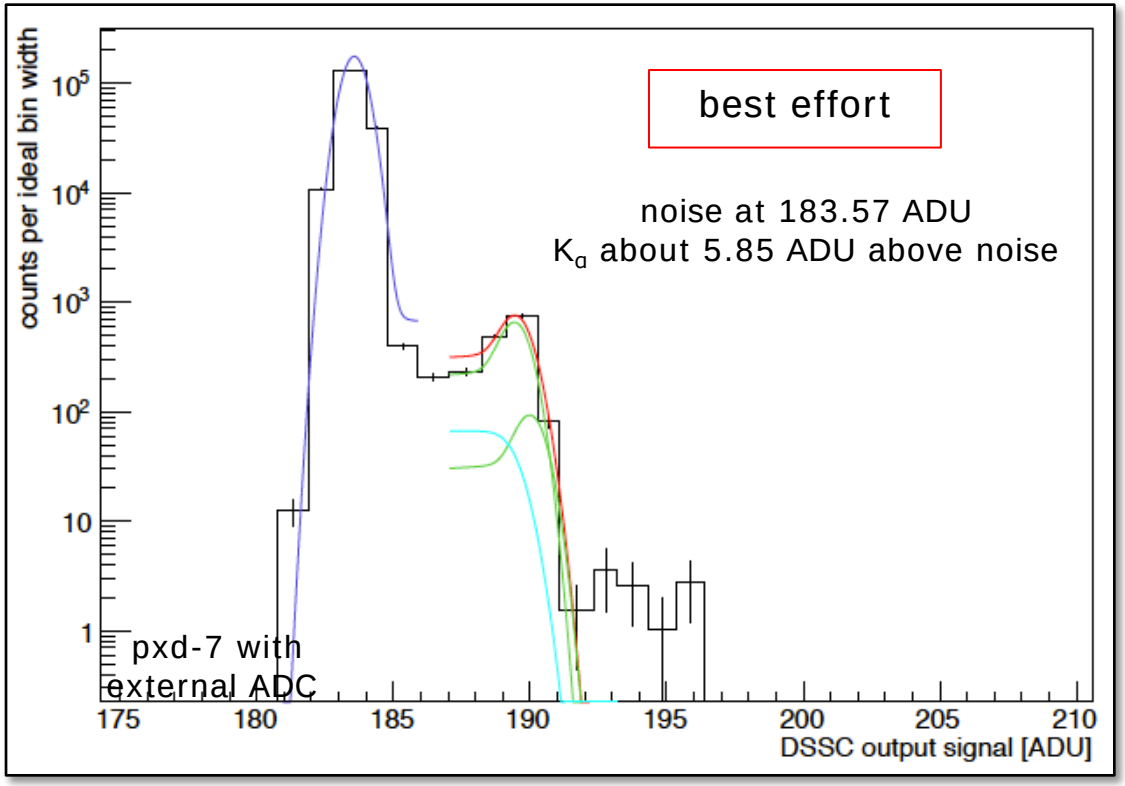
- not all functionalities of final ASIC available in MM2
- some implemented functionalities are limited (e.g. dynamic range)
- ADC with known (and corrected in MM3) deficiencies
  - o backward counting
  - o DNL



Example: Calibration of Set-up
Non-linear System Response I

First step:
single photon counting

- set ASIC offset and gain to count photons of given energy
- offset & gain: ^{55}Fe (noise & X-ray lines)
- fit of ^{55}Fe spectrum: spectral model from high resolution 14-bit spectra
- best setting from grid search
- so far: calibration for 1 keV photons



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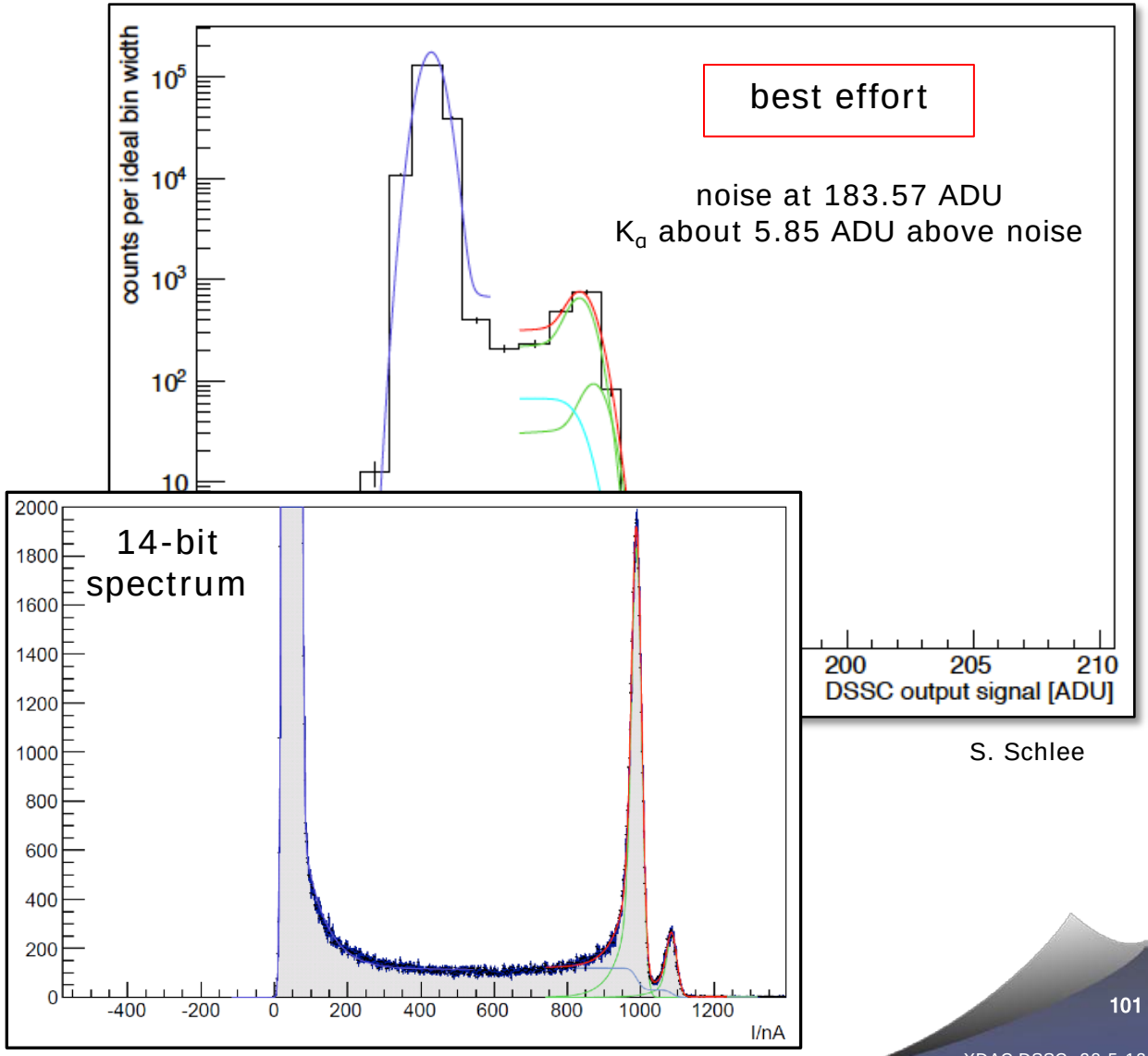
Example: Calibration of Set-up
Non-linear System Response I

First step:
single photon counting

- set ASIC offset and gain to count photons of given energy
- offset & gain: ^{55}Fe (noise & X-ray lines)
- fit of ^{55}Fe spectrum: spectral model from high resolution 14-bit spectra
- best setting from grid search
- so far: calibration for 1 keV photons



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Example: Calibration of Set-up
Non-linear System Response II

Second step:
non-linear region

- scan dynamic range of system, linear and non-linear region, by pulsed charge injection
- used internal charge injection via inner substrate contact
- calibrate charge injected per pulse by comparison to ^{55}Fe signal

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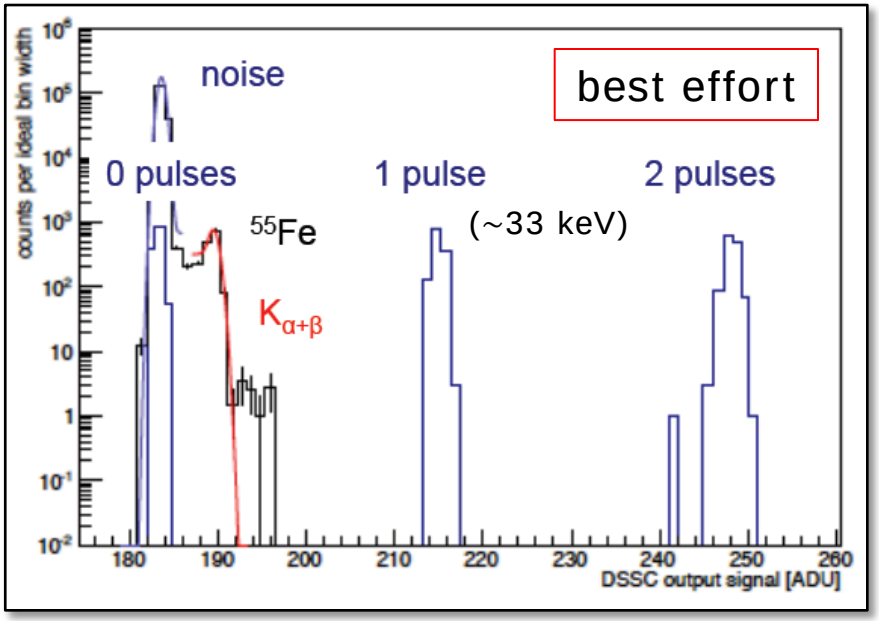
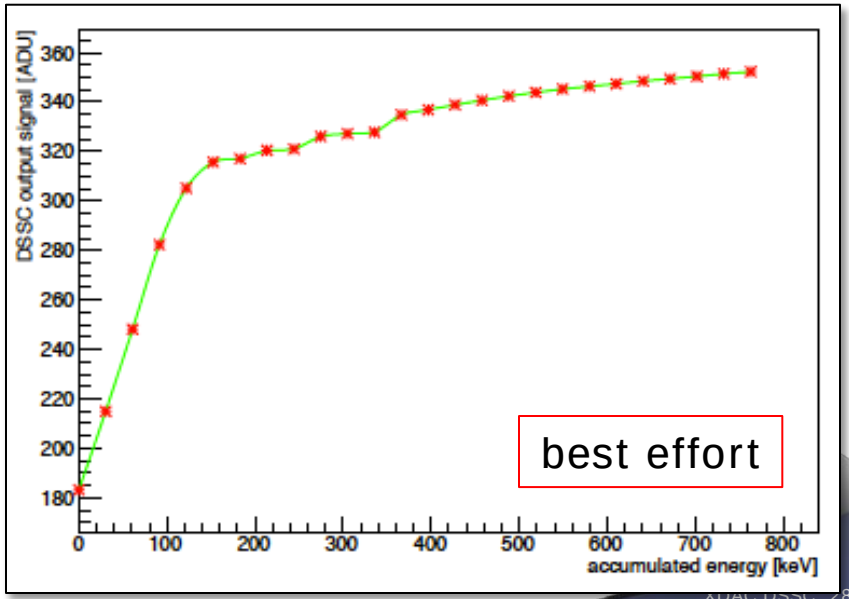
⇒ non-linear system response (NLSR), i.e. digital output as function of input charge (or equivalent energy)





Experimental Calibration of NLSR

Next steps:

- repeat using new (improved) set-up with MM3 ASIC prototype
- simultaneous calibration of all 7 pxd-7 pixels with MM3
- calibrate single pxd-8 pixel with MM3

Experimental Study of Calibration Properties of MM3 ASIC Prototype

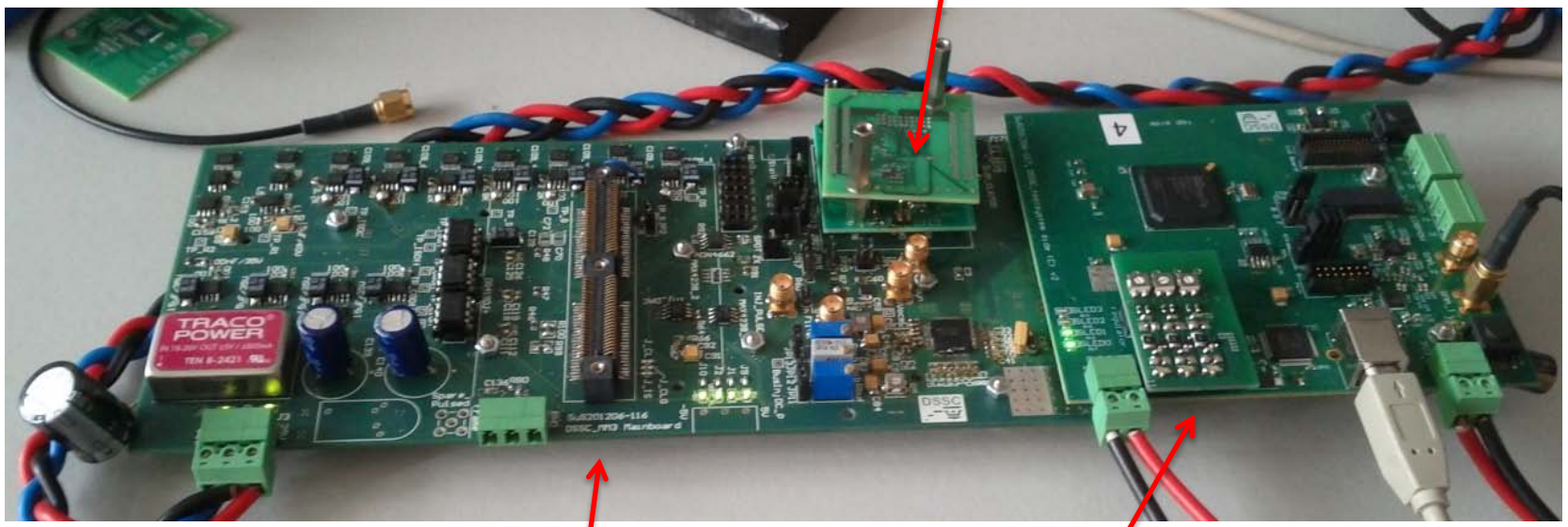
Studied properties include:

- accuracy of ADC bin boundary determination
- ADC functionalities for fine tuning offset and gain
- gain dependence on front end filter integration time
- gain dependence on ADC sample-and-hold capacitance
- pulsed charge injection
- measurement of ^{55}Fe spectra
- ...

Calibration strategy depends on ASIC calibration properties...

MM3 Prototype Set-up

MM3 ASIC
(below cover)



main board

FPGA board

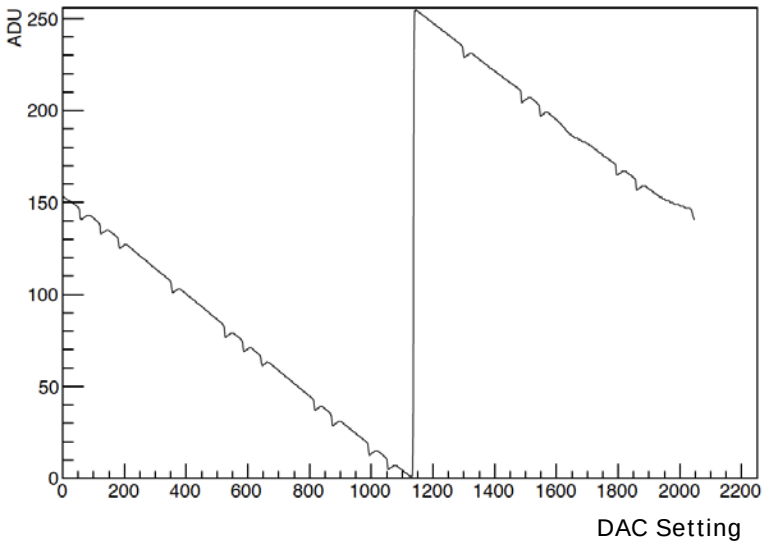
Until recently, set-up(s) still at Mannheim University for testing, optimization, operation and documentation.

Since two weeks: set-up and MM3 ASIC operated at HLL.

MM3 versus MM2

MM2:

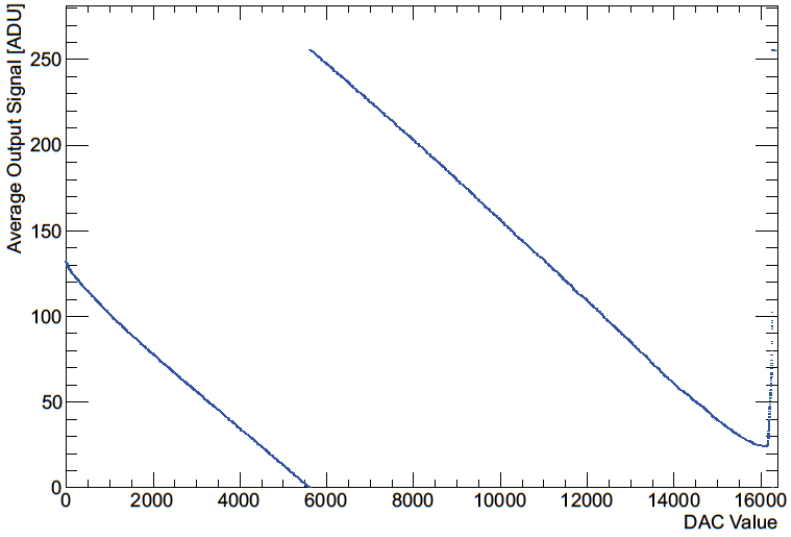
- ADC characteristic not always monotonous



- all channels: ADC with GCC
- limited settings for offset and gain

MM3:

- monotonous ADC characteristic



- 50/50: channels with GCC and in-pixel counter
- settings for offset and gain close to final

⇒ MM3 significant improvement
⇒ more accurate calibration tests

Status of Study

- measurement procedures and data formats established
- calibration software updated
- work in progress:

  optimization of set-up and MM3 ASIC operation

Next step:

systematic and detailed study of calibration properties

BACKUP SLIDES

2nd Generation: Mechanical Accuracy Budget (X & Y)

- *Only to MB frame, EXCLUDING inaccuracies in glued assembly*

- Single Ladder (relative to drawings):
  - *Maximum* error in X (cooling block to MB Frame) ~ 24 um
  - *Maximum* error in Y (cooling block to MB Frame) ~ 36 um
  - Expect ~ 20 um or so error in a single ladder's position
- Ladder-to-Ladder:
  - Expect ~40 um or so error ladder-to-ladder

- The above values are for initial assembly, and valid at RT.
- Repeat assembly FROM IDENTICAL PARTS is better, for single ladder
  - Maximum error in X given as 4 um, maximum error in Y given as 16 um
  - Expect ~ 10 um or so deviation from previous position in a single remounted ladder

Planarity of 1M module (1st and 2nd Generation)

Only to MB frame, EXCLUDING inaccuracies in glued assembly

"z variation" = deviation from drawings

For the fixed hole versions, the measures stop at the common mounting plate for the full 1M system. For the variable hole versions, we assume the mounting fixtures for the first part of the XY translation systems are perfect in space.

- 1st Generation, fixed hole:
  z variations 70 micrometers (20 of which from non-planarities of the back mounting plate, so adjacent ladders would see similar situation)
- 1st Generation, variable hole:
  z variations max. 110 micrometers, 60 of which would be common to the 4 ladders making up one quadrant.
- 2nd Generation, fixed hole:
  z variations max. 50 micrometers (20 of which from non-planarities of the back mounting plate, so adjacent ladders would see similar situation)
- 2nd Generation, variable hole:
  z variations max. 80 micrometers, 60 of which would be common to the 4 ladders making up one quadrant.

Cooling Options – in chamber

Investigations of cooling path options within the vacuum chamber have commenced. At this early stage, 3 options are being considered:

1. Liquid coolant flow to a (non-moving) interface within the vacuum,
   rigid (fixed-hole) or braided (movable quadrants) Cu paths to the cooling blocks.

   To achieve reasonable heat transfer, for a flexible solution on the order of 20 1.5cm-diameter Cu braids would be required per quadrant.

2. Liquid coolant flow to a “cooling end piece” inside the vacuum,
   requiring flexible hoses inside the vacuum in case of movable quadrants. This “end piece” is then attached to the cooling block.

3. Liquid coolant perfusion of the cooling block itself.
   This should give best temperature uniformity at the sensor, but also requires added complexity of the cooling block itself and may well require flexible hoses even for a fixed-hole solution.

Cooling Plant available for tests

Current baseline acquired:
JULABO FPW91-SL + Pump upgrade

- Cooling bath design (slow but stable)
- 2.7 kW cooling power at -40° C
- 1.5 kW cooling power at -60° C
- 350 W at -80° C
- Up to 3 bar pressure / 30 l/min (upgraded)
- Compact design (85x76x116 cm)
- 320 kg (empty, 22l coolant volume)
- PDMS (silicone oil) coolant
- Power consumption ~13 kW plant, ~1 kW pump -> about 1.1 kW dissipated to air, rest to cooling water

This cooling plant is probably overspec'd.

For first trials, shared with AGIPD.