Large Pixel Detector XDAC Review
27-28 May 2013

LPD Team:

Matthew Hart et al

Science and Technology Facilities Council
Rutherford Appleton Laboratory

Science & Technology Facilities Council

European XFEL

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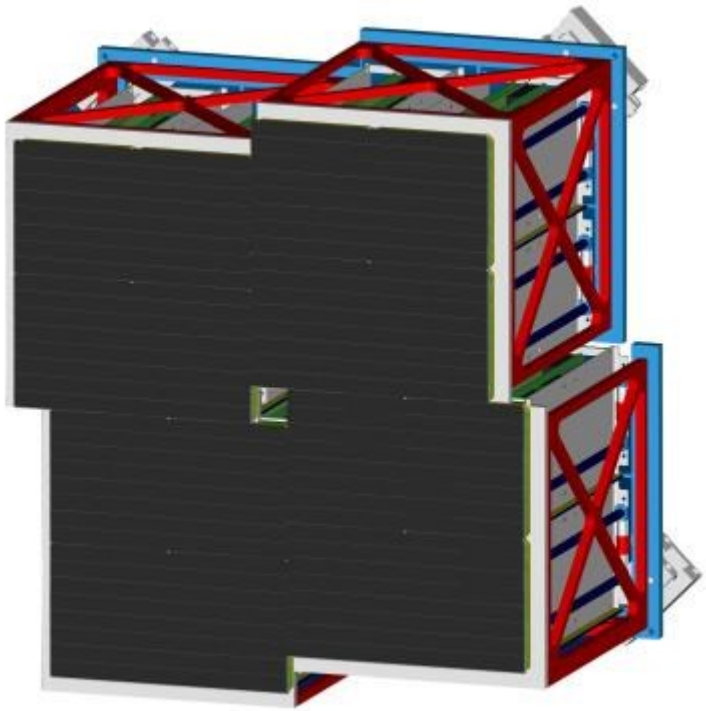
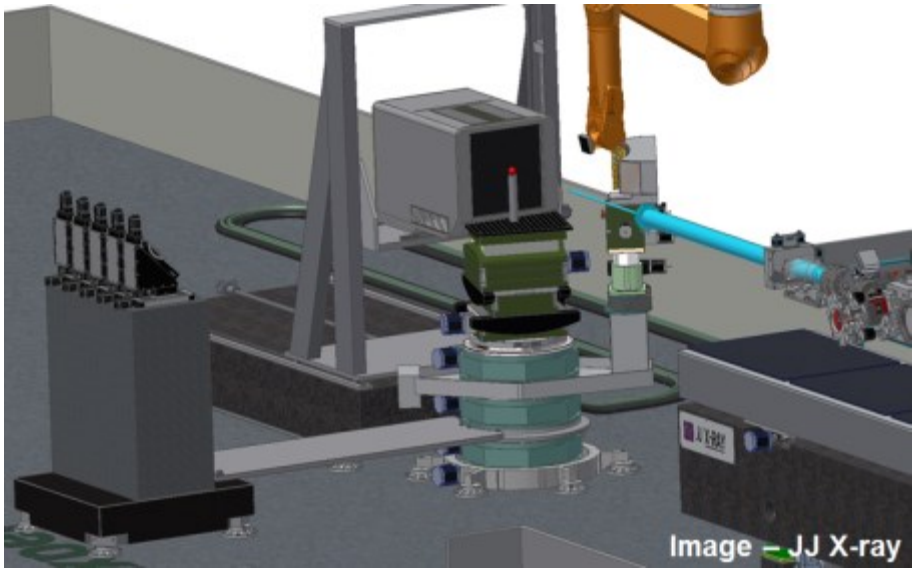
Overview

- Feedback from the last XDAC
- Project Status
  - The completion of Phase 1
  - Phase 2
- Highlights:
  - ASIC V2 First test results
  - 2-tile system @ XFEL
  - Beam tests at LCLS and Petra III
- Reports
  - Workpackage reports
- Summary and Next Steps



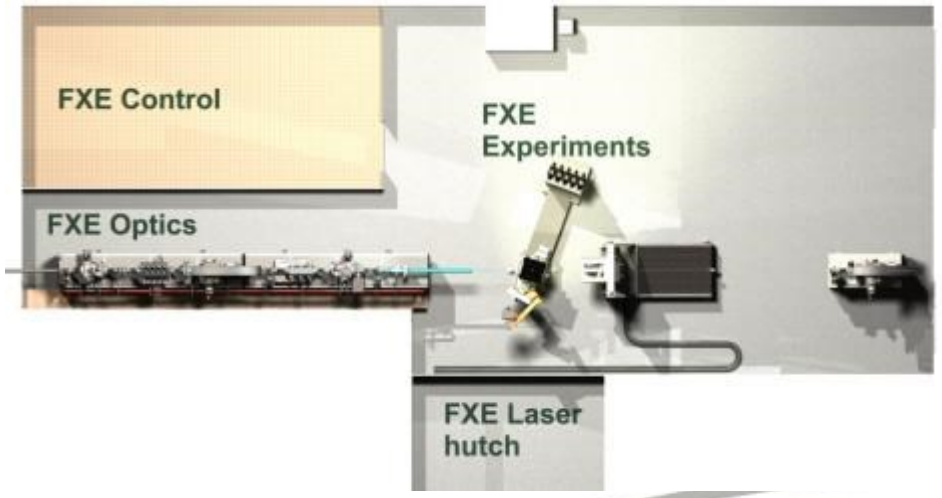
XDAC Feedback General Points: LPD beamlines on Day1

- Held meeting with JJ X-ray
- Actively sharing designs
- Ensuring the cabling and services are incorporated
- Will be sharing the full Mpix design shortly for review



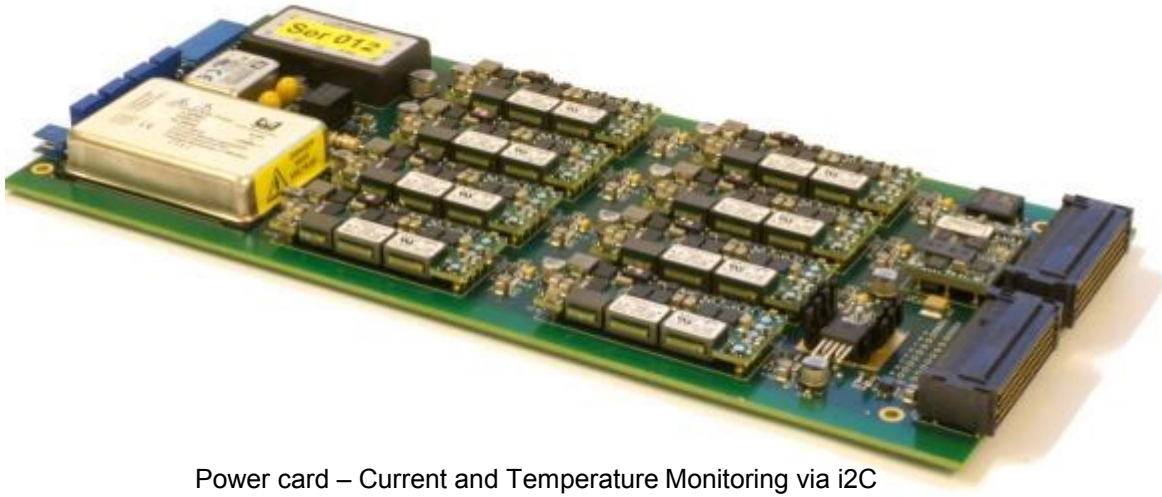
Goal:

Ensure full support and endstation readiness for LPD



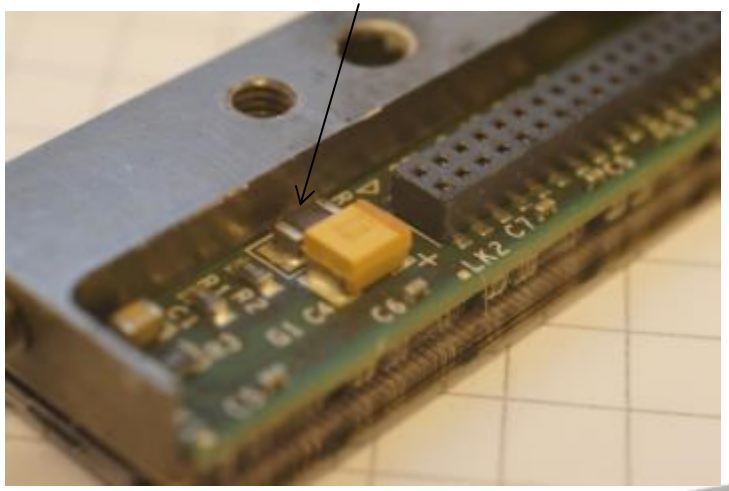
XDAC Feedback General Points: Hardware must “protect itself”

- System is fully instrumented with temperature and overcurrent monitoring and alarms
- Failsafe shutdown included that does not rely on external systems
- System records reason for shutdown so on reboot the reason can be identified
- System sequencing also included that starts Quadrants and modules in order and only enables system bias when powered
- Further high level protection in review



Power card – Current and Temperature Monitoring via i2C

Module PCB – Temperature sensors located on every tile.



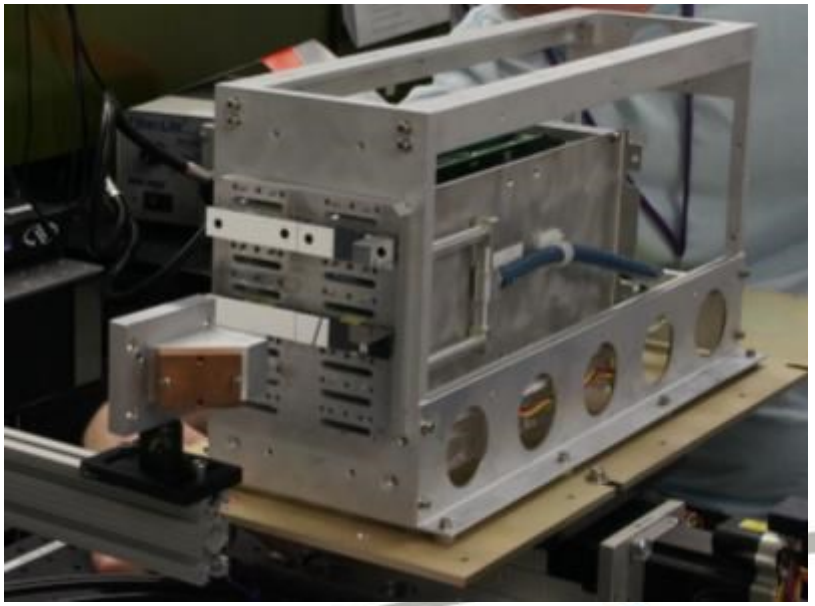
XDAC Feedback General Points: Requirement for small systems

• The 2-tile system is still supported and we will try to keep the design compatible throughout

Two tile system

• Longer term a single super-module may prove to be the better small scale system.

A super-module at LCLS



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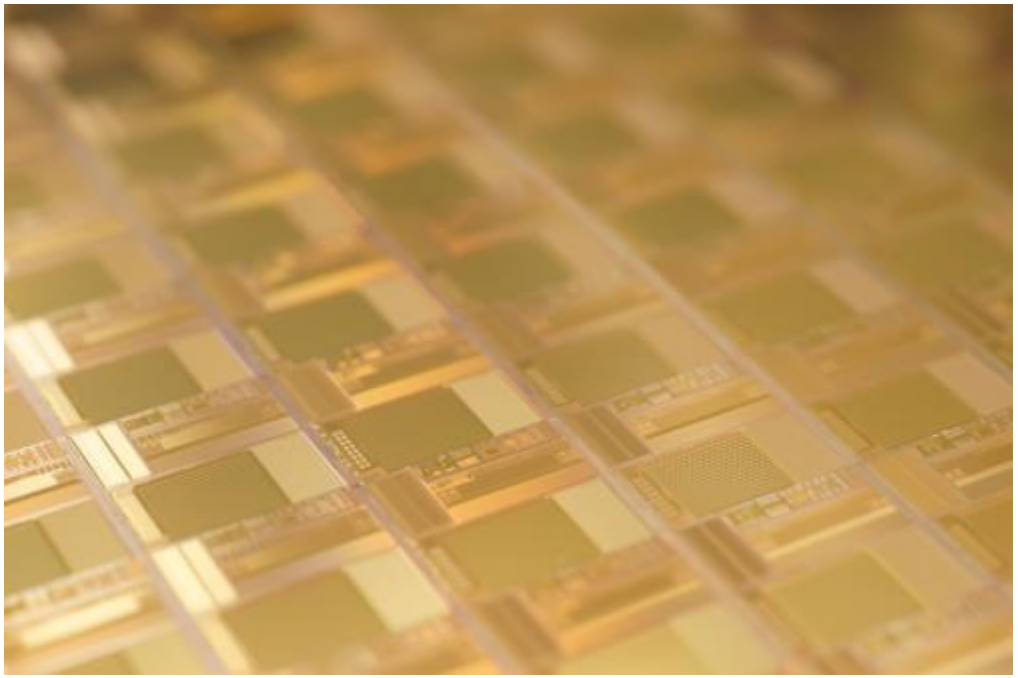
XDAC Feedback General Points: IBM Delays

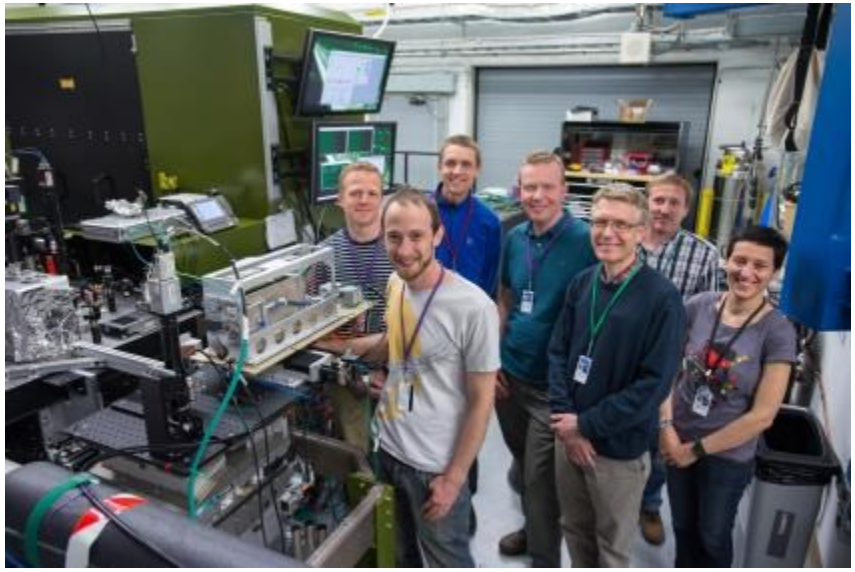
- We have reviewed IBM delays last year, much was caused by tape-out procedure and complexity with the shared wafer finish, it would have been ~4weeks quicker had we paid more…
- Quotes from CERN suggest 2-3 months for wafer production
- If we have approval all 1Mpixel wafers would be procured in one lot
- Also stock of current design exists at IBM (5wafers) that could be procured quickly

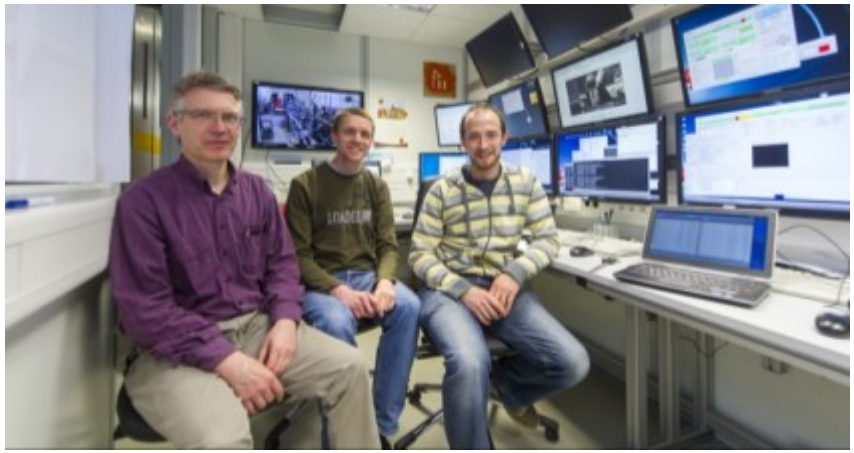


IBM Wafer

XDAC Feedback General Points: The use of Petra III

- Beamtests have proven invaluable (more later in presentation)
- We will discuss with XFEL about how we plan and resource further tests and future beamtime etc.
- The support from Desy and LCLS is very impressive and is much appreciated!





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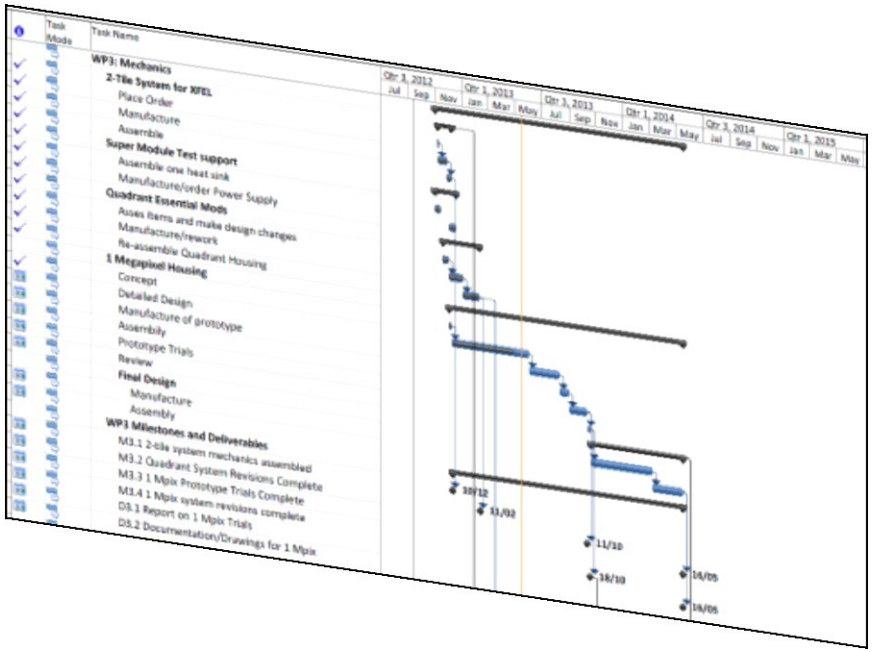
XDAC Feedback LPD Specific: ASIC Progress

- We agree that the project was very frustrated and held up
- There were complications with the multi-project run submission, we were one partner
- The wafer sharing is cost effective in the longer term and rapid testing of the V2 ASIC has enabled evaluation to proceed quickly

XDAC Feedback LPD Specific:
The requirement for clearer planning

- We have a full plan we are tracking in Phase 2
- The additional load of the two beamtests have had some impact
- Currently holding weekly telephone meetings to ensure the programme is communicated in XFEL and plan revisions discussed
- Have included a copy of the plan at signoff for Phase 2 to the XDAC report this time



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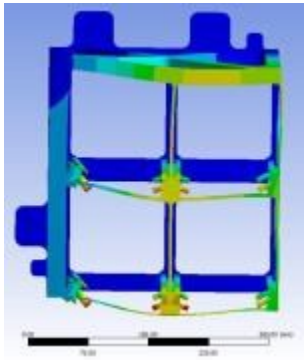
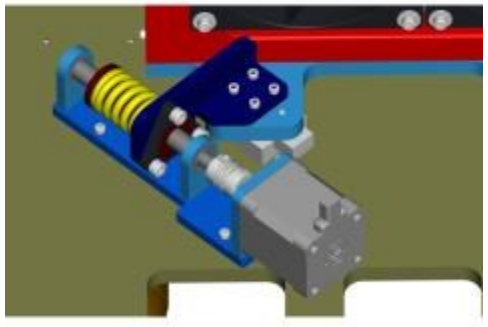
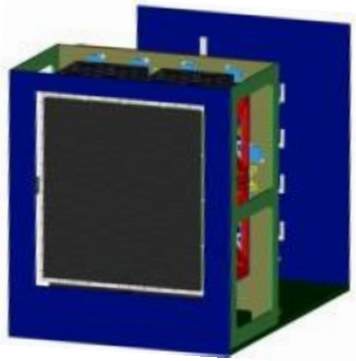
XDAC Feedback LPD Specific:

The lack of visible progress with mechanics

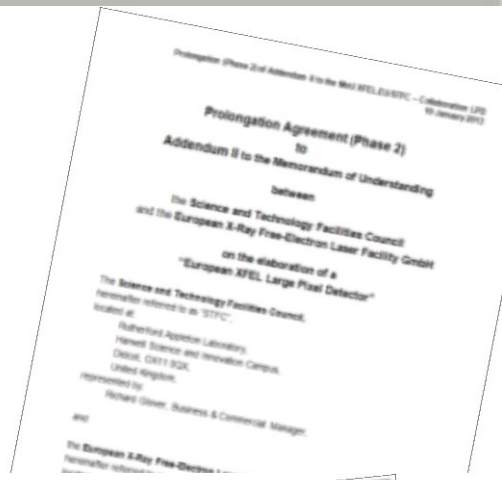
- The design is now quite far advanced and close to reviewing with XFEL prior to manufacture
- This will be covered in the WP section later in this presentation







The start of Phase 2



Meeting held 15-16th Jan

- Phase 1 Project Report reviewed and signed off
- Funding agreed to complete first LPD instrument
- Prolongation Agreement signed

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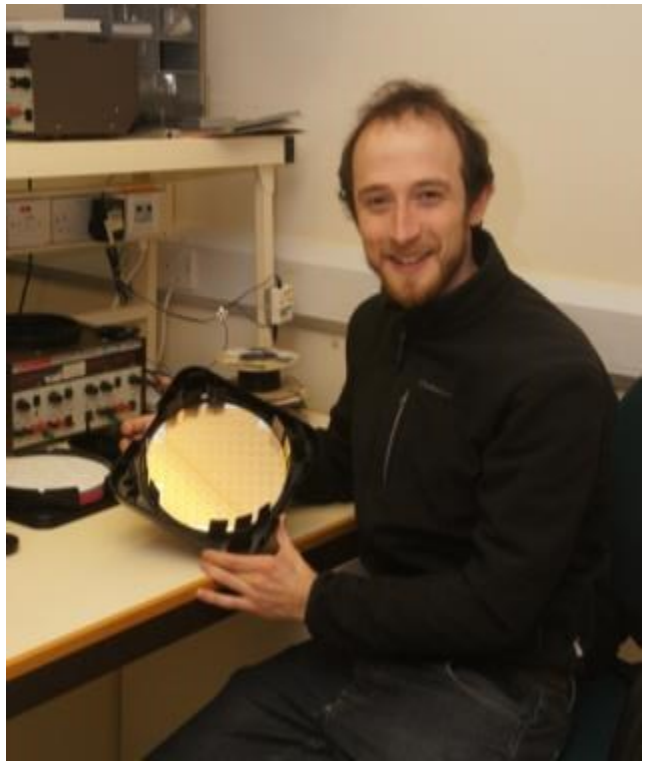
ASIC V2

• First tests on the probe station confirmed basic function in the first week.

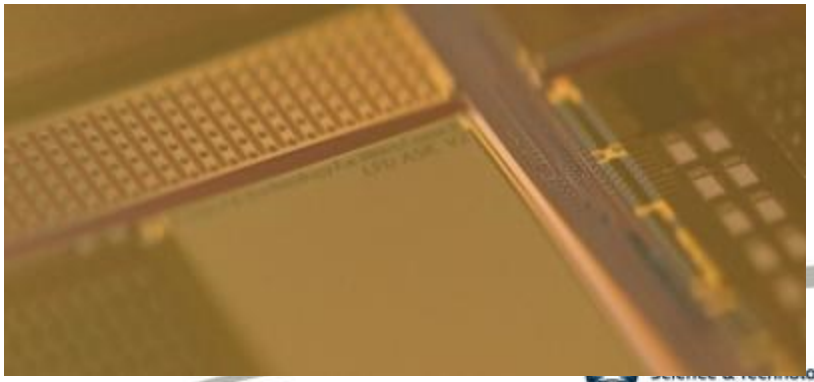
• Correction to ADC works. System can now work constantly at full speed.

• All other features look OK



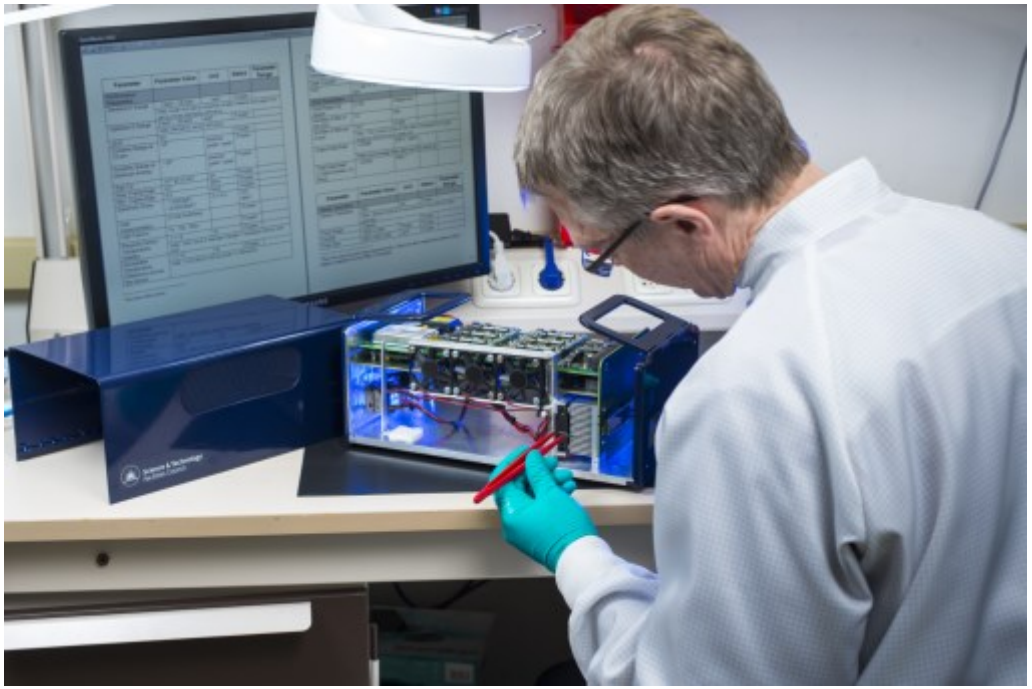
What we have done:

- Half wafer diced for single chip tests – to confirm noise performance and other tests
- 5 wafers probed and diced for assembly of V2 modules ready for beam tests.



2 Tile System Delivered to XFEL and now installed at Hera South

- Multiple copies of two tile system available, with one permanently at XFEL all with STFC built PC and software
- Originally shipped with V1 ASICs the system is now upgraded to V2 ASIC tiles and firmware
- Additional trigger card provided to allow synchronisation of tests at Petra with the beam structure
- Enables single bunch selection and readout



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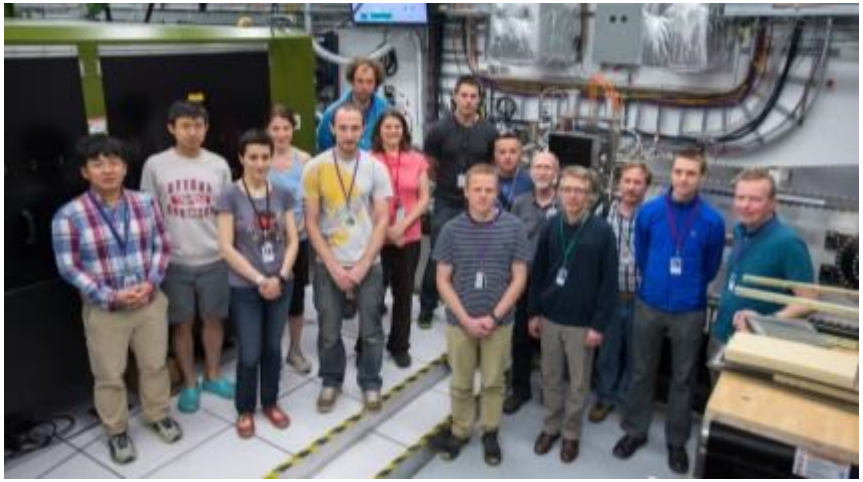
Beam Test1: LCLS May 2nd to 3rd

- Earlier visit to LCLS ~18th-20th March took place to meet and plan
- Took partially populated super module system with RAL 2-tile as backup
- Key Goals: Explore timing, dynamic range and flood performance of LPD
- Excellent support and cooperation from LCLS Team

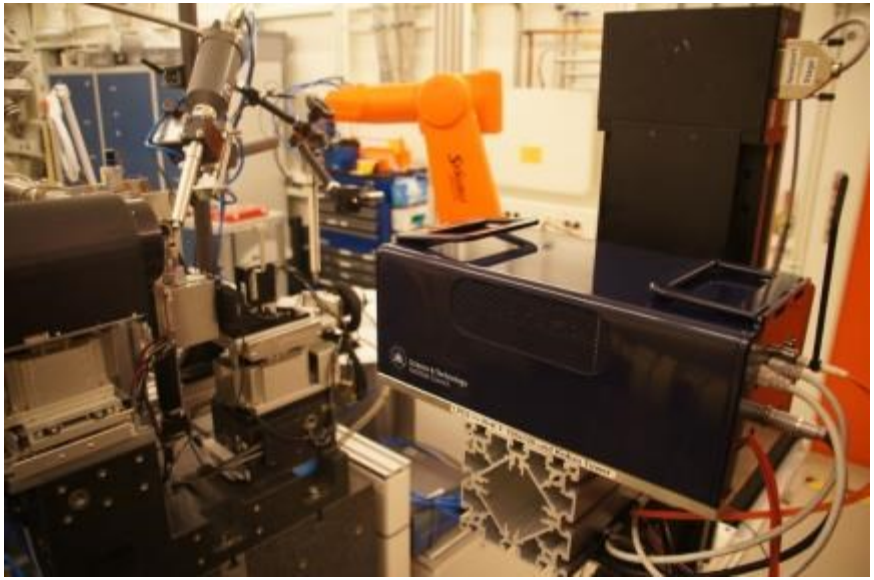


XPP Beamline at LCLS May 2013

SLAC

Beam Test2: PetraIII 8th to 14th May

- XFEL 2-tile system
- Undertook fast timing and radiation damage studies
- Measured noise and position resolution
- Also integrated the s/w with Karabo



LPD 2tile system at P11

PetraIII

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LPD Work Packages

WP1: Sensors - **CLOSED**

WP2: Front End Electronics (ASIC) - **CLOSED**

WP3: Mechanical Design

WP4: On Detector Electronics

WP5: Data Acquisition

WP6: Software, Controls and Integration

WP7: Calibration and Characterisation - **NEW**

WP8: System Build - **NEW**

WP3 Mechanical Design

WP Leader: Stephen Burge

Team: Martin Baldwin

- Second 2-tile system assembled for XFEL
- Complete the modifications to the quadrant detector
- Commence the design of the 1Mpix mechanics with adjustable hole

WP 3 – Mechanical Design

- Second 2-tile system assembled February 2013
- Delivered with readout PC early March 2013

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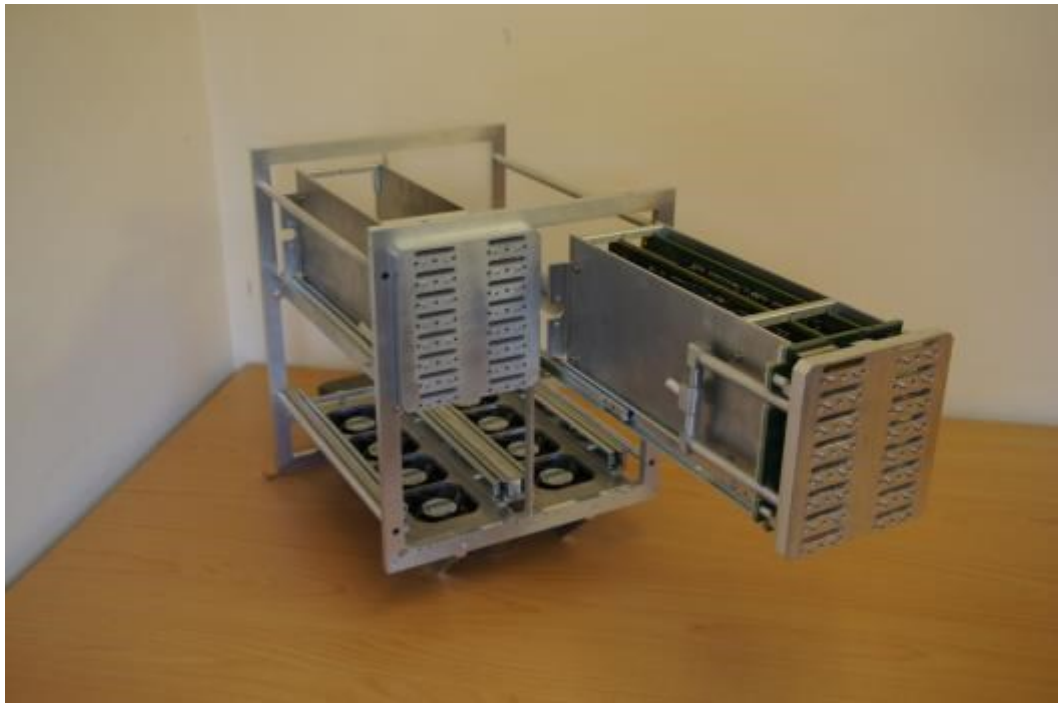
WP 3 – Mechanical Design

- Modifications to the Quadrant detector
  - Heat sink
    - sides trimmed down after gluing step,
    - higher grade glue now in use.
    - Improvements to pipe connectors
  - Easy super-module loading mechanism with sliding rails.
  - Super-module chassis redesigned
    - Thicker plate for greater strength
    - Smooth load into sliding rails
    - Bar to lock FEM and Power card in place
    - Better access to Module attachment screws.
  - Sensor face moved back 10mm from window

WP 3 – Mechanical Design

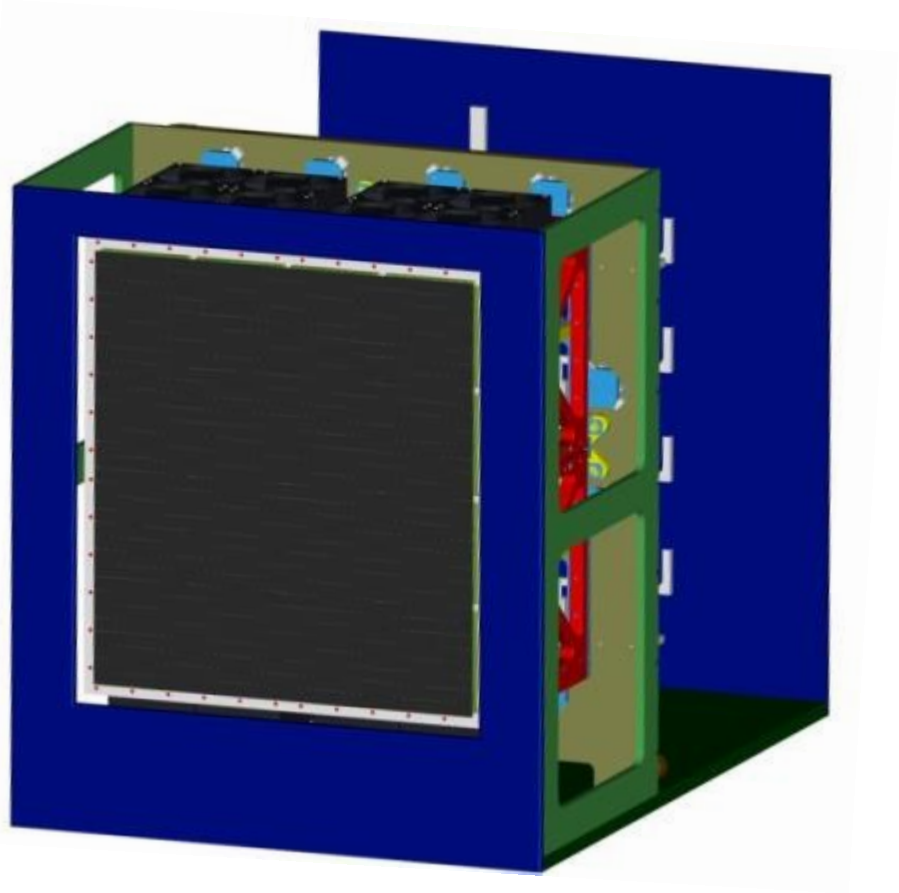
The Super-Module rail loading mechanism in action

- Widely accepted that the detector will be damaged and systems should be in place to easily replace elements of the detector



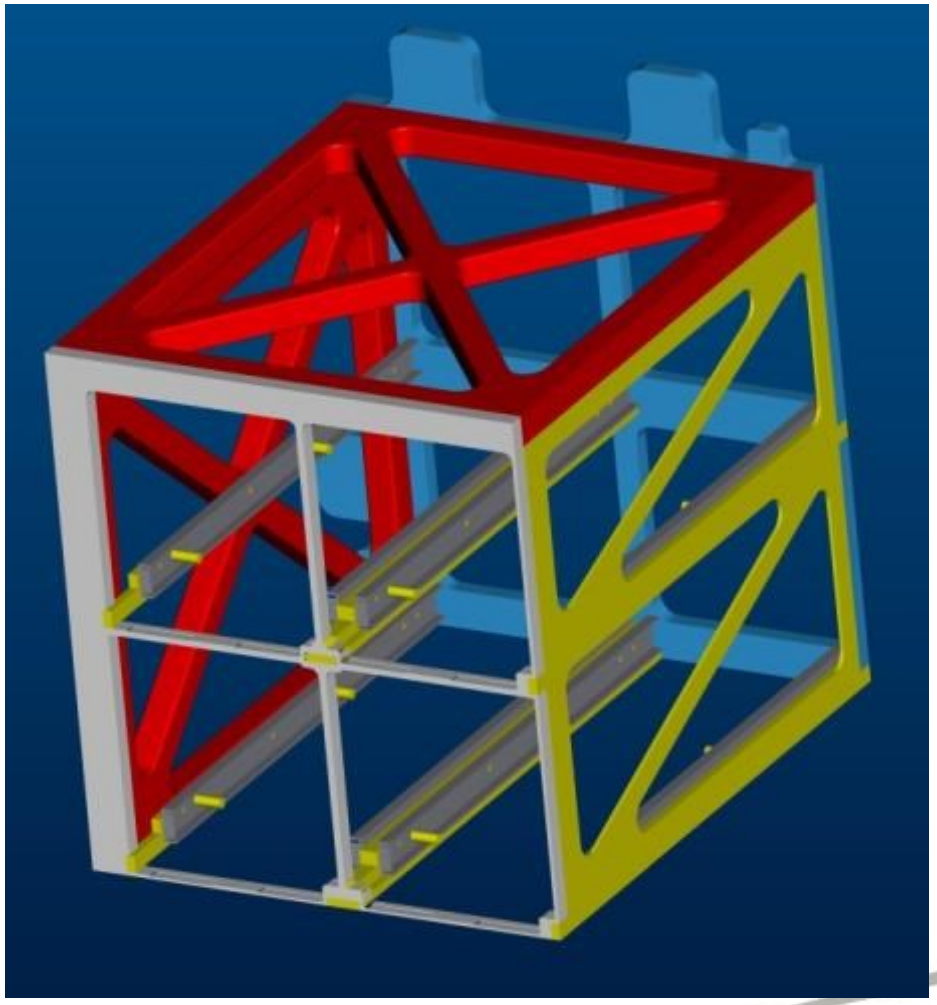
WP 3 – Mechanical Design

- 1Mpix Mechanics with Adjustable Hole



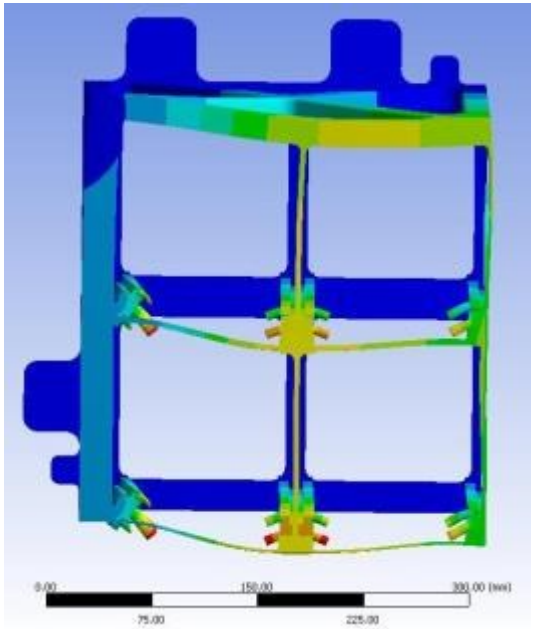
WP 3 – Mechanical Design

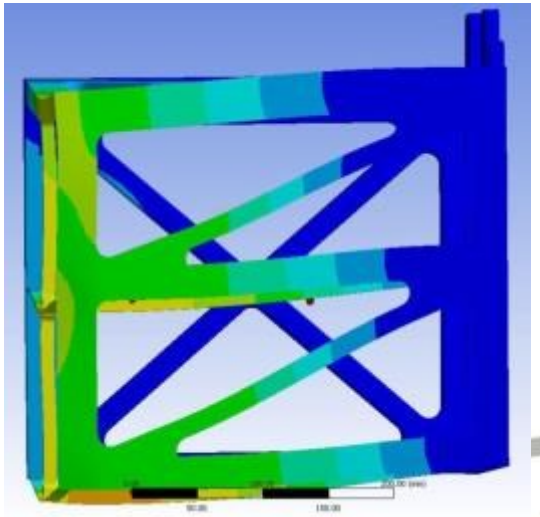
- 1Mpix constructed from 4 quadrant cages



WP 3 – Mechanical Design

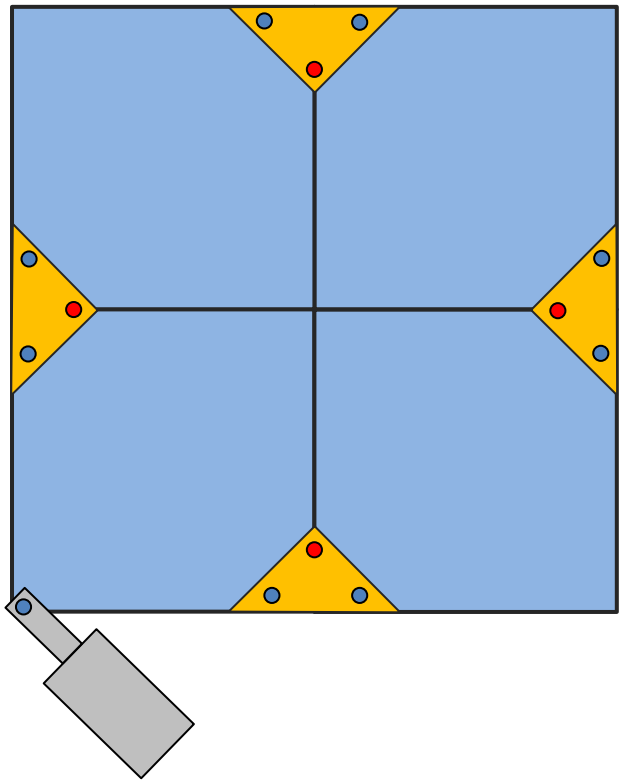
- FEA Analysis of Mpix
  - Quadrants simulated with super-module weight.
  - Maximum deflection is in the front of each frame - 15um
  - More bracing has been added to the center to reduce this further.
  - For comparison specification agreed with XFEL is +/-100um for pixel positions following hole size changes.
  - Gap between quadrants is 100um





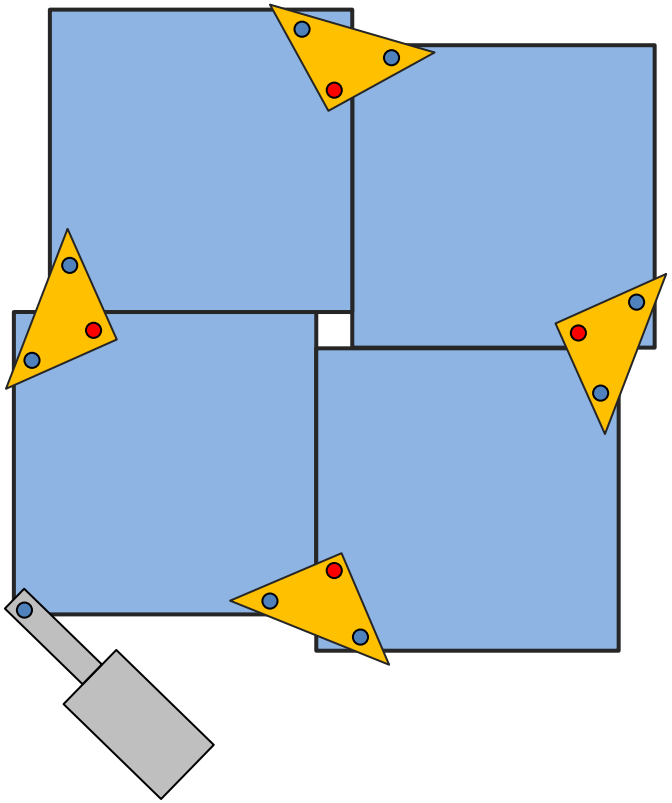
WP 3 – Mechanical Design

- Sliding Hole – Stepper Motor and Bell Crank Linkage



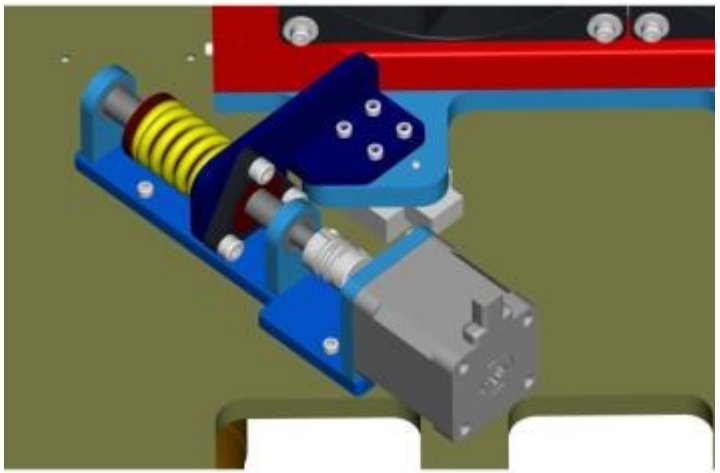
WP 3 – Mechanical Design

- Sliding Hole – Stepper Motor and Bell Crank Linkage



WP 3 – Mechanical Design

- Beckhoff Stepper Motor
  - EtherCAT system
  - Lead screw
  - Anti-backlash bearing
  - Cannot move when unpowered



- Bell-crank Linkage
  - Only one quadrant is driven
  - Quadrants move together
  - Weight of quadrants balances through linkage.

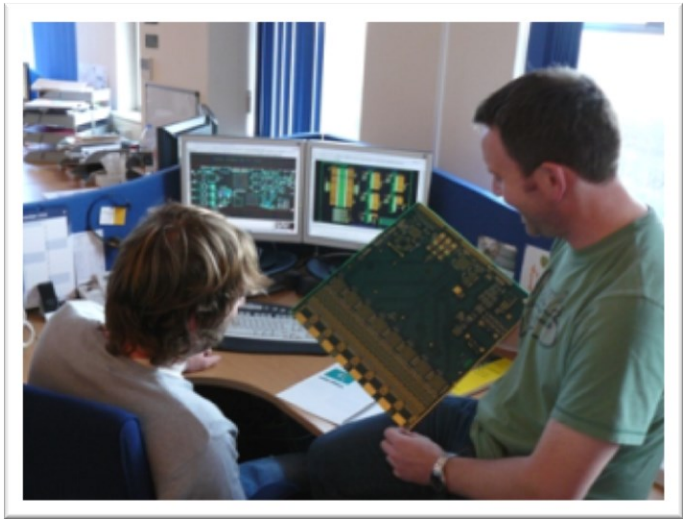
WP 4 – On Detector Electronics

WP4 On Detector Electronics

WP Leader: Stephen Burge

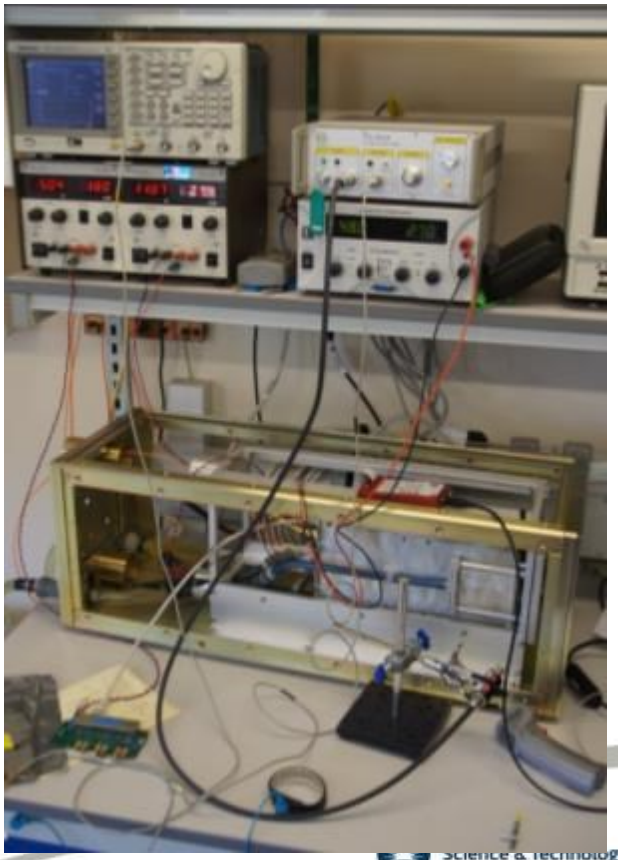
Team: RAL Drawing Office

- Interface Board for Super-Module and Quadrant Scale Systems
- Modified Feed-through Cards for improved noise performance.



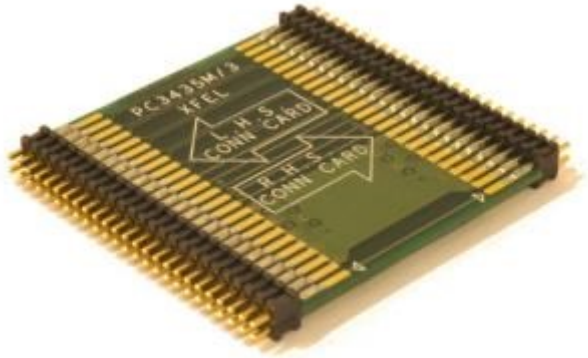
WP 4 – On Detector Electronics

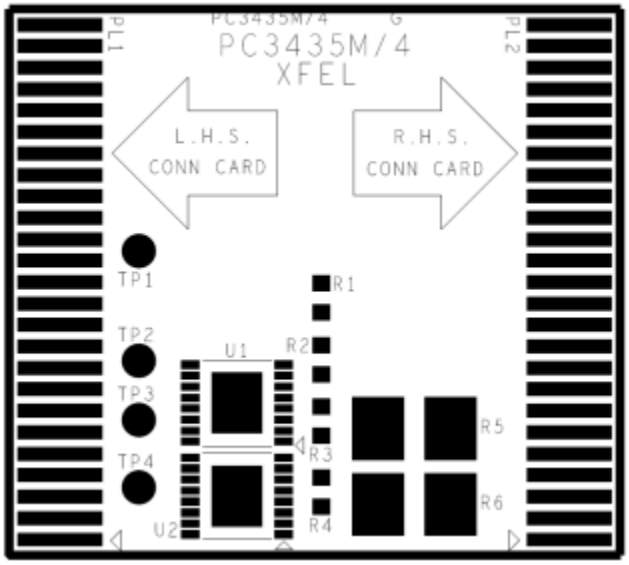
- Interface Board (Trigger Box) for Super-Module and Quadrant Scale Systems
  - TTL to LVDS converter for triggers and clock signals
  - Outputs compatible with the clock and control port on the FEM
  - Used on LCLS and PETRA III

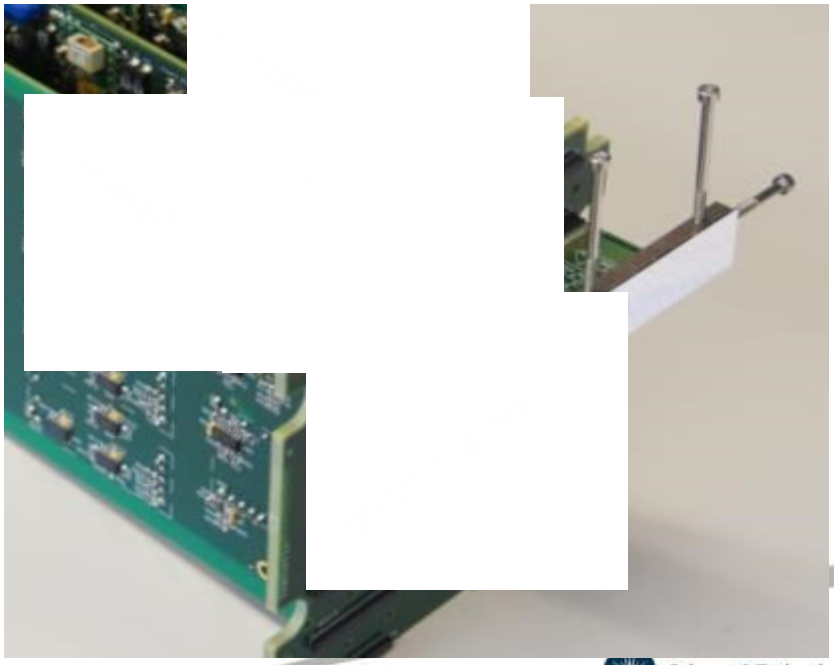


WP 4 – On Detector Electronics

- Modified Feed-through Cards for improved noise performance.
  - Power supply ripple is too great to achieve full noise performance. >10mV
  - Low drop-out regulators added to the feed-through card will bring this back to specification.







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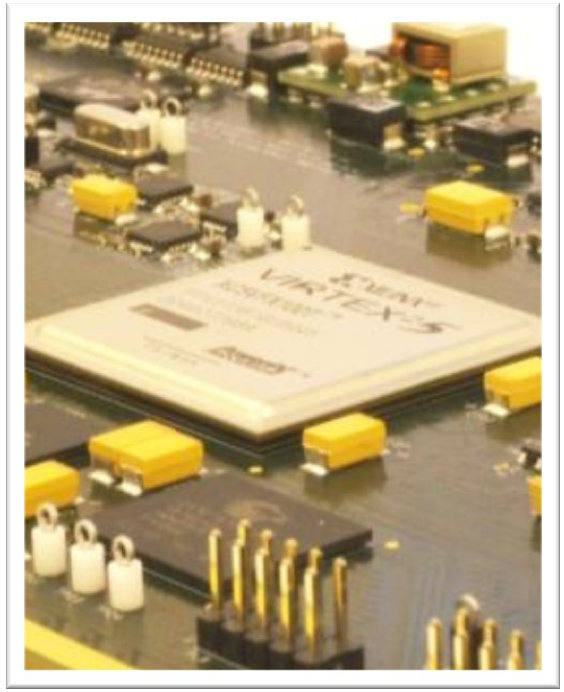
WP5 Data Acquisition

WP Leader: John Coughlan

- System testing at RAL and XFEL
- First Beam Tests with LPD detectors @
  - LCLS
  - PETRA III
- Future work



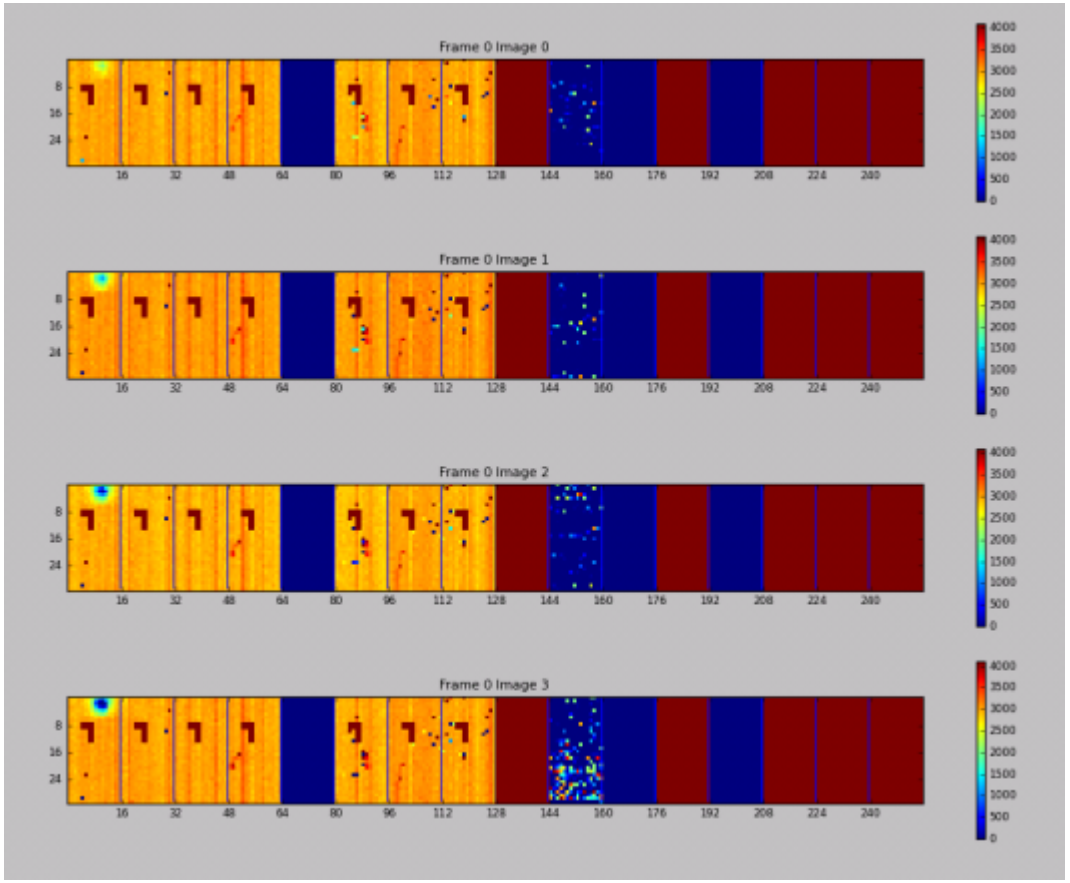
WP 5: Firmware & System Testing

@ XFEL 2-Tile system delivered in Q1 2013

@ RAL

- FPGA firmware adapted first to handle readout of ASIC vers 1 (slowed clock).
- Firmware allowing FPGA loading from Compact Flash memory card released.

WP 5: Firmware & System Testing



Testing control and readout at RAL on 2-Tile with sensors populated with ASIC vers 2.

Laser pointer spot on 2-Tile (only LHS sensor fitted).

Asics are programmed for “long exposure” without resets.

4 Images each separated by 10 bunch periods show spot intensity increasing.

WP 5: Beam Test Firmware

- Main effort was on Firmware (& python scripts) for first beam tests with LPD detectors.

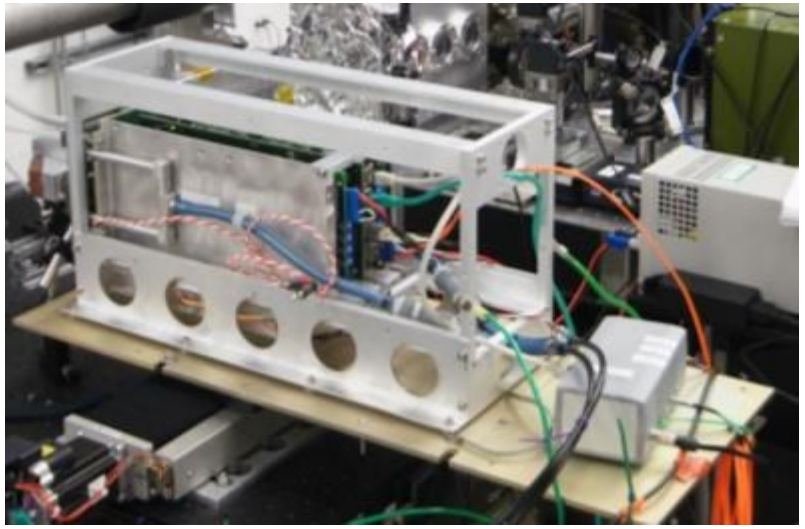
- Firmware Operation:
  - One FPGA bit file. Configuration for two beam tests via software registers.
  - Beam Synchronous Start Strobe initiates a pre-assigned (programmable) readout sequence of Triggers read from .xml file. Up to ~ 500 images per train.
  - **NEW:** Test mode permitting to readout ALL 3 gain values (by re-reading ASIC pipeline memory)

WP 5: Beam Test Firmware

- Interface to FEM Clock and Controls via RAL Trigger box
- Two different sets of machine signals.

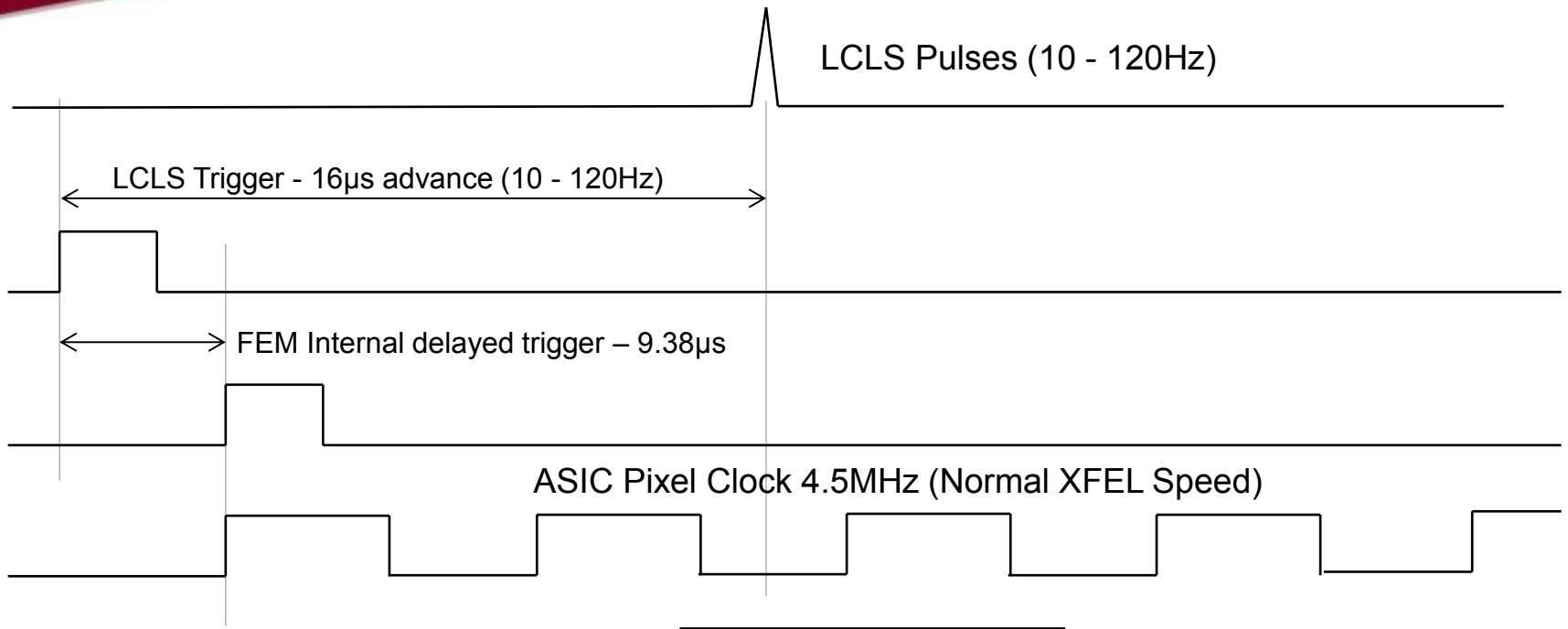
- LCLS Operation XFEL pulses @ 120 Hz:
  - Synchronous start strobe from LCLS
  - FEM local 100 MHz clock => 4.5 MHz Asic clock
  - Trains of ~ 10 bunches (one filled with X-ray pulse)

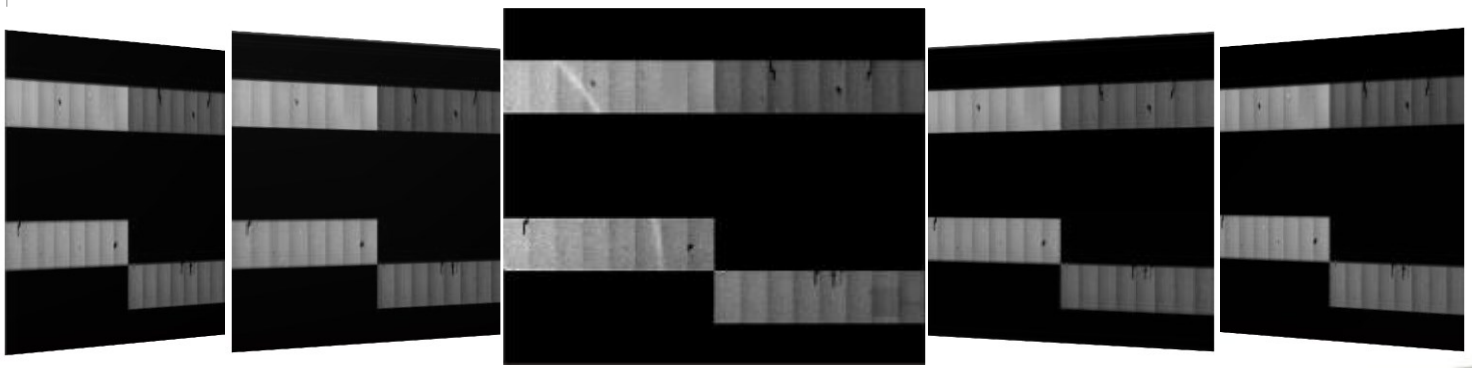
- PETRA III Operation X-ray pulses @ 5.2 MHz (exceeds XFEL design spec):
  - Petra III clock @ 5.2 MHz to drive Asic clock
  - Also used to derive the Synchronous start strobe
  - Async shutter signal to gate capture
  - Trains of up to 500 bunches.



WP 5: Beam Tests at LCLS

- Operation mode at LCLS





Pre-pulse Images | Pulse Image | Post-pulse Images

WP 5: Beam Tests at PETRA III

- May 8th – 14th (week after LCLS tests!)
- LPD detector tests and scientific experiments

- Synchrotron X-rays
- Test Synchronisation to PETRA III bunch structure @ 5.2 MHz.
- Test Radiation hardness.

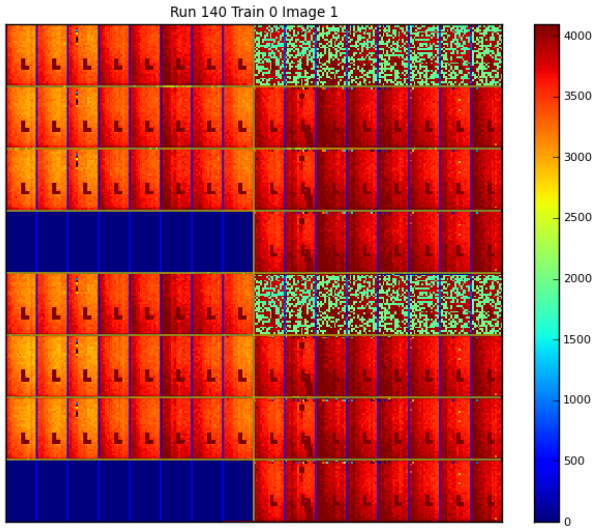
- 2-Tile populated with Asic Vers 2 sensor tiles
  - one FEM + 10G link

- Control and Readout via 10G links to local PC.
- Some Integration with Petra-III machine.

Future Work

- Resolve some issues identified running with Super-module:
  - 2 sensor locations have timing shifts
  - 2 sensor locations inhibiting booting of FEM FPGA
    - Cause identified – solution under investigation

- Implement firmware for LPD Phase 2:
  - Reintroduce PPC for data processing
  - Test C&C firmware with dynamic vetoes.
  - Add data header with veto information
  - Work with TrainBuilder project on pixel image reordering.
  - & others.



Summary

- Successful beam tests at LCLS and PETRA III
- 2-tile system operating at XFEL
- Another 10 FEMs ordered for LPD
  - likely to need more 10G FMCs next year

WP6 Software, Controls and Integration

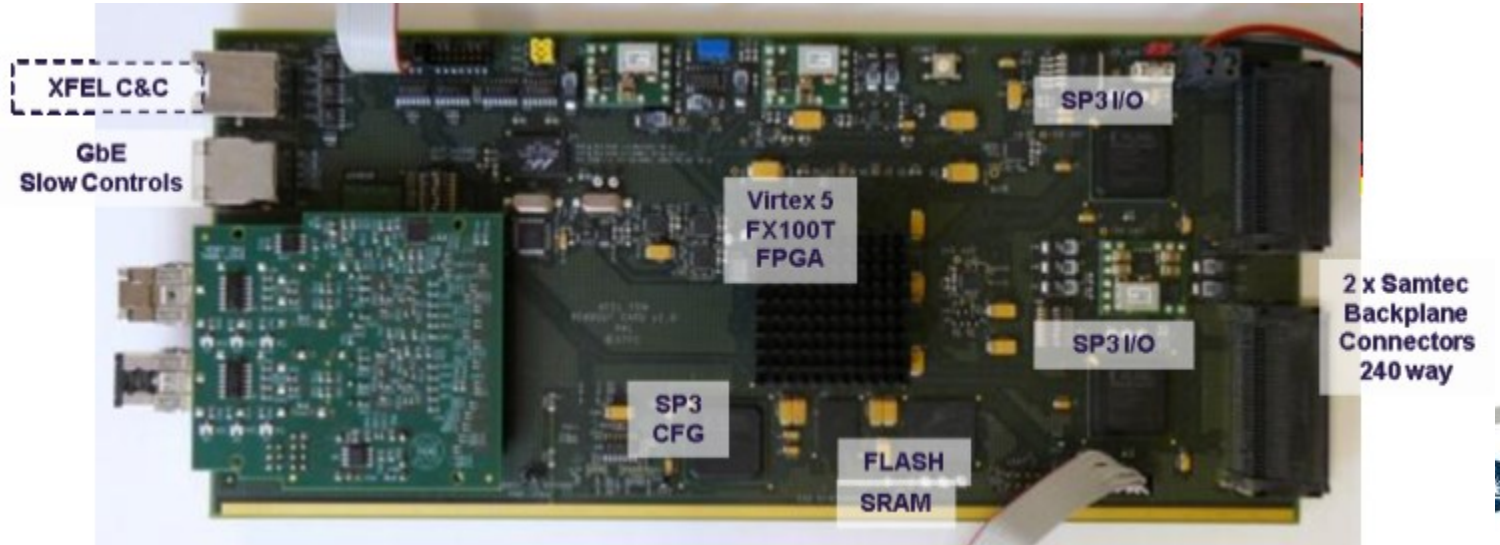
WP Leader: Tim Nicholls

Team: Christian Angelsen and Matthew Thorpe

- Completion of software for use with 2-tile systems and super-module systems
- Integration with Karabo
- Prototype data sink server
- Standalone GUI application
- Future

Architecture - HW & FW

- LPD readout based around FEM – 1GigE control path, (2x) 10GigE data path
- Control: Core V5 FPGA runs XilKernel/LwIP-based embedded software on one PPC core.
- Custom TCP binary transaction protocol to communicate between client and FEM (synchronous request-response, multiple concurrent clients)



Architecture - Software

- Client library implements FEM transaction protocol and provides access to all **control functionality** of FEM (data path not included)

- Implemented in Python module using small number of classes
  - **FemTransaction** – encoding of binary transaction protocol
  - **FemClient** – TCP socket communication and low-level access (r/w) primitives (memory, I2C, RDMA, internal etc)
  - **LpdFemClient** – LPD-specific functionality: control of firmware, management of ASIC setup etc
  - Helper classes to implement e.g. functionality of LPD power card (accessible via FEM external I2C bus)

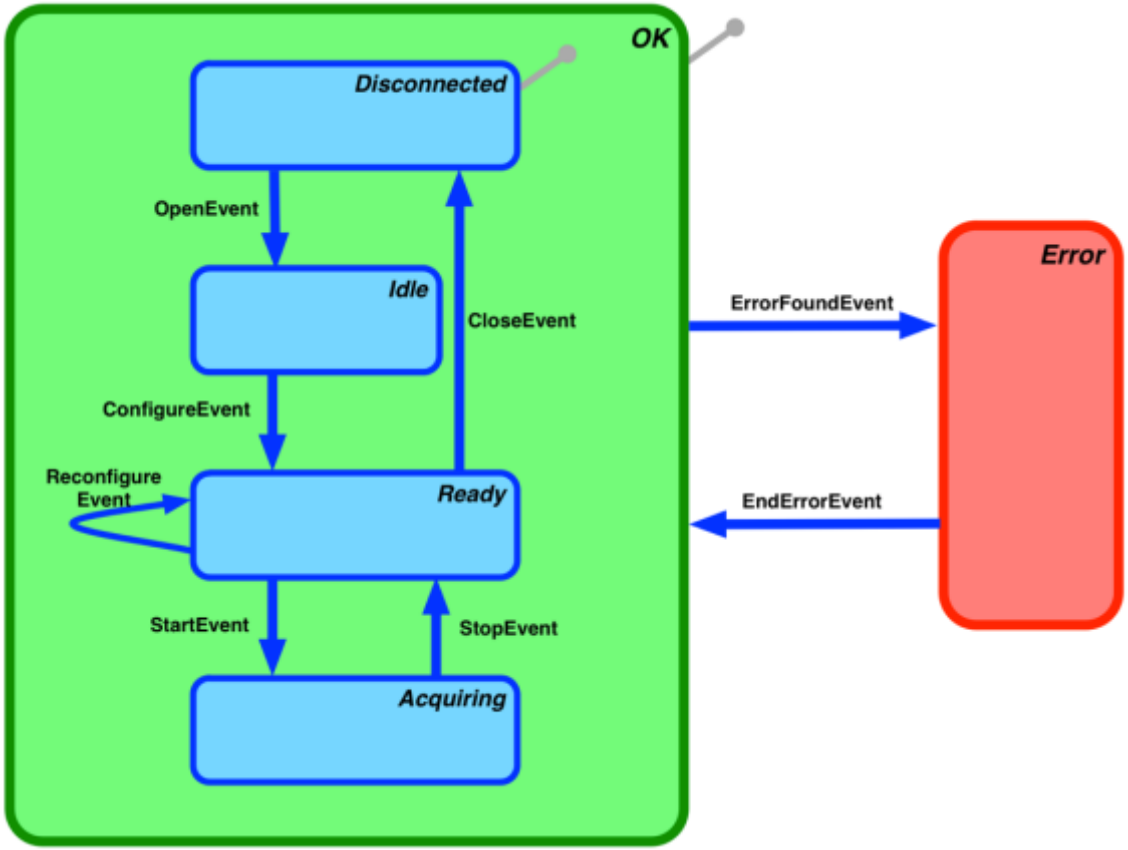
- Also tested basic **FemTransaction/FemClient** implemented in C++ using Boost ASIO – no difference in performance

Karabo Integration

- Integration through API agreed with WP76 in additional layer: **LpdDevice**
- **LpdDevice** is a Python class, which implements:
  - **open(), close(), configure(), start(), stop()** actions
  - **paramSet(<name>, val), paramGet(<name>)** accessors
- List of allowed parameters (“expected parameters”) defined through **LpdDeviceParameters** helper class
- Karabo **LpdFem** device implementation instantiates one **LpdDevice** instance per FEM
  - 1 FEM per supermodule, 16 total for megapixel detector
- Karabo device server architecture handles compositeness

LpdFem Finite State Machine

- **LpdFem** manages device through simple finite state machine
- State transitions associate
  etc.)
- Error transition and recove
- Async monitor thread polls



Expected Parameters

- **LpdDeviceParameters** defines allowed parameters
- **paramSet()/Get()** calls validate name, type, range
- Class generates Karabo “expected parameters” schema:

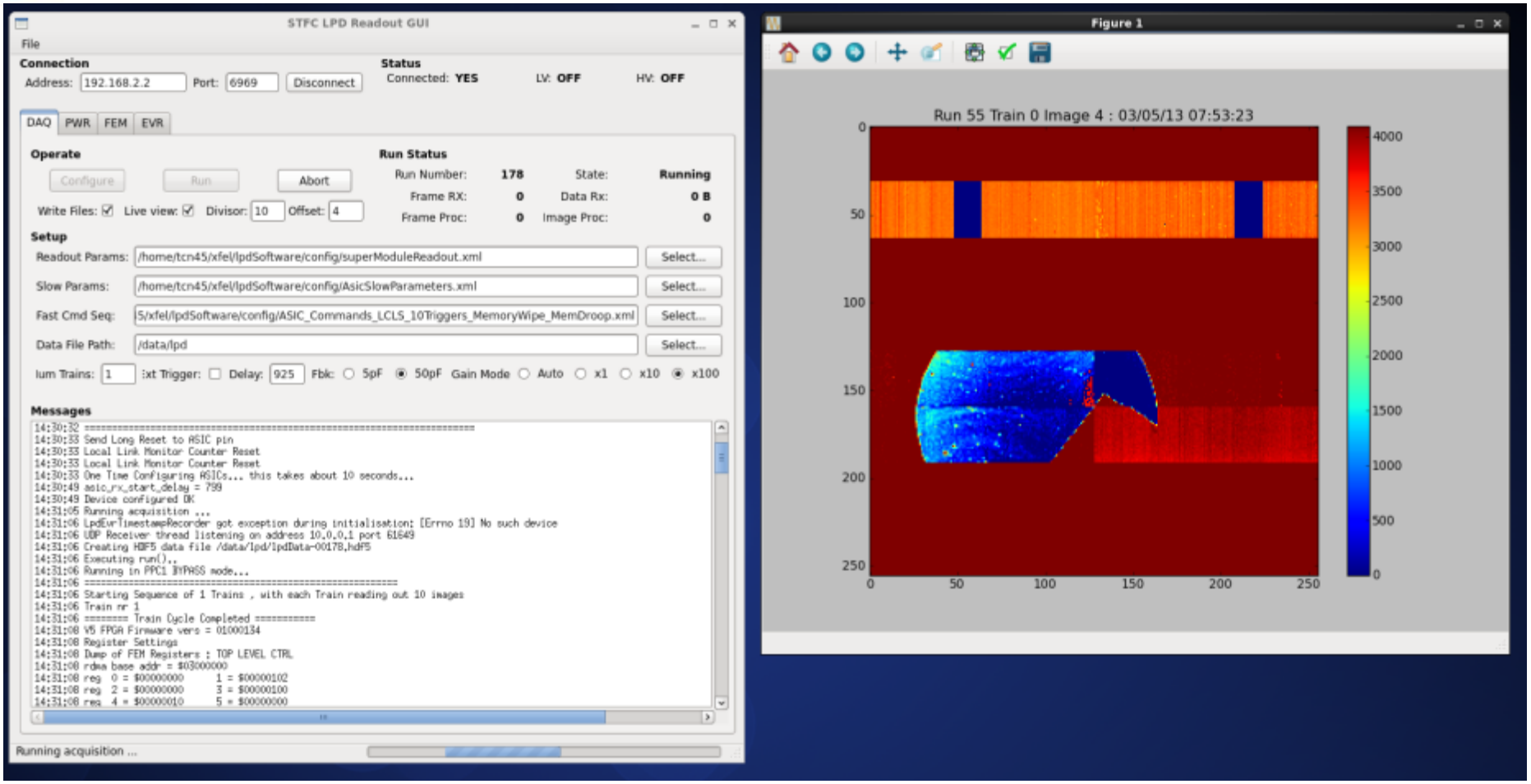
```
e = UINT32_ELEMENT(expected)
e.key("femAsicModuleType").displayedName("FemAsicModuleType")
e.description("Selects type of ASIC module 0=supermodule, 1=single ASIC, 2=2-tile module, 3=stand-alone")
e.assignmentOptional().defaultValue(0).reconfigurable()
e.allowedStates('AllOk.Disconnected')
e.commit()

e = DOUBLE_ELEMENT(expected)
e.key("sensor0Temp").displayedName("Sensor0Temp")
e.description("Sensor 0 Temperature [C]")
e.readOnly()
e.commit()
```

- Defines configurable vs monitor, allowed states, readable description etc
- Currently “cut’n’paste” into LpdFem device, will be callable generation

Karabo Integration Progress

- LpdDevice API is now used for all testing of LPD systems
- Standalone programs for receiving and decoding 10GigE data stream (aka “data sink”) – HDF5 file I/O
- LpdDevice stub library – simulated API allowed WP76 to develop LpdFem without h/w
- Full integration with Karabo undertaken on 2-tile system @ PETRA-III last week – SUCCESS!

WP 6 – Software, Controls and Integration



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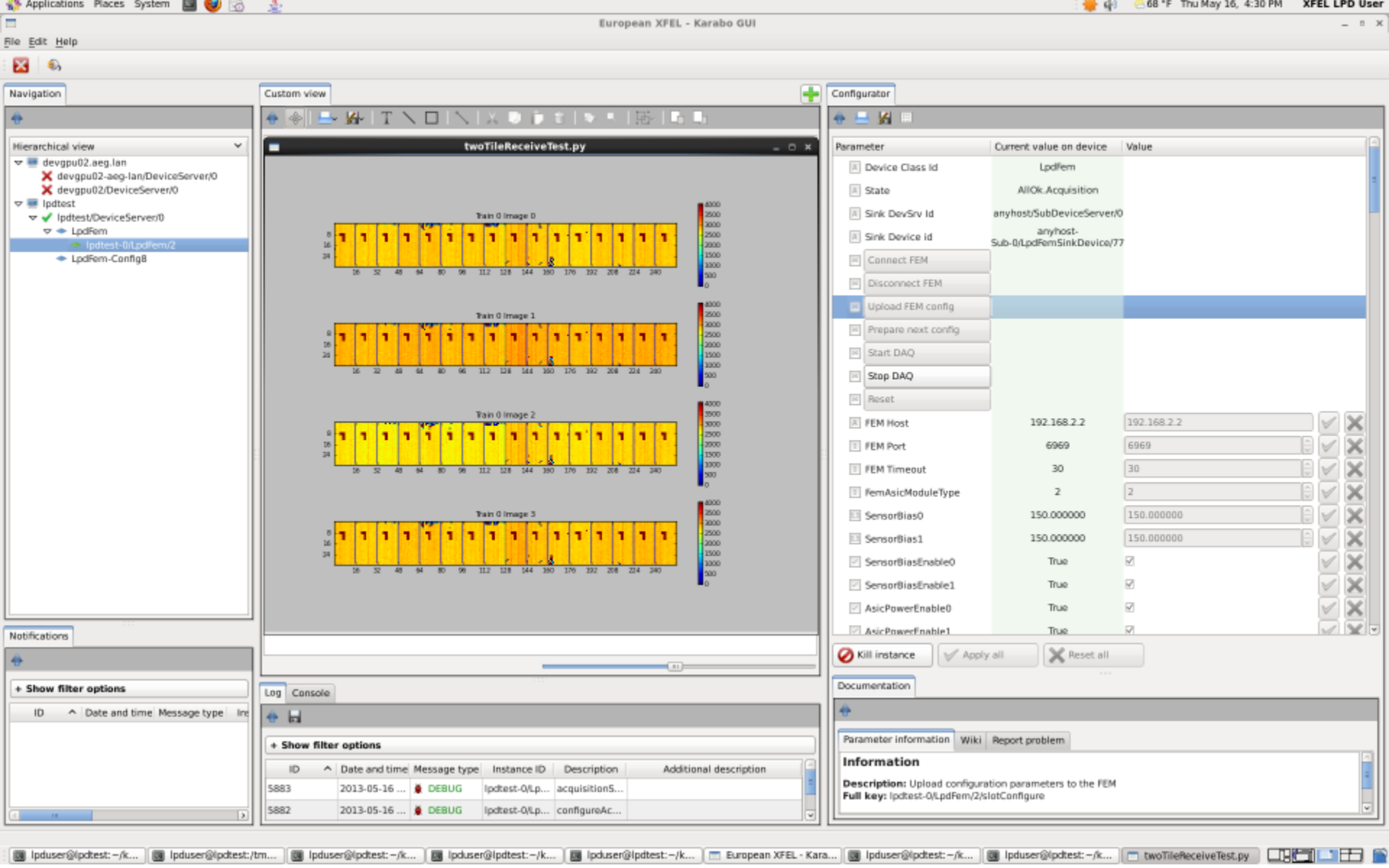

Applications Places System
68 °F Thu May 16, 4:30 PM
XFEL LPD User
European XFEL - Karabo GUI
File Edit Help
Navigation
Custom view
Configurator
Hierarchical view
devgpu02.aeg.lan
devgpu02-aeg-lan/DeviceServer/0
devgpu02/DeviceServer/0
lpdtest
lpdtest/DeviceServer/0
LpdFem
lpdtest-0/LpdFem/2
LpdFem-Config8
twoTileReceiveTest.py
Train 0 Image 0
Train 0 Image 1
Train 0 Image 2
Train 0 Image 3
Parameter
Current value on device
Value
Device Class Id
LpdFem
State
AllOk.Acquisition
Sink DevSrv Id
anyhost/SubDeviceServer/0
Sink Device id
anyhost-Sub-0/LpdFemSinkDevice/77
Connect FEM
Disconnect FEM
Upload FEM config
Prepare next config
Start DAQ
Stop DAQ
Reset
FEM Host
192.168.2.2
FEM Port
6969
FEM Timeout
30
FemAsicModuleType
2
SensorBias0
150.000000
SensorBias1
150.000000
SensorBiasEnable0
True
SensorBiasEnable1
True
AsicPowerEnable0
True
AsicPowerEnable1
True
Kill instance
Apply all
Reset all
Notifications
Show filter options
ID
Date and time
Message type
Log
Console
Show filter options
ID
Date and time
Message type
Instance ID
Description
Additional description
5883
2013-05-16 ...
DEBUG
lpdtest-0/Lp...
acquisitionS...
5882
2013-05-16 ...
DEBUG
lpdtest-0/Lp...
configureAc...
Documentation
Parameter information
Wiki
Report problem
Information
Description: Upload configuration parameters to the FEM
Full key: lpdtest-0/LpdFem/2/slotConfigure
lpduser@lpdtest:~/k...
lpduser@lpdtest:/tm...
European XFEL - Kara...
twoTileReceiveTest.py
Science & Technology Facilities Council

Conclusions/Outlook

- Initial LPD FEM integration with Karabo has gone well:
  - Effective collaboration / communication with WP76 Karabo developers (esp. Sergey Esenov & Burkhard Heisen)
  - Agreed“contract” for API at LpdDevice layer with FSM & parameters defined
  - Stub library allowed early prototyping, device server concept in Karabo is robust
  - Karabo package developer role maturing rapidly, easy to obtain development environment and integrate code

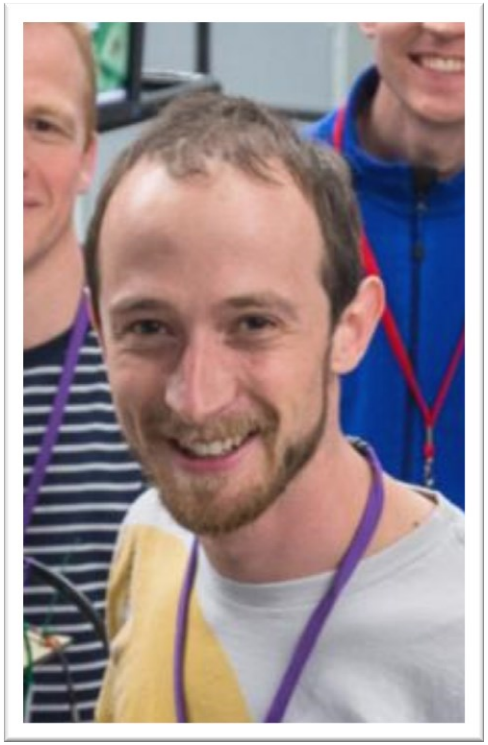
- Future activities:
  - Iteration on FSM, API parameters and expected parameters generation
  - Tracking FEM firmware development for 2-tile, supermodule, quadrant, megapixel
  - LpdFemSink device (C++) to receive data streams without TB/PCL infrastructure
  - Aiming at supporting LPD detectors in 1st official Karabo release on 31.7.13
  - Longer term: handle composite devices (>1 FEM), e.g. quadrant in Q4 2013

WP7 Calibration and Characterisation

WP Leader: Matthew Hart

Team: Stephen Thomas

- Super-Module Testing
- ASIC V2 Testing
- LCLS Beam Time
- PETRA III Beam Time
- Future



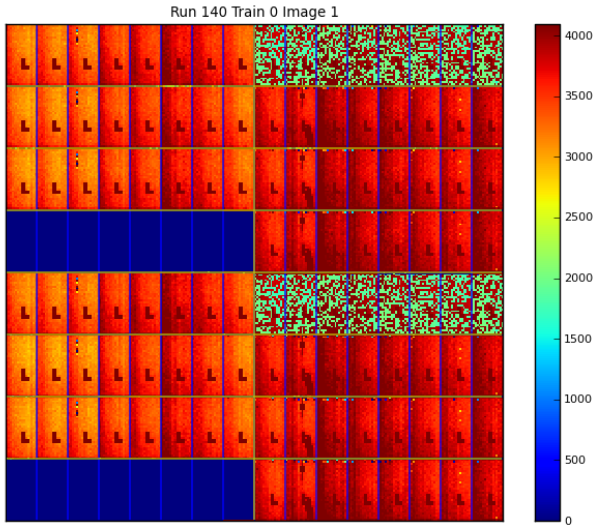
WP 7 – Calibration and Characterisation

Super-Module Testing

- Testing water cooling
- Testing electronics cards working together
- Learning about handling and assembly

Outcomes

- Software and firmware developed to super-module standard
- Heat sink operated for over 360 hours. Other sample heat sink constructions operated continuously for months.
- Problem module locations found and causes identified.
- Power supply noise issue identified

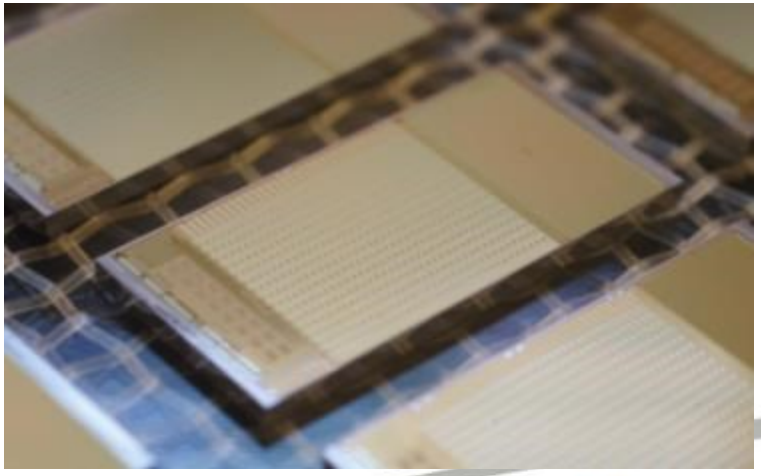


ASIC V2

- First tests confirmed basic function
- Correction to ADC seems ok at full speed
- All other features look OK

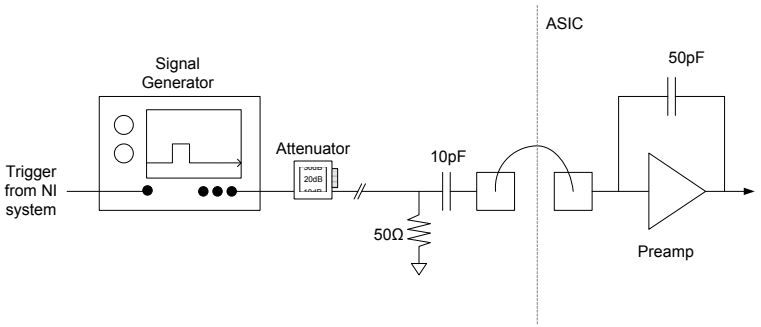
What we have done:

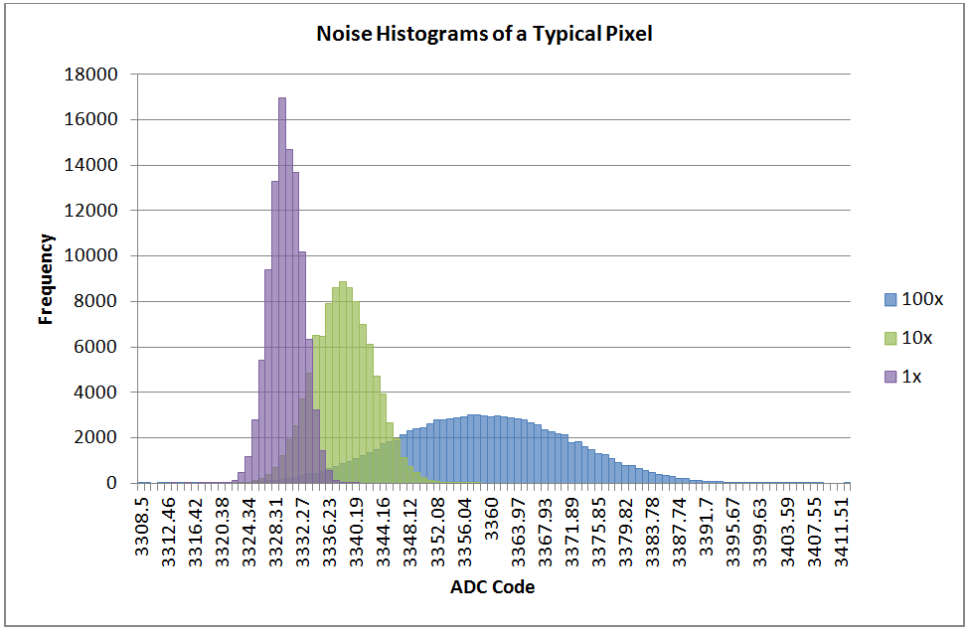
- Half wafer diced for single chip tests – to confirm noise performance and other tests
- 5 wafers of stock
  - One batch of 2 -> 20 ASIC V2 modules ready for beam tests
  - Second batch of 3 -> further stock
  - Now all 5 are probed



ASIC V2 – Single Chip Measurements

- Used simple method with test card and pulse generator
- Confirmed ranges worked as expected
- Measured noise histograms for each range and capacitor combination





Mode	Gain	Noise (stdev) in ADUs	Noise in Photons
50pF	1x	3.49	107.38
	10x	4.65	14.01
	100x	11.52	4.07
5pF	1x	3.559	11.09
	10x	4.659	1.57
	100x	11.47	0.46

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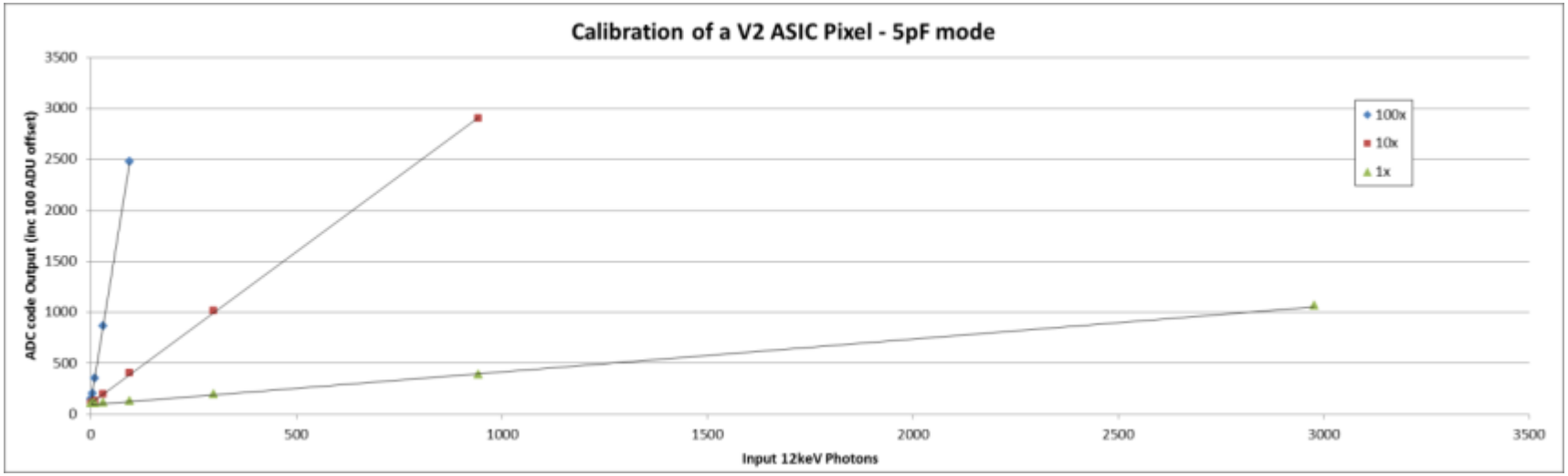
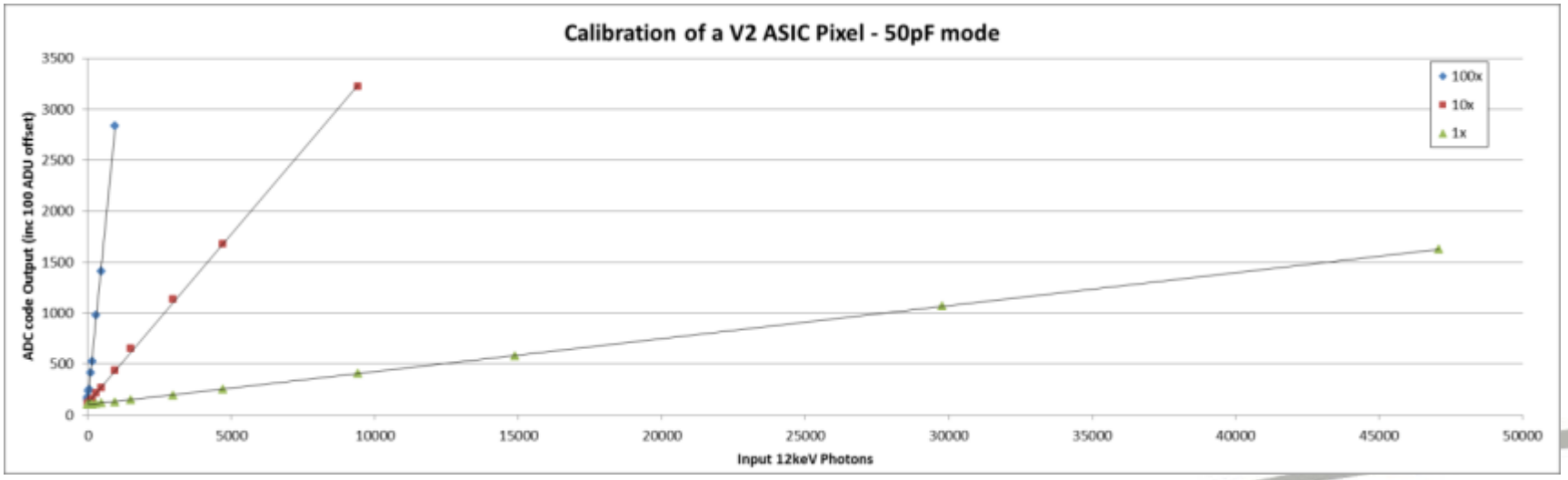
ASIC V2 – Gain Measurements both gain ranges





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ASIC V2 – Noise actual compared with simulated

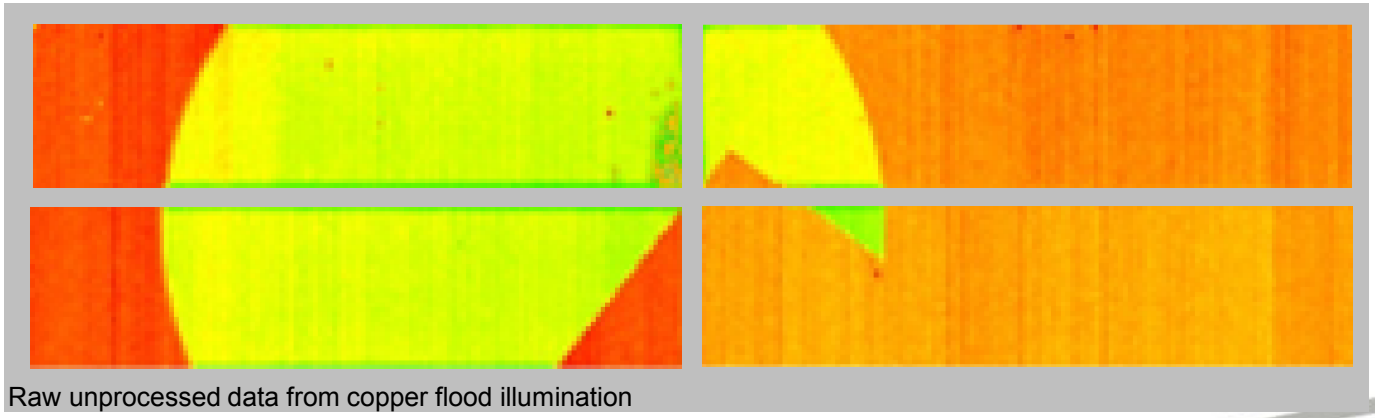
- Current issue with x100 stage, other ranges look close or better than simulated
- Further investigations ongoing to study correlations in time etc.
- Issue thought to be related to reset switching so looking at timing and the control of reset edges

		Noise (σ) in photons (12keV)		
		ASIC V1 measured	ASIC V2 Simulation	ASIC V2 measured
50pF	1	133	100	107.4
	10	30	20	14.01
	100	7.7	1.9	4.07
5pF (10pF for V1)	1	53	10	11.09
	10	6.9	4	1.57
	100	1.9	0.3	0.46

Beam Test at LCLS

First Test: Flood florescence

- Test uniformity of detector. Copper foil, with machine at 9keV gives 8keV uniform florescence across detector.
- Shots gave between 0-1000 photons per pixel – Allows basic gain/linearity measurements.



Raw unprocessed data from copper flood illumination

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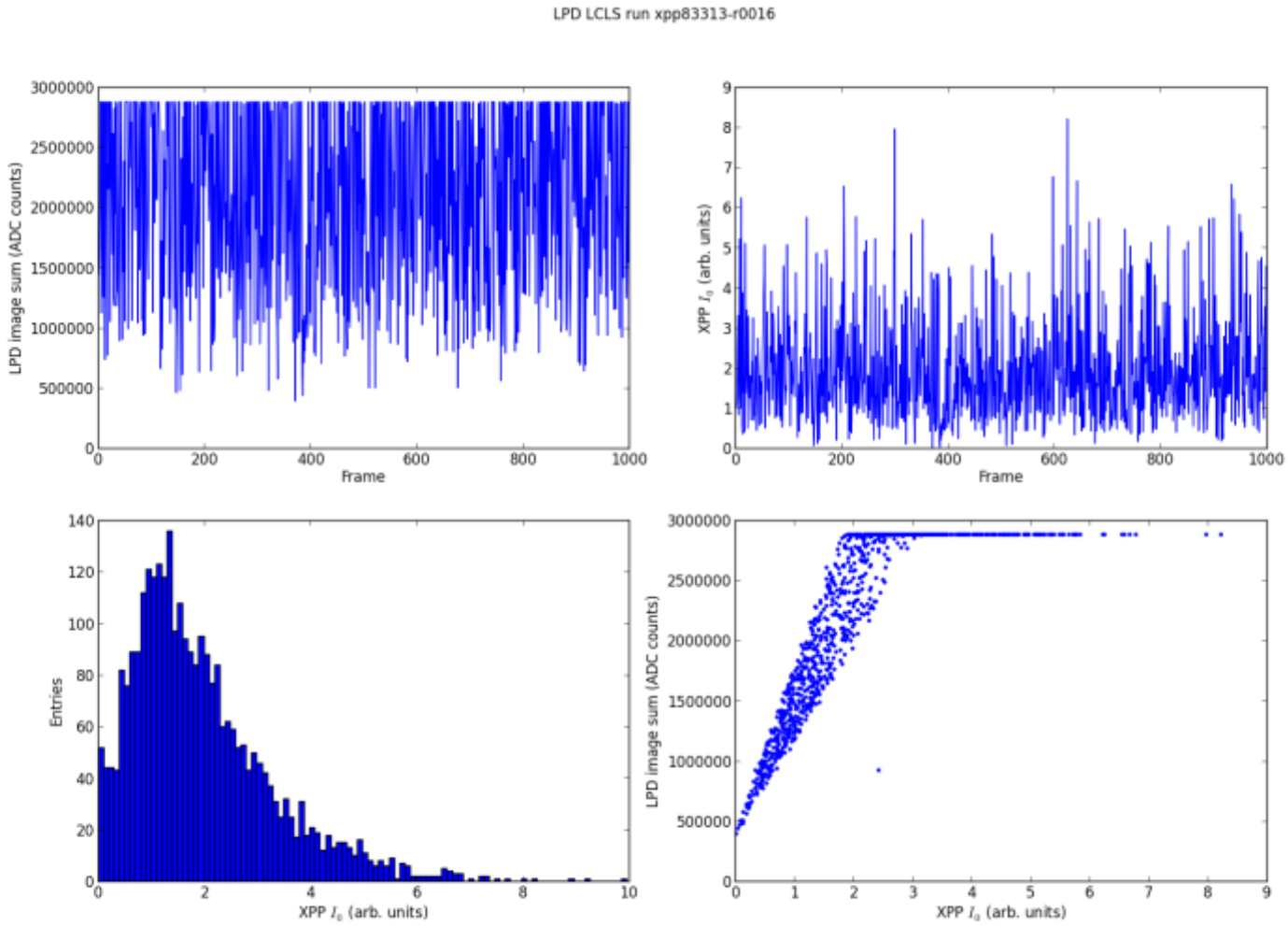
Beam Test at LCLS

Flood florescence

- Observations: Detector Bias

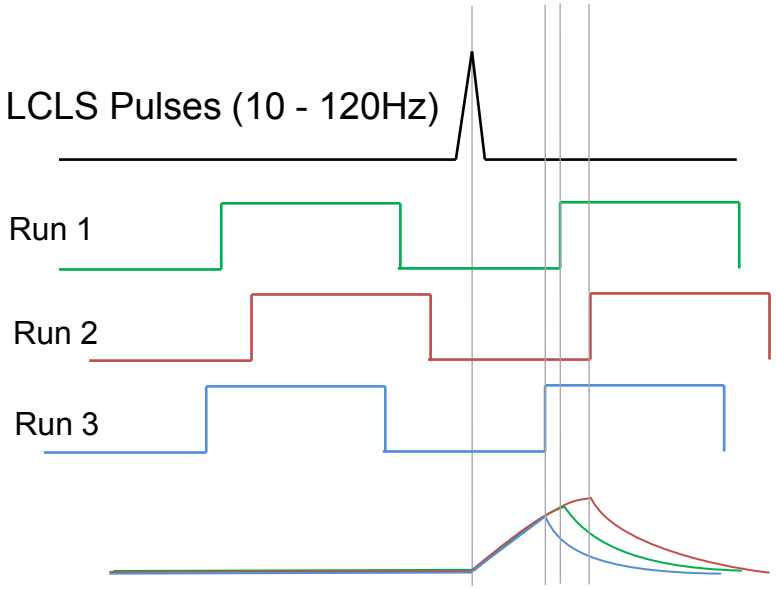
Beam Test at LCLS

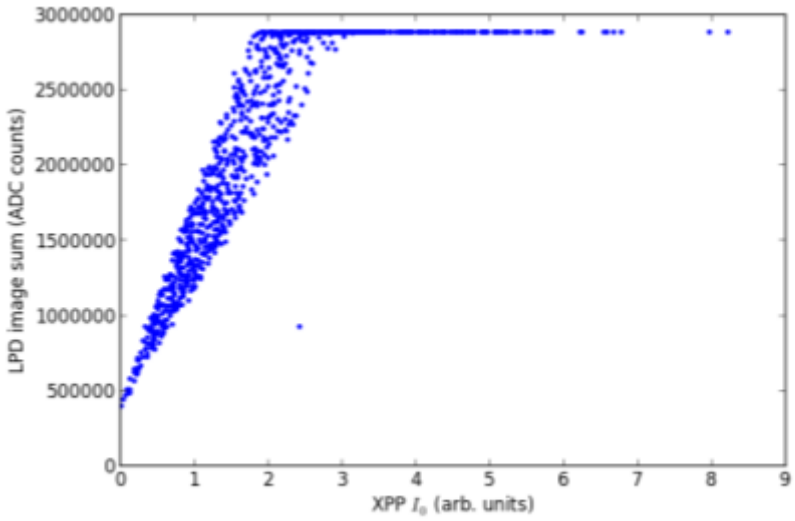
Florescence measurements against i0 record



Beam Test at LCLS

- Dispersion in gain – Synchronisation Jitter.



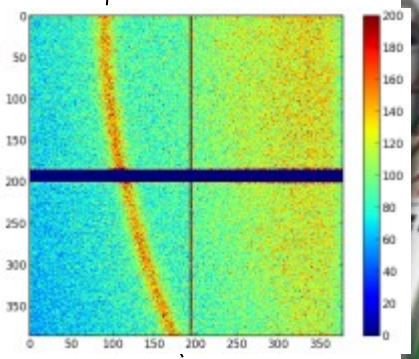


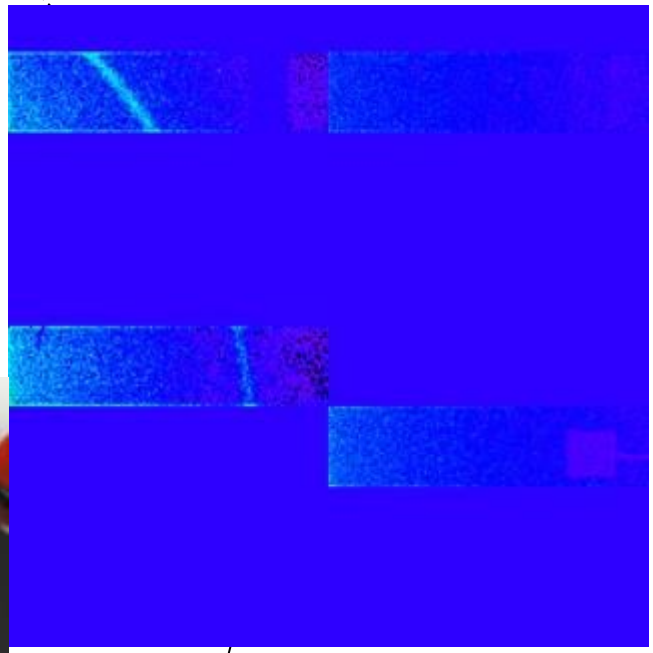
- The ASIC Pixel Clock 4.5MHz is driven by asynchronous 100MHz Clock
- 10ns run to run jitter + 8ns LCLS trigger jitter
- Conservative alignment of LCLS pulse within the integration window.

Beam Test at LCLS

Scattered Patterns

- Sample of Titanium oxide between layers of kapton created diffraction rings captured by LPD and CSPad side by side





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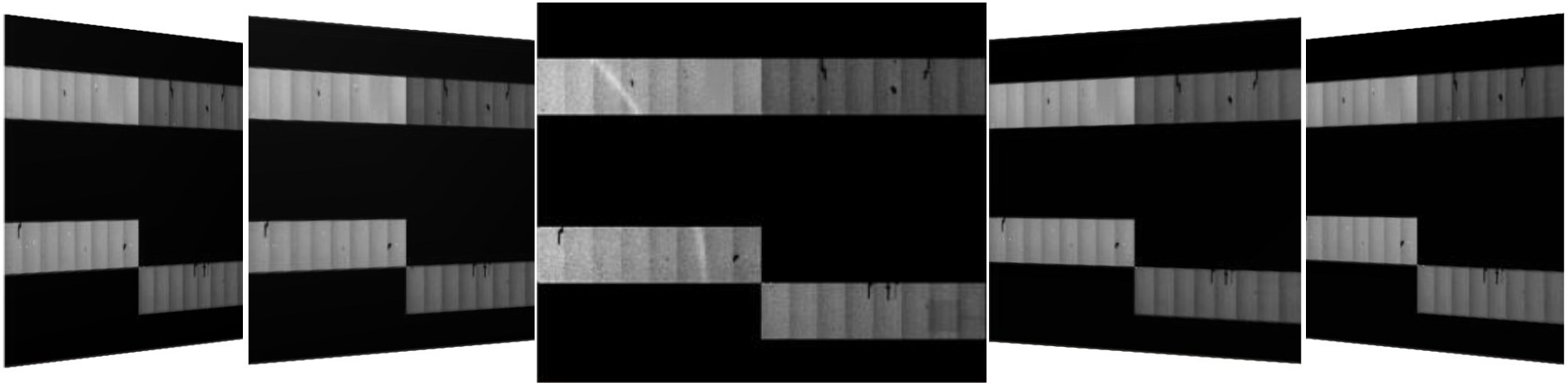
Beam Test at LCLS



Titanium Oxide powder ring (medium shot)

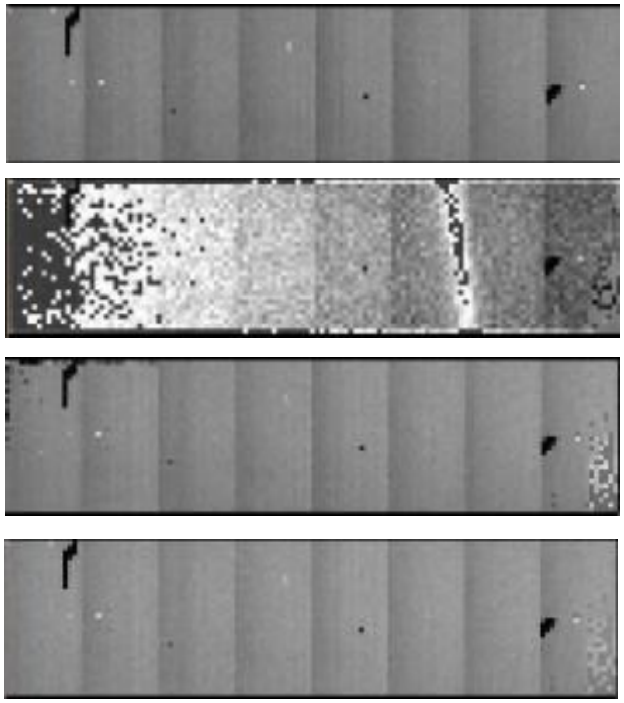
- System running at **4.5MHz** capturing trains of 10 images
- Image taken in **5pF** mode with **100x gain**

Beam Test at LCLS

Titanium Oxide powder ring (bright shot)

- Image taken in **5pF** mode with **auto gain** selection
- Some persistence of the ring seen in the following image
- Optimisation of saturation recover settings required (LCLS Test 2?)

Beam Test at LCLS



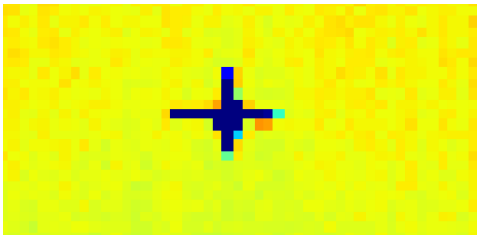
Unconnected Pixels

- Signal in unconnected pixels appears as a brighter response in adjacent pixels
- Since unconnected pixels are not be biased up correctly signal present in these pixel takes much longer to arrive in the neighbouring pixels.

Beam Test at LCLS

Direct beam

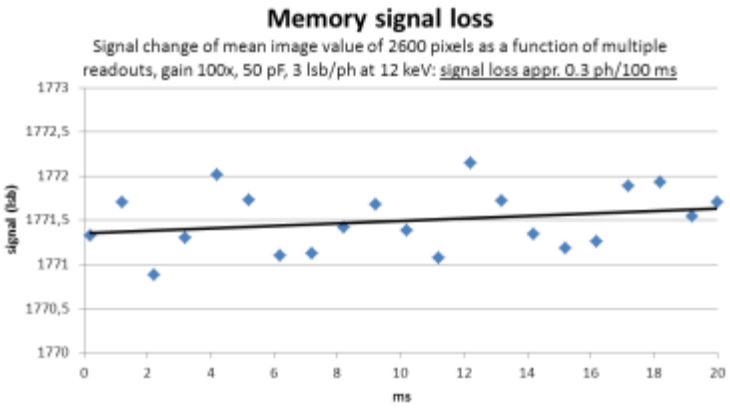
- Operating the full dynamic range of the ASIC. We had access to add some filters in the beam to reduce the intensity. Direct beam in mono is around $10^{10\text{-}11}$ photons. With some slits this was expected to be reduced to around 10^{8}
- The image below shows an example of direct LCLS beam hitting the sensor. The beam was confined to 100um in size
- The ‘cross’ shape is thought to be caused by coherent diffraction of the beamline slits

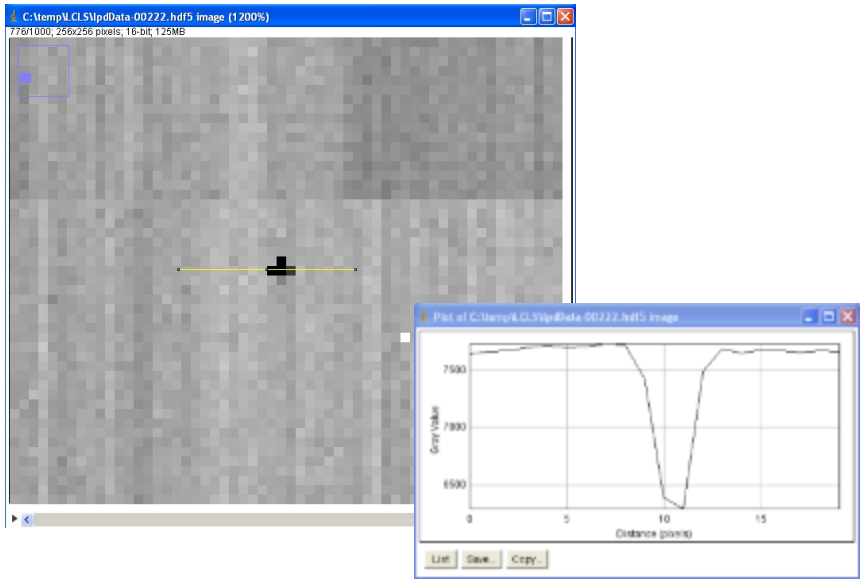


Zoom of spot detail showing diffraction ‘cross’ and some scatter

1st Preliminary results from the LCLS data

- Signal loss (memory droop) ~0.3 ph/100 ms (12 keV)
  - Consistent with V1 ASIC
- Crosstalk measured at ~10x saturation for a single pixel.
  - No crosstalk visible at saturation





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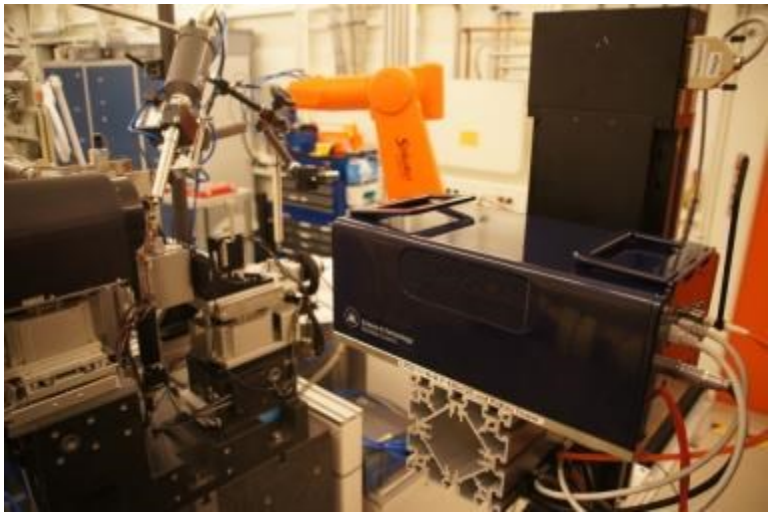
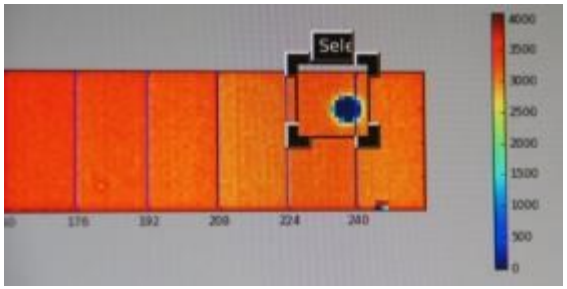
Test program PETRA

All tests at 12 keV, defocused beam appr. 2x3 mm^2.

- Readout noise (with improved power supply, external).
- Test special modes, e.g. 3 gain readout, long integration times.
- Radiation hardness, using direct beam.
- Temporal crosstalk, a ms shutter was used.
- Linearity. Over all 3 gain settings.
- Spatial resolution. Scan with pencil beam, using a 100 mm pin-hole.
- Sample tests $Fe(CN)_6$ (hexacyanoferrate) solution in water, 12 keV





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Test program PETRA

Readout noise:

- 0.6 ph rms 12 keV, for the whole system but with an external power supply
- This is an improvement of a factor of 3x c.f. Asic V1

Radiation hardness:

- On pixel level 50 MGy with slight impact but no pixel failures
- This is an improvement of 100x The memory cells are now shielded with Ta foils, no visible effect

		Noise (σ) in photons (12keV)		
		ASIC V1 measured	ASIC V2 Simulation	ASIC V2 measured
50pF	1	133	100	107.4
	10	30	20	14.01
	100	7.7	1.9	4.07
5pF (10pF for V1)	1	53	10	11.09
	10	6.9	4	1.57
	100	1.9	0.3	0.46

Table 3: V1 and V2 ASIC noise comparison

WP 7 – Calibration and Characterisation

Next 6 months

- Analysis of data from beam tests
- Calibration Software
- Continuation of ASIC V2 Tests

Critical Issues

- Understanding issues with detector response.

WP 8 – System Build

WP8 System Build

WP Leader: Viraj Perera

Team: Paul Booker, Paul Adkin and Ivan Church

- ASIC V2 Wafer Probing and dicing
- Assembly Production Line
- Radiation Hard Tiles
- QA procedures
- Automated Testing

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ASIC V2 – Wafer Testing

• For building V2 modules known good die are required to deliver the required assembly yield

• First version of test programme used on 5 wafers

•Programmed tests:

All Channels respond

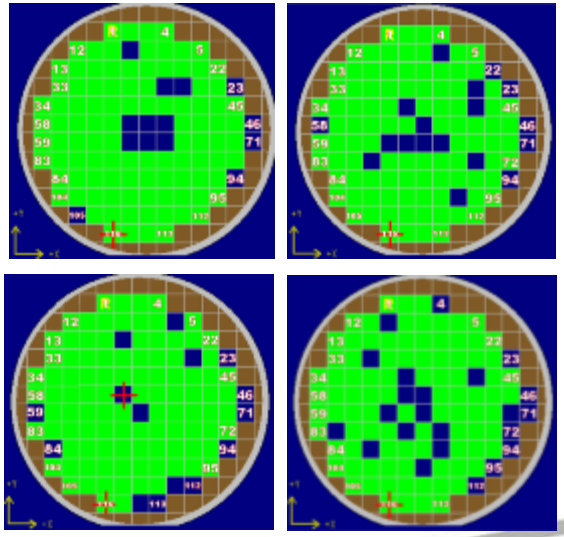
Pedestals within reasonable range

Power consumption is as expected

Write and read to all registers

• Results:

Currently getting ~80% chip yield



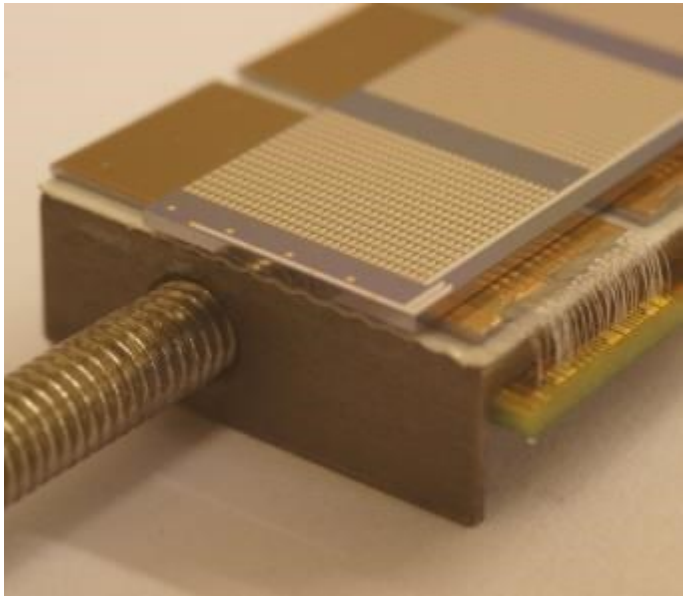
Example wafer maps

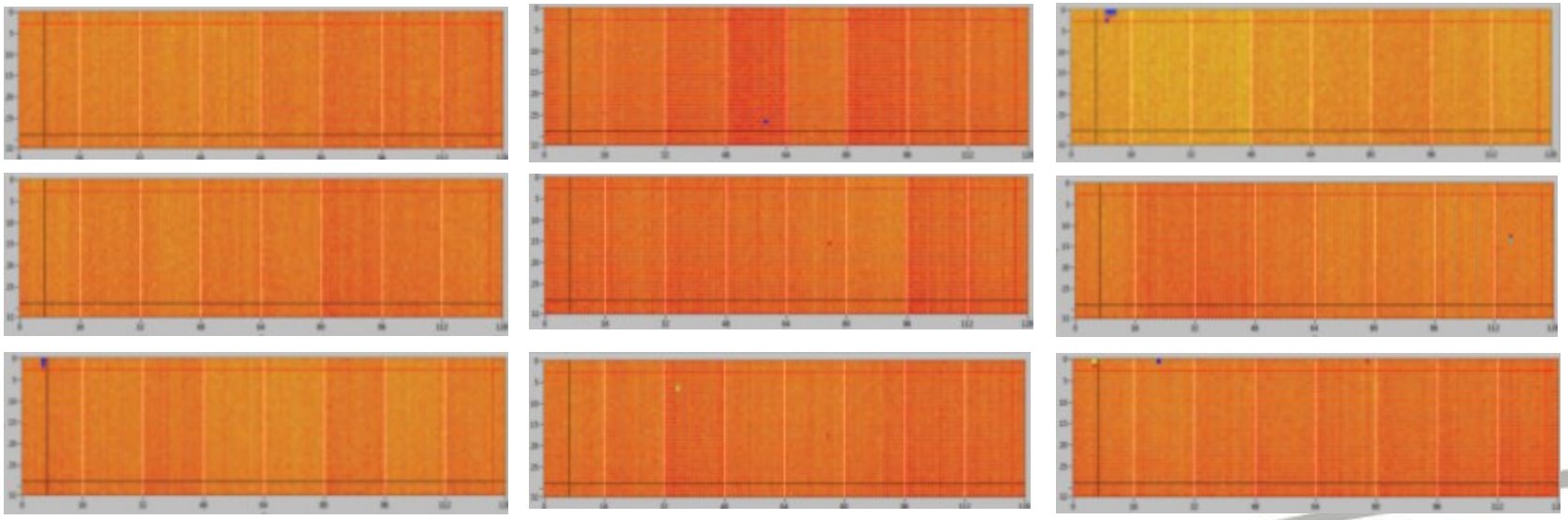
WP 8 : Assembly Production Line

- LPD Modules are now produced in larger batches.
- A trial batch of ~16 V1 Modules was manufactured over Christmas – New year to develop and optimise the process
- Speed and Quality are greatly improved

WP 8 : V2 Modules

- 14 V2 LPD Modules were manufactured ready for beam tests in May
- All chips on all modules work – Wire bonding process is perfect.
- High quality bump bonding and screen printing at the ASIC interposer boundary.





Note: Images taken prior to sensor bonding (as in top right picture)

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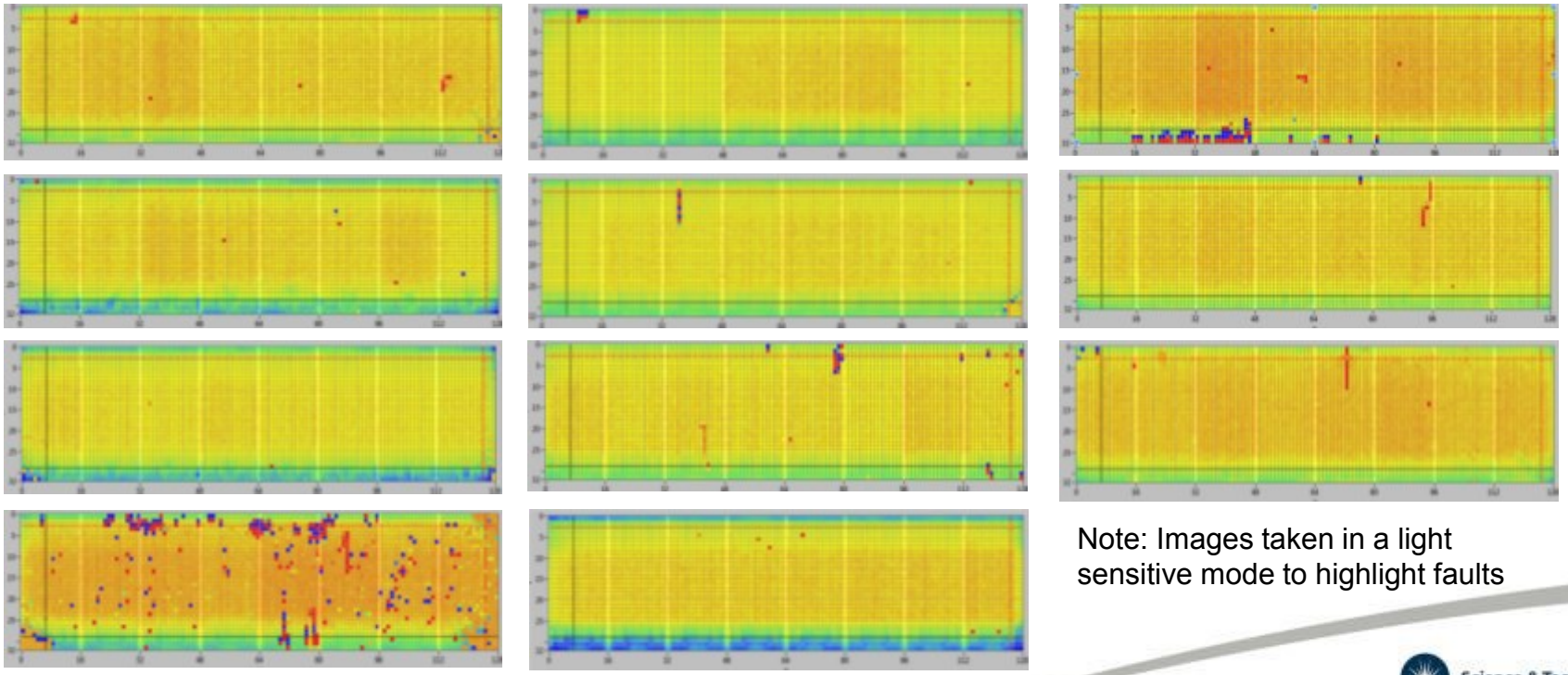
WP 8 : V2 Modules

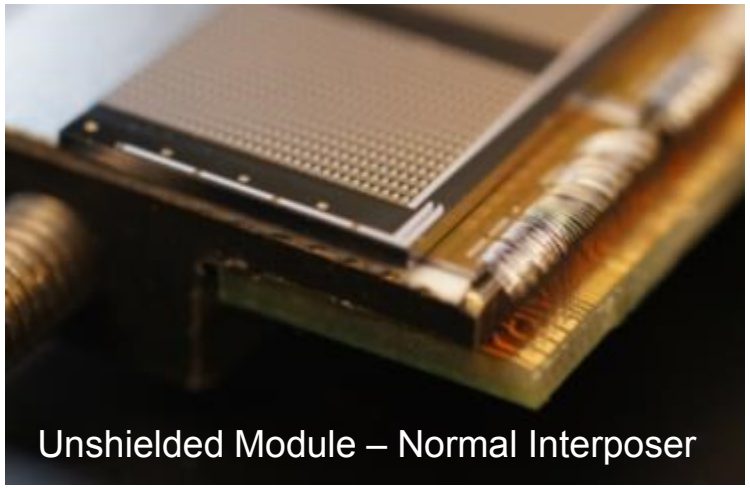
- The most significant bonding issue is with the final Interposer to sensor bump bonding step.
- Following this step we see increased numbers of shorts and opens.
- Associated with poor quality finish on the molybdenum support blocks and issues with the jig on the flip chip bonder



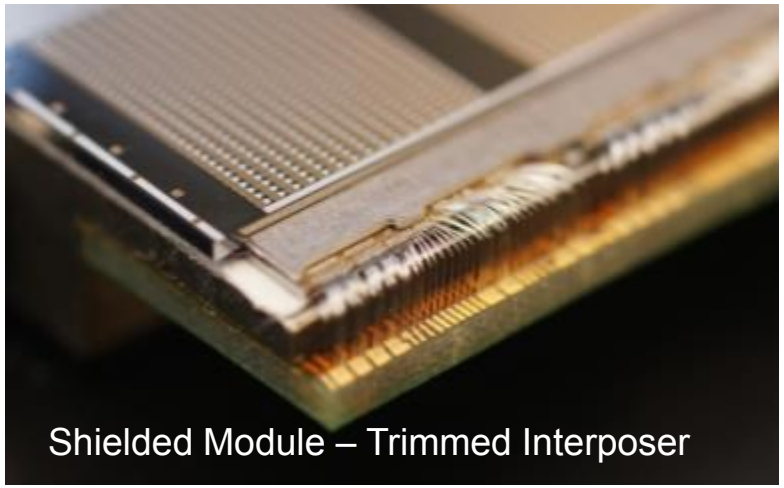
Note: Images taken in a light sensitive mode to highlight faults

WP 8 : Rad Hard V2 Modules

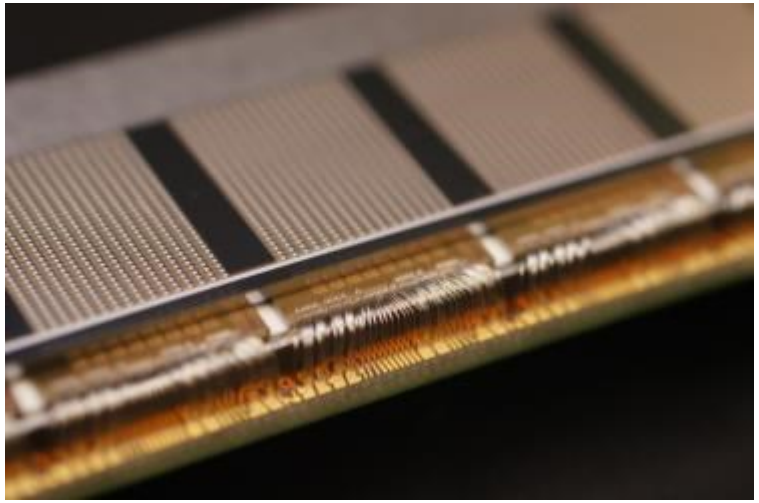
- 6 V2 Modules have been constructed with full rad-hard Tungsten shielding
- These were tested at LCLS and PETRA



Unshielded Module – Normal Interposer

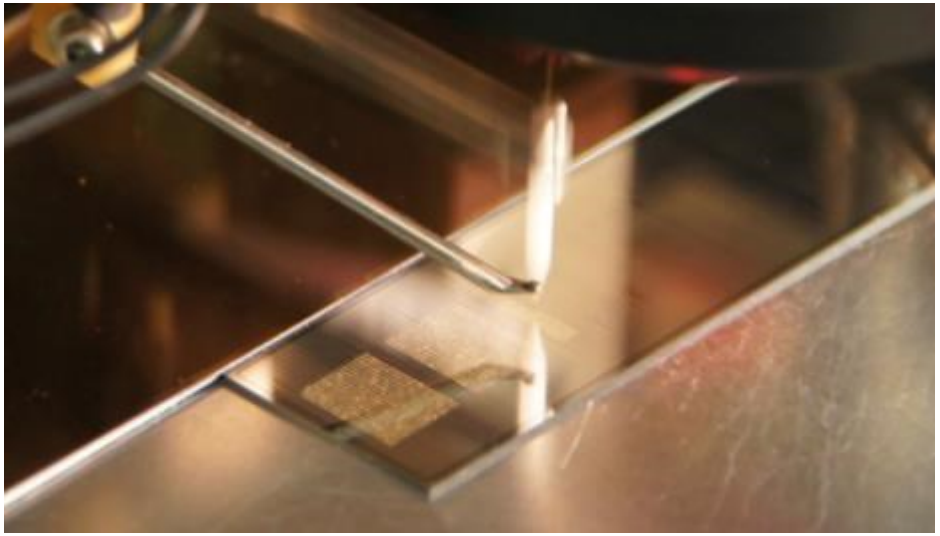


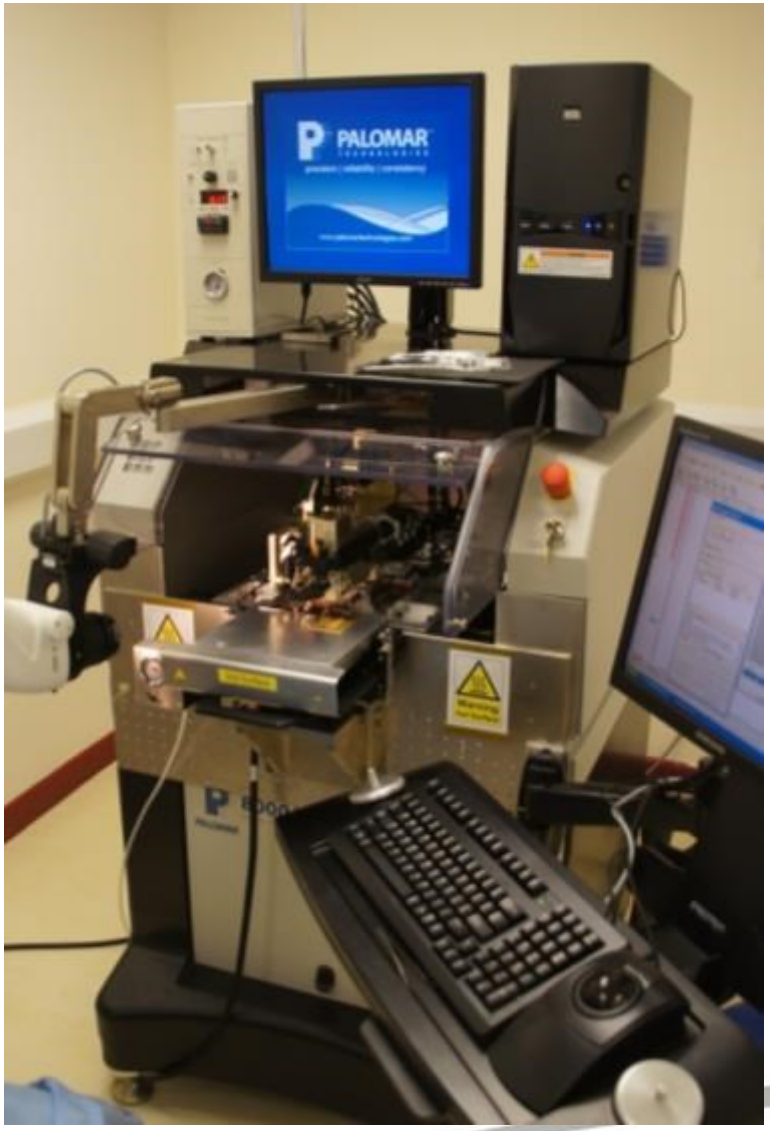
Shielded Module – Trimmed Interposer



WP 8 – System Build

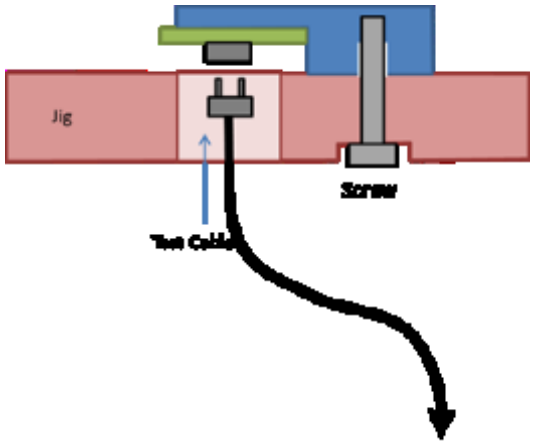
- STFC recent investment in assembly processing:
  - Palomar 8000 bonding machine
  - Increased ball deposition rate by >10x

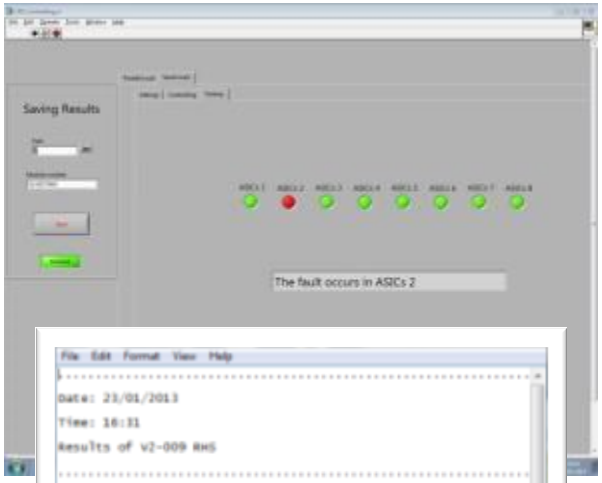


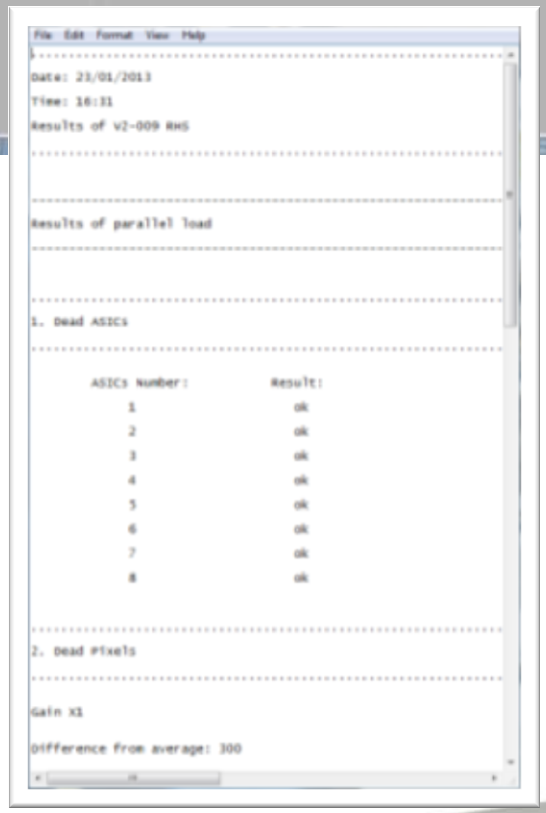


WP 8 – System Build

- Automated Testing on the bonding production line.







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WP 8 – System Build

QA and Production

- All projects in the Detector and Electronics Division are managed within a system that meets ISO9001:2008 and certified by BSI
- EU tendered Framework agreement to manufacture and assemble PCBs
- Production takes place in Cleanroom
- ESD measures and control
- Stock Management
- Goods-in inspection
- Route Card
  - Serial numbers
  - Product traceability, etc.

Production Steps

XFEL LPD detector Module Production

Science & Technology Facilities Council

WP 8 – System Build

Next Steps

- Ordering components (384 Modules) – some in stock
- Investigate issues with Moly block and screen printing.
- Run another batch of 20 modules following any changes
- Agree with XFEL to go ahead with full production.

Milestones

Work Package		Ref	Milestone	Date
Mechanics	WP3	M3.1	2-tile system mechanics assembled	Dec-12
		M3.2	Quadrant system mechanical revisions complete	Dec-12
		M3.3	1 Mpix Prototype Trials Complete	Jun-13
		M3.4	1 Mpix system mechanical revisions complete	Jan-14
Electronics	WP4	M4.1	Detector tile connector card V3 manufactured	Jan-13
		M4.2	1/4 Mpix Interface Board manufactured	Feb-13
		M4.3	1 Mpix Interface board manufactured	Jun-13
		M4.4	Mpix qty. of all boards manufactured (Power, Backplane, FEM, connector etc.)	Jun-13
		M4.5	Spare quantities of all boards manufactured	Jul-13

Milestones

Work Package		Ref	Milestone	Date
DAQ	WP5	M5.2	Essential Firmware Features	Dec-12
		M5.3	Firmware compatible with Super-Modules	Feb-13
		M5.4	Firmware enabled with basic beam line features	Apr-13
		M5.5	Firmware enabled with Advanced Beam line features	Jul-14
		M5.6	Final Firmware Complete	Oct-14
Software, Controls and Integration	WP6	M6.1	Software ready for use with FEMs on bench	Nov-12
		M6.2	Software ready for use with the 2-tile	Nov-12
		M6.3	Software ready for use with the Super Module Tests	Jan-13
		M6.4	Software ready for use with the Quadrant	Apr-13
		M6.5	Software ready for use with the Mpix	Dec-13

Milestones

Work Package		Ref	Milestone	Date
Calibration and Characterization	WP7	M7.1	Super Module operational with V1 ASIC	Jan-13
		M7.2	ASIC V2 Qualification Complete	Mar-13
		M7.3	Detailed qualification of 2-Tile detector with ASIC V2 under X-rays finished	Apr-13
		M7.4	Qualification of ¼ MPix under X-rays finished (ASIC V2)	Oct-13
		M7.5	Calibration software development complete	Aug-13
		M7.6	End-to-End Test (full 1 MPix detector working)	Oct-14
		M7.7	Initial commissioning at exp. station finalized, inc. calib. and characterisation.	Sep-15
System Build	WP8	M8.1	Modules Manufactured for Super Module tests	Nov-12
		M8.2	Wafer Probing Complete and wafers diced	Jan-13
		M8.3	Radiation Shields manufactured and interposers trimmed for Rad hard Tiles	Jan-13
		M8.4	Assembly of production detector tiles starts	Mar-13
		M8.5	Assembly of production detector tiles Finishes (Inc. spares)	Jan-15

Issues for Discussion:

- Support of beam tests – maintaining PETRA compatible firmware.
- Smaller LPD systems – Single-super module or 2-tile system.
- Ordering of more ASIC V2 wafers.
- Interposers – now available with improved via yield, upgrade option.

Summary:

- Key points – to be completed