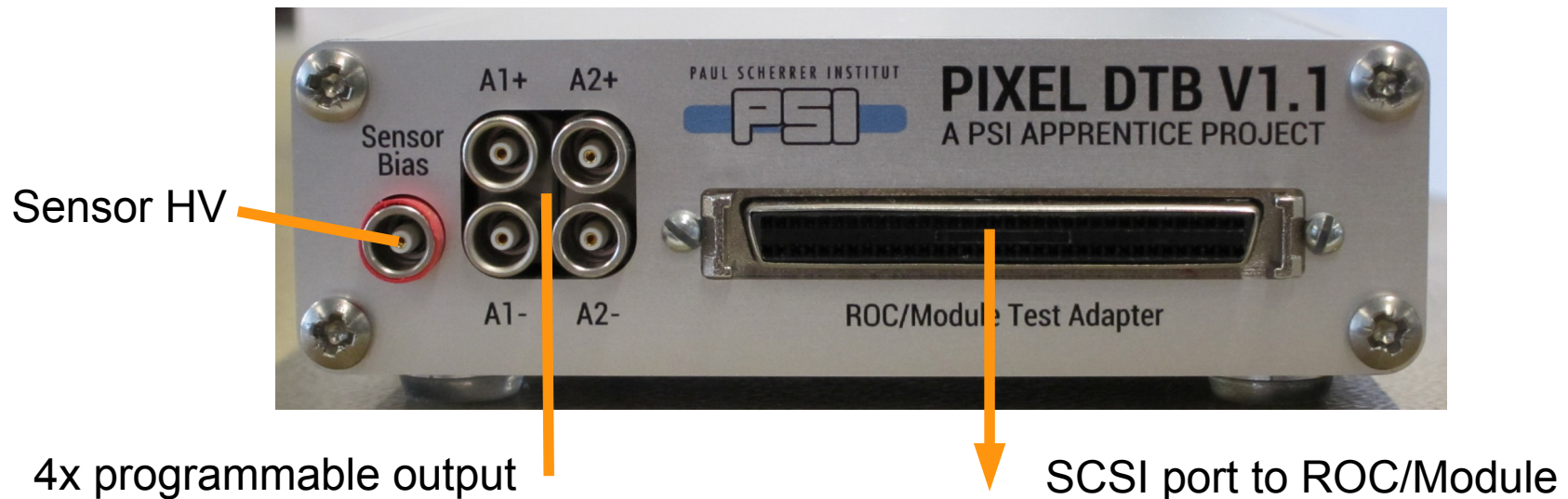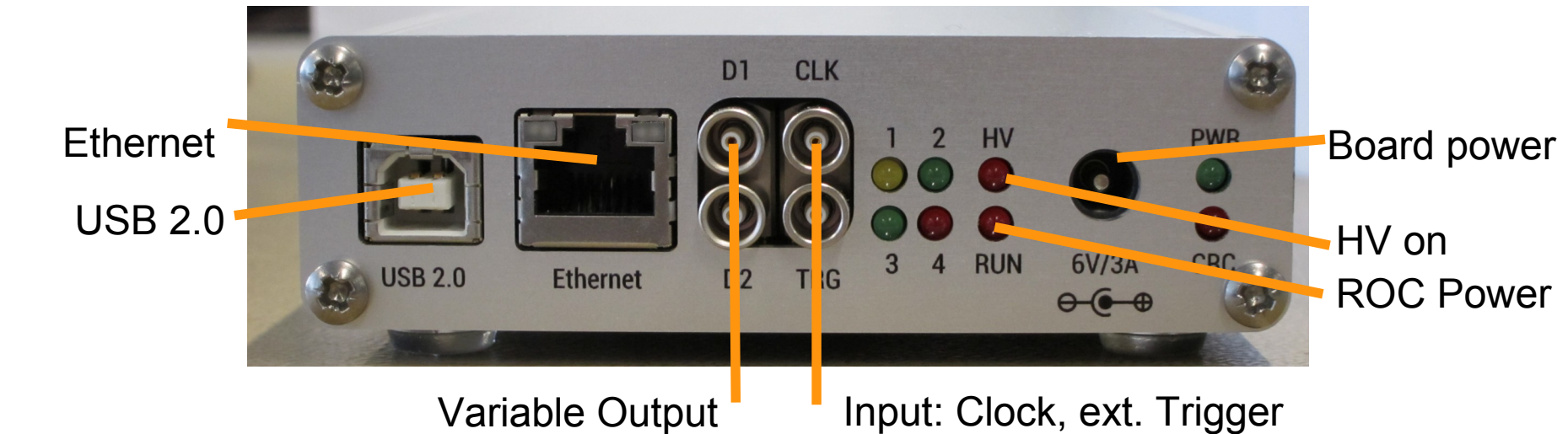# THE BRAND NEW
PSI DIGITAL TEST BOARD (DTB)

Simon Spannagel
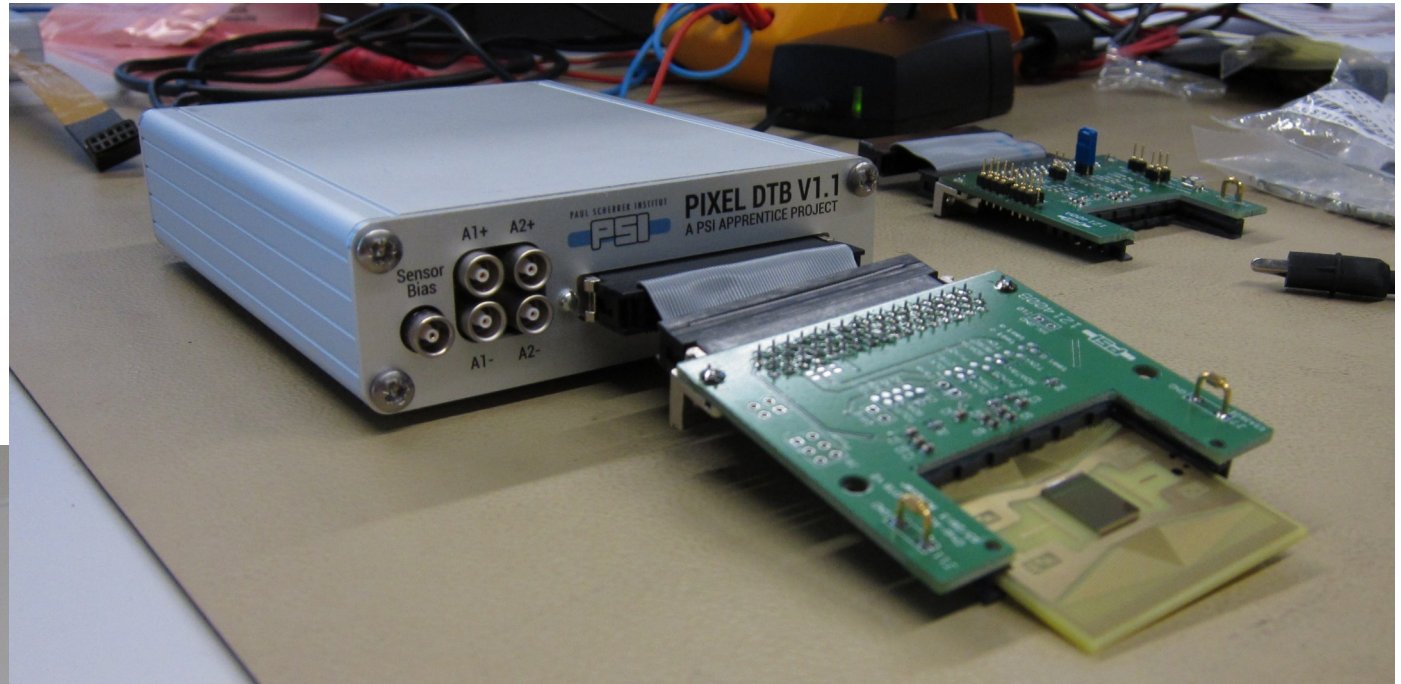Weekly Phase I
19/04/2013

New Digital Testboard

> 8 pre-series production boards arrived last week at PSI

> Another 170 on hold for final production

- Will start in about 2-3 weeks, after design approval

> Boards currently run with adapted analog firmware

> New digital firmware in preparation (Beat)

- Takes another two to three weeks to finish probably

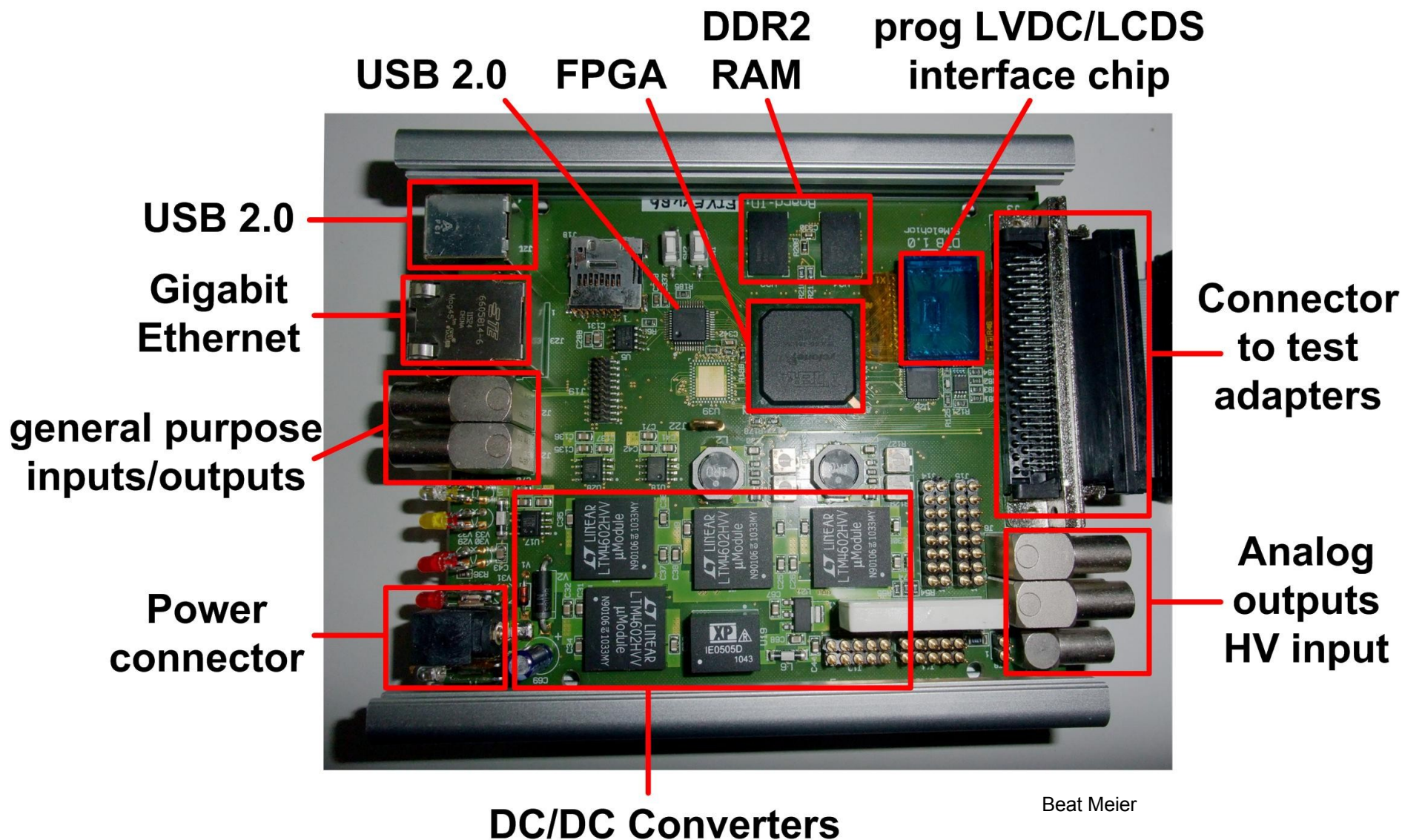> Already one at DESY for first tests and firmware development

Hardware

Ethernet

USB 2.0

Variable Output

Input: Clock, ext. Trigger

Board power

HV on

ROC Power

Sensor HV

4x programmable output

SCSI port to ROC/Module

USB 2.0   FPGA   DDR2 RAM   prog LVDC/LCDS interface chip

USB 2.0

Gigabit Ethernet

general purpose inputs/outputs

Power connector

DC/DC Converters

Connector to test adapters

Analog outputs HV input

Beat Meier

Features

> SCSI: has more pins, allows for separation of signal lines with ground for defined impedance

  ▪ Allows long cables, e.g. for mounting in X-Ray tube

> DDR2 RAM now 128 MB

> USB2.0: faster data readout, future features like direct readout during run, single event readout, …

> Ethernet: currently not supported yet, Nebraska working on implementation for TCP/IP connection for readout

> More General IO pins on the board, usable for things like TLU handshake e.g.

> Crosspoint Switch allows easy monitoring of signals (see next slides)

DESY

# New Firmware Schematics

Beat Meier
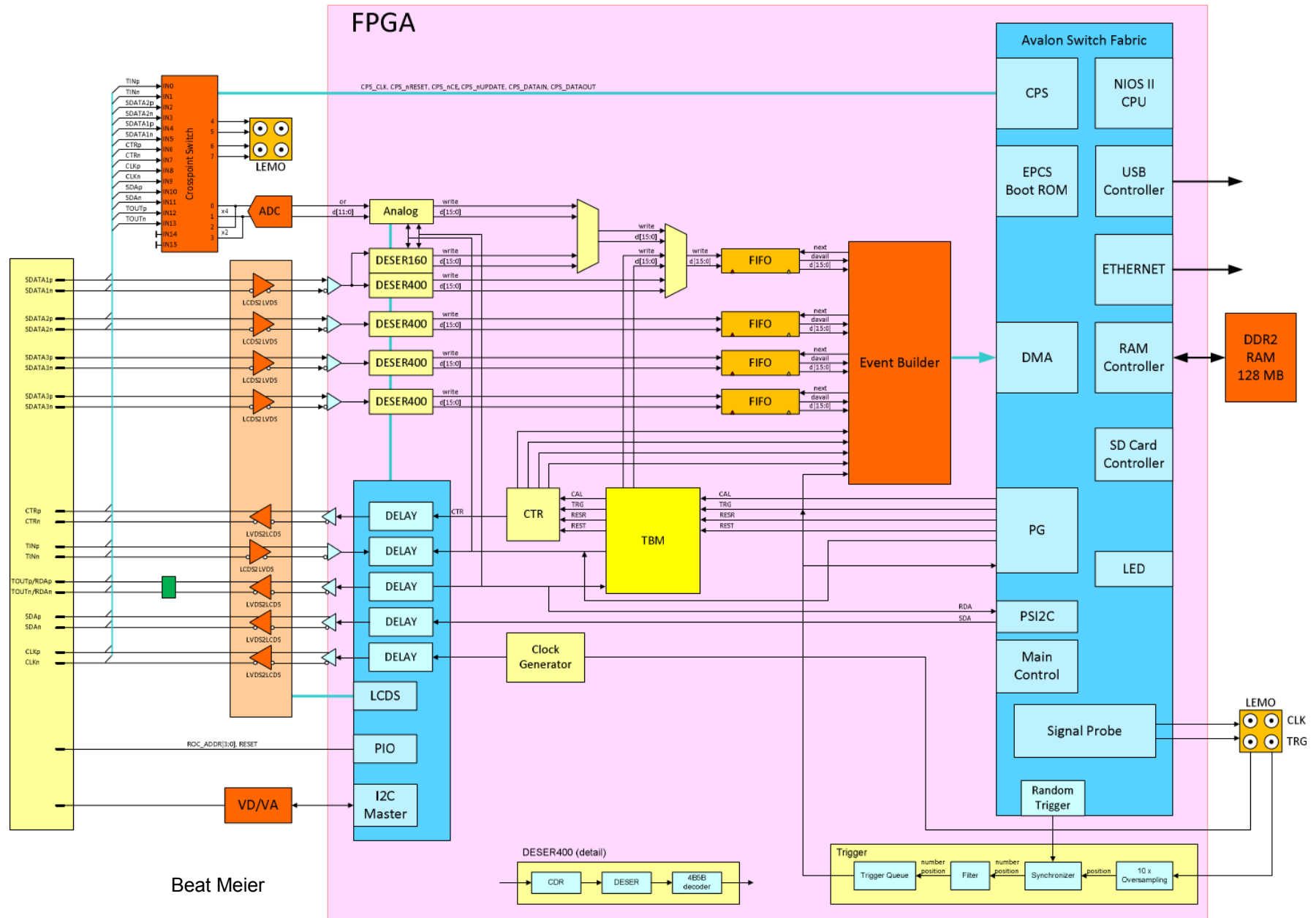
New Firmware Features

> More in microcontroller

- Allows e.g. more accurate delay settings for tin/clk/ctr

> ADC for both analog data digitizing and crosspoint switch feeding

- Allows digital readback of analog output ("digital scope")

> Crosspoint switch can map signals from in/outputs to LEMO connectors, changeable via software commands, no dip switch needed

- sdata, tokens, clock, …
- Similar to the scope connection points on the old testboard, but not affecting the signal by using the crosspoint switch with buffer

> Deserializer for 160 and 400 MHz for single ROC and TBM readout

> Two front LEMO connectors as internal FPGA signal probes, adjustable

"Readback"

> Uses additional bits in the digital ROC data format to provide slow control
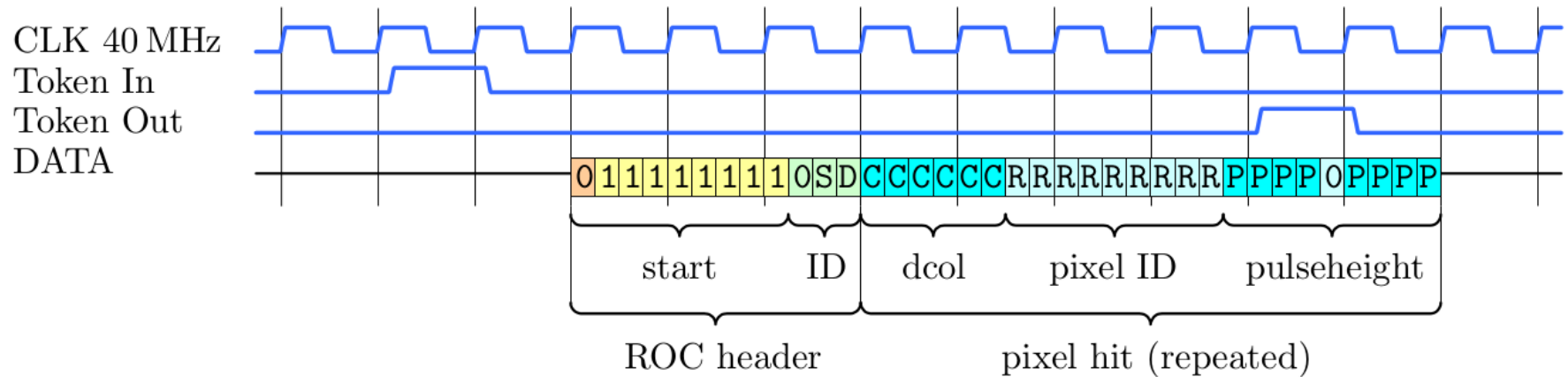
> "S" sends start bit

> In the following 16 readouts the "D" bit contains 1bit each from a 16bit word

> The content of that word can be programmed using DAC 255, can be e.g. unregulated voltages on the ROC, the lastDAC, ...

Summary

> Let there be testboard.