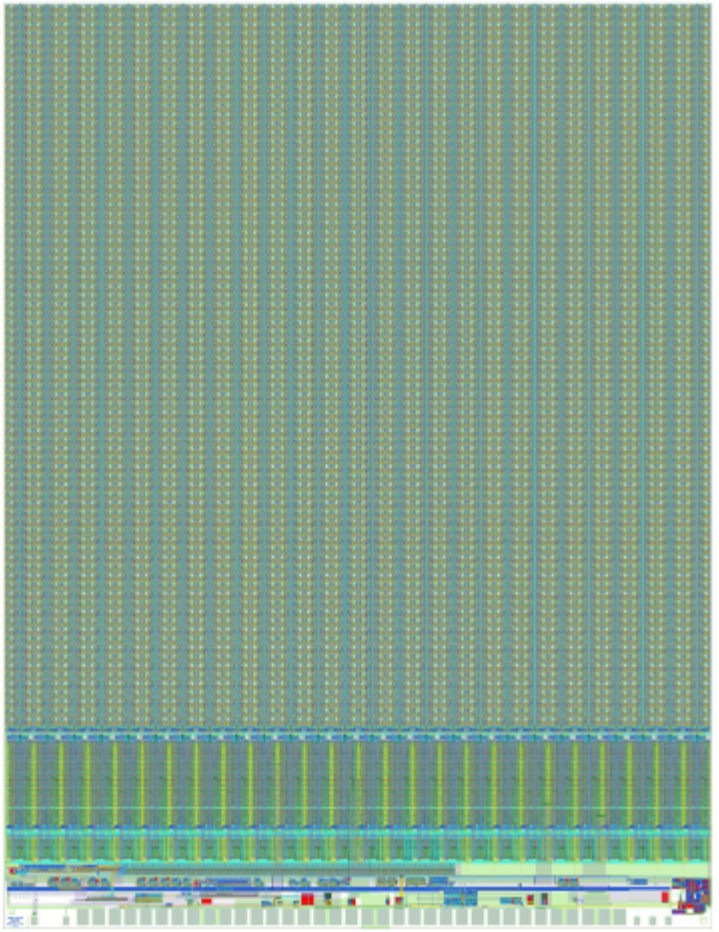
psi46digV2 ROC Tests

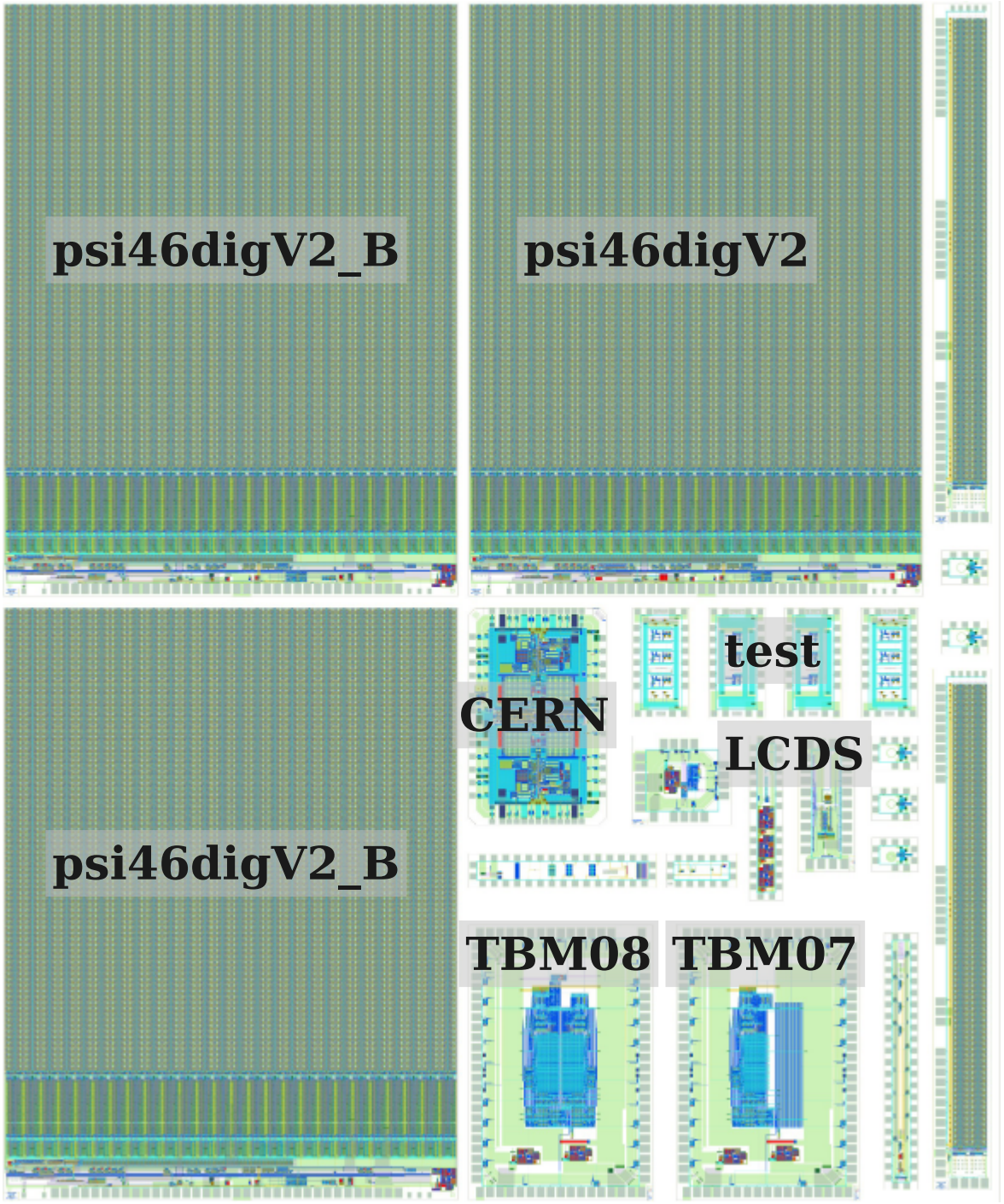
Daniel Pitzl

HH CMS pixel upgrade meeting, 19.4.2013



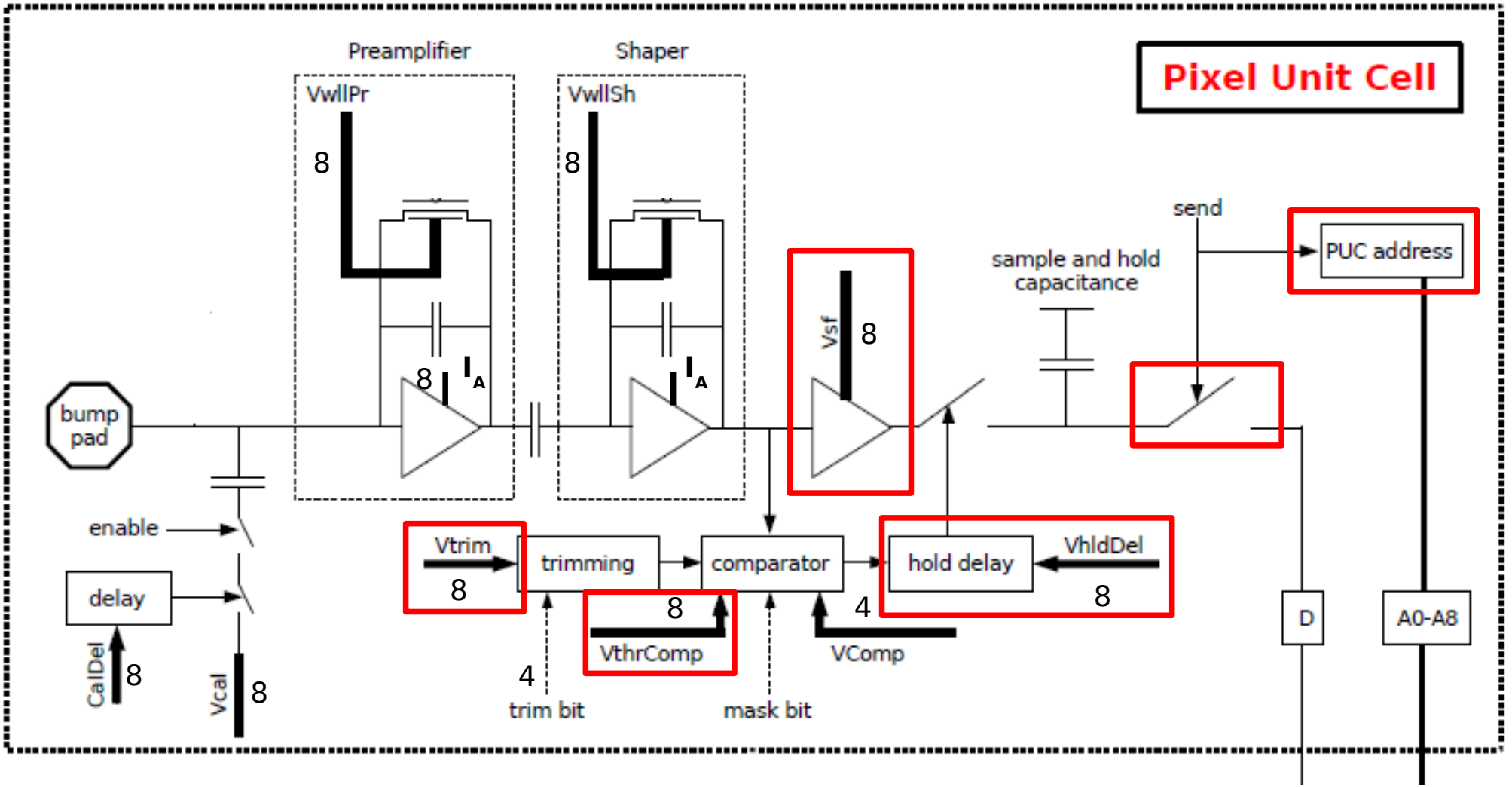
- psi46digV2
- lab tests:
  - power
  - timing
  - threshold
  - noise
  - gain

2013A IBM ROC submission



- 0.25 um IBM CMOS
- 62 recticles per wafer
  - 180 ROCs per wafer
- submission Feb 2013
- received early April 2013
- 6 wafers:
  - one diced
  - three get UBM for In bumps
- 24 more wafers will follow soon

psi46dig pixel unit cell

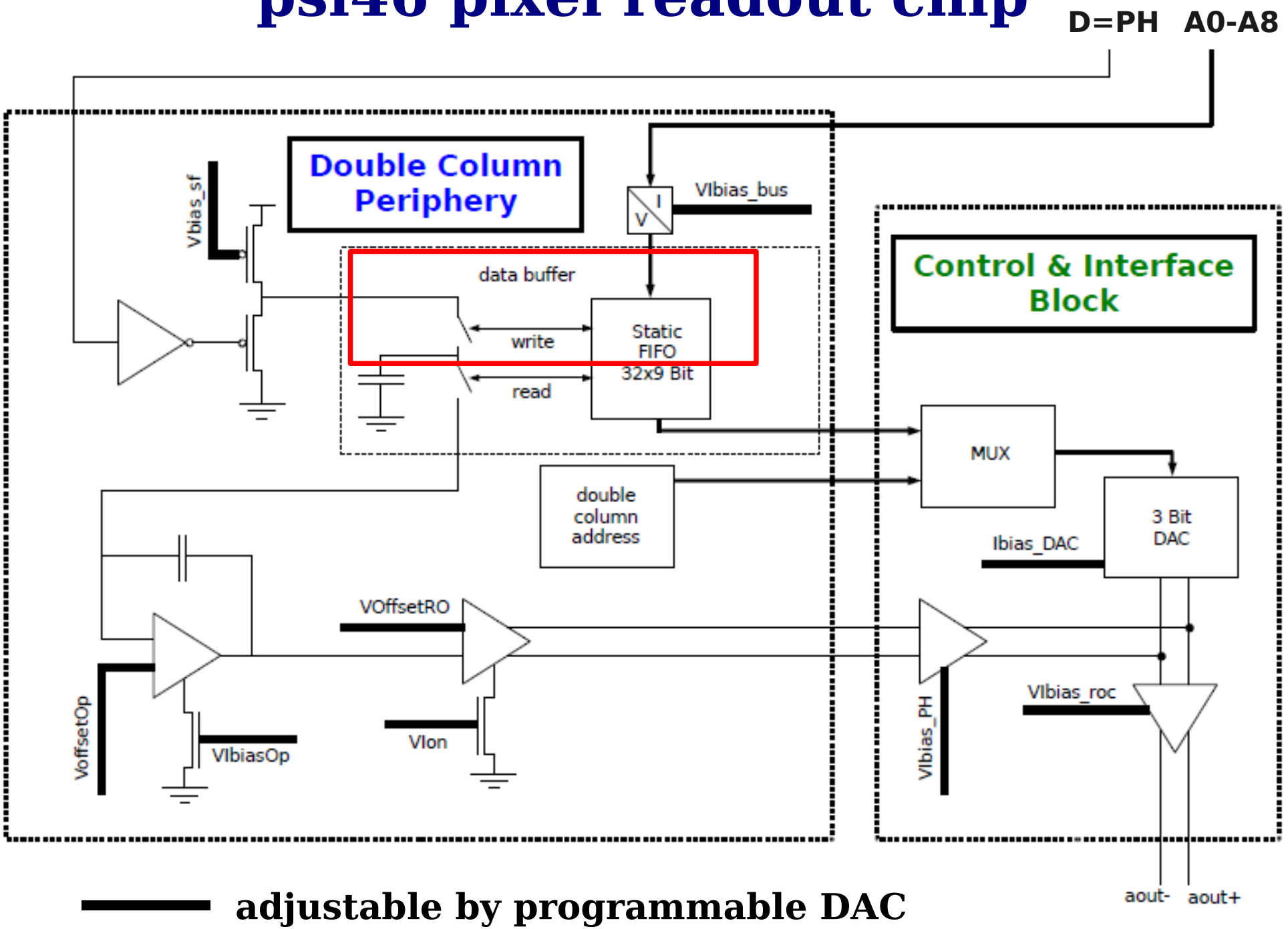


name
bits

adjustable by programmable DAC

modified in psi46digV2

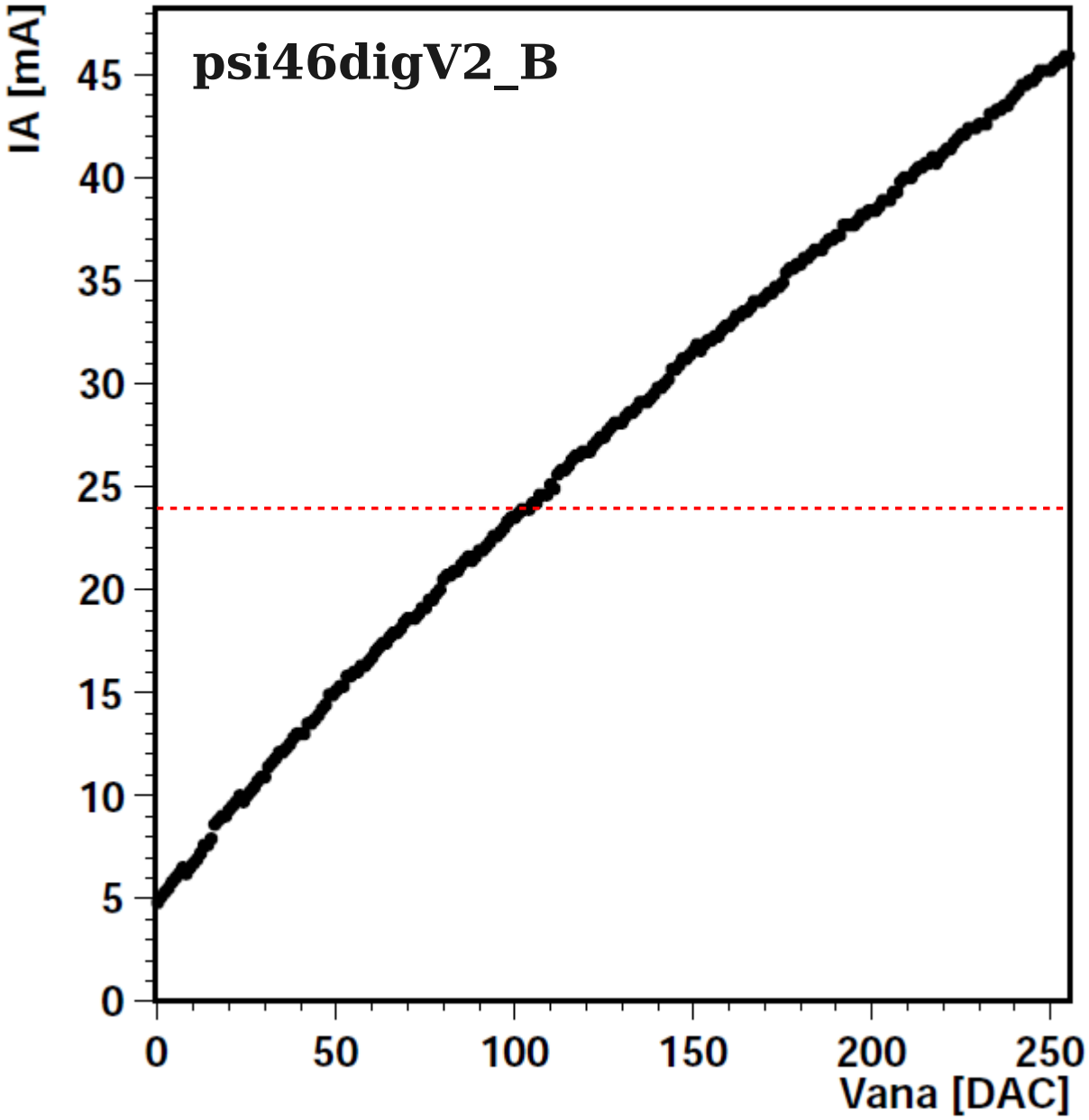
psi46 pixel readout chip



adjustable by programmable DAC

Analog current

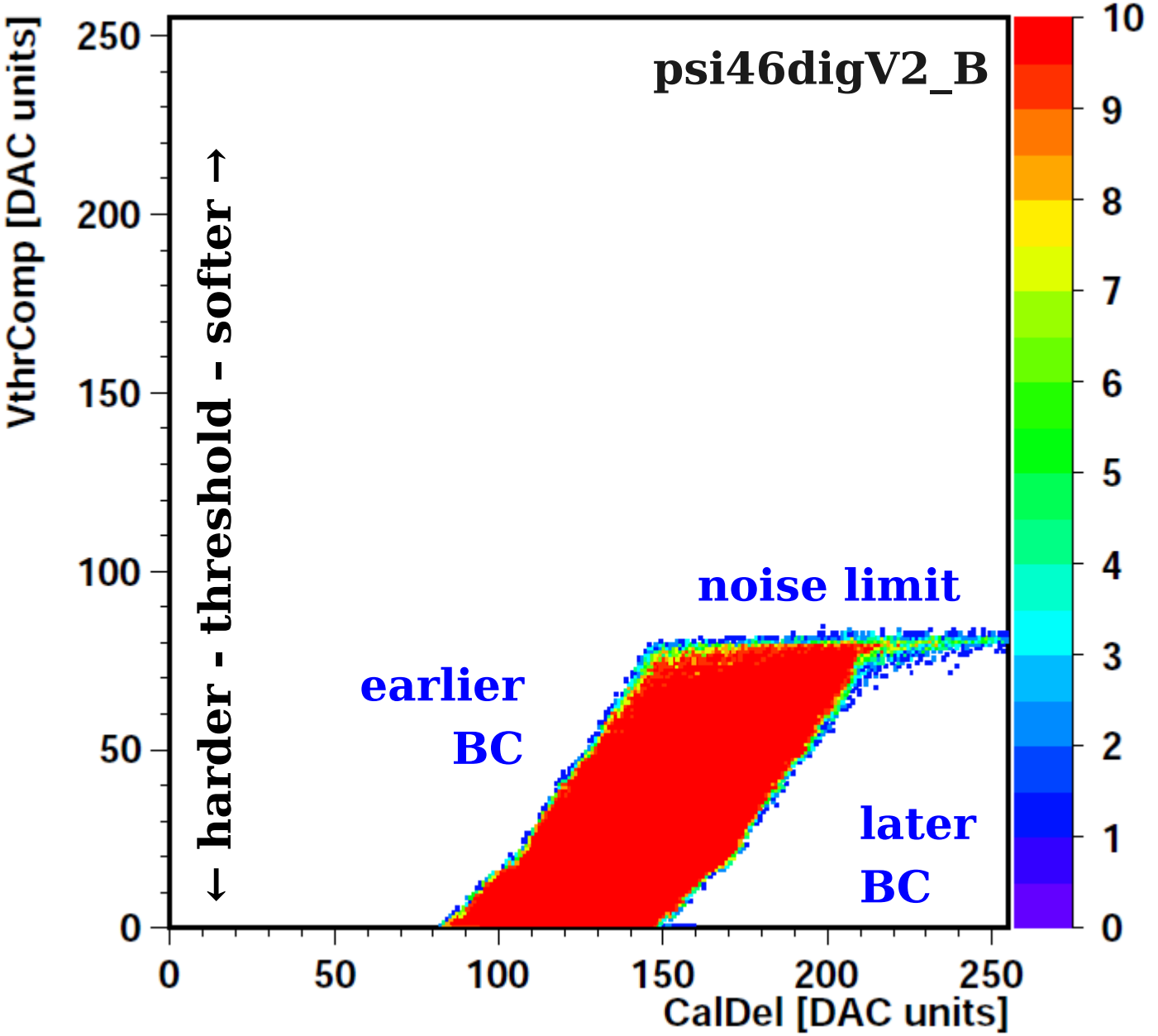
IA vs Vana



- psi46digV2_B
  - chip 300
- Current measured with an old test board
- IA range is 5 to 46 mA
  - fine adjustment: 0.16 mA/DAC
- Target operating current is 24 mA/ROC

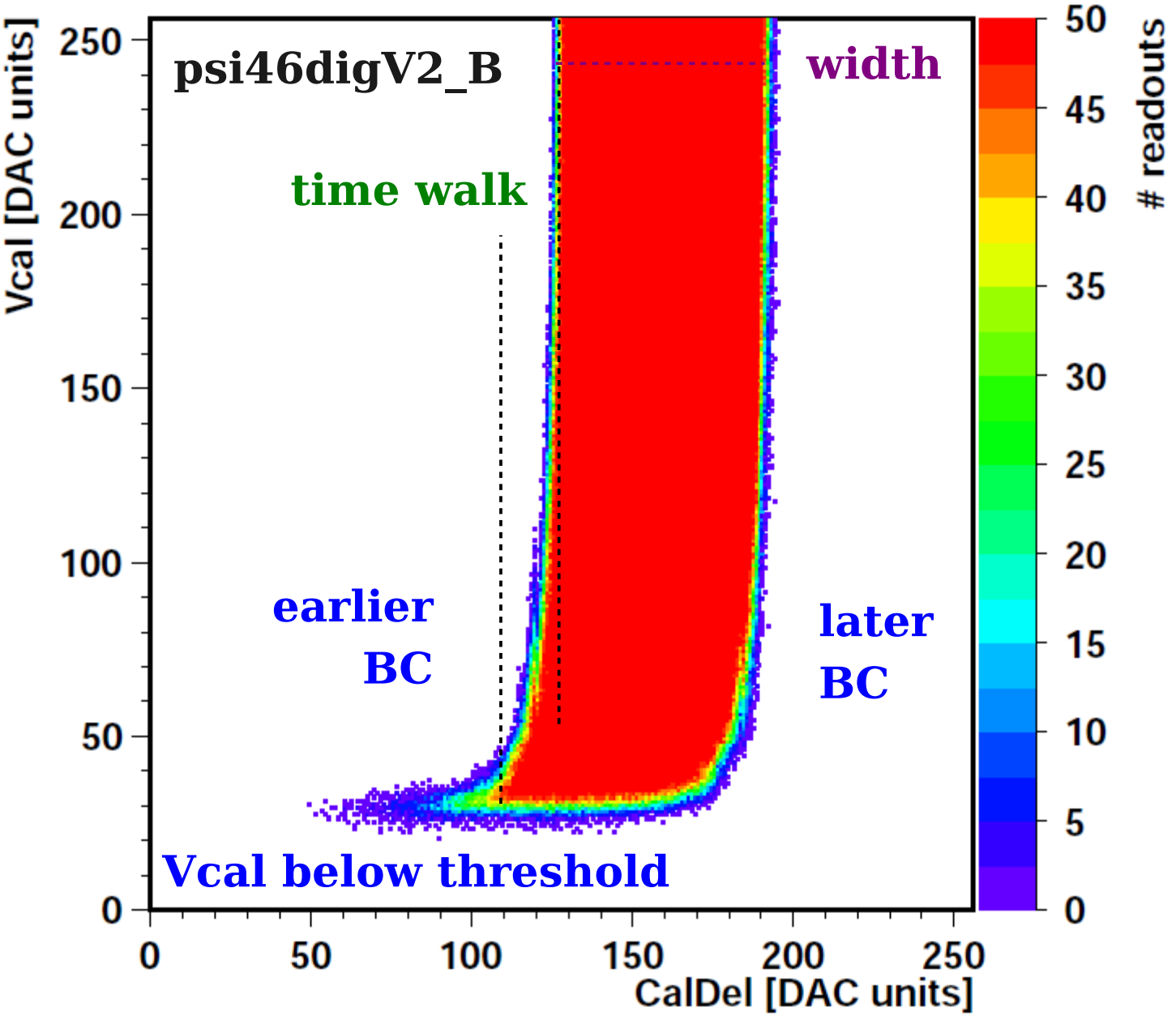
Timing

tornado plot digV2



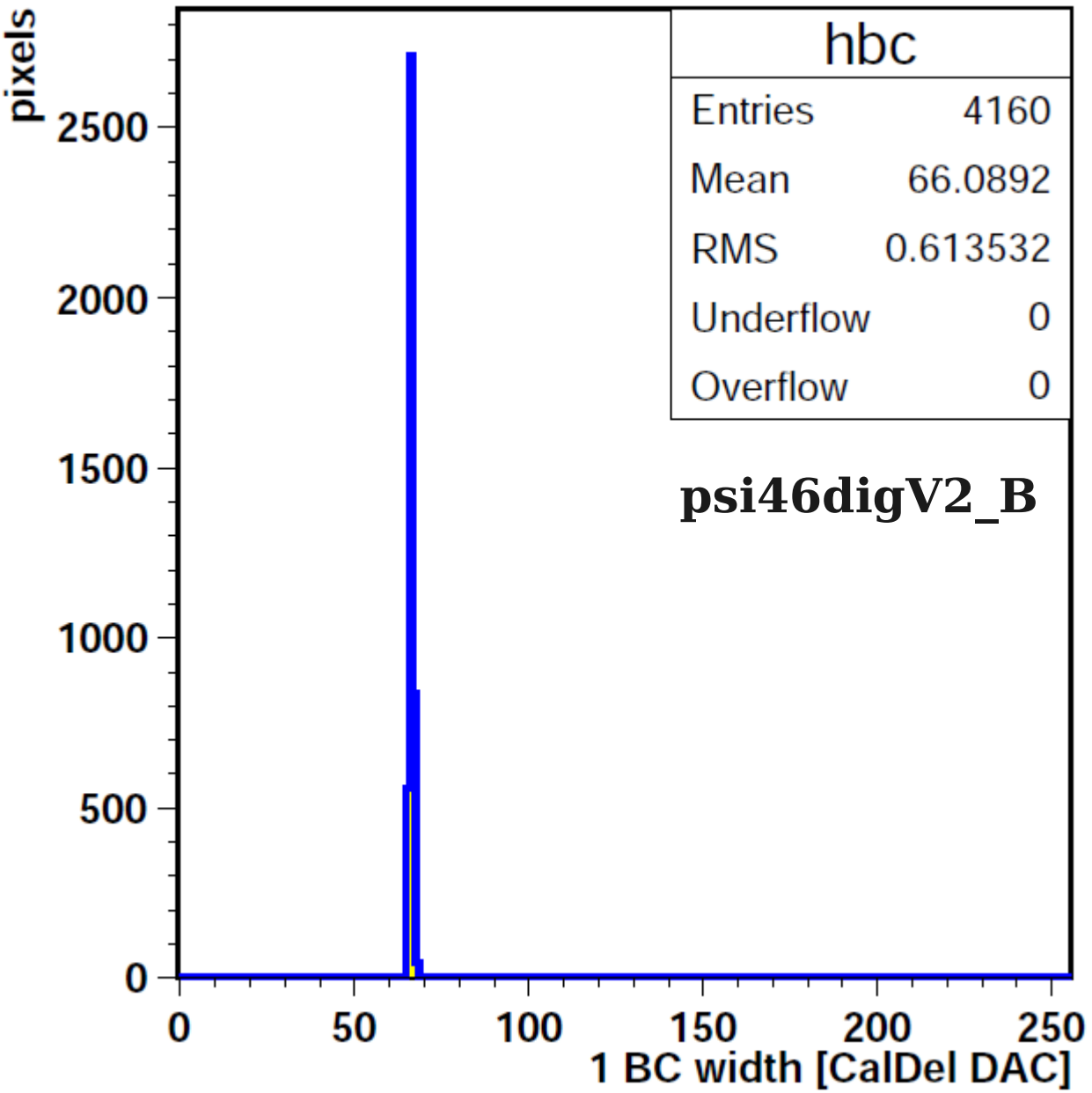
- psi46digV2_B
  - chip 300
  - Ia 27 mA
- Vcal 200 (low range)
- 2-D scan in VthrComp vs CalDel
  - 10 triggers per point
- Operation window is 25 ns wide (1 BC)
- VthrComp range is low

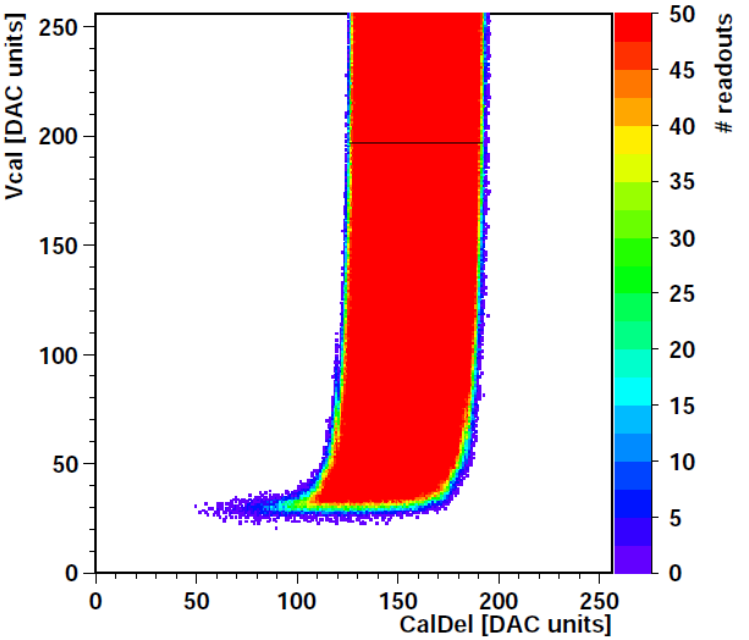
Time walk psi46digV2



- psi46digV2_B
  - chip 300
  - Ia 27 mA
  - VthrComp 48
- 2-D scan in Vcal vs CalDel
  - 50 triggers per point
- Operation window is 25 ns wide (1 BC)
- Time walk at small Vcal is less than 1 BC

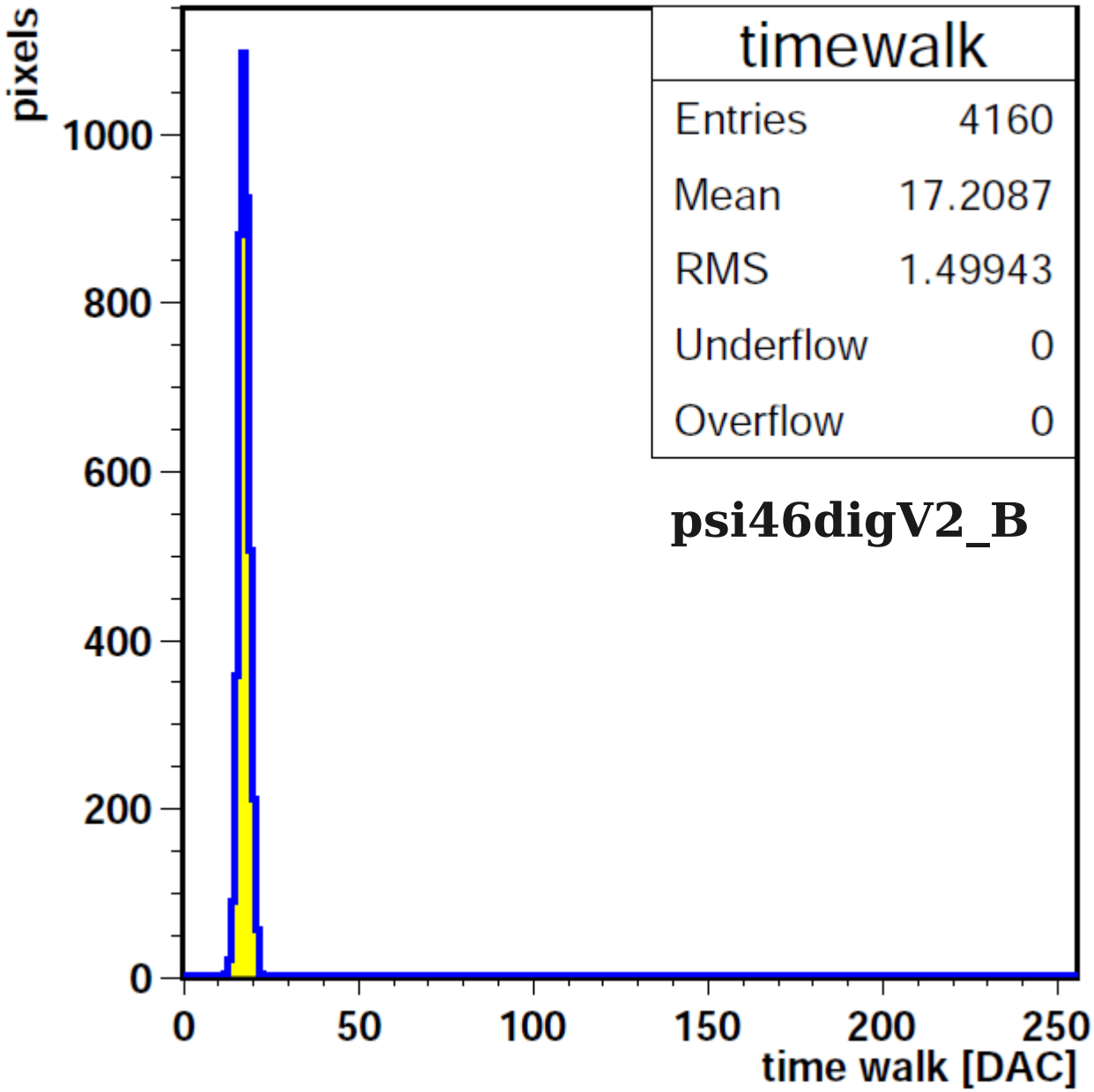
Width of timing window

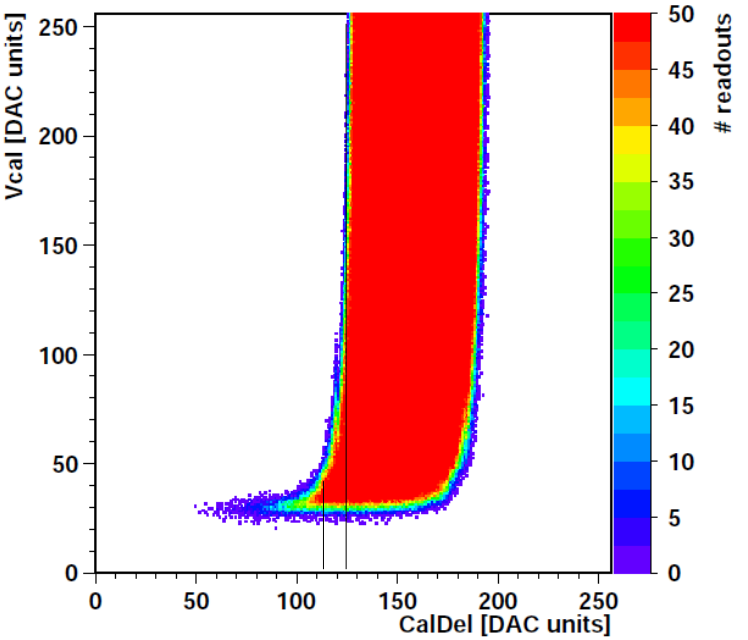




- psi46digV2_B
  - chip 300
- width of CalDel window for Vcal 200
- sharp distribution
- Mean: 66 CalDel DACs correspond to one BC (25 ns)

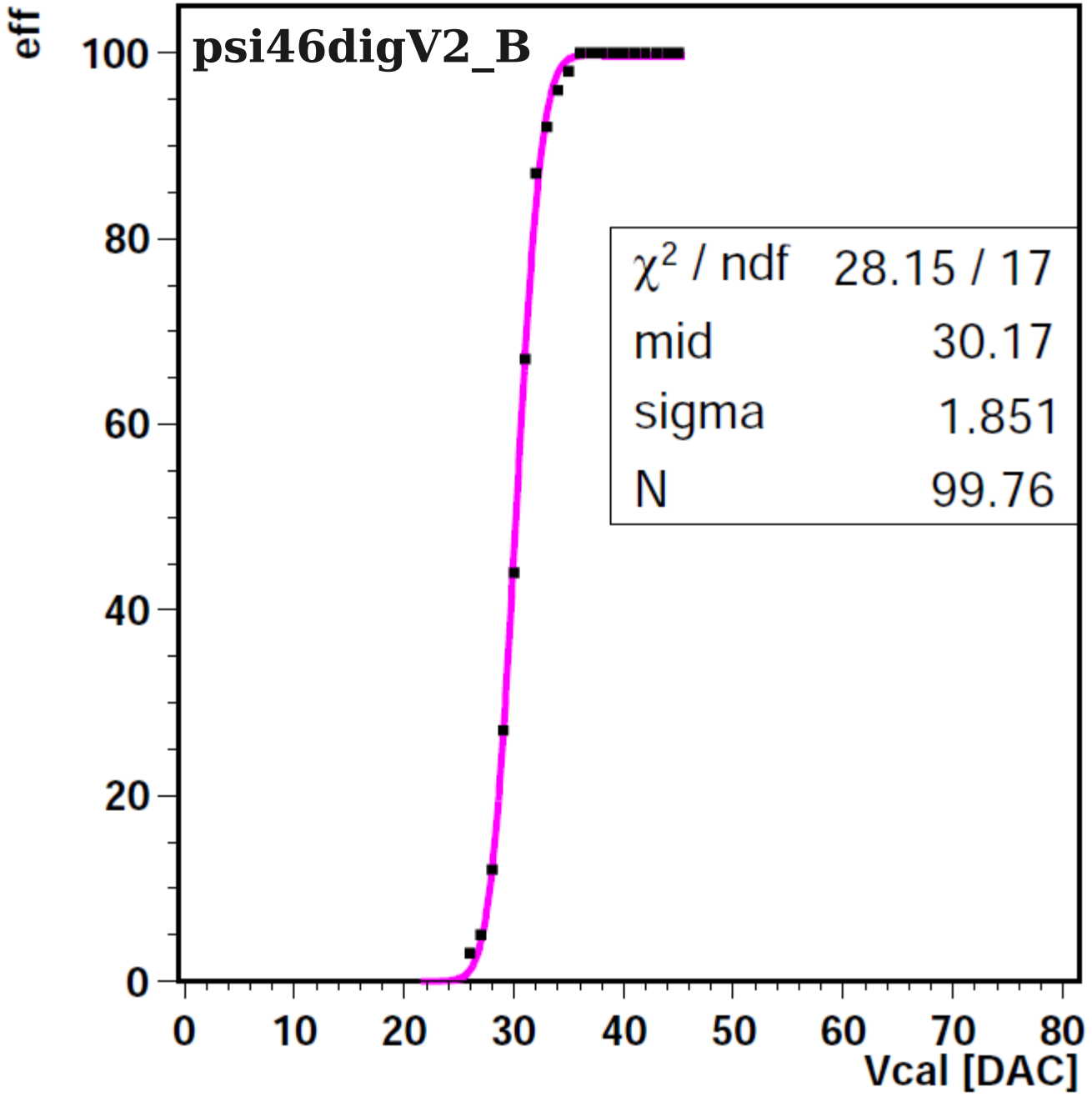
Time walk distribution





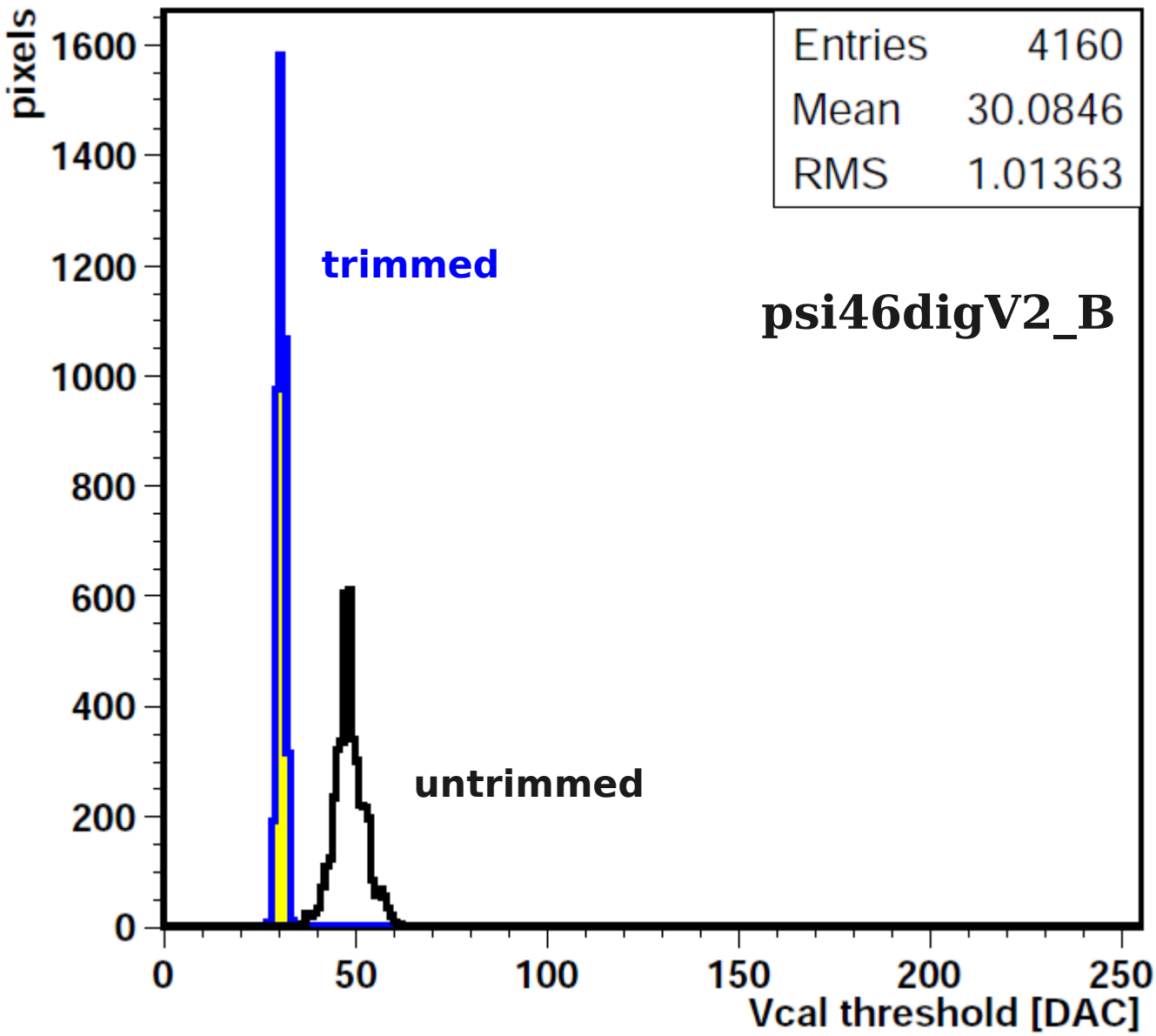
- psi46digV2_B
  - chip 300
- Time walk:
  - CalDel left edge at Vcal 200
  - – CalDel left edge at Vcal 40
- Mean: 17 CalDel DACs = 6.5 ns

Threshold curve



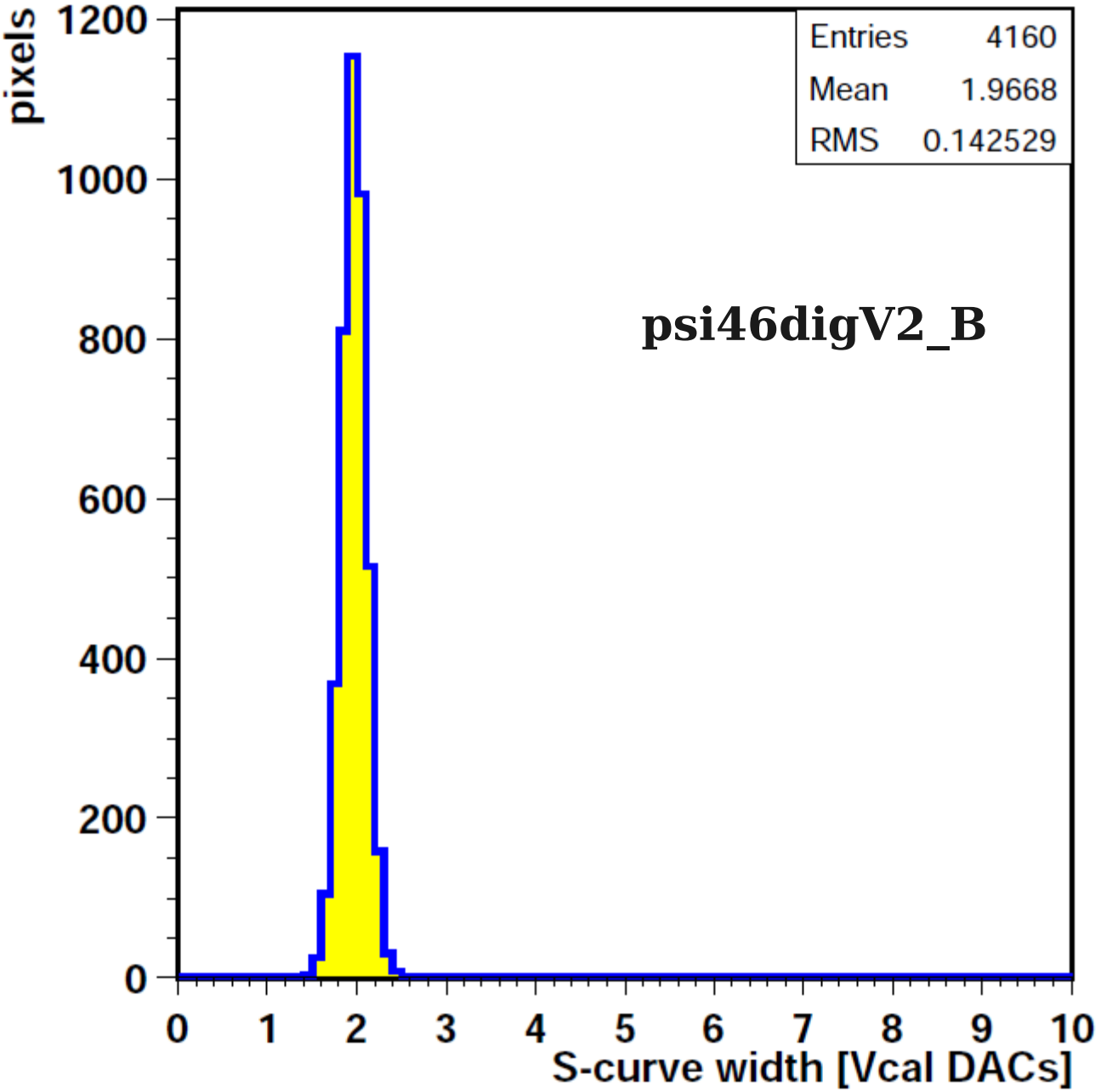
- psi46digV2_B
  - chip 300, no sensor
  - Ia 27 mA
  - trim to 30
- valid readouts vs Vcal
- threshold curve:
  - error function
  - width = noise
  - noise = 1.9 DAC
  - = 100 electrons.

Threshold trimming



- psi46digV2_B
  - chip 300
  - Ia 27 mA
- standard trimming procedure to target Vcal 30
  - converges nicely
- narrow threshold distribution after trimming

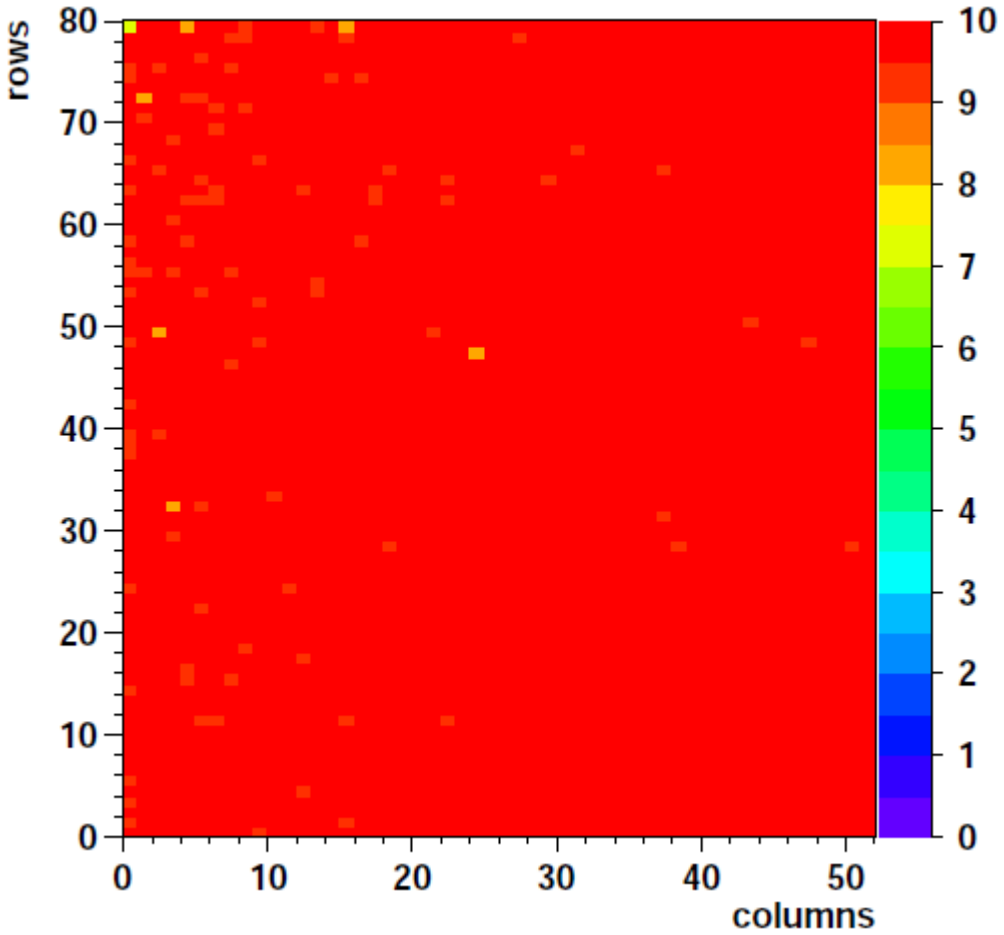
noise



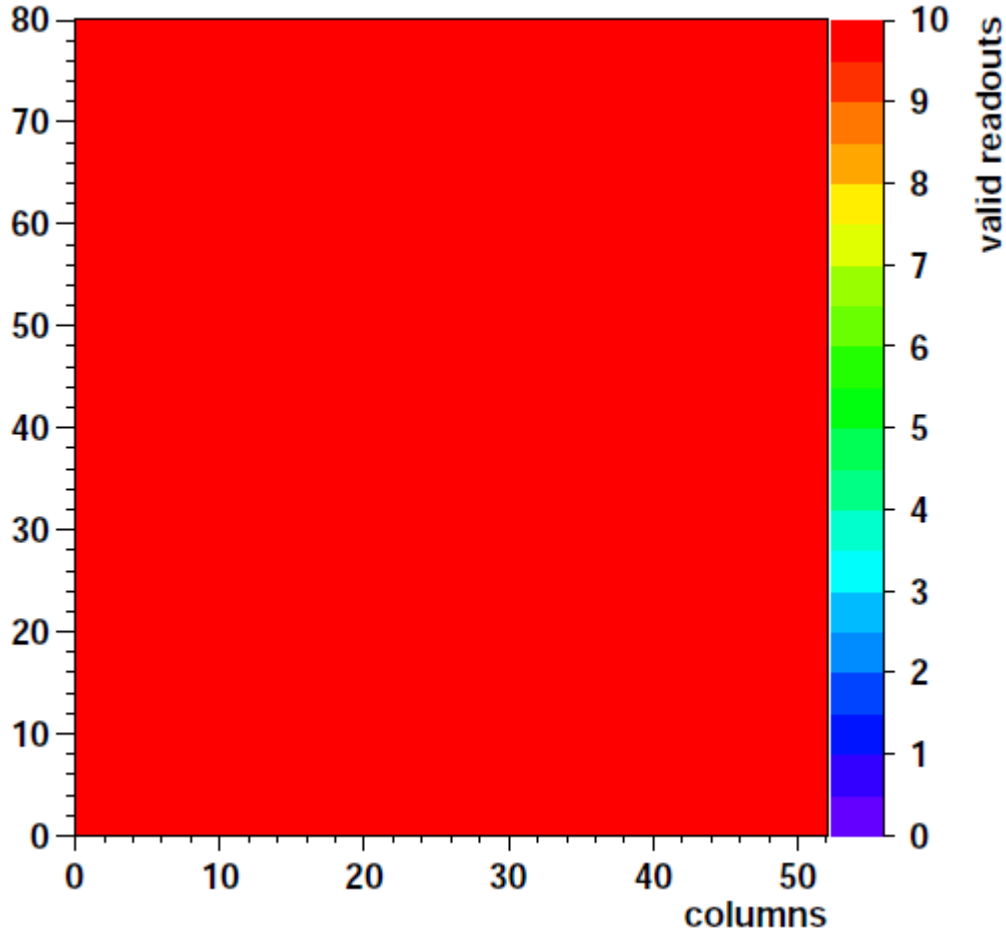
- psi46digV2_B
  - chip 300, no sensor
  - Ia 27 mA
  - trim 30
- width of threshold curve = noise
  - mean = 2 Vcal DACs = 100 e (nominal)

Pixel Alive test psi46digV2_B

Ia 25 mA

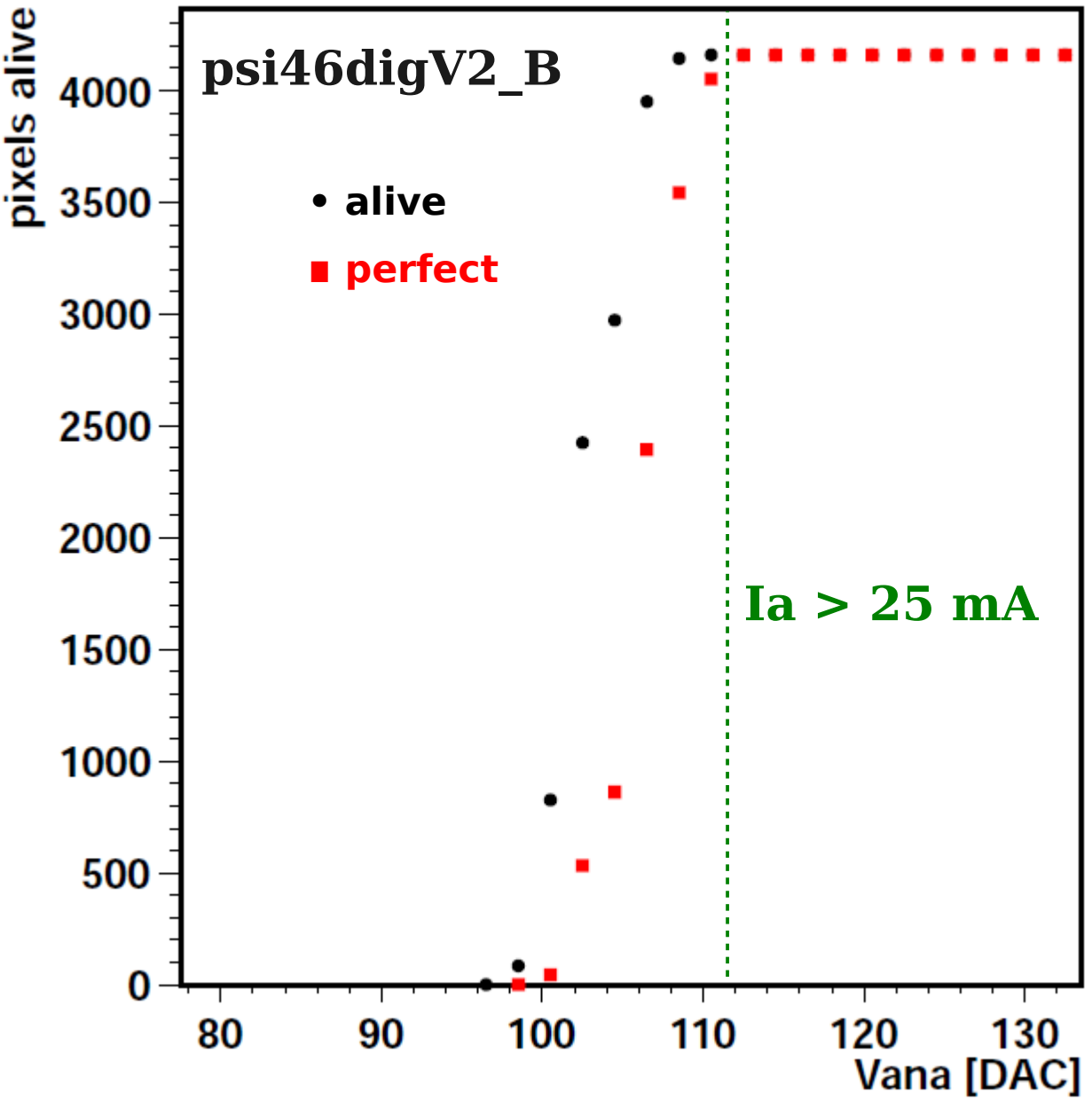


Ia 27 mA



all pixel 100%

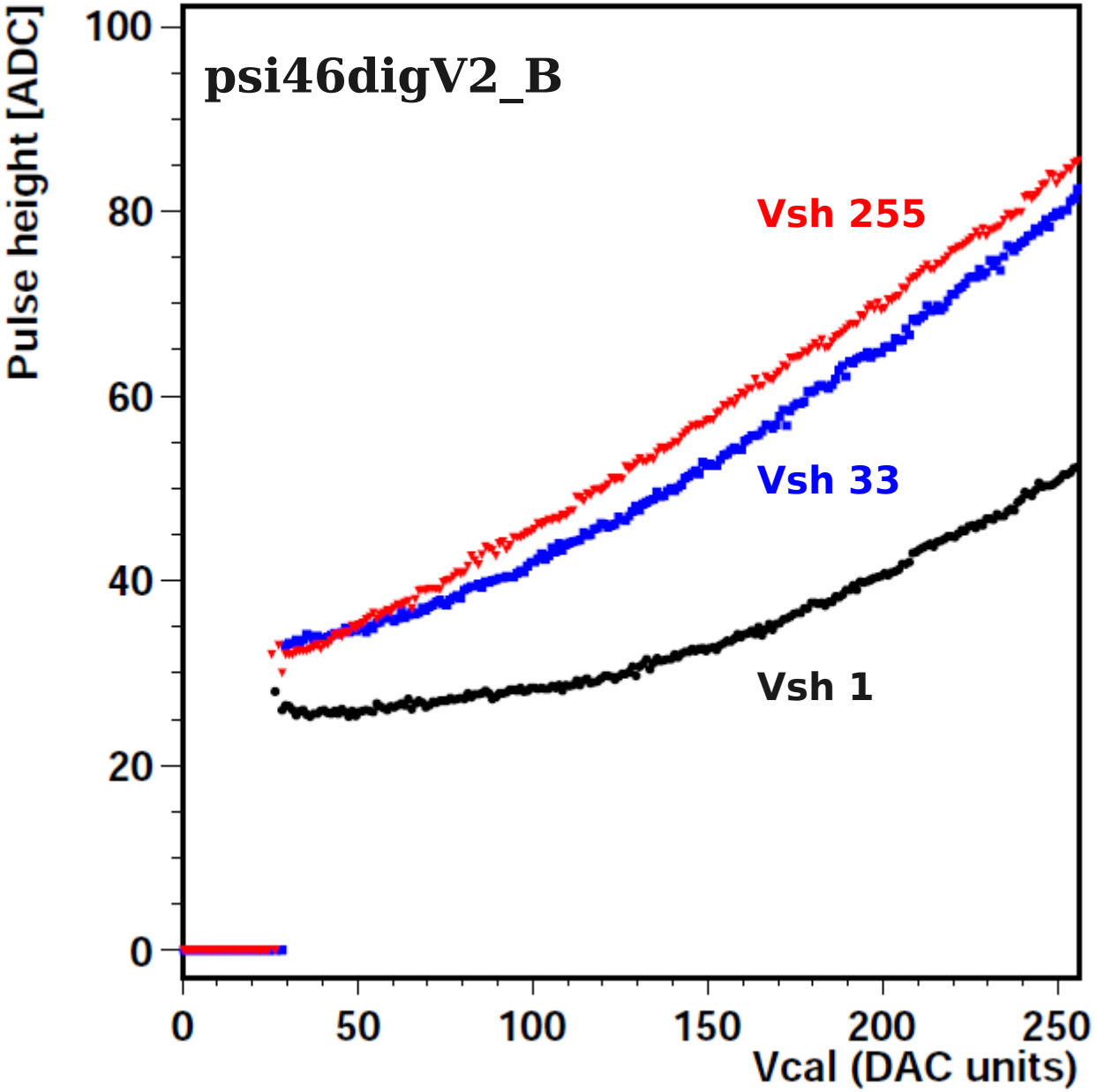
chip efficiency vs Vana

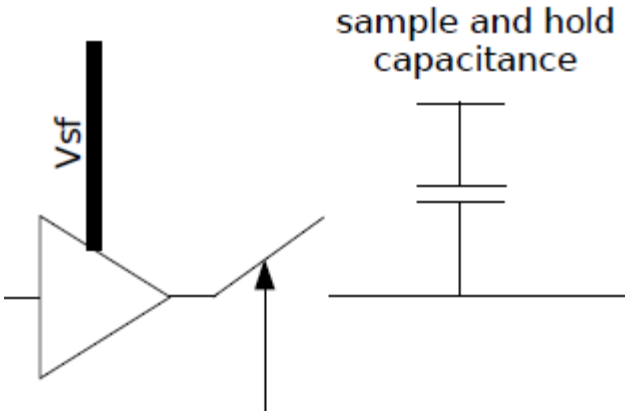


- psi46digV2_B
  - chip 300, no sensor
  - trim 30
- give 10 triggers per pixel per point
  - 50% = alive
  - 100% = perfect
- need Vcal > 111 DACs
  - Ia > 25.6 mA

pulse height

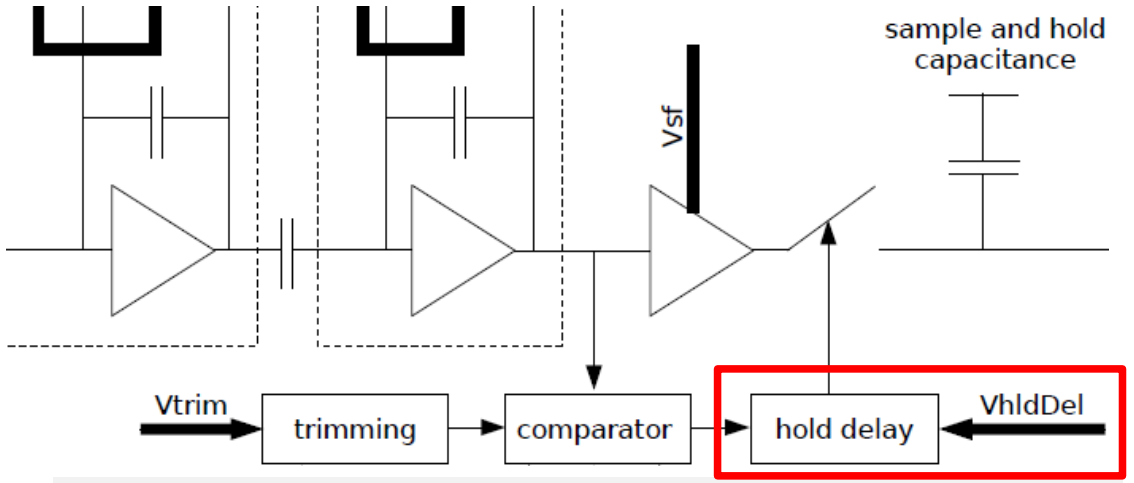
PH vs Vsh psi46digV2

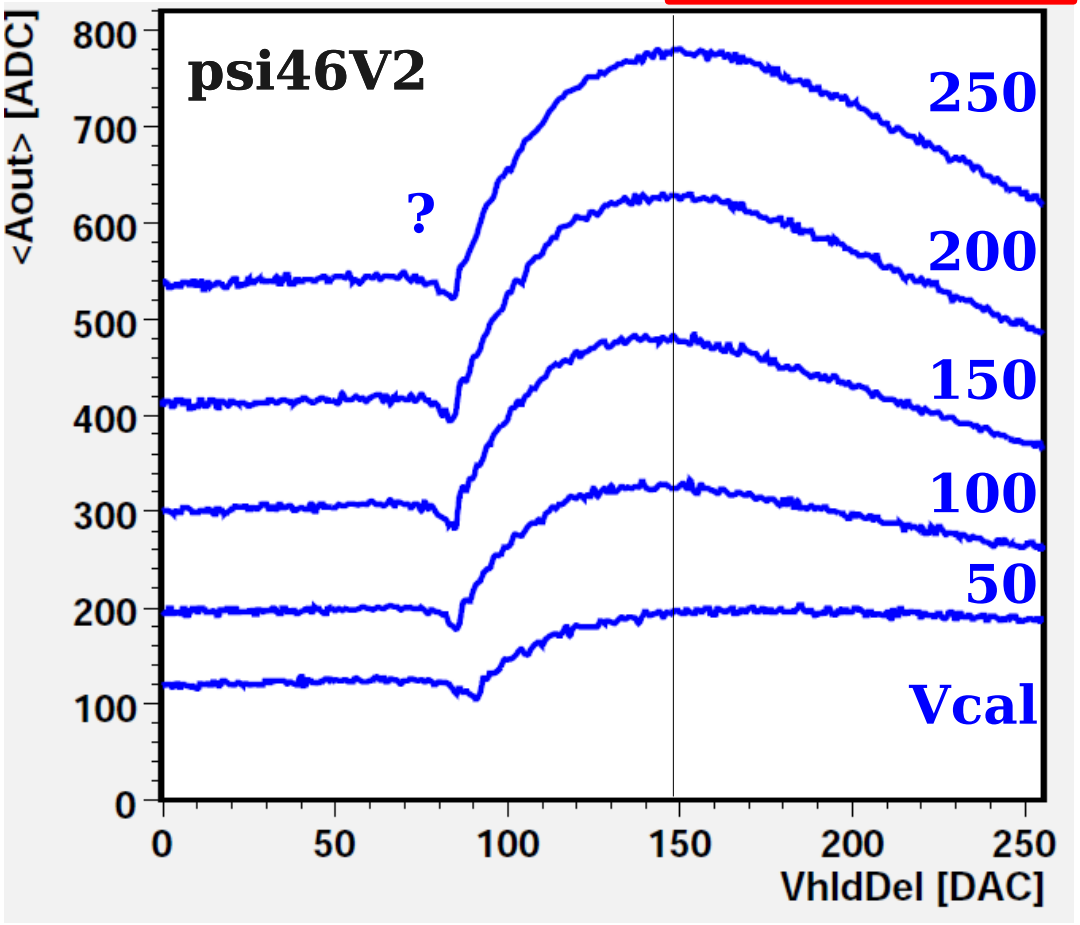




- psi46digV2_B
  - chip 300
  - Ia 27 mA
  - trim 30
- small Vcal (CtrlReg 0)
- **need large Vsh (Vsf) for best linearity**

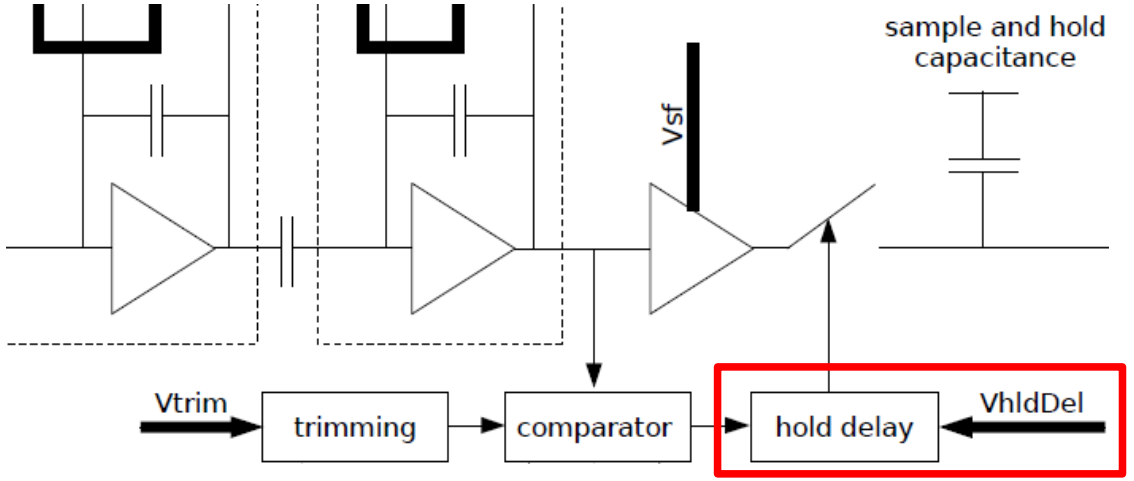
Sample and hold delay psi46

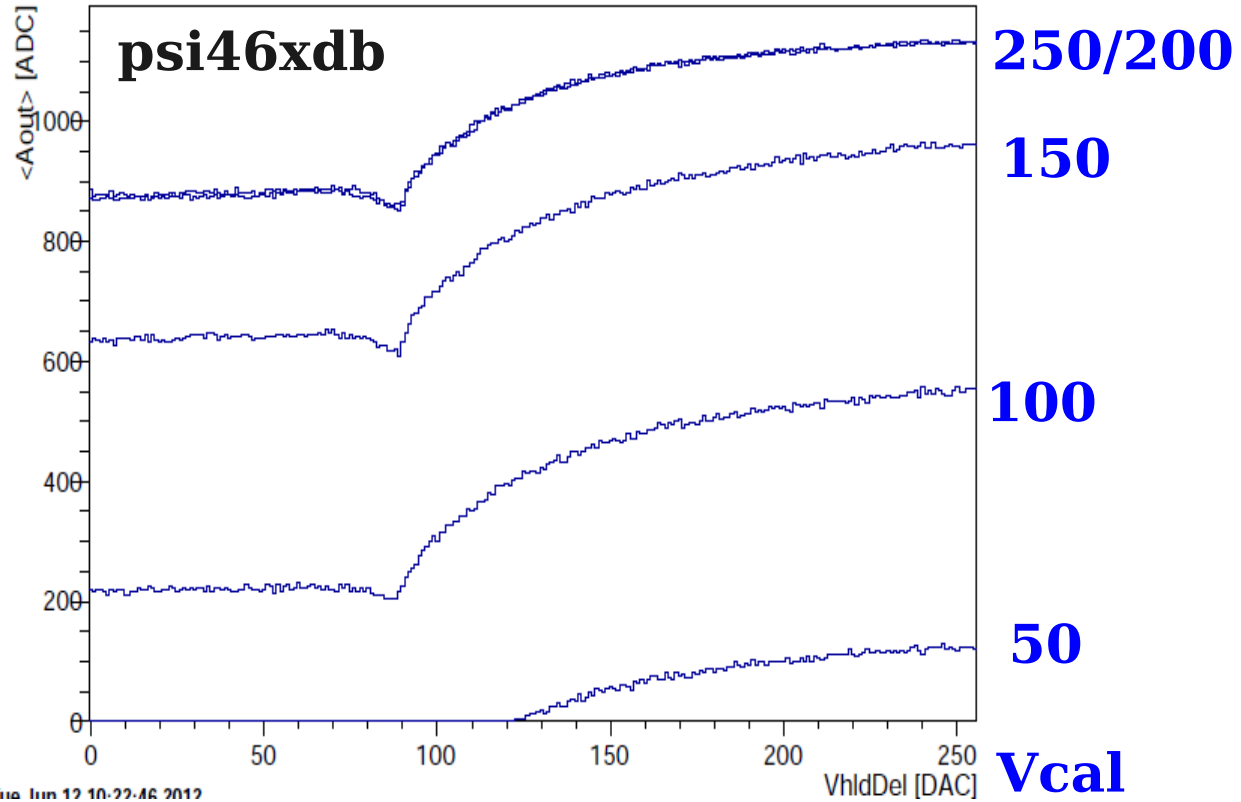




- analog psi46 chip 5
- VhldDelay changes sampling point on pulse
- full pulse shape visible

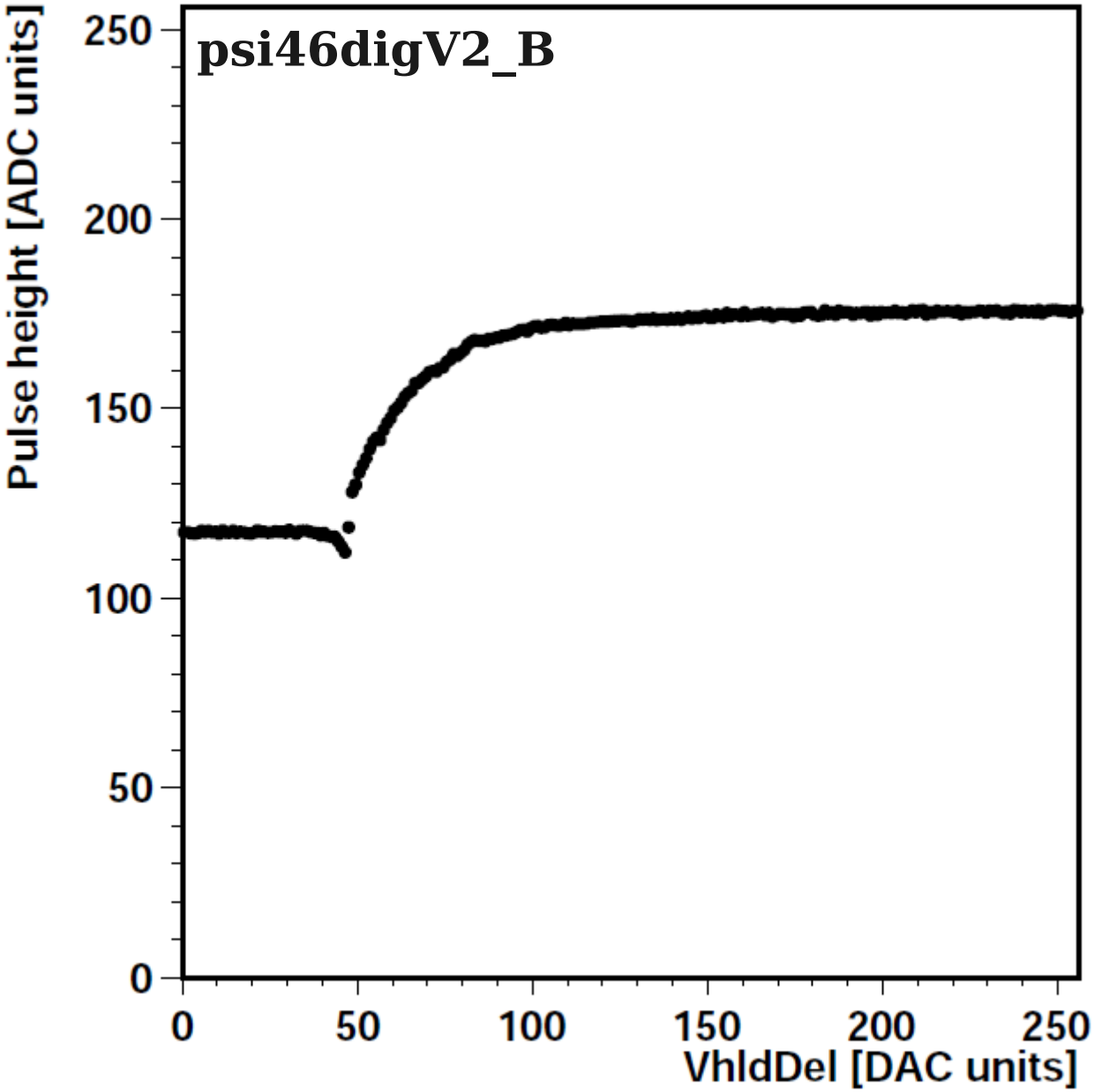
Sample and hold timing xdb





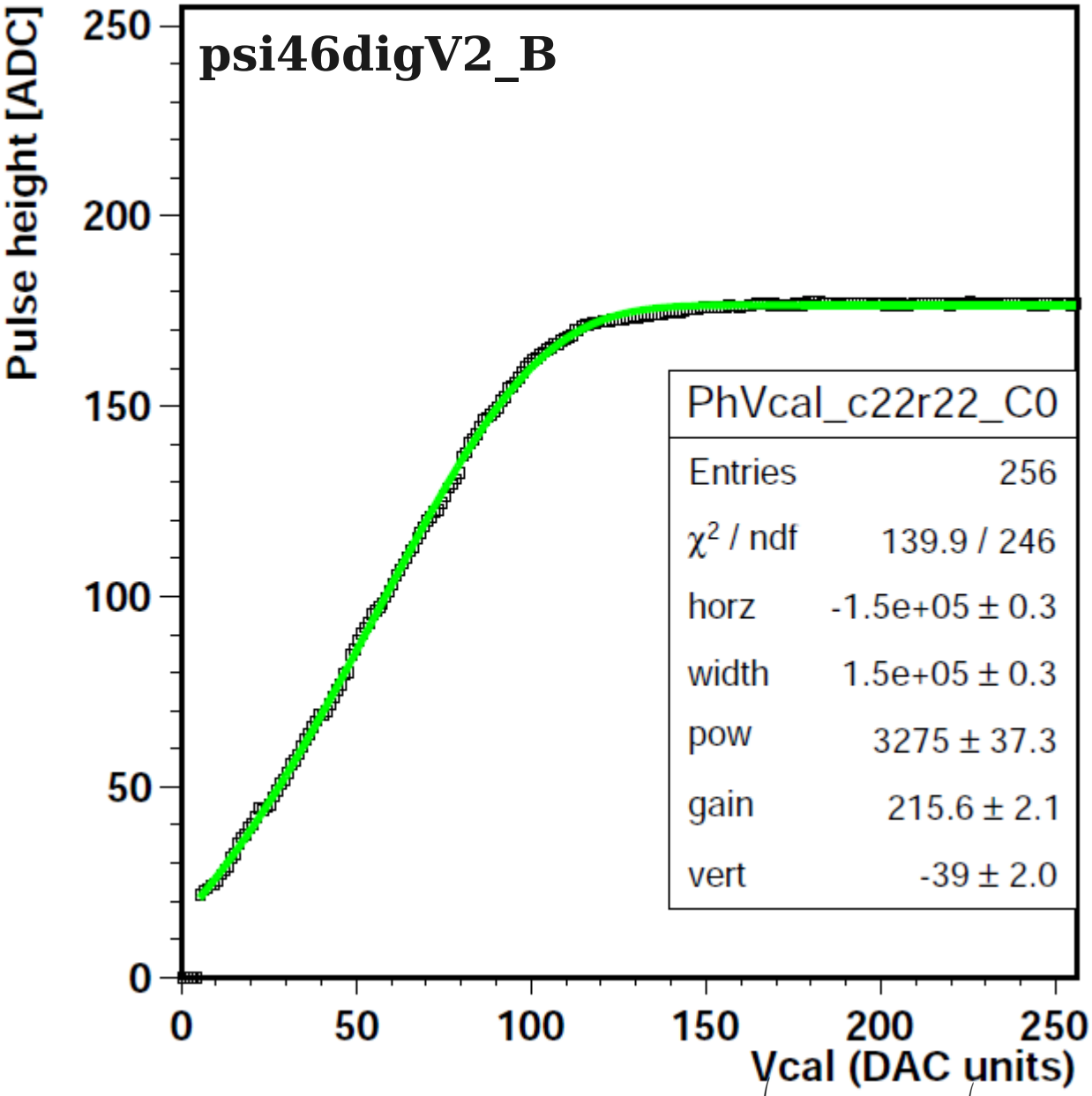
- psi46xdb (2012)
  - psi46dig (2012) similar
- Vsf is faster than comparator
- only falling end of pulse visible
- operate with VhlDel 252

Sample and hold timing psi46digV2



- psi46digV2_B
  - chip 300
- large Vcal 200 (CtrlReg 4)
- only falling end of pulse visible

PH vs Vcal

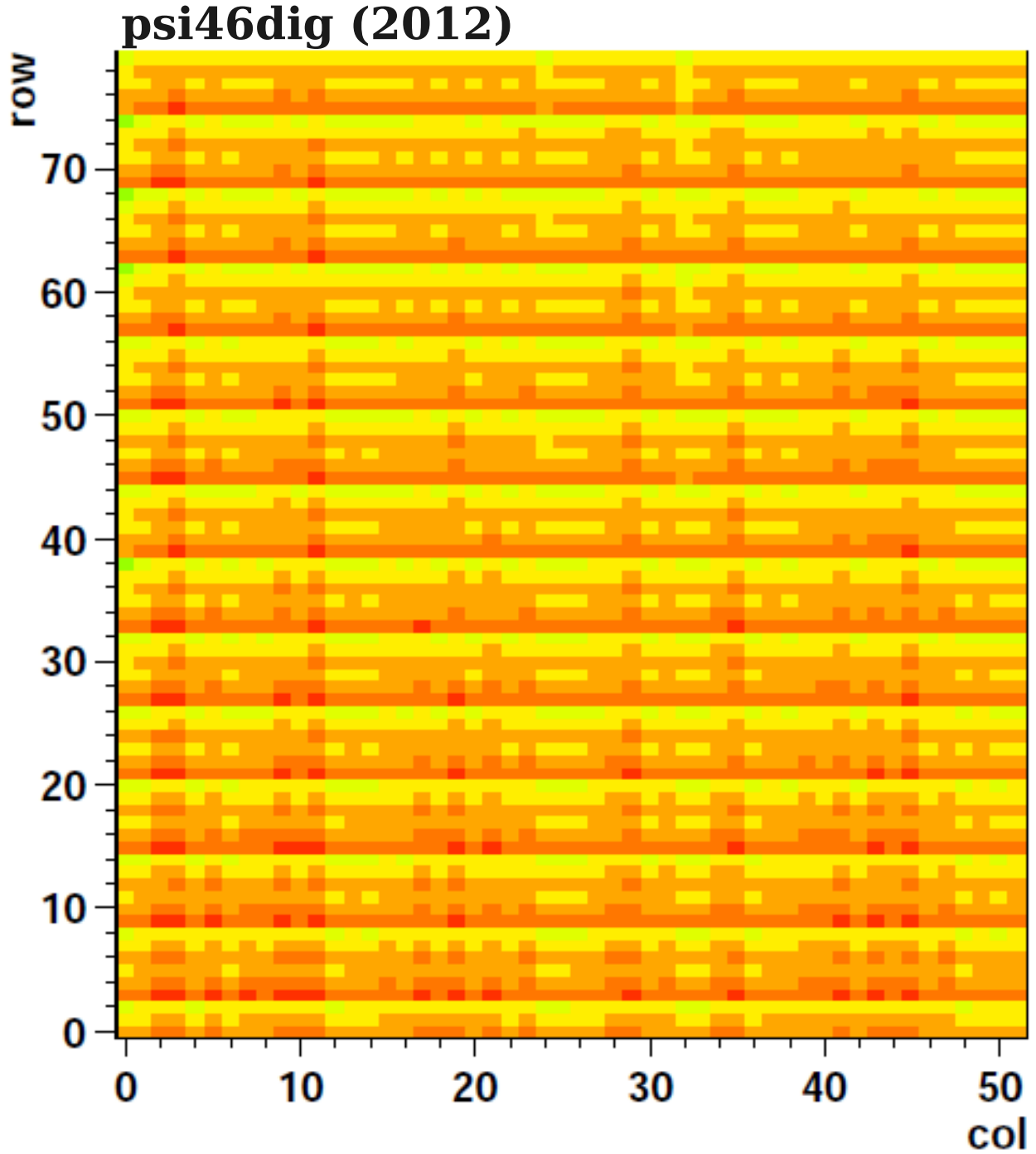


- Pulse height vs large Vcal
- Fit by Weibull function:
  - good fit from threshold to saturation
  - 5 parameters

Weibull: $PH = p_4 + p_3 \left(1 - \exp\left(-\left((V - p_0) / p_1\right)^{p_2}\right)\right)$

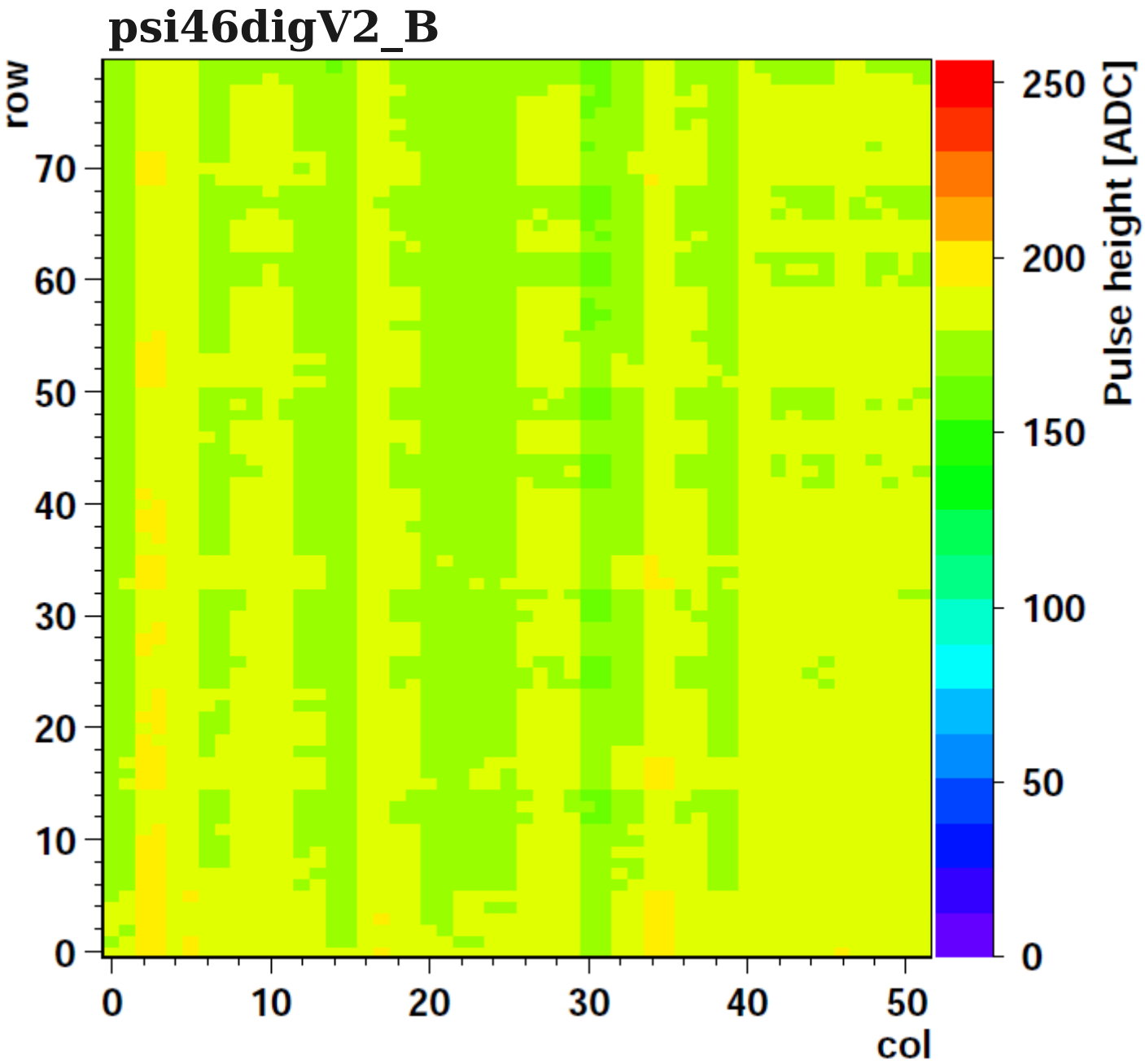
inverse: $V = p_1 \left(-\ln\left(1 - (PH - p_4)/p_3\right)\right)^{1/p_2} + p_0$

Pulse height map psi46dig (2012)



- psi46dig (2012)
  - chip 202
  - Ia 35 mA
- large Vcal 255 (CtrlReg 4)
- ADC pulse height:
  - row-wise variation with period 6
  - chip simulation said: address to PH cross talk in the data buffer

pulse height map psi46digV2_B



- psi46digV2_B
  - chip 300
  - Ia 27 mA
- large Vcal 200 (CtrlReg 4)
- ADC pulse height:
  - row-wise variation gone (was cross talk)
  - some column gain variation visible: gets calibrated away

DACs for psi46digV2_B

1	Vdig	6	
2	Vana	122	(27 mA)
3	Vsf	233	linearity
4	Vcomp	12	
7	VwllPr	60	
9	VwllSh	60	
10	VhldDel	252	PH peak
11	Vtrim	140	
12	VthrComp	48	
13	VIBias_Bus	20	
14	Vbias_sf	14	PH gain
15	VoffsetOp	67	PH range
17	VOffsetR0	140	PH range
18	VIon	45	PH gain
19	Vcomp_ADC	100	
20	VIref_ADC	60	PH gain
22	VIColOr	100	
25	Vcal	200	
26	CalDel	152	
253	CtrlReg	0	
254	WBC	100	

Summary

- The new psi46digV2 works!
- Improvements confirmed:
  - power startup circuit OK (no scratching of lines needed)
  - pixel row address OK (was inverted, danger of confusion with header)
  - row-dependent cross talk on pulse height in data buffer cured
  - comparator (from xdb) has time walk much less than one BC
  - comparator (from xdb) operates at low threshold (<1500e)
- Not yet tested:
  - bandgap reference temperature compensation
  - second ADC for slow read back of ROC internal voltages
  - stacked trigger problem solved (2^{nd} trigger before readout possible)
  - fixed DAC supply voltage (independent of Vdig, only on V2 chip)
  - PH independent of Vdig and of X-ray rate

Summary 2

- psi46digV2 'features' and 'issues':
  - VthrComp has limited range (<4500 e)
  - need large Vsf for pulse height linearity
  - range of VhldDel increased, but rising edge of pulse not visible
- Next steps:
  - more lab measurements
  - get ROCs with sensor for DESY beam test May 20-26
  - get ROCs with UBM for irradiation in Karlsruhe (bump bond sensor afterwards)

Back up