

New 32 Channel ADC design

Wednesday 11 December 2013 14:50 (8 minutes)

This talk describes an MTCA.4 compliant AMC and μ RTM for high channel count analog to digital conversion applications, developed within HVF.

The AMC provides 32 ADCs with 12 or 14 Bit resolution. Depending on the ADC used, sample rates up to 20 Msps are possible.

A powerful clock distribution allows the use of backplane-distributed or on-board generated clocks as ADC sample clock.

A Kintex-7 FPGA provides the ability to transfer ADC data via x4 PCI-Express Gen 2. In addition, on-board DDR3 memory allows to store ADC data for subsequent readout.

The ADCs analog inputs connect to a μ RTM via Zone 3 with a pin assignment according to Class A1.2.

Signal conditioning and analog input connectors are located on the μ RTM, allowing easy adaption to different user requirements.

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Session Classification: New products

Track Classification: New products