

Open hardware / open software MTCA.4 - based beam position measurement system

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Agenda

- A few words about Creotech Instruments SA
- What is Open Hardware
- Some OH products
- Beam Position systems based on MTCA.4
- OH MTCA.4 development at CTI and WUT
- WR-MCH

Who we are?

Creotech Instruments S.A.:

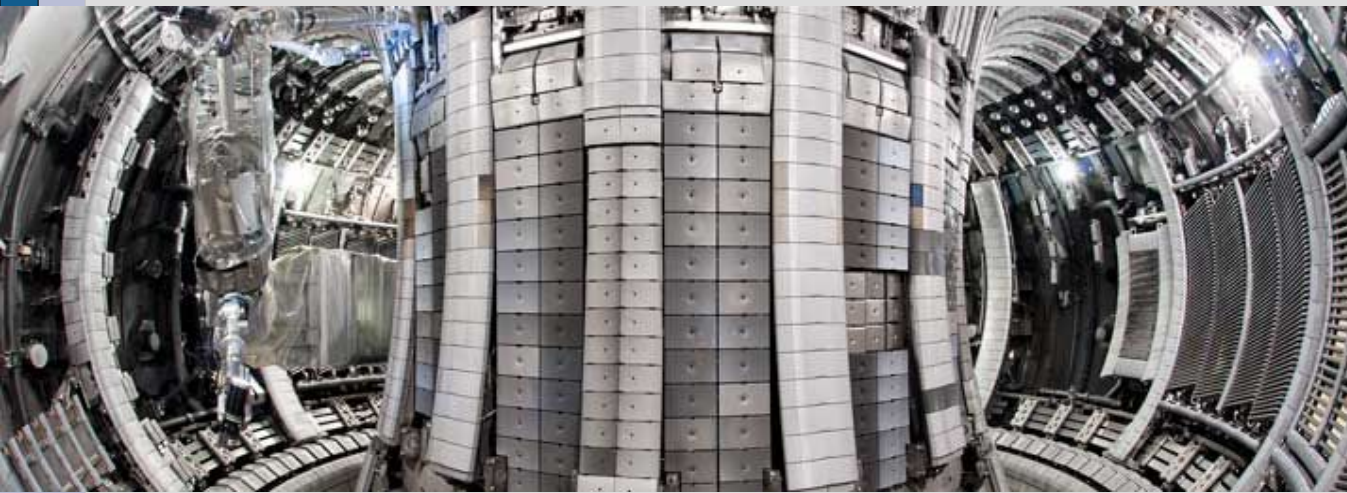
- Creotech Ltd. was founded in 2008 by 3 CERN workers
 - 2011 – the joint-stock company Creotech Instruments S.A. was created
 - 2012 – two private share emissions, work on ISO9001 started
 - 2013 – an investment in a cleanroom facility, start of space technologies projects
- First ASIM (ISS) project completed



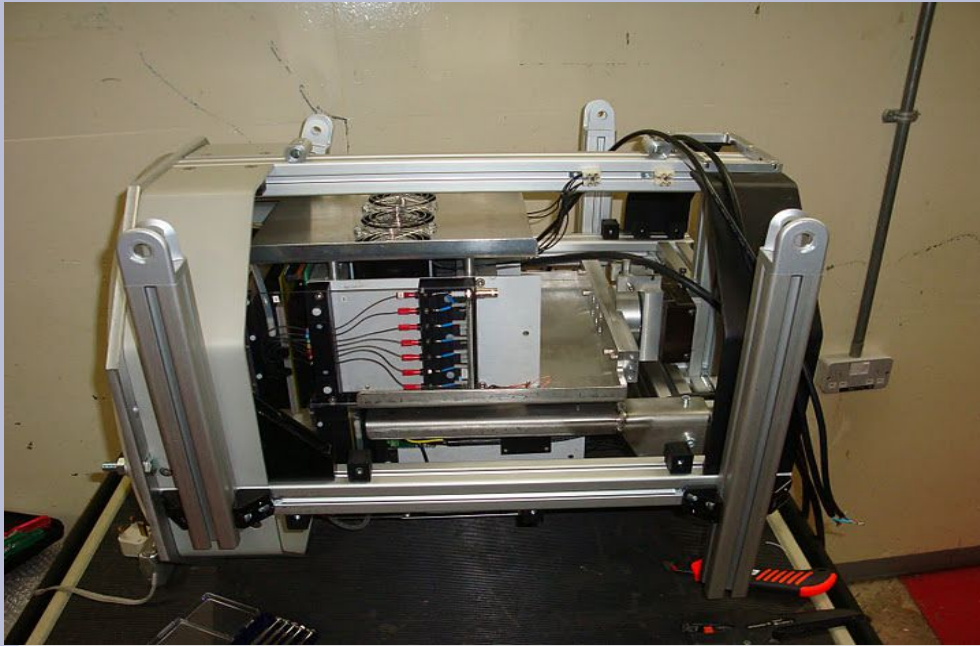
- 14 people employed (2 PhD, 12 engineers)

Who we are?

Our proprietary solutions were tested in international research projects



JET Tokamak spectrometer

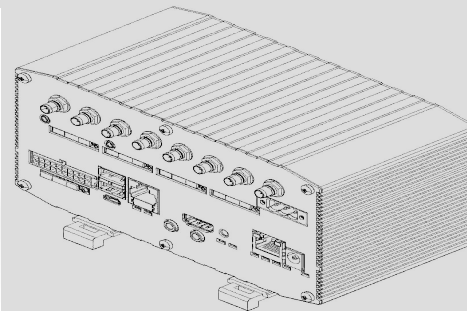
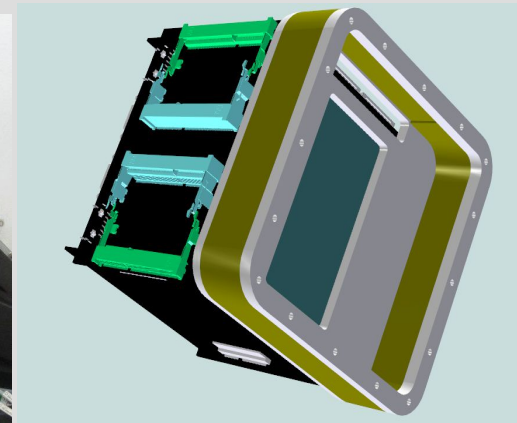
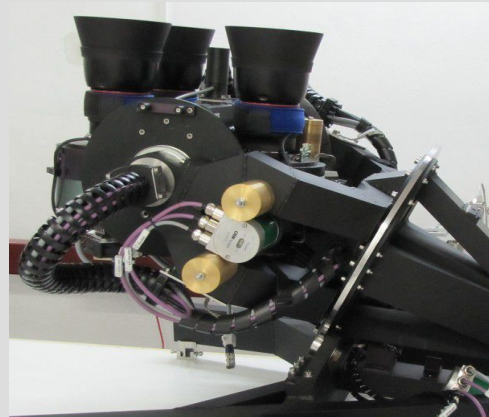
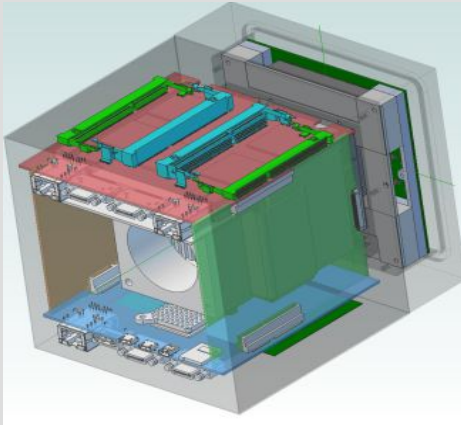


- 512 AFE+ ADC channels, 100MS/s, 10 bit
- Custom processing backplane
- 48 FPGA used
- Embedded x86 CPU
- Dedicated 7-channel HV supply



We do it not only for science..

But interaction with scientific projects improves our skills and know-how




How OH gives us business opportunity

- It's great place to **advertise company capabilities**, skills and expertise and collect more orders
- It's **place to exchange ideas**, collect feedback and product improvements
- Here the company may show realized projects and get recommendations
- Sharing hardware and firmware files encourages other companies to do the same and lets us gain part of their know-how
- Next products can be created much **faster** thanks to modification or **re-use of existing ones**, developed and tested by someone else
- Thanks to opening design files in early stage of product, other engineers may **find bugs or suggest modifications** which leads to better product – **the peer review**
- By sharing own product HW and FW files, company **gets vantage over competition** – some clients will choose such solution which they can control, modify or repair in the future (after warranty period)

	Commercial	Non-commercial
Open	Best of both worlds	Whole support burden falls on developers
Proprietary	Vendor lock-in	Dedicated non-reusable projects

Examples of successful OH projects

HELP




The following companies are actively using the OHR site to develop or produce open hardware, software and drivers. These companies may be paid for the open developments. Please not that companies may in fact be involved in more areas than described in the table below. This table only reflects work done in the OHR site.

Name	Description	Country	HW development	HW commercialisation	HDL development	SW development	Projects	Members
Cosylab	Your trusted control system partner	Slovenia	✓		✓		2	3
Creotech	An enterprise of zeal and excellence	Poland	✓	✓			24	1
Digicom Electronics	Detail oriented, Integrated solutions, Guaranteed, Industrious, Capable, On-time, Manufacturing Excellence	USA		✓			1	0
Elproma	ELPROMA presents next generation IEEE1588 (PTPv2)	Poland					0	0
Gnudd	Helping our partners to master technologies	Italy				✓	18	2
HLP Technologies	Create Design Develop and Maintain	France	✓	✓	✓	✓	1	0
Igalia	Open source consultancy for innovative projects	Spain				✓	2	3
INCAA Computers	Your partner in automation	The Netherlands	✓	✓		✓	5	1
Integrasys	Building Success from Innovation	Spain			✓	✓	2	3
Janz Tec	Industrial Computing Architects	Germany		✓			1	0
MagentaSys	MagentaSys	Switzerland	✓				2	0
Milky Mist	Eyecandy on a Chip	France			✓		1	1
OCLogic	Hardware design and simulation	UK			✓	✓	1	0
ORSoC	FPGA, ASIC, DSP – embedded SoC design	Sweden	✓				1	0
Seven Solutions	An Open Company!	Spain	✓	✓	✓	✓	13	6
Splendeo Innovación	Intuitive, easy to use web applications	Spain				✓	1	1

Glossary

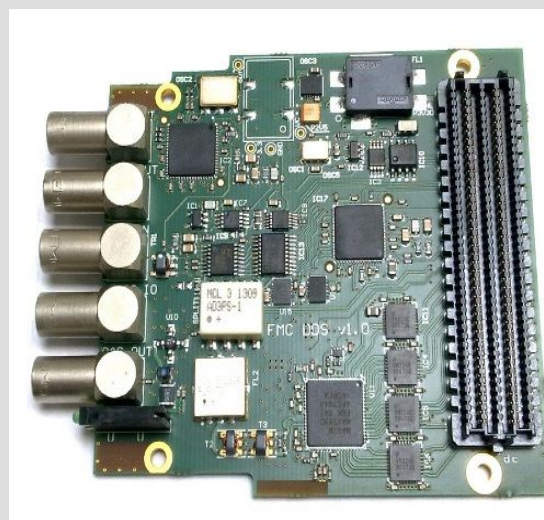
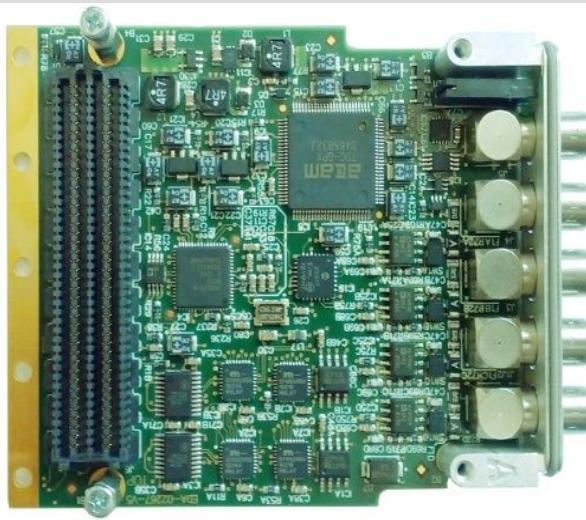
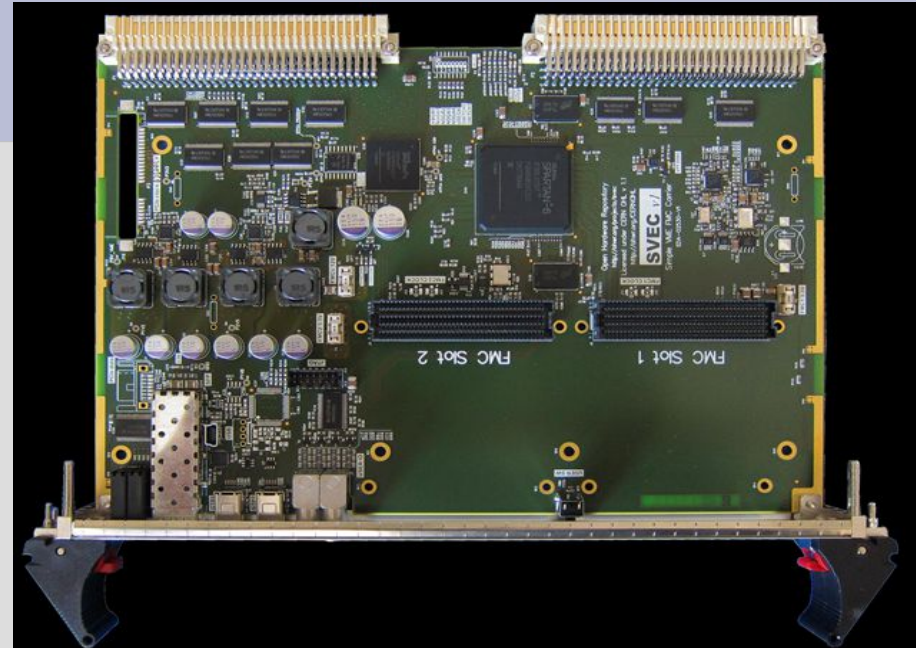
- HW development: Hardware development
- HW commercialisation.: Hardware commercialisation
- HDL development: Firmware development (e.g. VHDL)
- SW development: Software and driver development



Powered by ChiliProject

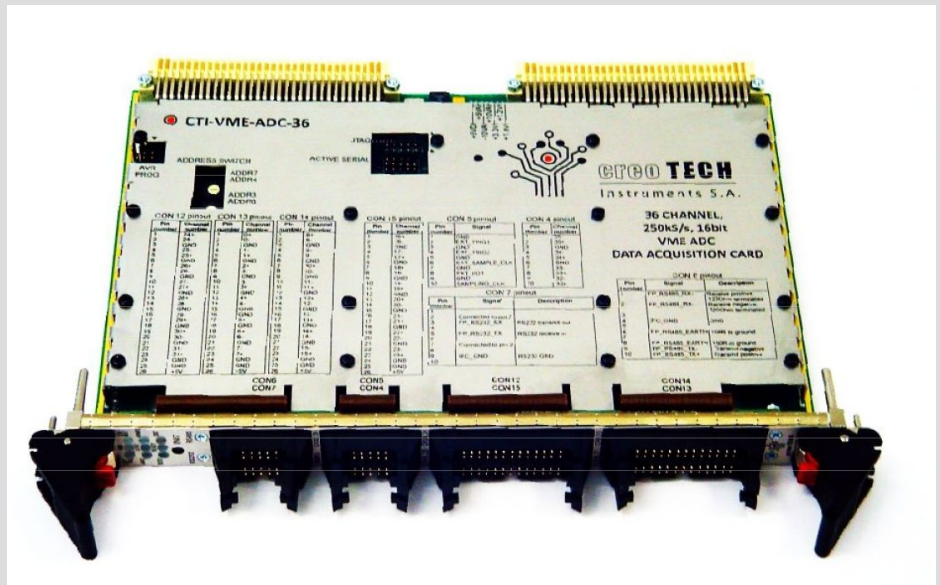
How we started OHWR : SPEC, SVEC, TDC/DTC

- SPEC, SVEC, FMC DEL, FMC DDS, were outsourced by CERN to CTI
- Several hundreds pieces produced by 3 companies
- Used worldwide



VME ADC board

- 36 ADC channels, simultaneously sampling
- 16 bits
- 250kHz
- 64MB of RAM
- MPV901 compatible
- Main application: SEM grids
- OHWR design



**Product developed in close collaboration with CERN,
180 pieces produced**

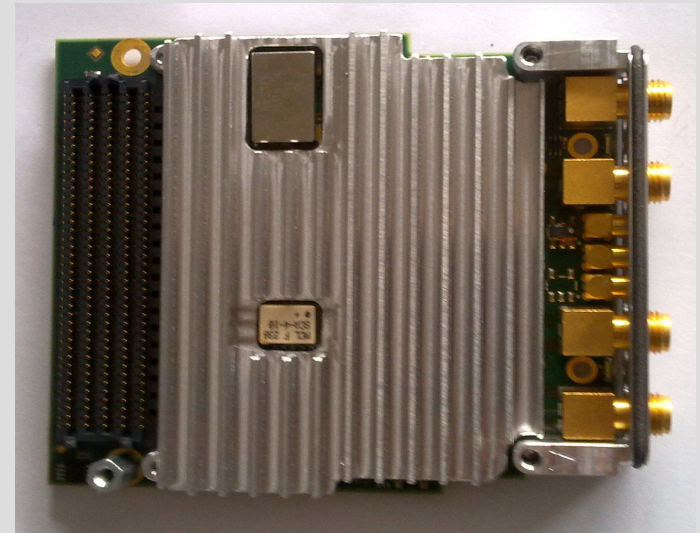
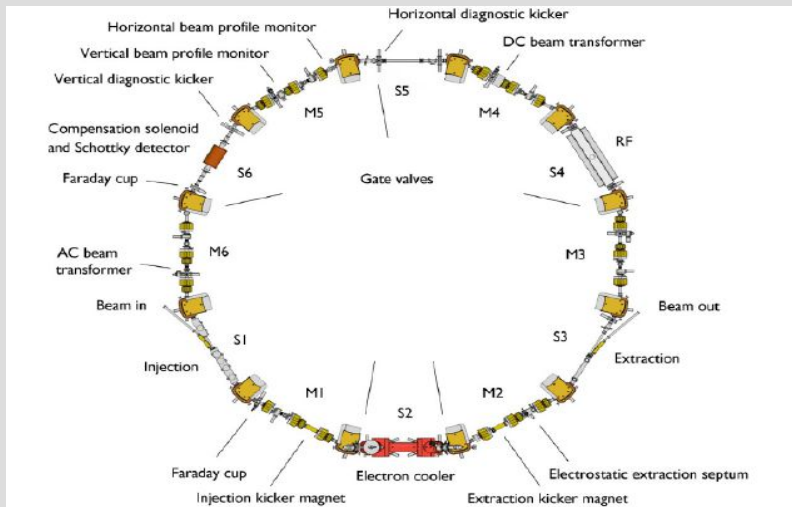
**Application: Linac 4 SEM grid readout, DC transformer DAQ
CERN requested OH licensing in call for tender**

BPM system for Cryring GSI

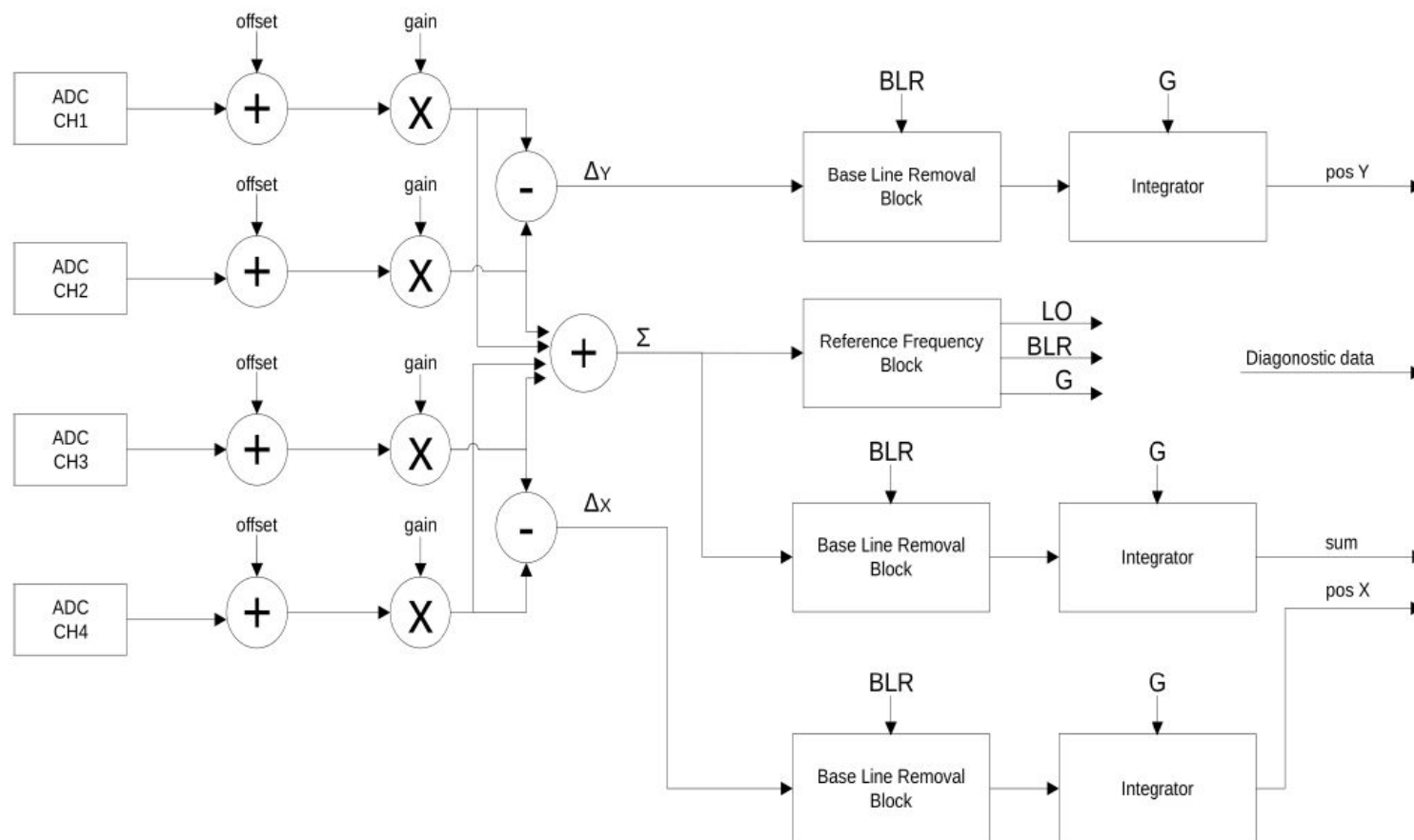
BPM system for Sirius (LNLS)

BPM system for Cryring GSI

- 8 PU units
- Trajectory and orbit measurement
- Adaptive PLL algorithm in FPGA
- uTCA system with custom AMC and ADC
- 5 AMC FMC carriers
- 8 quad channel, 250MHz, 16bit FMC cards
- Sub-ns synchronisation, WR-enabled

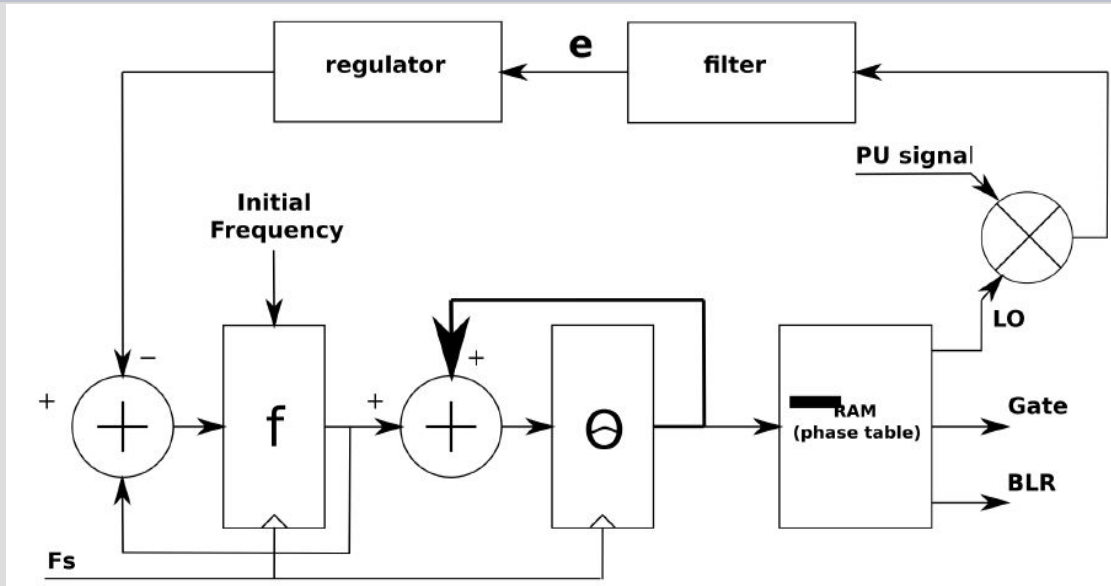


BPM system for Cryring (GSI)

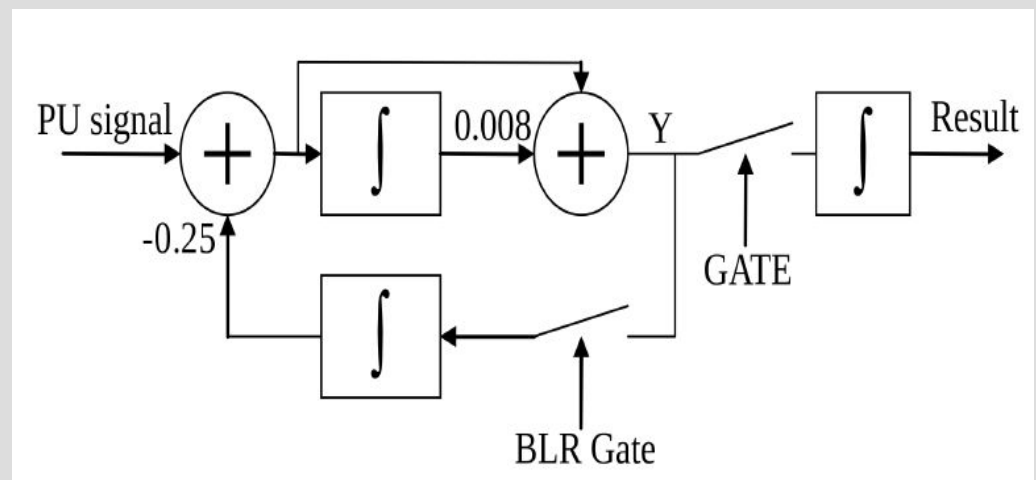


BPM signal processing

BPM system for Cryring (GSI)

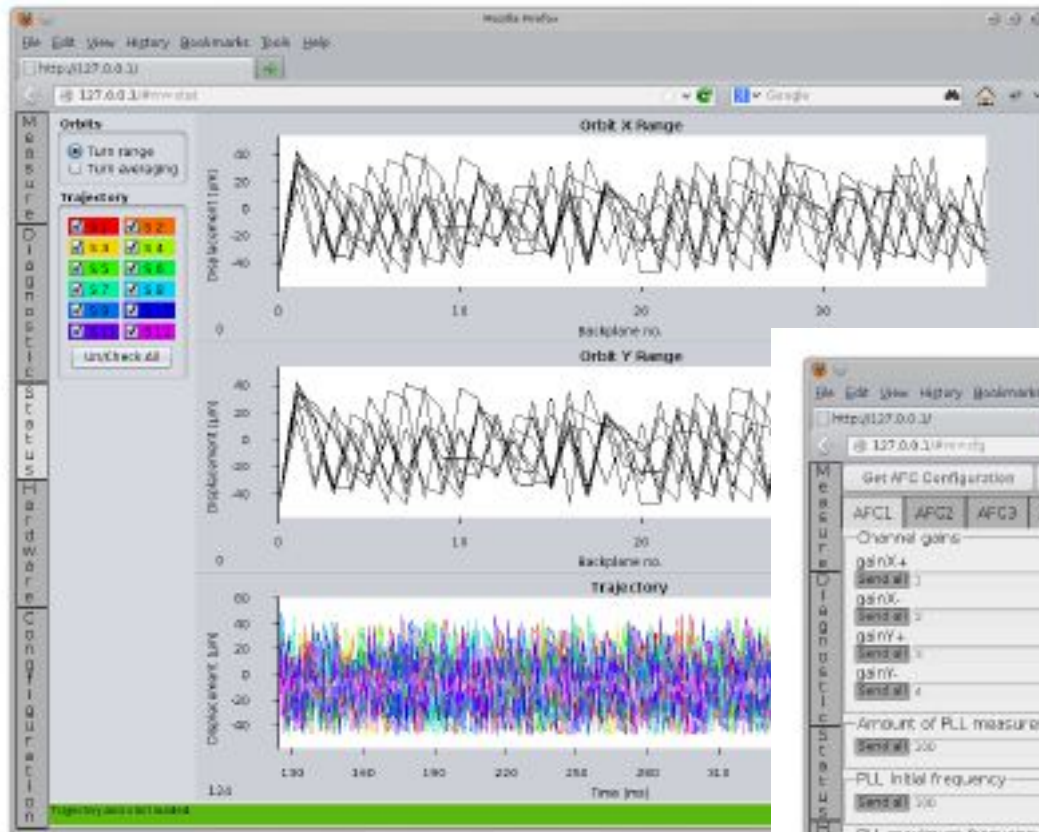


Digital PLL



Baseline removal

BPM system for Cryring (GSI)



Diagnostic web
interface

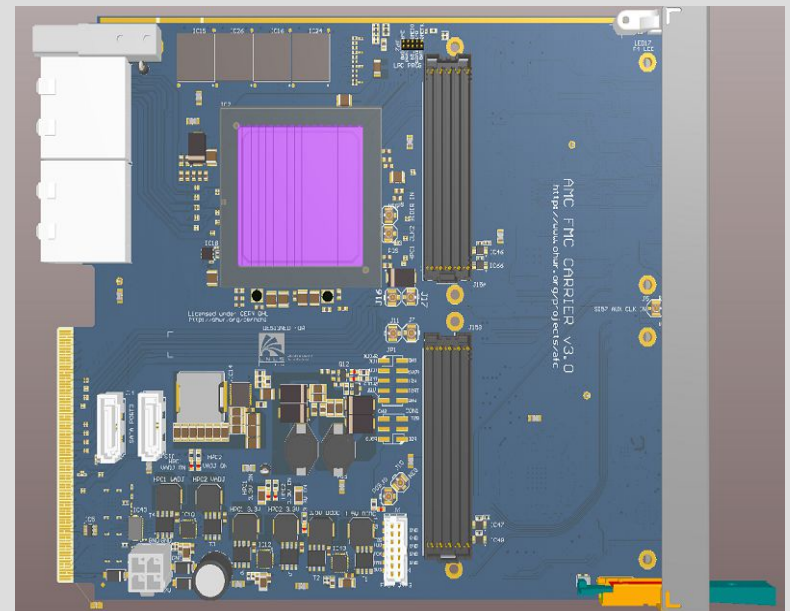
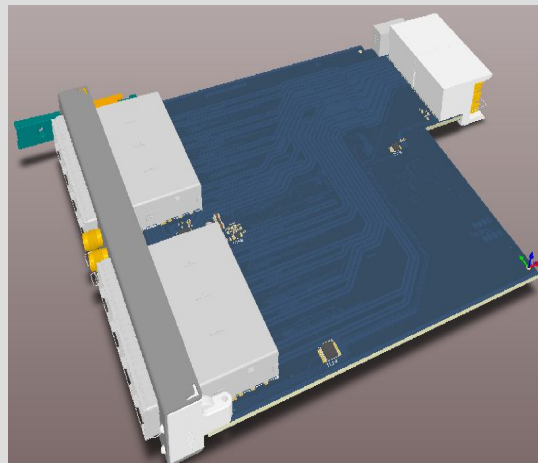
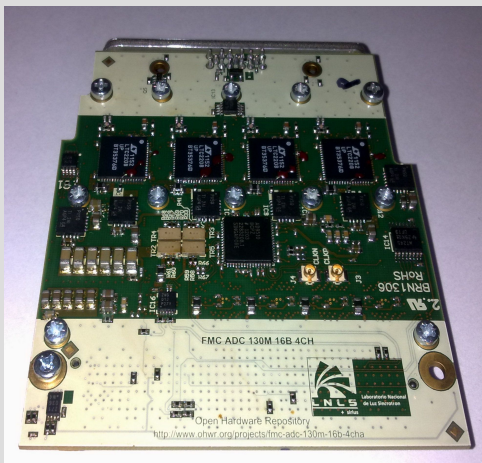
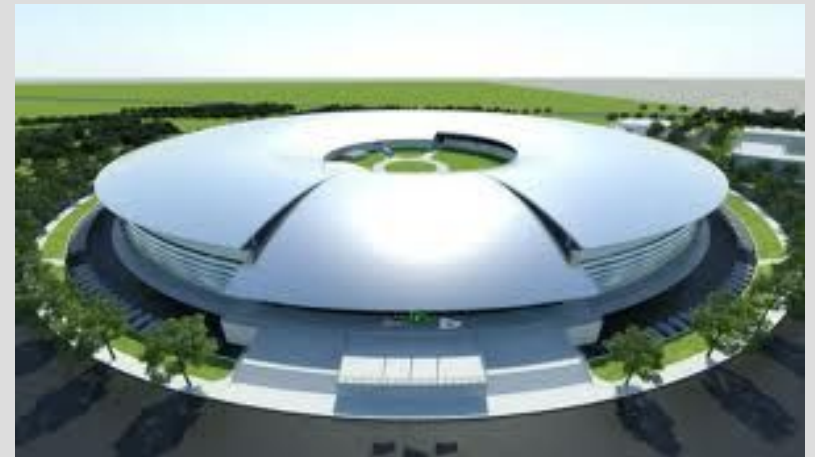
The screenshot displays the configuration web interface of the BPM system. It features a table with 16 columns representing different AFCs (AFC1 to AFC16) and several rows of configuration parameters. The parameters are grouped into sections:

- Channel gains:** Includes parameters like `gainX+`, `gainX-`, `gainY+`, and `gainY-` for each AFC.
- Channel offsets:** Includes parameters like `Offset+`, `Offset-`, `Offset+`, and `Offset-` for each AFC.
- Amount of PLL measures:** Includes parameters like `Send all` and `Send all` for each AFC.
- PLL initial frequency:** Includes parameters like `Send all` and `Send all` for each AFC.
- PLL maximum frequency:** Includes parameters like `Send all` and `Send all` for each AFC.
- Initial phase:** Includes parameters like `Send all` and `Send all` for each AFC.
- BLR length/BLR stop:** Includes parameters like `Send all` and `Send all` for each AFC.
- Gate position:** Includes parameters like `Send all` and `Send all` for each AFC.
- Length control/Position control:** Includes parameters like `Send all` and `Send all` for each AFC.

At the bottom, there is a 'Configuration saved' status bar.

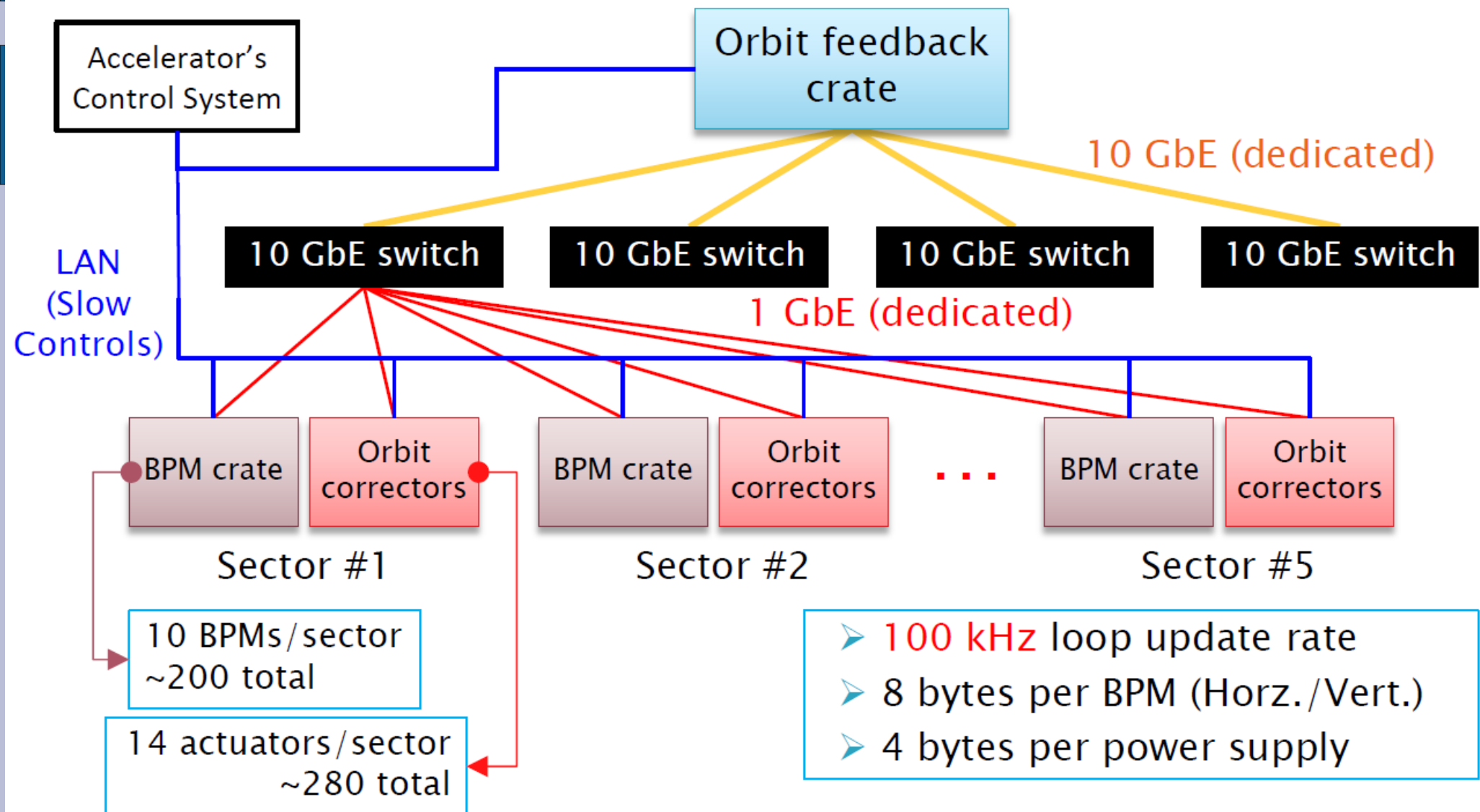
BPM system for Sirius (LNLS)

- 3Gev 3-rd gen light source
- 520m circumference
- 160 BPM units (640 ADC channels)
- Custom, quad channel 130Mhz, 16bit FMC cards
- AMC FMC with RTM SFP
- Sub-sampling of 500 MHz RF
- On-line processing



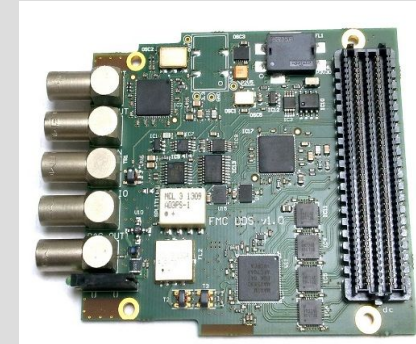
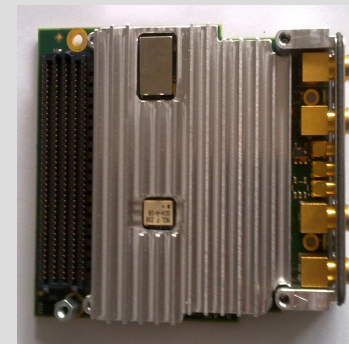
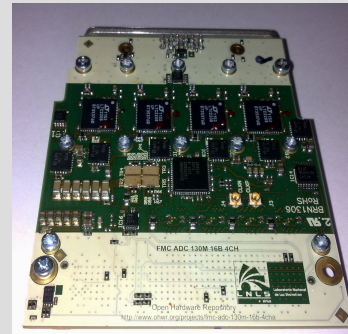
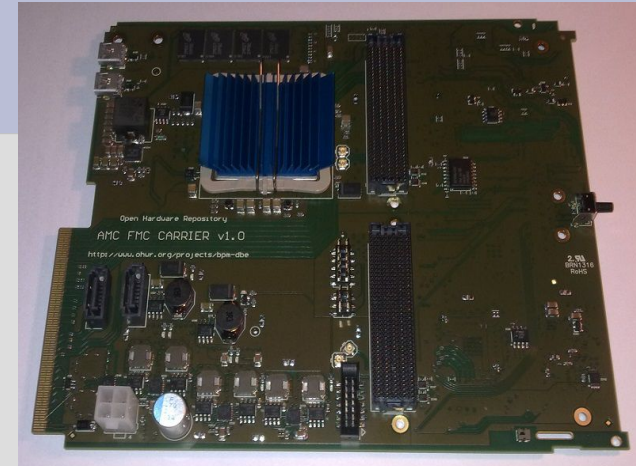
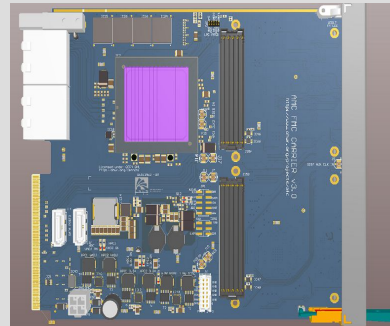
BPM system for Sirius (LNLS)

► Storage Ring orbit feedback – interfaces (planning)



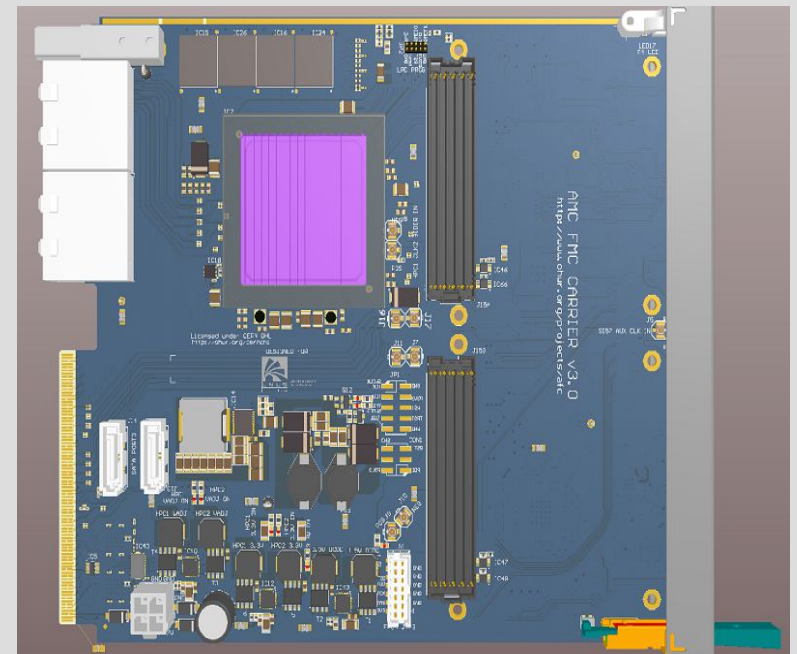
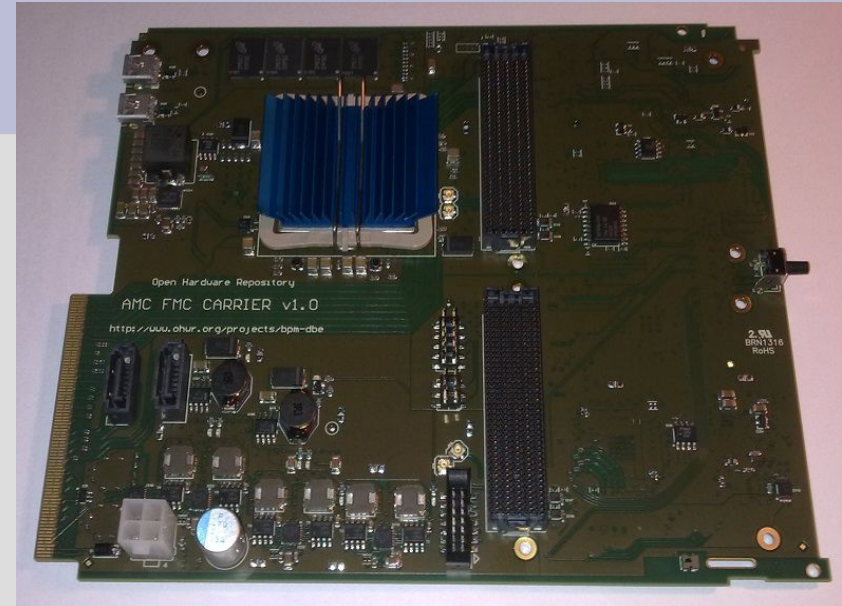
MTCA.4 development at CTI and WUT (OHWR)

- AMC FMC v2 (Artix 7)
 - AMC FMC v3 (Artix 7) with RTM
 - AMC FMC with Kintex 7 FPGA *
 - AMC QSFP *
 - AMC CPU
 - RTM SFP
 - AMC DSP
 - WR MCH + CPU *
- + several compatible CTI OH FMC extensions
- FMC ADC 100M 14b 4CHA
 - FMC ADC 125M 12b 16cha
 - FMC ADC 130M 16B 4cha
 - FMC ADC 250M 16B 4cha
 - FMC TDC/DTC
 - FMC DEL 4cha 1ns
 - FMC fast DIO 5
 - FMC DIO32
 - FMC HV +/- 8kV *
 - FMC SENS 12cha *
 - FMC DDS (WR-RF)
 - FMC ADC 125M 14b DAC 600M 16b
- * during development



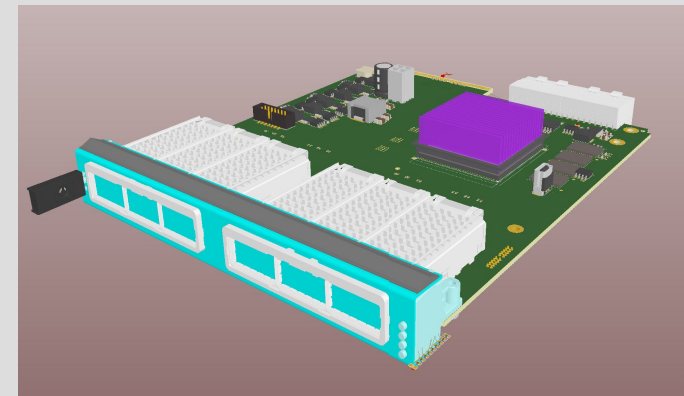
AMC FMC board

- 7-series FPGA, Artix 200T
 - **Kintex 7** version available soon
 - Dual HPC FMC
 - Clock crossbar
 - 4Gbit SDRAM
 - 2x 256Mbit FLASH
 - Custom NXP MMC
 - SCANSTA JTAG switch
-
- Version 3 with RTM
 - Used for GSI TMS, LNLS Sirius and others
 - Custom MMC working with Vadatech MCH



AMC FPGA QSFP board (CBM)

- Kintex 7 FPGA (XC7K420T or XC7K480T), 32 GTX, 760 LC, 34,380 Kb RAM, PCIe Gen 2 core,
- 6 **QSFP**, 24 x10Gbit/s optical links per board
- RTM for additional optical transceivers
- clock distribution circuit with crosspoint switch, VCXO, WR clock recovery
- QDR RAM, 800MHz, 3 individual controllers
- configuration FLASH. Update via JTAG from MCH2
- 1x GTX (Port0) for Ethernet (MCH1)
- 1x GTX (Port1) for WR (MCH2)
- 4xGTX (FP1) PCIe from MCH1
- 4xGTX (FP2) crossbar from MCH2
- 24xGTX 6xQSFP
- Stand-alone operation possible
- Coming soon



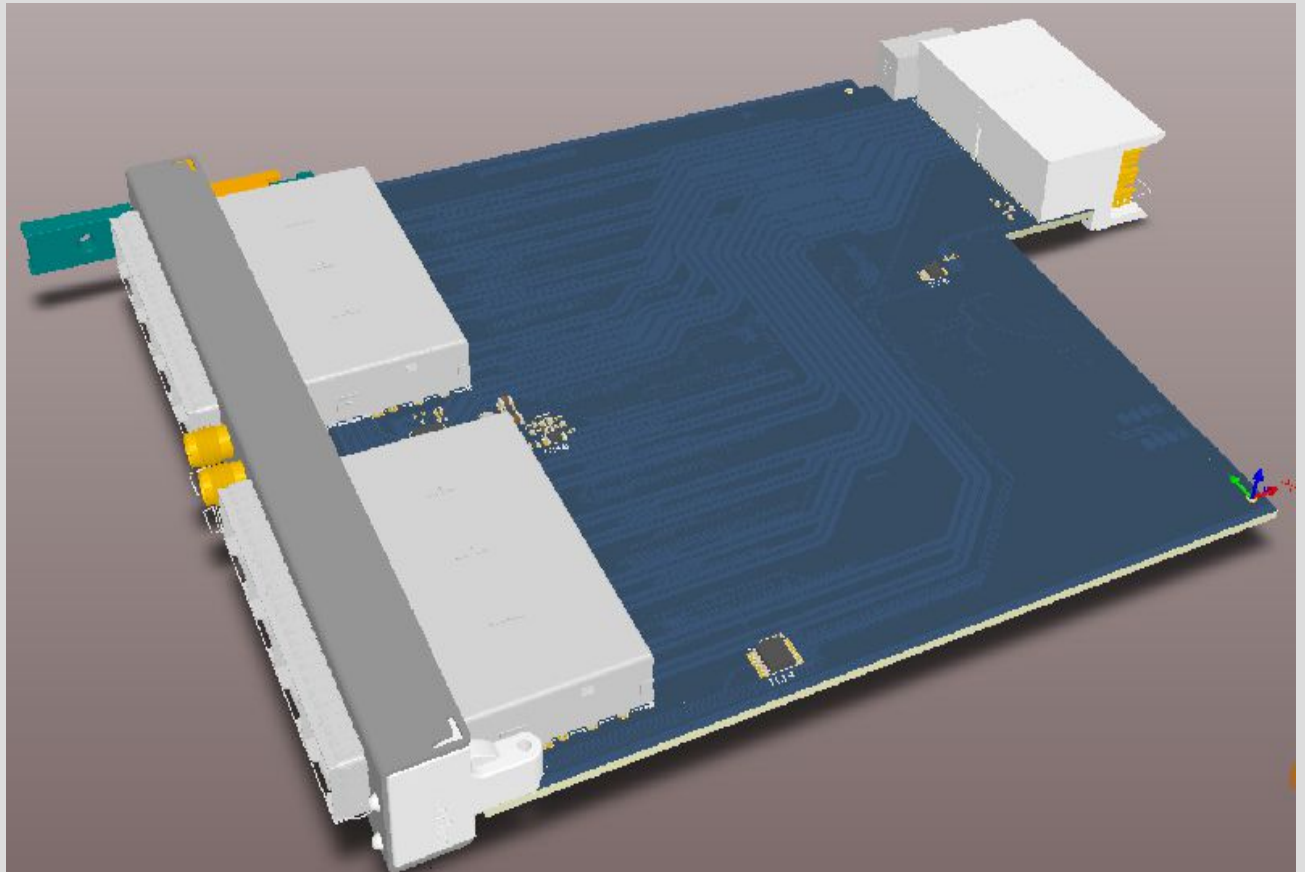
AMC-CPU-COM EXPRESS 6

- Troubles with Concurrent i7 CPU and Vadatech crate interoperability
- Own AMC-CPU designed.
- No more troubles with IPMI
- Recent I5 & I7 cores
- Supports SSC, FP1, FP2
- Gen 3 PCIe
- FPGA extension module
- Plenty of IO, USB, eSATA, VGA
- mPCIe (WiFi, 3G modem)/ mSATA
- 2 gigabit ports with P0, P1 support
- Low cost, i5 CPU < 2k EUR



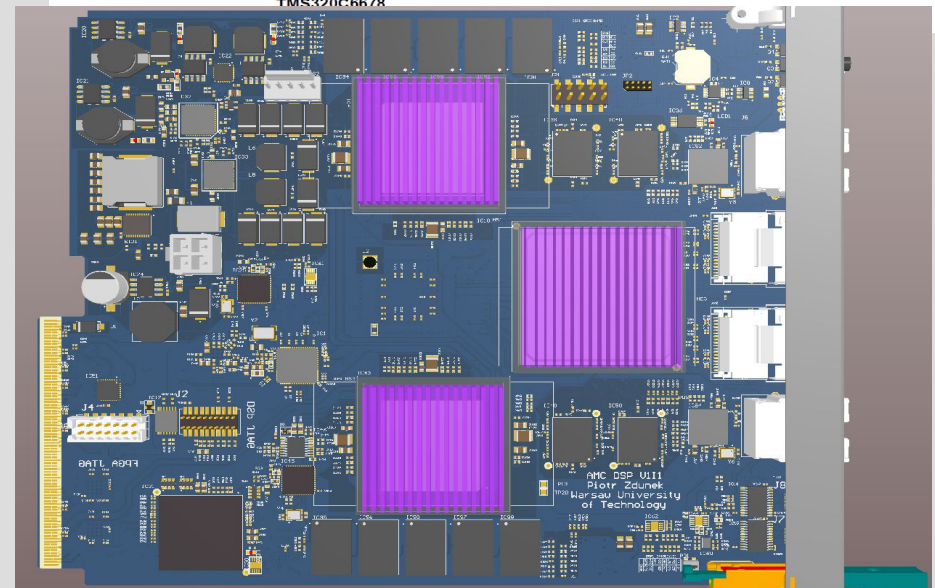
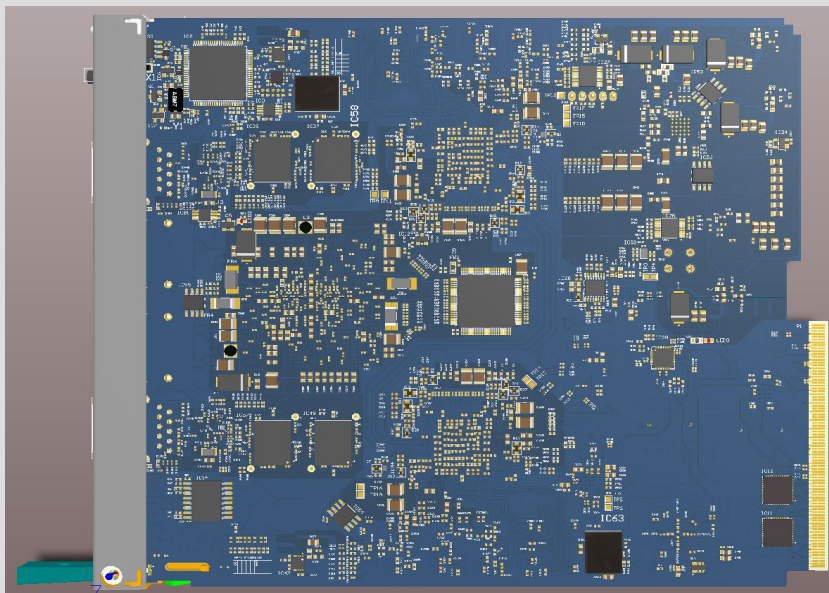
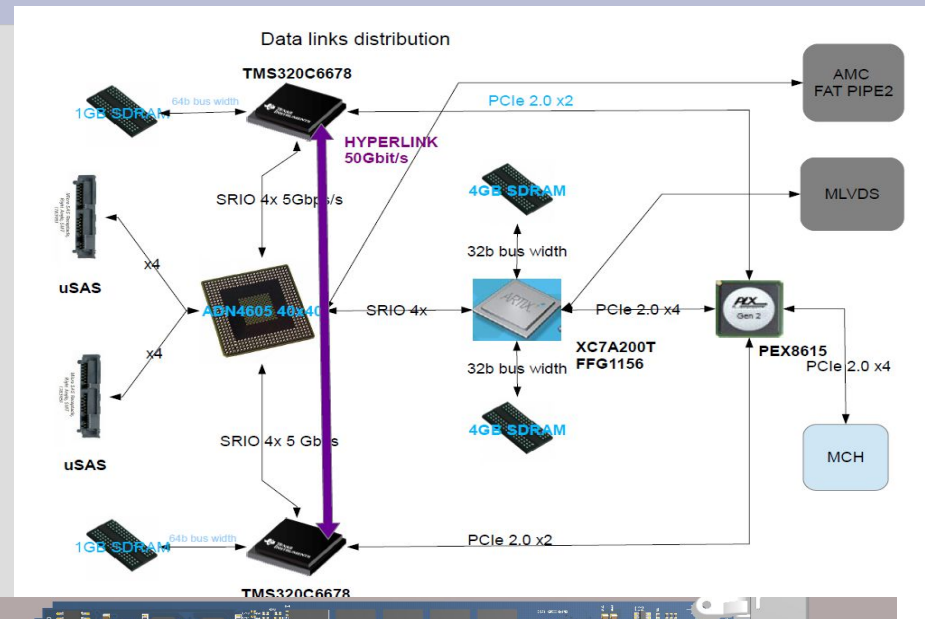
RTM-SFP+8

- Compatible with:
- AMC-FMC v3
- AMC-FMC Kintex
- WR-MCH
- Prototype stage



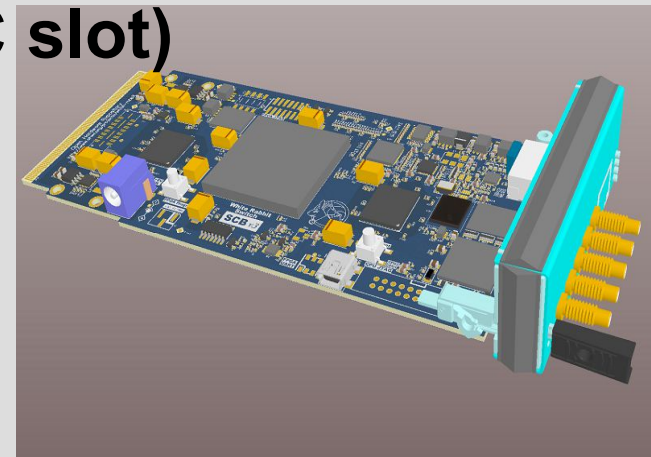
AMC DSP accelerator – 16 cores with flexible crosspoint switch

- 16 TI DSP cores
- Artix FPGA
- Crossbar switch
- 2x 20Gbit quad lane mSAS connectors
- 2x Gigabit Ethernet
- Designed for GEM detector signal processing
- Prototype stage

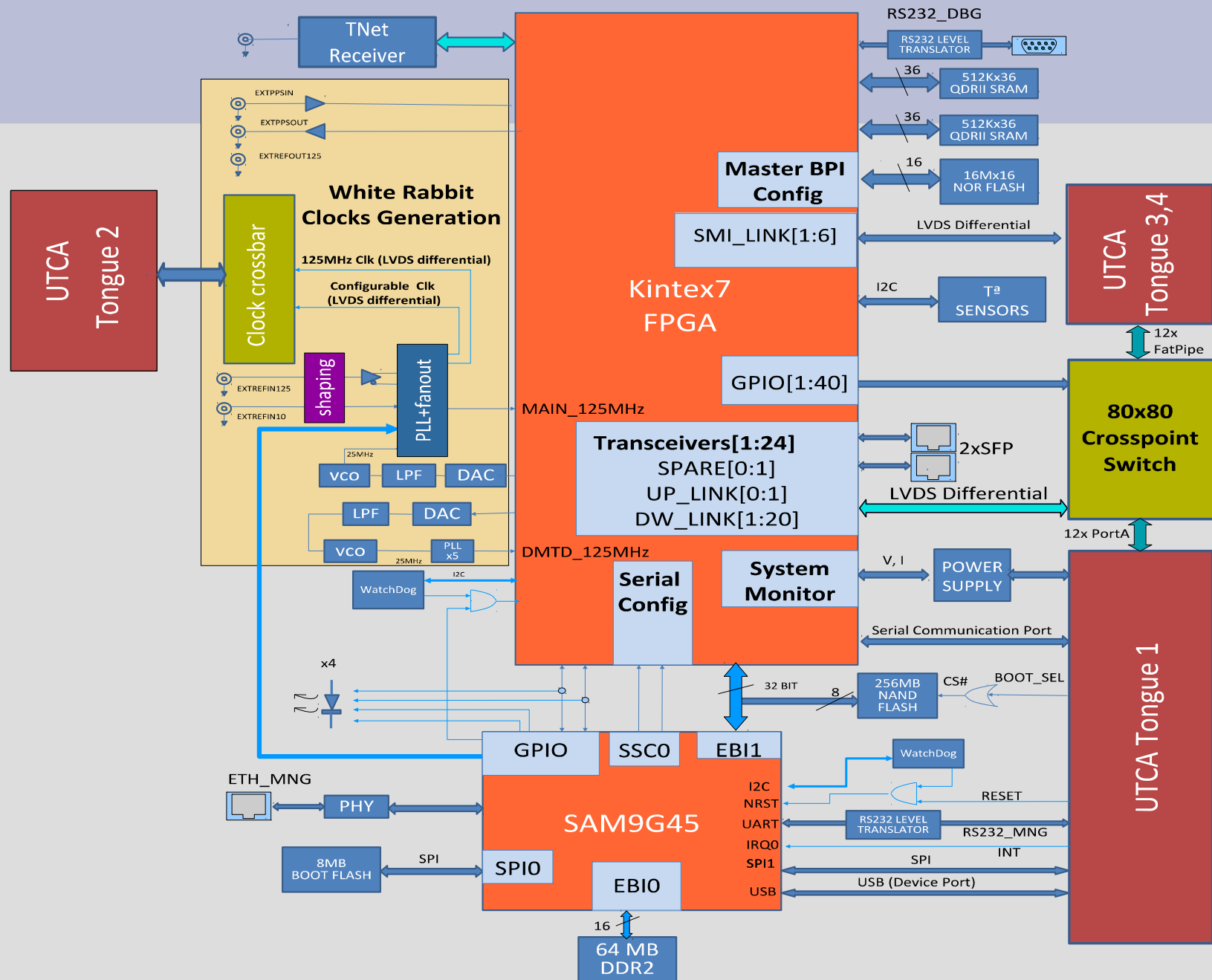


MCH WR timing receiver/switch

- **Modified standard 18 port WR switch from OHWR**
- Additional 4.25Gbit Crosspoint Switch (crossbar)
- **Sub-ns accuracy (~20ps) over 1Gbit fiber**
- **Low jitter clock distribution based on crossbar with WR-RF synthesizer and PLL**
- Dedicated timing receiver connector
- IPMI based on Linux CPU
- **JTAG access to JSM (via USB-IP) with Xilinx/Altera support**
- **Optional RTM for CPU (saves one AMC slot)**
- **GenIII PCIe or crossbar switch options**
- Can be used as basic or redundant MCH
- Under development



MCH WR timing receiver/switch



Join Open Hardware community

