IOxOS Technologies SA

MTCA.4 Product Line

IFC_1410 - RTM_1411

Company Overview

IOxOS Technologies is an electronic design company founded in 2007 in the Geneva area (Switzerland)

Offers innovative solutions to system integrators in:

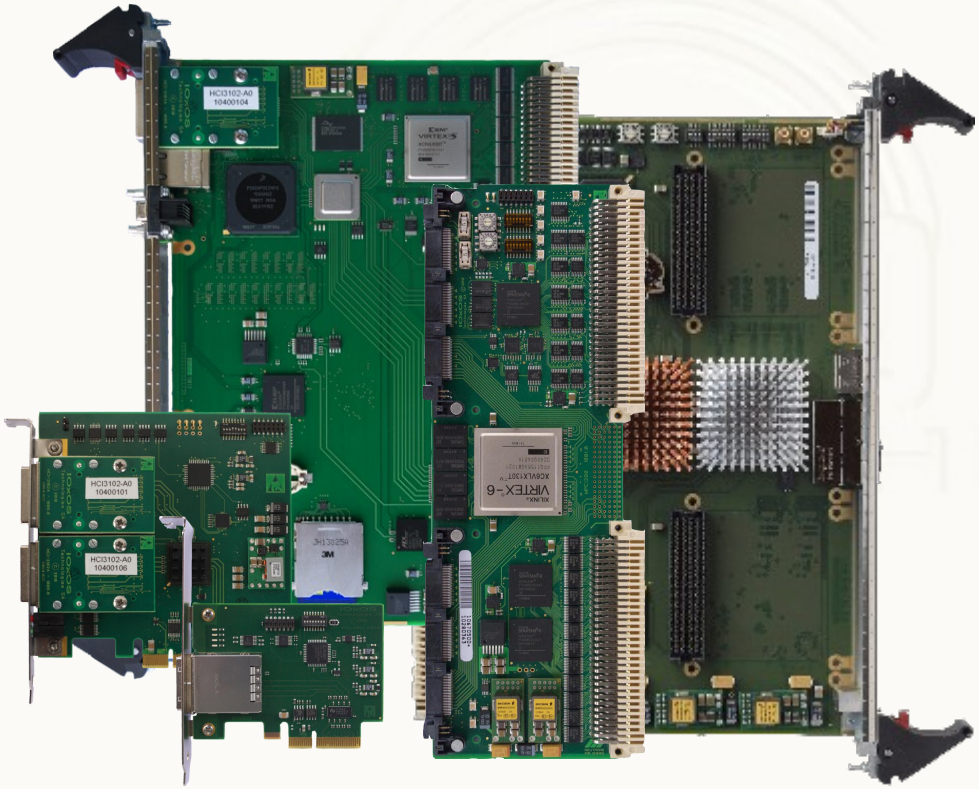
- Physics
- Energy
- Aerospace

Combines a comprehensive product line with engineering, consulting and training services

Fields of competence ranging from System level down to IP Core development

IOxOS Technologies headquarters in Gland (Geneva area)

Fields of Competence



- PCI Express based COTS solutions (Single Board Computers PowerPC/x86, IO Interfaces, Mezzanines Modules) in the most popular industry form factors such as VME64x, VXI, PMC, XMC and FMC among others
- FPGA Design, combining IOxOS Technologies own IP Core library with high-performance FPGA Design Kits based on Network on Chip (NoC) architecture
- Analog front-end ADC/DAC in VITA57 FMC form factor
- Software support and Device Drivers compatible on LINUX, VxWorks and Windows

IFC_1210 – P2020 SBC

6U VME64x Single Board Computer

Freescale PowerPC P2020 computing core (Long term availability)

Dual VITA 42.3 XMC / Single PMC slots

Dual VITA 57 HPC FMC slots

UHM P0 Extension (7 Gbps) PCI Express GEN2 Interconnect

Based on Xilinx Virtex-6T FPGA with user's area for custom applications

Fully configurable (SW + FPGA) over the network

Applications:

Accelerator control, Instrument controls

- PSI Swiss FEL Common Platform
- ILL, Grenoble
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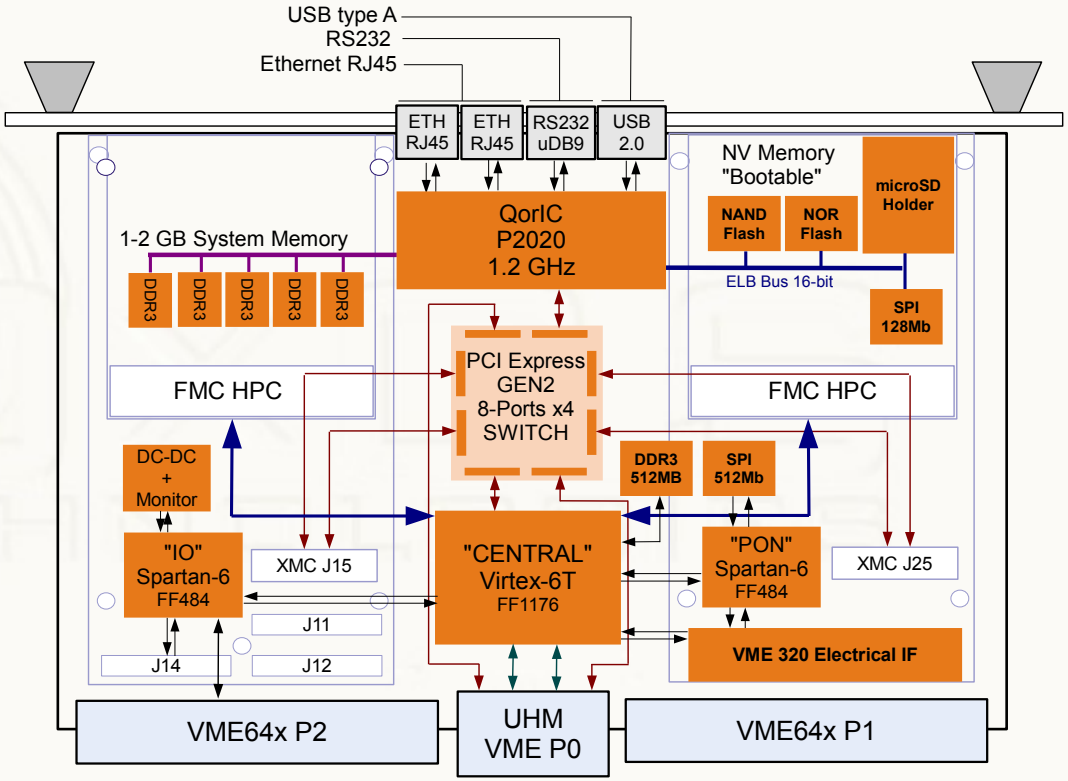
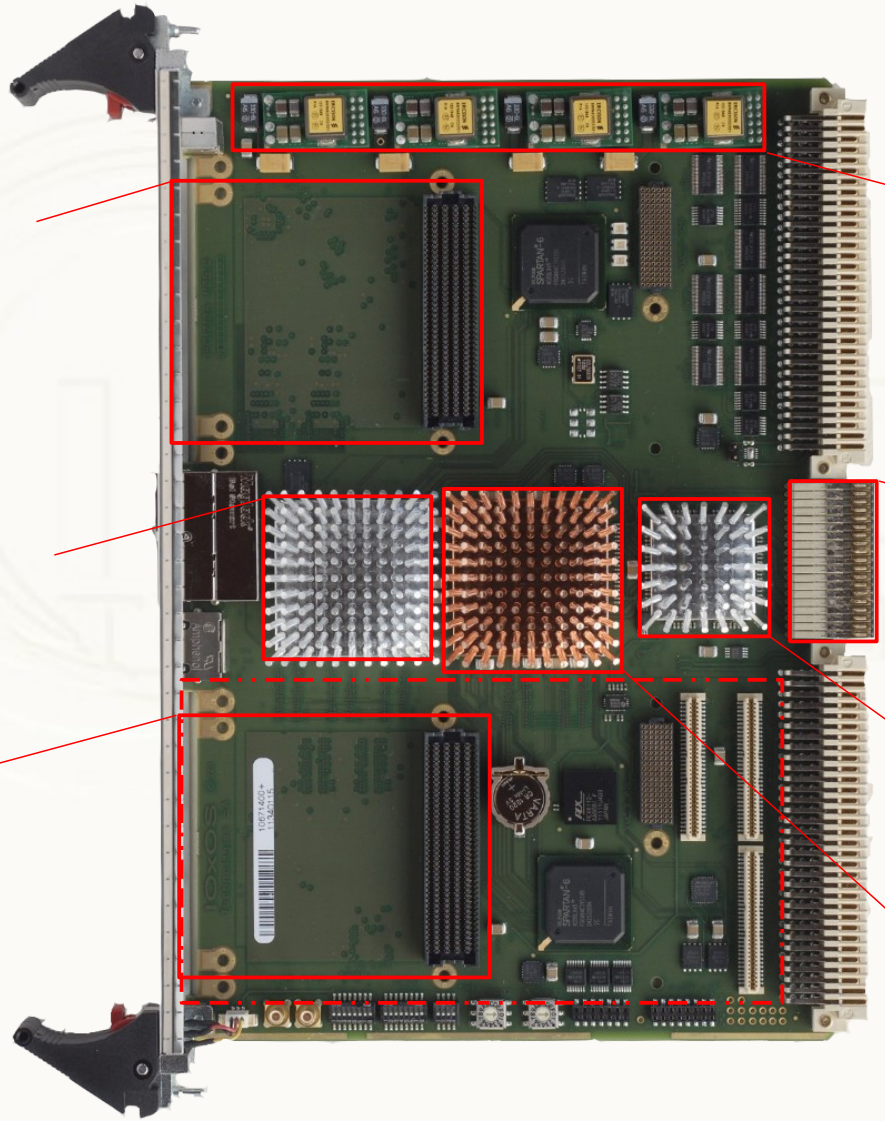


IFC_1210 Key Features



VITA57 FMC #1
High Pin Count
GND Shield on top side
(Noise / Cooling)

PowerPC P2020
2 GETH
1 RS232
1 USB

VITA57 FMC #2
High Pin Count
GND Shield on top side
(Noise / Cooling)

Power supplies
PM Bus Management
multi phase control

PCIe GEN2 Interface
1/2/4/8 Ports
8 Lanes
2 NT Ports

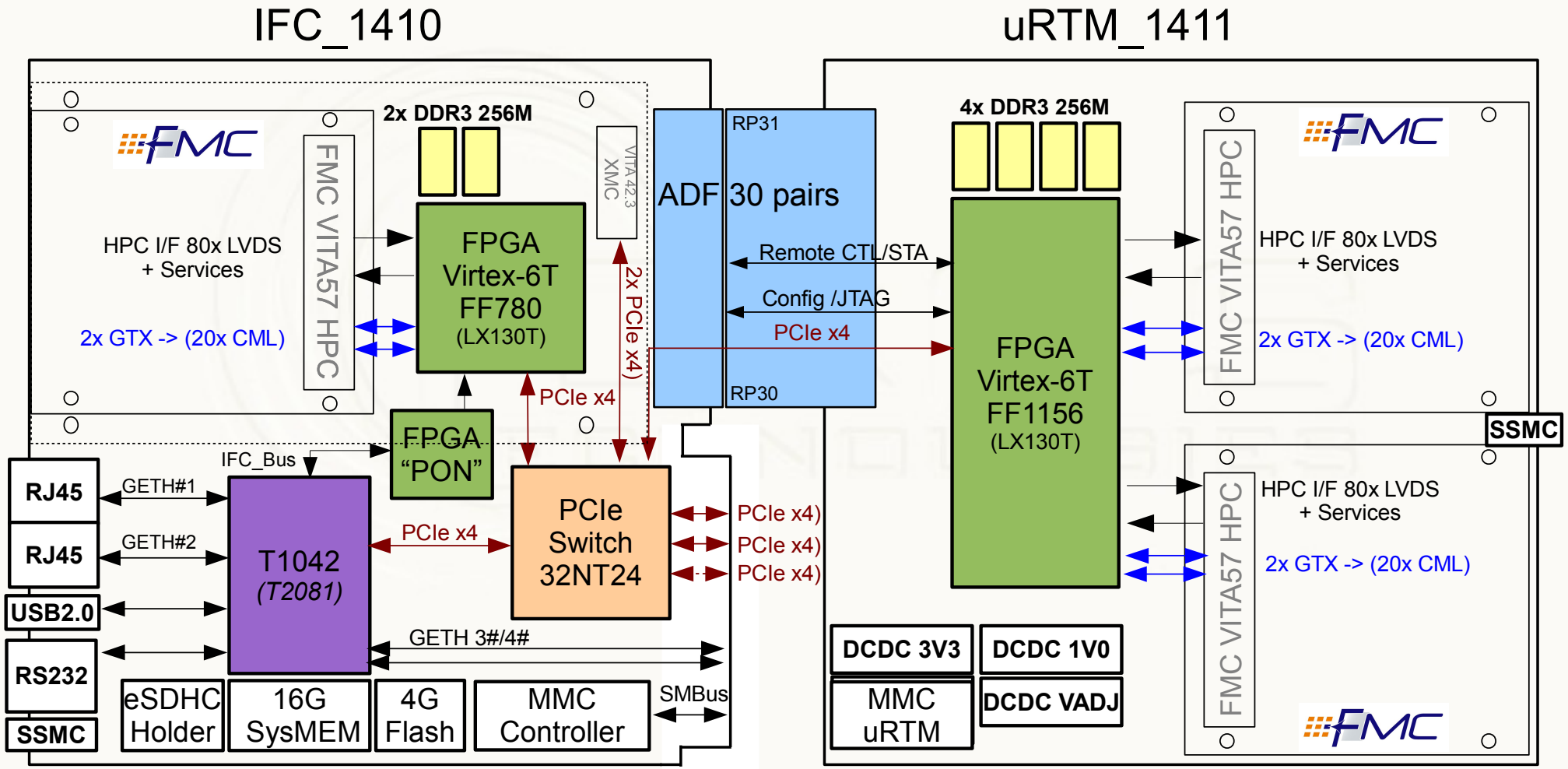
PCIe GEN2 Switch
24 Ports
32 Lanes

Virtex-6T FPGA LX130/LX240T
Dual FMC HPC I/F
512M DDR3
PCIe GEN2 EP

MTCA.4 PRODUCT LINE

Introduction

- New product Line based on existing /deployed COTS
  - → IFC_1210 Form factor re-fitting
- Proven Expertise
  - FREESCALE QorIQ PowerPC family T2081/T1042
  - Software and Application UBOOT, LINUX, VxWorks, XprsMON, EPICS
  - PCI Express GEN2 Switched Architecture, FPGA End Point with NT(Non Transparent) and DMA Support
  - FMC VITA57.1 with Virtex-6T FPGA based interface (TOSCA II)
- What's really NEW
  - MTCA.4 form factor
    - Engineering experience on AMC units
  - MMC IPMI control
    - Engineering experience on AMC units
    - Use of TBD COTS related micro-controller



Advantage solutions

- Leverage on actual VME64X IFC_1210
  - Off the shelf turn-key solution (Minimal engineering effort. 100% SW/FW/HW compatibility
  - Proven environment (already used/deployed in several different application cases)
  - Several Year/Engineer SW (EPICS/LINUX,
  - Several Year/Engineer FW FPGA (PCIe DMA, FMC support
- Configurable through Ethernet
  - NFS Boot LINUX + Application
  - FPGA configuration bit-stream
- OPEN environment
  - All SW/FW/HW sources available
  - VHDL RTL Simulation environment with Bus Functional Model (BFM)
- Local Processing Support
  - PowerPC multi-core QorIQ T Serie 28nm
  - Optimal Power/Performance ratio
  - ALTIVEC support for efficient DSP
  - Long term availability (> 10 years)
  - UBOOT extensions (FPGA configuration from network)
- Local PCI Express Switch
  - GEN2 Low latency, Multi Partition, DMA, NTB Port, Multicast, Clock domain isolation
  - Allows to built local/isolated PCI Express network
  - NT Port (Non Transparent) connection to MTCA PCI Express
  - Private board-to-board PCI Express link (AMC Port 12-15)

AMC Ports Assignment

AMC Port	Functions	IFC_1410
0-1	Ethernet 1G	Direct connection to T2081/T1042
2-3	SATA	Not Supported
4-7	PCIe GEN2 x4	PCIe Switch Port_N (EP or NT) → MCH#A
8-11	PCIe GEN2 x4	PCIe Switch Port_K (EP or NT) → MCH#B
12-15	4x Point to point connections	**PCIe Switch Port_L (Upstream, EP , NT)** • 4x PCIe GEN2 x1
16	TCLKC, TCLKD	Clock infrastructure Dispatcher
17-20	Trigger, Interlock	MTCA Clock Controller. Wired to Virtex 6T FPGA of IFC_1410 and RTM_1411
Clk_1		Clock Infrastructure Dispatcher
Clk_2		Clock Infrastructure Dispatcher
Clk_3		PCIe Clock (Rx CML)

TOSCA II FPGA Design Environment

TOSCA II FDK

FPGA Design Kit for the development of high-end applications based on Xilinx Virtex-6T device

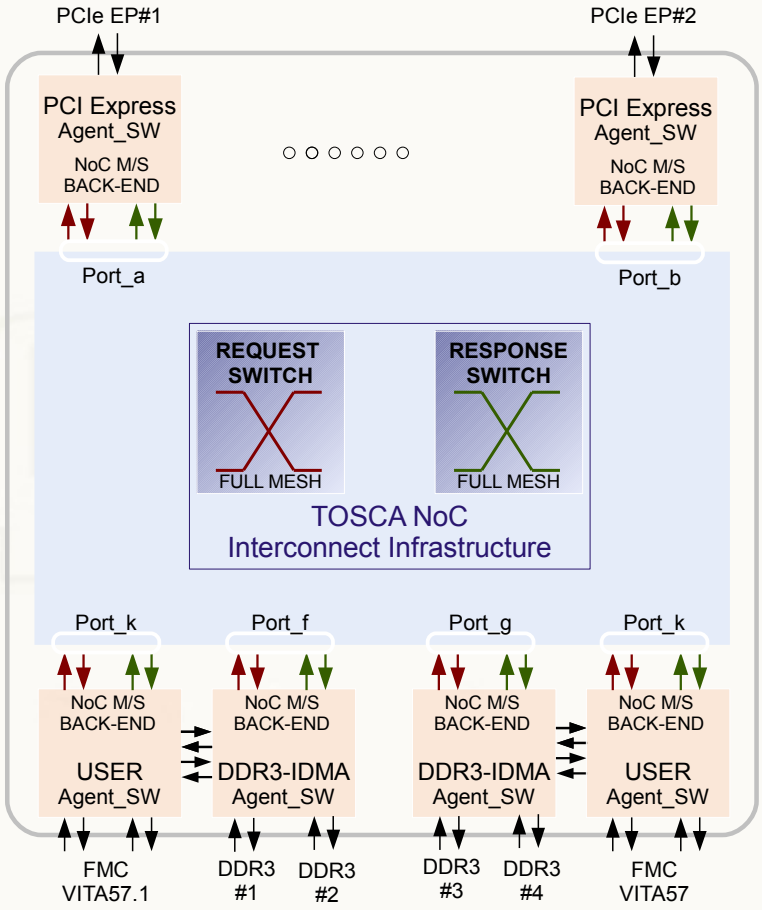
Network on Chip (NoC) solution based on a full-mesh non-blocking switch

VHDL source code fully available

Full support provided at Hardware, Firmware and Software levels

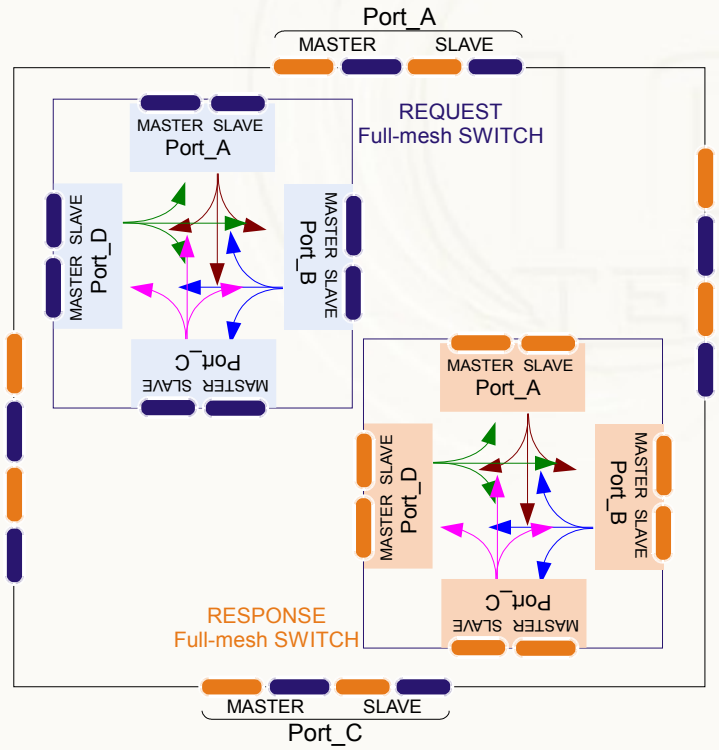
Drastically reduces development time, focusing on the user application:

- Access to IOxOS IP Core library
- User-area dedicated simulation environment
- Delivered with reference designs
- Software support at LINUX and EPICS Level



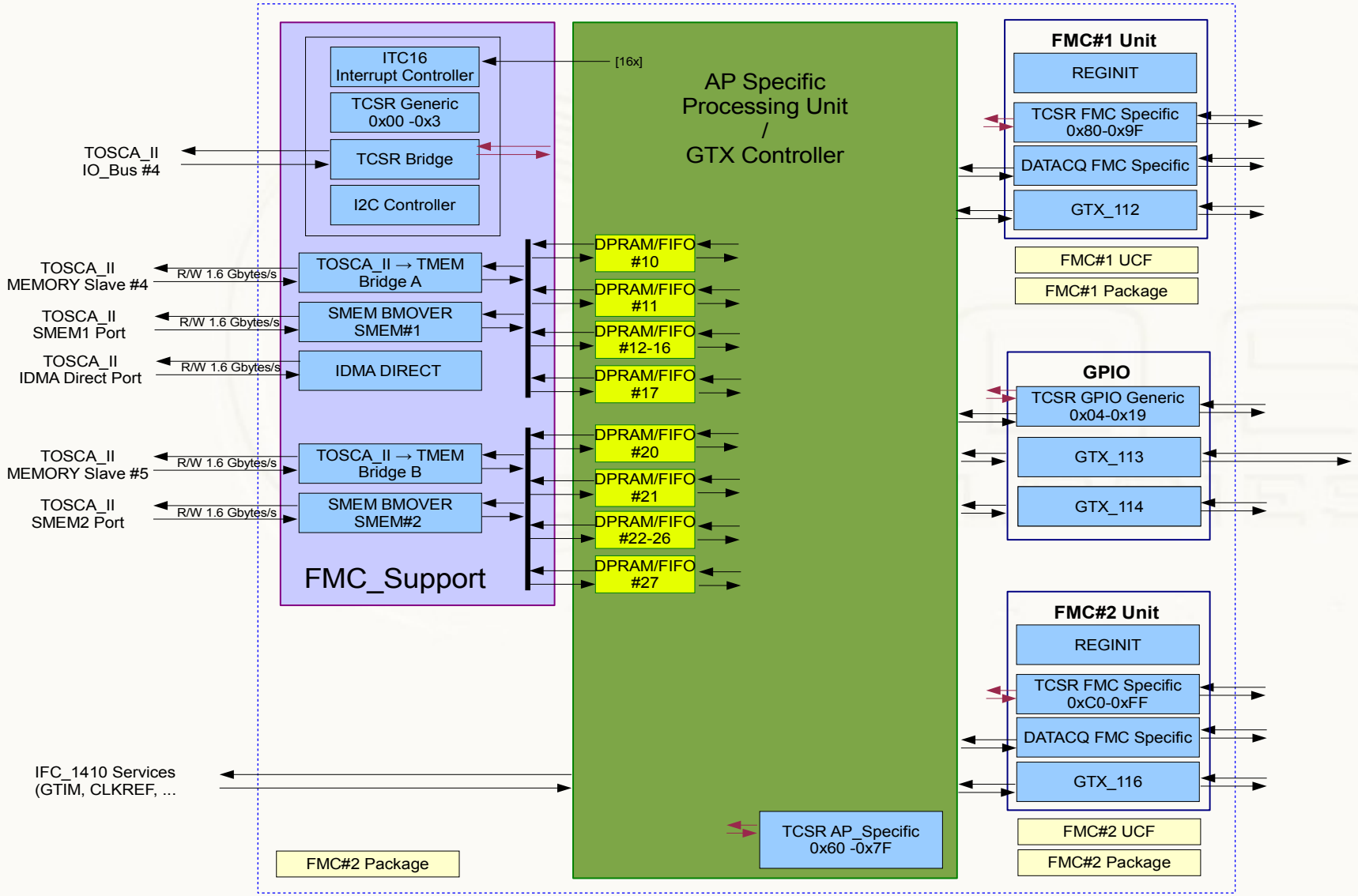
Non Blocking Transactions

- NoC Central Switched
  - Dual layers full mesh SWITCH
    - WRITE Transactions
    - READ Transactions



- TOSCA II NoC Transactions
  - Optimized for XILINX Virtex-6T FPGA
    - INgress/OUTgress DPRAM Buffering
    - Embedded Time Domain Isolation
    - Switch operating at 200 or 250 MHz
    - 64-bit Data paths
  - PCI Express TLI packet format
  - Six(6) Port Implementation
    - PCIe EP #1
    - PCIe EP #2 (optional)
    - SMEM 12 Dual DDR3 with IDMA Controller
    - SMEM 23 Dual DDR3 with IDMA Controller
    - USER1 → XUSER FMC #1 Controller
    - USER2 → XUSER FMC #2 Controller
  - Infrastructure routing ready for up to Eight(8) Ports

XUSER Block



IOxOS FMC VITA57.1 ADC/DAC

IOxOS FMC VITA57.1 Mezzanines

- ADC_3110 Octal 16-bit 250 Msps ADC
  - AC coupled +/- 1.0[V]
  - TI ADS42LB69 ADC
  - External Clock Reference
  - On-board Ultra low noise 100 MHz oscillator
  - TI LMK04906 clock distribution
    - Dual PLL
    - Very low noise jitter (<100[fs])
  - Complete FPGA Design Kit
    - Generic VHDL Source code (XILINX)
    - Fully integrated in TOSCA II + EPICS
  - Ten(10) SSMC Coaxial Connectors
- ADC_3111 Octal 16-bit 250 Msps ADC
  - DC coupled +/- 0.5[V]
  - TI ADS42LB69 ADC
  - External Clock Reference
  - On-board Ultra low noise 100 MHz oscillator
  - TI LMK04906 clock distribution
    - Dual PLL
    - Very low noise jitter (<100[fs])
  - Complete FPGA Design Kit
    - Generic VHDL Source code (XILINX)
    - Fully integrated in TOSCA II + EPICS
  - Ten(10) SSMC Coaxial Connectors

IOxOS FMC VITA57.1 Mezzanines

- ADC_3112 GSPS Quad 12-bit ADC
  - TI/NS ADC Dual Channel 12-bit Gs/s range
    - ADS*5409*
  - Differential DC coupling Inputs
  - High Precision Trigger Input with 10 [ps] time tagging resolution
  - TI LMK04906 clock distribution
    - Dual PLL
    - Very low noise jitter (<100[fs])
- Complete FPGA Design Kit
    - Generic VHDL Source code (XILINX)
    - Fully integrated in TOSCA II + EPICS
  - Ten(10) SSMC Coaxial Connectors

- ADC_3113 Dual DAC + Dual ADC
  - Dual 16-bit DAC up to 500 MHz
    - Low latency AD9783 DAC controller
    - 6th order output filter
    - Programmable Offset Compensation
  - Dual ADC 16-bit 250 Msps DC coupled
    - Differential inputs DC coupled
  - TI LMK04906 clock distribution
    - Very low noise jitter (<100[fs])Dual PLL
  - Complete FPGA Design Kit
    - Generic VHDL Source code (XILINX)
    - Fully integrated in TOSCA II + EPICS
  - Six(1) SSMC Coaxial Connectors
  - One(e) eSATA II Connector for differential DAC output

PRODUCT Availability

Product Availability

- IFC_1410 / RTM_1411
  - Pre-Serial Q2-Q3/2014 - Production Q1/2015
- FMC ADC_3110/3111 (AC/DC 8 channels 16-bit 250Msps)
  - Production Q1/2014 (Now)
- FMC ADC_3112 (4 channels 12-bit 1Gsps range)
  - Pre-Serial Q1/2014 - Production Q2/2014
- FMC DAC_3113 (2 channels 16-bit DAC + 2 channels 16-bit ADC)
  - Production Q1/2014
- MTCA IFC_1410/RTM_1411 Starter Kit (turn-key system)
  - IFC_1410 + RTM_1411 + 1x ADC_3110/3111
  - TOSCA II VHDL source files
  - UBOOT + LINUX + XprsMON
  - Q2-Q3/2014