Diagnostics Use Case Examples in different form factors - MTCA.4, ATCA and PXIe

Stefan Simrock, ITER

Outline

- ITER Control System Overview
- Instrumentation Needs
- Fast Controller Standards
- Diagnostics Use Case Examples
- Needs from Industry

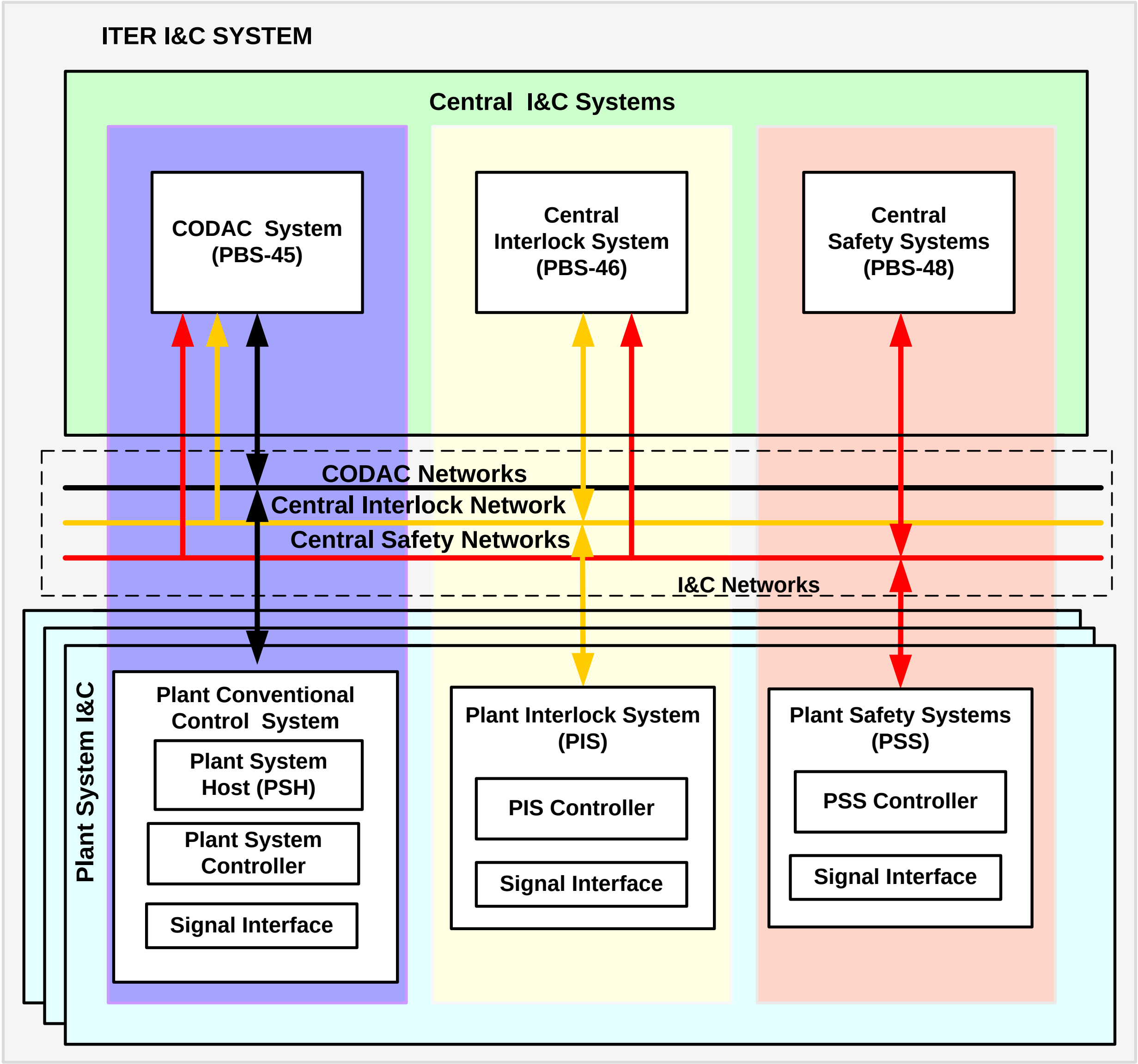
ITER

- **The objective of the ITER project is to demonstrate the feasibility of commercial production of fusion energy**
- **ITER is based on magnetic confinement of the plasma using a "Tokamak" as opposed to inertial confinement**
- **ITER is an international project with seven members (China, Europe, India, Japan, Korea, Russia and USA)**
- **ITER is based on IN-KIND procurement arrangements, where the members mainly provide systems/components, not money**


ITER construction site, France, Aug 30, 2013

ITER Control System Overview

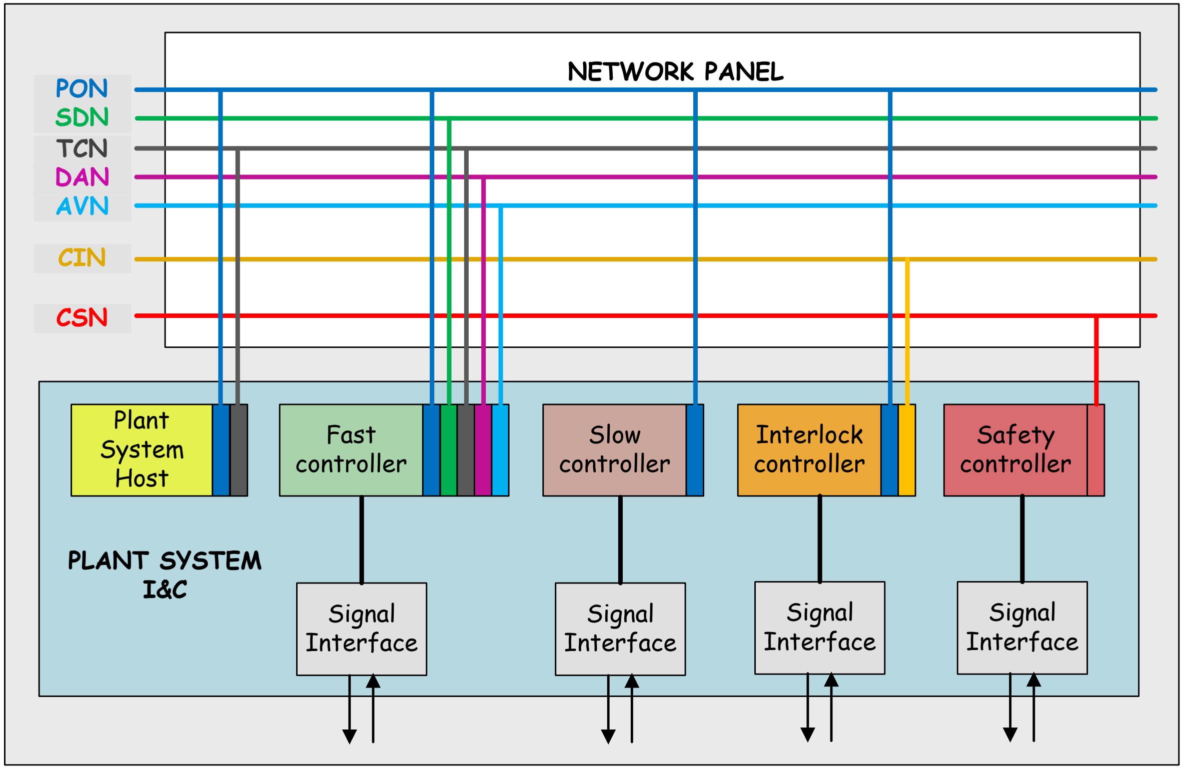
Control System Overview



Central I&C

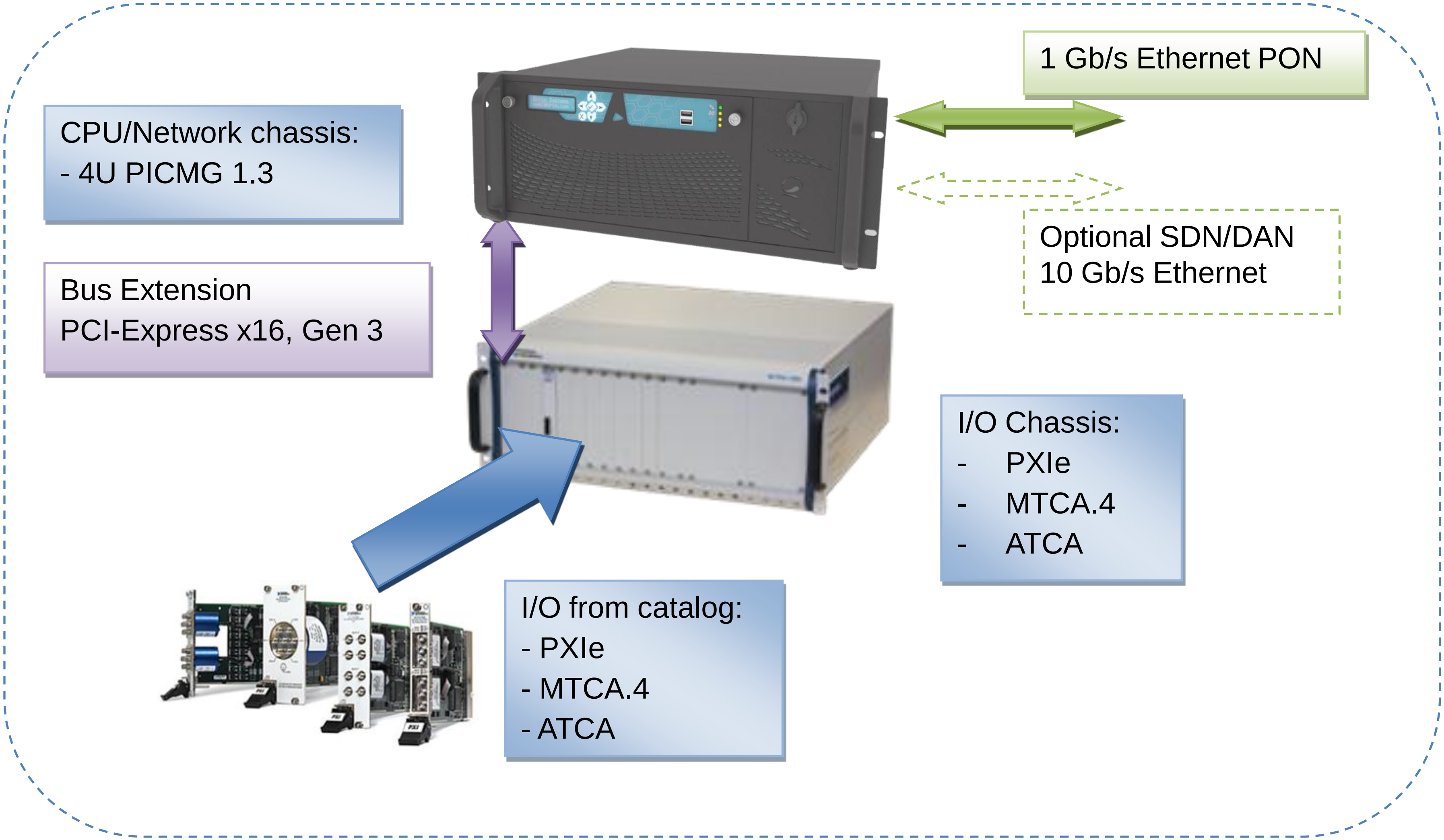
Plant system I&C

Network Interfaces



- ✓ Plant Operation Network (PON): **Industrial Ethernet**
- ✓ Synchronous Databus Network (SDN): **UDP multicast on 10 Gb Ethernet**
- ✓ Time Communication Network (TCN): **PTP, IEEE 1588**
- ✓ Audio-Video Network (AVN): **10 Gb Ethernet**
- ✓ Data Archiving Network (DAN): **10 Gb Ethernet**
- ✓ Central Interlock Network (CIN): **Industrial Ethernet**
- ✓ Central Safety Network (CSN): **Industrial Ethernet + Hard Wires**

Fast Controller Standard


CPU/Network chassis:
- 4U PICMG 1.3
Bus Extension
PCI-Express x16, Gen 3
1 Gb/s Ethernet PON
Optional SDN/DAN
10 Gb/s Ethernet
I/O Chassis:
- PXIe
- MTCA.4
- ATCA
I/O from catalog:
- PXIe
- MTCA.4
- ATCA

Different Grades of Fast Controllers

High Demands on Instrumentation and Controls for ITER:

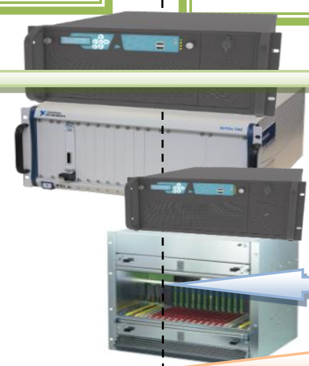
1. High Performance DAQ (ADC, Camera) ~ 15.000 channels
2. Data Processing (FPGA, CPU, GPU) ~ Gigaflops
3. Data Streaming (Real-time, Archiving) ~ 1ms , ~ 100 GB/sec

Demonstrated industrially available solutions:

PXIe
MTCA.4
ATCA

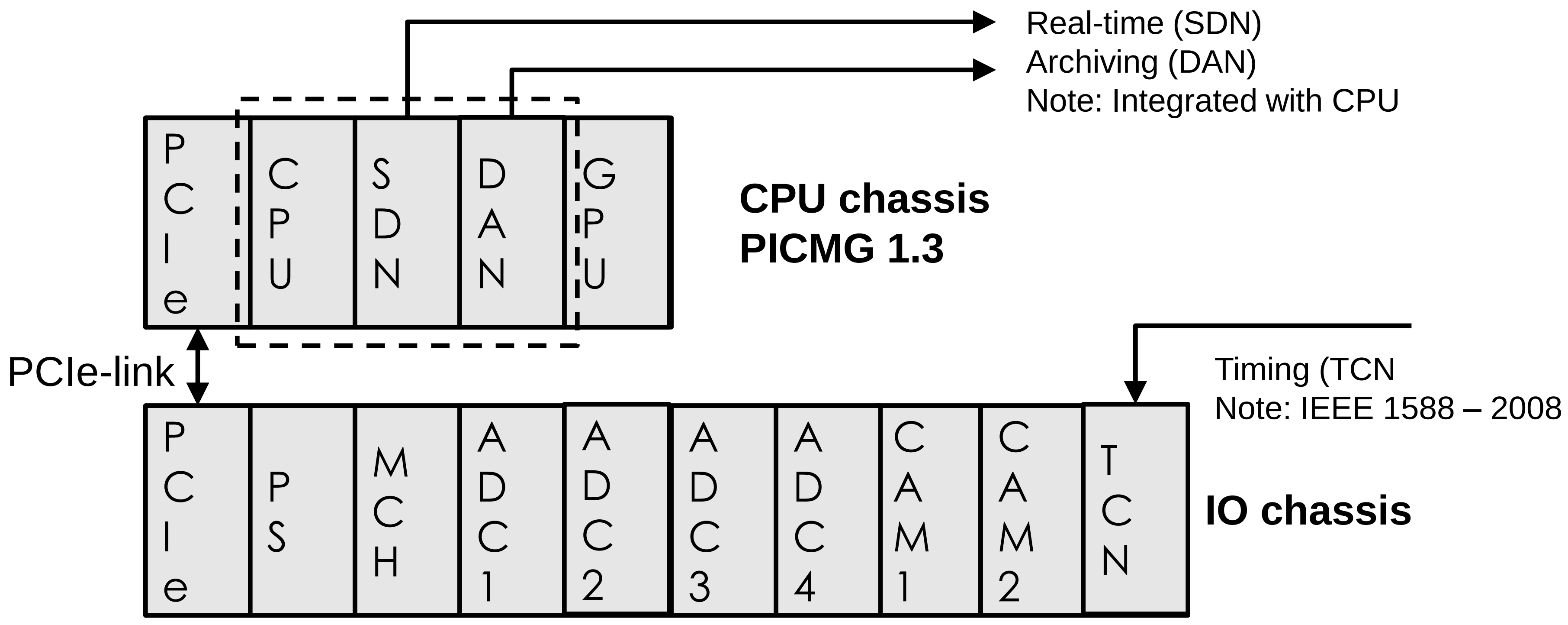
Main Challenge: Integration

Perf. Grade	I & C	DAQ	DAQ
Interconnect Technology	PCIe – PXIe I/O PCIe – cRIO I/O	PCIe - MTCA.4/µRTM PCIe – PXIe I/O	ATCA w/ Extns. for Physics
(product range coverage)			
Slow Controller (PLC) I&C application range	Fast Control I&C and Interlock (ex. ICH)	Diagnostics Data Acquisition (ex. Magnetics)	Demanding Diagnostics, I&C and Interlock tasks (ex. Plasma Control System)



Control loop frequency, Processing power Network capacity, Real-time constraints, Complexity, Price, Availability

Fast Controller Boards

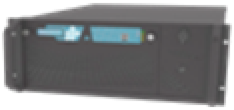


- IO chassis (~12 slot)
- PCIe-uplink
- Power supply
- MCH
- ADC 1 (32 ch.,1 MHz, 18-bit):
- ADC 2 (16 ch., 10 MHz, 16-bit)
- ADC 3 (10 ch. 100/250 MHz, 16-bit)
- ADC 4 (4 ch., 1-2 GS/s, 12/14-bit)

- CAM 1 (Camera-link)
- CAM 2 (Coax-press)
- CAM 3 (Other)
- TCN (IEEE1588)
- Other
  - FMC carrier / modules
  - RTM (pre-amp, chopper, downconverter, VM)

Examples from Catalog (1)

5.1 I&C Grade PICMG 1.3 PC 4U Computer



Manufacturer's Reference	*Short Form Description*	*ITER Reference and Datasheets*
ID01549-A-001/ITER	PICMG 1.3 (PCIe 3.0), 2 x Xeon = 8 cores, 8 GB DRAM, 2xSSD(RAID-1)	BKLT5Z
ID01549-B-001/ITER	Same as above but with 16 GB + NVIDIA Quatro 400 GPU + Drive bay (w/o extra disks)	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PLAN**	**PCDH**	**PLAN**	N/R

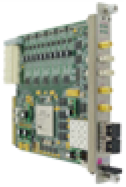
5.2 DAQ Grade PICMG 1.3 PC 4U Computer

Manufacturer's Reference	*Description*	*ITER Reference and Datasheets*
ID01550-A-001/ITER	PICMG 1.3 (PCIe 3.0), 2 x Xeon = 16 cores, 24 GB DRAM, 2xSSD(RAID-1)	BNXX8V
ID01550-B-001/ITER	as above but 32 GB + NVIDIA GTX680GPU(Kepler)	

Support	*SOFTWARE*	*SIG.IF*	*CABLE*	*THERM*	*RELBTY*	*MAGFLD*	*RADFLD*
Availability	CCS	N/R	N/R	**PLAN**	**PCDH**	**PLAN**	N/R

Examples from Catalog (6)

8.4 DAQ Grade MTCA.4 I/O Boards and Bundles

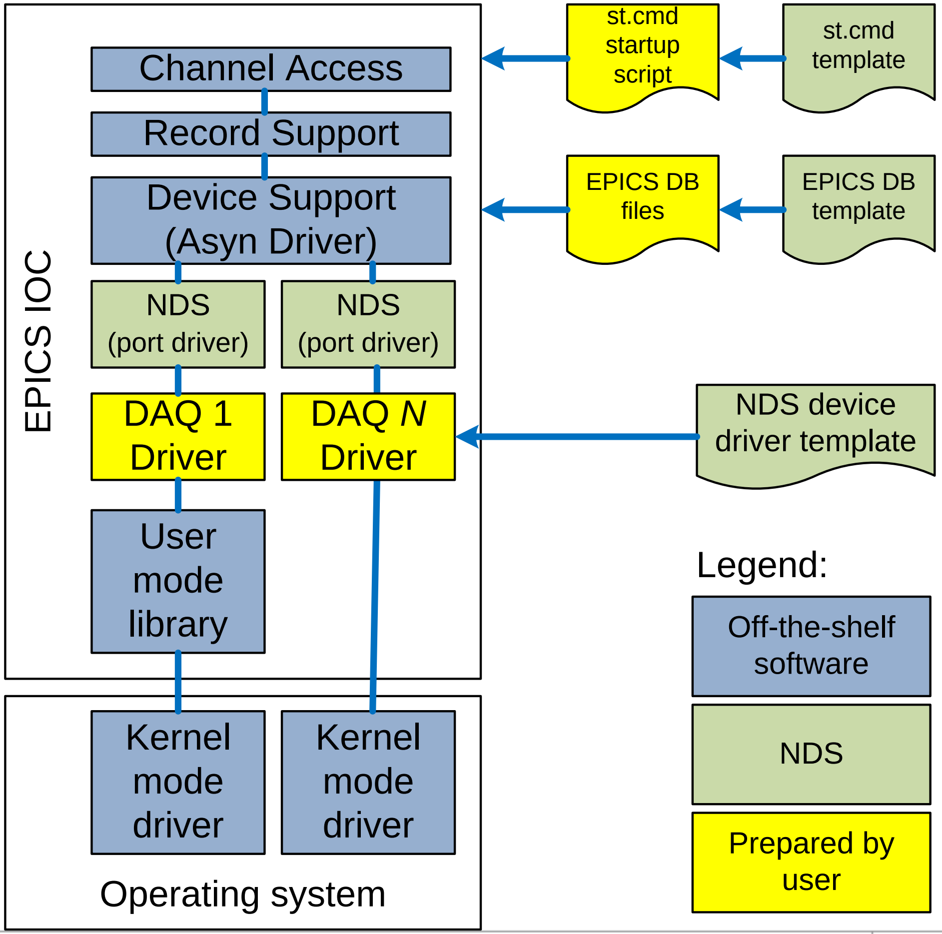


Manufacturer's Reference	***Description***	***ITER Reference and Datasheets***
SIS8300 04075 / SIS8900	10 x AI (16-bit) **125 MS/s** w/ single-ended RTM-module	C8TB4C
ADQ412-3G-MTCA	2/4 x AI (12-bit) **3.6 GS/s** 2 GHz	
SIS8300 04075 / RTM 7201	10 x AI (16-bit) **125 MS/s** 10 kHz – 1 MHz Chopper Integrator 4 channels ±5V / ±50V (50 ms) 1 kΩ, int.error < 200μVs / 1000 s	
TAMC640-12R / FMC-200	FPGA / Image Acquisition Bundle Camera Link (7.14 Gb/s) 85 MHz pixel clock	

Support	***SOFTWARE***	***SIG.IF***	***CABLE***	***THERM***	***RELBTY***	***MAGFLD***	***RADFLD***
Availability	ALPHA	**PCDH**	**PCDH**	**PCDH**	**PCDH**	**PCDH**	PLAN

Standardization of Device Support

- ***Nominal Device Support*** (NDS)
  - A C++ “base class” from which device-specific drivers are to be derived
  - Templates
    - makeBaseApp.pl
    - EPICS database
    - Example device driver
  - Documentation
    - User’s manual
    - Test plan



- Based on the C++ *asynPortDriver*

Instrumentation Needs

Scientific computing for ITER Operation

Diagnostics Type	Data Acquisition ADC / Camera	Data Rate for Archiving	Signal Processing complexity / resource	Algorithms
Magnetics	(0.1 – 1) MS/s	Moderate	Moderate, FPGA, CPU	Integrators, Magnetic reconstruction
Neutronics	100 Ms/s	Medium	Medium, distributed, FPGA, CPU	Pulse analysis
Optical	1 GS/s	High (peak)	Medium, FPGA, CPU	Pulse analysis
Optical Spectrometers	1 Mpixel (50 Hz)	High	Medium, FPGA, CPU	Spectral analysis
Microwave systems	1 GS/s	High (peak)	High, FPGA, CPU, GPU	Complex filtering, Bottollier-Curtet
Imaging systems	1 Mpixel (1 kHz)	High	High, FPGA, CPU, GPU	compression, reflection removal, event detection

Basic Diagnostic Needs for I&C

- Data Acquisition
  - 1 MS/s ADCs (16+ bit resolution, 10 ch.)
  - 10 MS/s ADCs (16+ bit resolution, 10 ch.)
  - 100 MS/s ADCs (14+ bit resolution, 10 ch.)
  - 1 GS/s (12 bit resolution, 4 ch.)
  - (Digital) Frame Grabber for Cameras (full CameraLink)
- Signal Processing
  - FPGA
  - DSP
  - CPU
  - GPU
- Communication Links
  - PCI express (PCIe)
  - Gigabit Ethernet (GbE)

Note: Covers most diagnostics fast controller needs

Summary of ITER Fast Controller Needs

- ~15000 fast ADC (1 MS/s – 1 GS/s) channels
- ~ 300 camera interfaces
- ~ 10000 digital IO
- ~ 500 timing receivers
- ~ 250 real-time network interfaces
- ~ 250 archiving network interfaces
- FPGA, GPU and CPU processing of data
- ~ 500 IO chassis with PCIe uplink to external CPU
- Formfactor PXIe, ATCA, MTCA.4
- Installed in ~ 350 racks in diagnostics building

Note: For slow IO (< 100 Hz) needs ITER will use Siemens S7 PLCs. However some channels will be implemented in fast controller for cost optimisation

Diagnostic Use Case Examples

Background of Diagnostics I&C Use Case Example

Why Diagnostic I&C Use Case Examples:

1. Produced on demand by DAs for examples
2. Provide incentives to follow PCDH by simplifying work from design to commissioning i.e. reduce cost).
3. Verify I&C can be be implemented in PCDH standards.

Note: Basic functionality represents only a fraction of each diagnostics I&C.

Benefits:

1. The diagnostics use case examples provide a framework in which domestic agencies can immediately start deploying their applications
2. Examples cover basic functions of many plant systems.
3. Demonstrate usage of components from fast controller catalog using supporting software.
4. Documentation templates provided. .

Products:

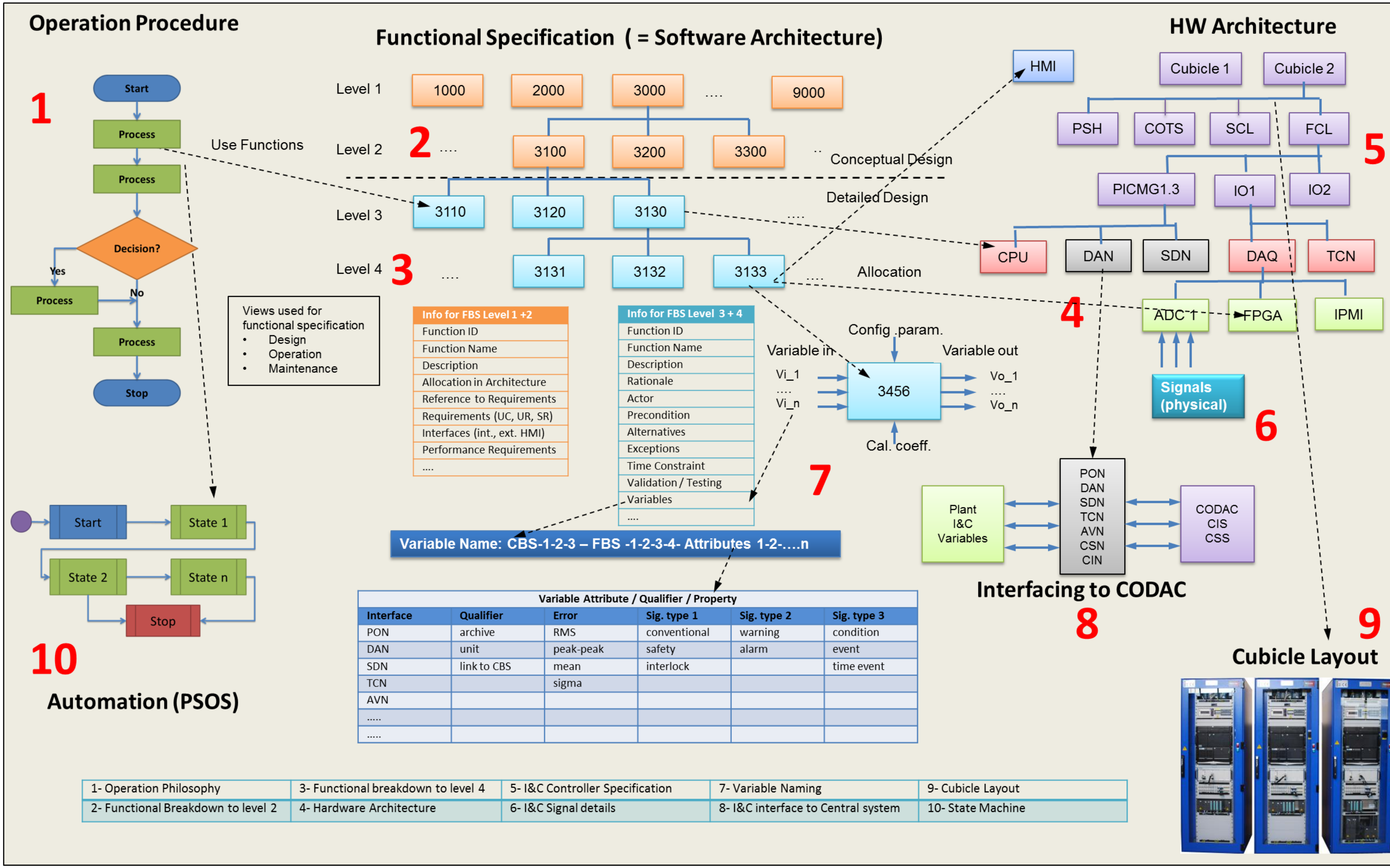
Documentation Products:

- System Requirement Specification (SRS)
- System Design Specification (SDS)
- System Manufacturing Specification (SMS)
- System Test Plan/Reports (STP)
- System Operation / Maintenance Manual (OMM)
- Diagrams in DB based repository

HW and SW Products:

- Complete working example system with basic functions.
- HW in fast controller catalog
- SW in SVN: Linux Driver and EPICS device support
- Automation (PSOS, COS)
- Network Interfaces (TCN, DAN, SDN…)

Design Deliverables for Plant I&C

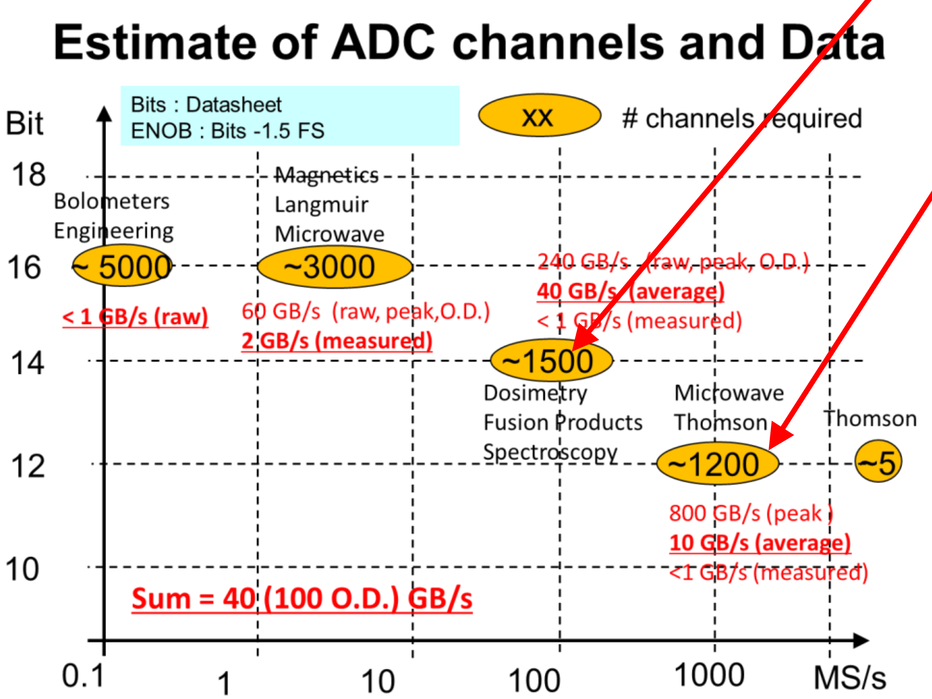


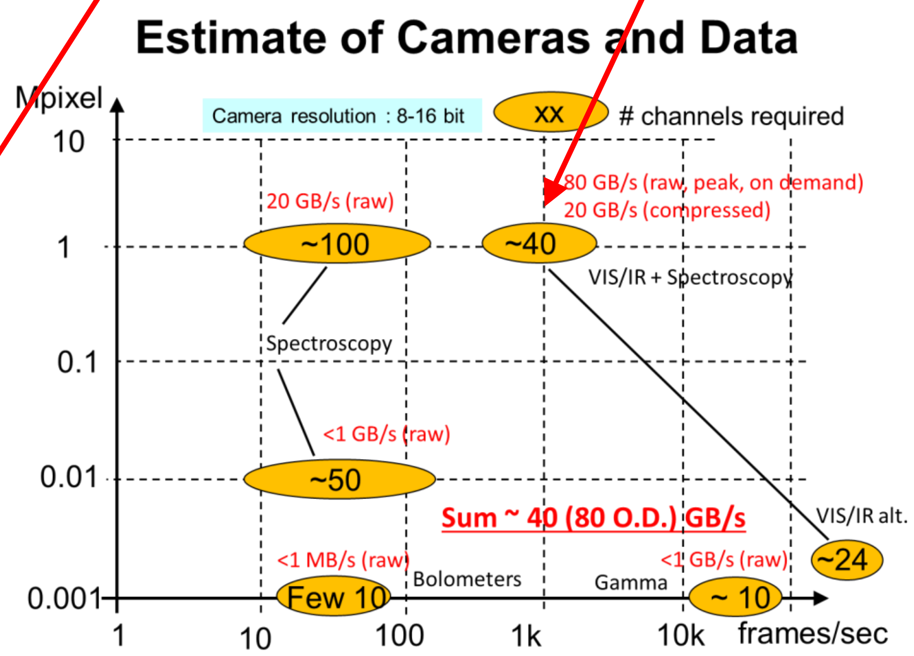
Variable Attribute / Qualifier / Property					
Interface	Qualifier	Error	Sig. type 1	Sig. type 2	Sig. type 3
PON	archive	RMS	conventional	warning	condition
DAN	unit	peak-peak	safety	alarm	event
SDN	link to CBS	mean	interlock		time event
TCN		sigma			
AVN					
.....					
.....					

1- Operation Philosophy	3- Functional breakdown to level 4	5- I&C Controller Specification	7- Variable Naming	9- Cubicle Layout
2- Functional Breakdown to level 2	4- Hardware Architecture	6- I&C Signal details	8- I&C interface to Central system	10- State Machine

Selection of Use Cases

- Neutronics Diagnostics (MFC) — 100 MHz ADC
- Image acquisition (VIS/IR) — Mpixel / kHz framerate
- Microwave Reflectometry — 1-2 GS/s ADC
- Magnetics Integrator — Signal Conditioning

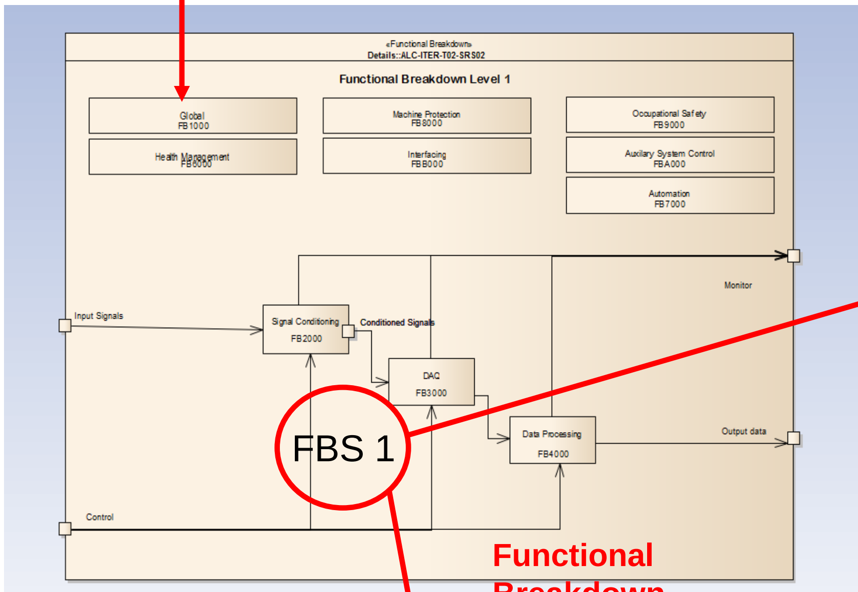




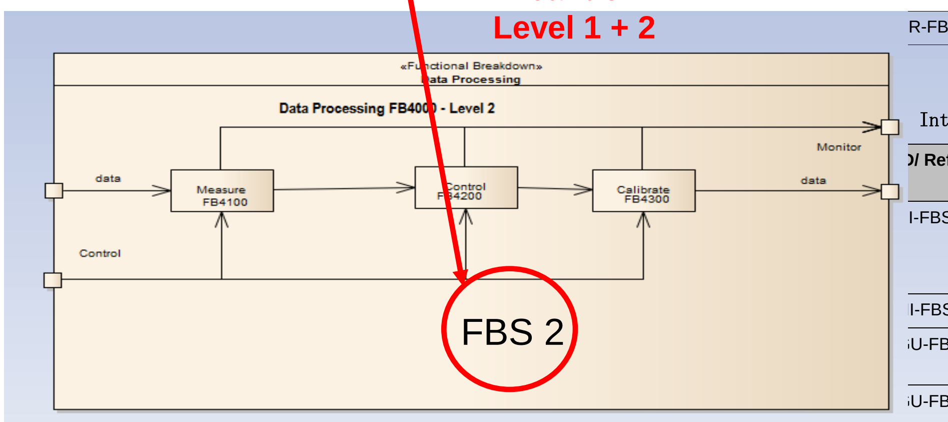
MFC – SRS Example

SRS
FBS: 1 +2

SDS
FBS 3+4+5



Functional Breakdown Level 1 + 2



Interaction with other plant systems

Information for Functions:

Interaction with other plant systems	
Actor	System
Pre-conditions	None
Description	1. Carry out global measurements 2. Carry out global control functions 3. Carry out global automation functions
Alternatives	Operate in standalone mode for testing without plasma
Exceptions	In case of error inform operator
Non-Functional Requirements	Any constants in the system (fixed gains etc.) shall be available as read-only PVs
Post-conditions	N/A The system normally runs continuously
Operation Scenarios	This use case is active during plasma operation

Use Cases

Table – Interactions with other Plant Systems

User and System Requirements

User and System Requirements

ID	Name	Text	FB	HMI
R-FBS1000-01	Measurement	Provide Global Measurement Functions	1100	N/A
R-FBS1000-02	Control	Provide Global Control Functions	1200	N/A
R-FBS1000-02	Automation	Provide Global Automation Functions	1300	N/A
R-FBS1000-01	Global Data	Provide EPICS Channel Access interface	1000	N/A

Table – User and System Requirements Table

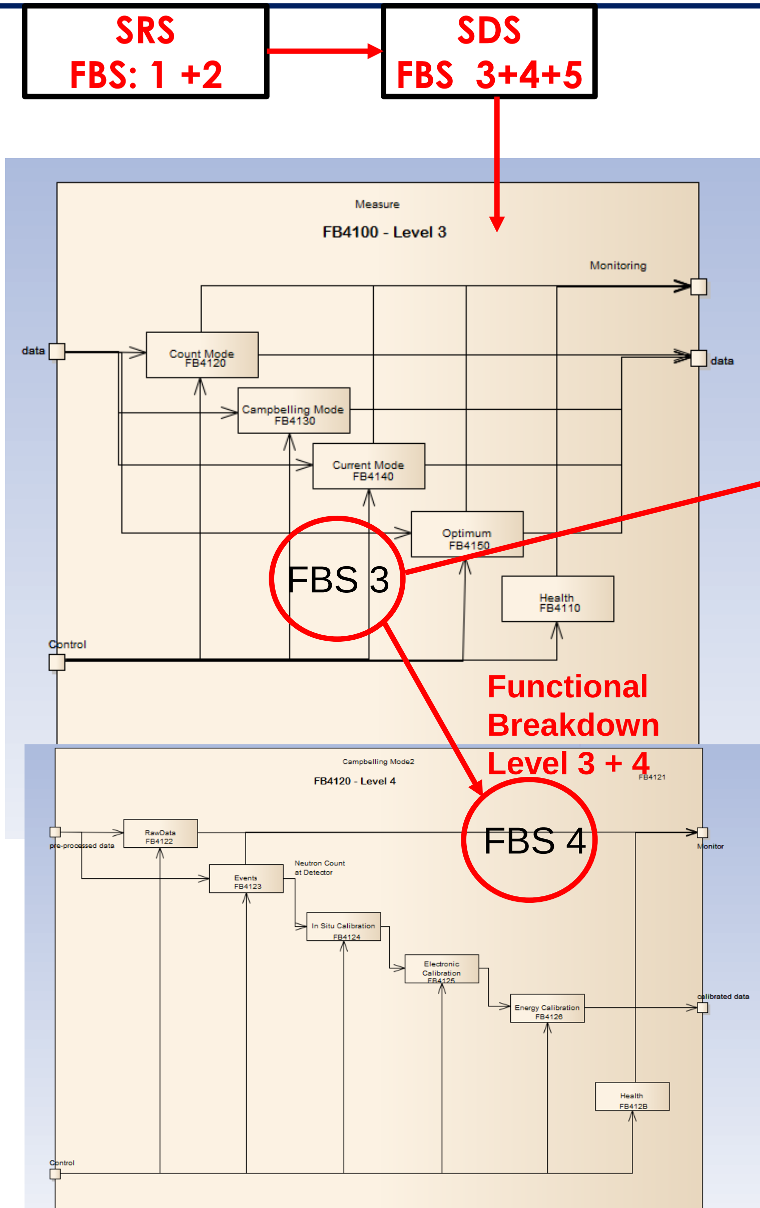
Interfaces – External Software (SW), Hardware (HW), GUI

ID/ Ref	Function	Interface Name	I/O (Widget)	Note
I-FBS1000-01	Provide Interface to data in other plant systems via channel access.	CA		
I-FBS1000-01		PON	I/O	Interface to PON network
U-FBS1000-01	Measurement	PON	Binary indicator	Show Health of Measurement function
U-FBS1000-02	Control	PON	Binary indicator	Show Health of Control Function
U-FBS1000-03	Automation	PON	Binary indicator	Show health of Automation function

Interfaces

Table - Interfaces Table

MFC – SDS Example



Events (EV) FBS-4123 **Information for Functions:**

This function provides:

1. Arrays of 1000 values each of which represents the count of events over 1ms
2. The count of events every ms for transmission on SDN to the PCS.

Timing Constraints

Ref	FBS	Constraint	Description
TC4.5.1.2.2.1.1	4123	Data arrives under interrupt	The reading of event counting is linked to the pulse – they arrive every ms during a pulse. For EPICS the array of events arrive every 1S

(Include sequence charts where appropriate)

Design Rationale

Design Decisions

Ref	FBS	Decision	Rational
DD4.5.1.2.2.2.1	4123	Use FPGA, Linux Driver, EPICS Driver, and EPICS.	FPGA needed due to fast data rate.
DD4.5.1.2.2.2.2	4123	Runs on PCF	Where time-critical functions run
DD4.5.1.2.2.2.3	4123	Data is sent to SDN at 1ms rate by a interrupt driven process that receives data from the Linux driver	To achieve the 1ms rate

PV List **Process Variable**

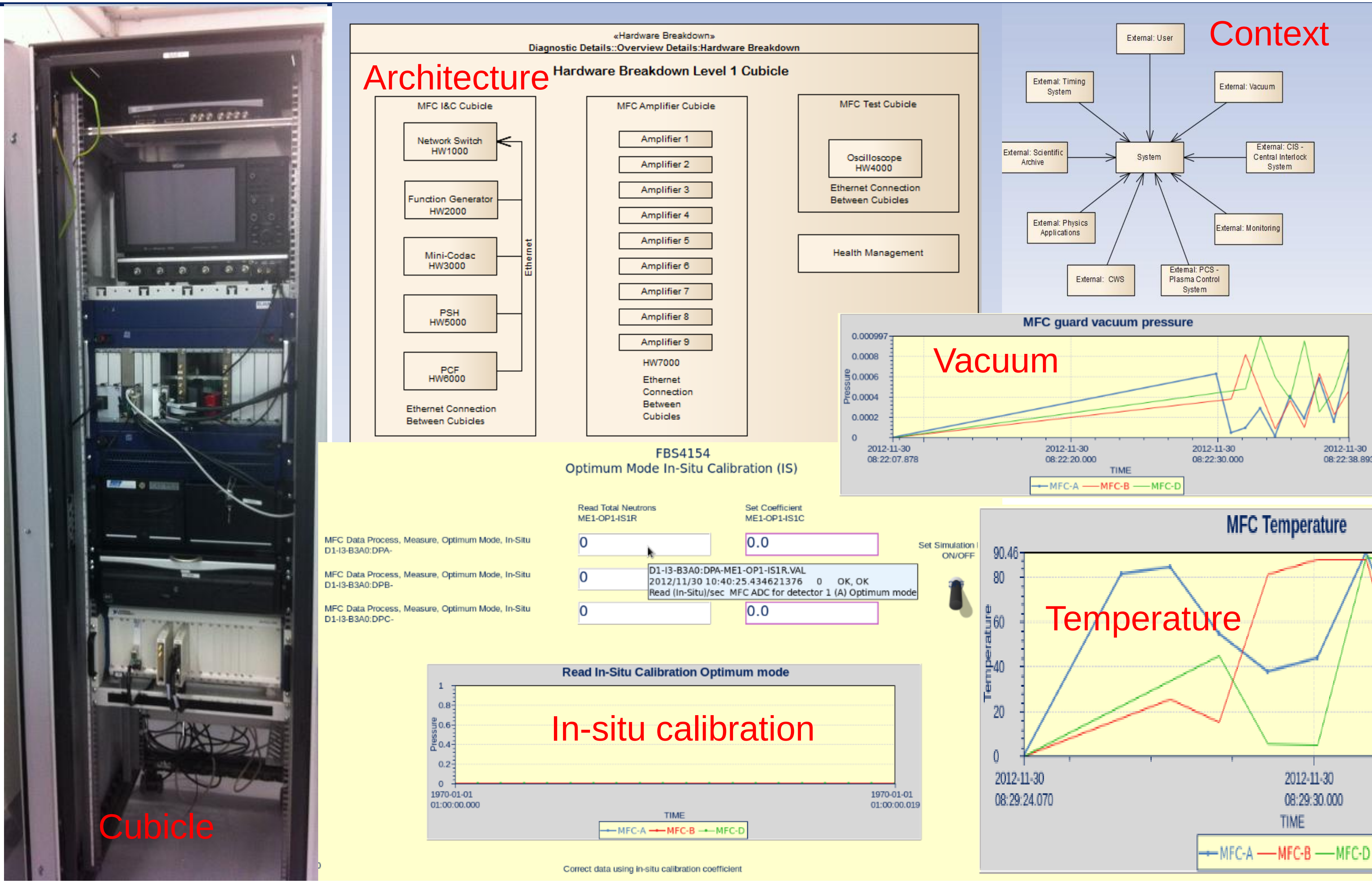
Ref	FBS	PV	Description
PV4.5.1.2.2.3.1	4123	D1-I3-B3A0:DP1-ME1-CO1-EV1R	Read Events/sec MFC ADC for detector 1 (A) Count mode
PV4.5.1.2.2.3.2	4123	D1-I3-B3A0:DP4-ME1-CO1-EV1R	Read Events/sec MFC ADC for detector 2 (B) Count mode
PV4.5.1.2.2.3.3	4123	D1-I3-B3A0:DP7-ME1-CO1-EV1R	Read Events/sec MFC ADC for detector 3 (C) Count mode

Ref	FBS	PV	Description
PV4.5.1.2.2.3.4	4123	D1-I3-B3A0:DP1-ME1-CO1-EV1A	Read Events array MFC ADC for detector 1 (A) Count mode
PV4.5.1.2.2.3.4	4123	D1-I3-B3A0:DP4-ME1-CO1-EV1A	Read Events array MFC ADC for detector 2 (B) Count mode
PV4.5.1.2.2.3.5	4123	D1-I3-B3A0:DP7-ME1-CO1-EV1A	Read Events array MFC ADC for detector 3 (C) Count mode

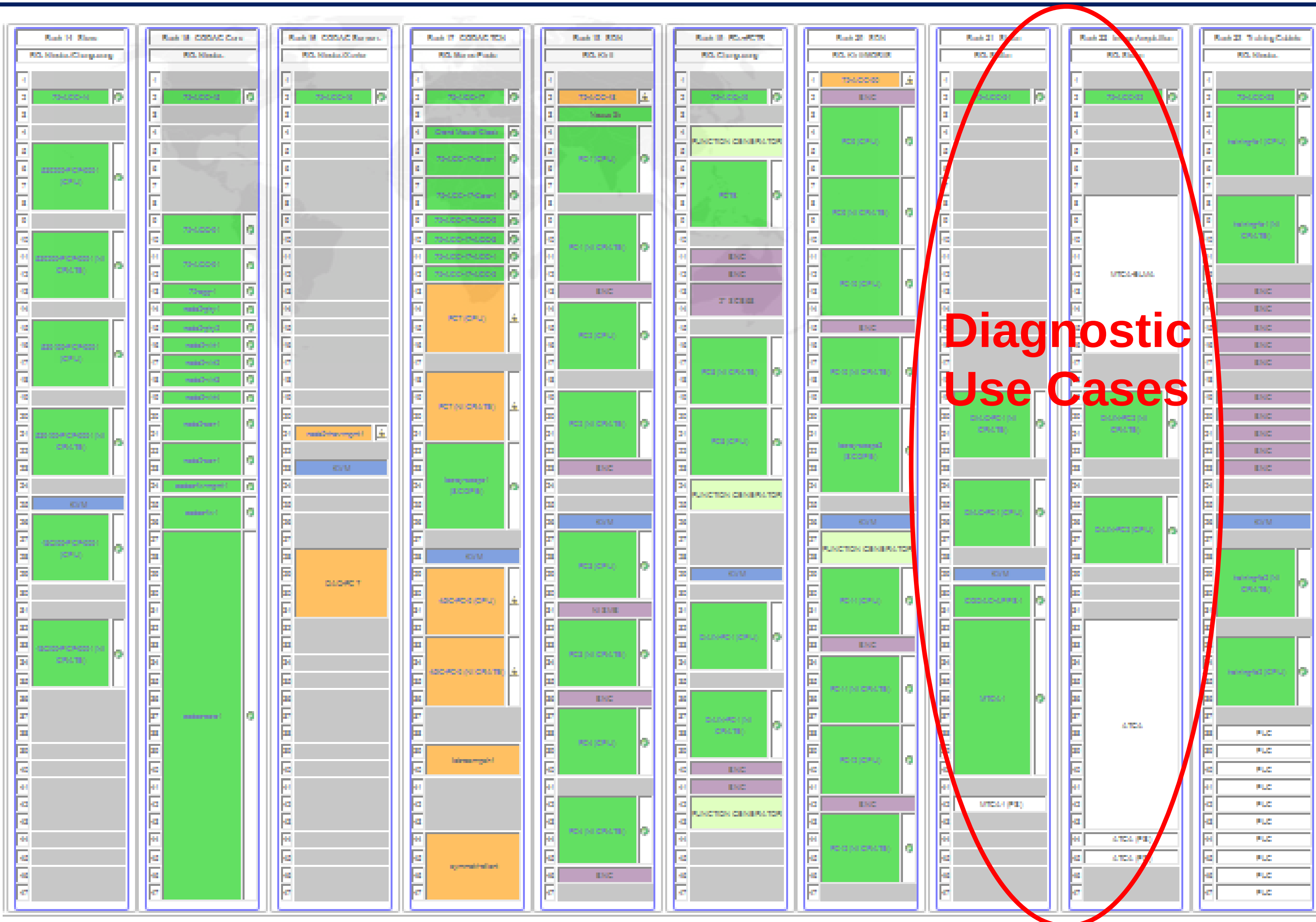
Validation **Validation**

Ref	FBS	Validation	Description
VA4.5.1.2.2.4.1	4123	Test value above low limit	Generate alarm if 0

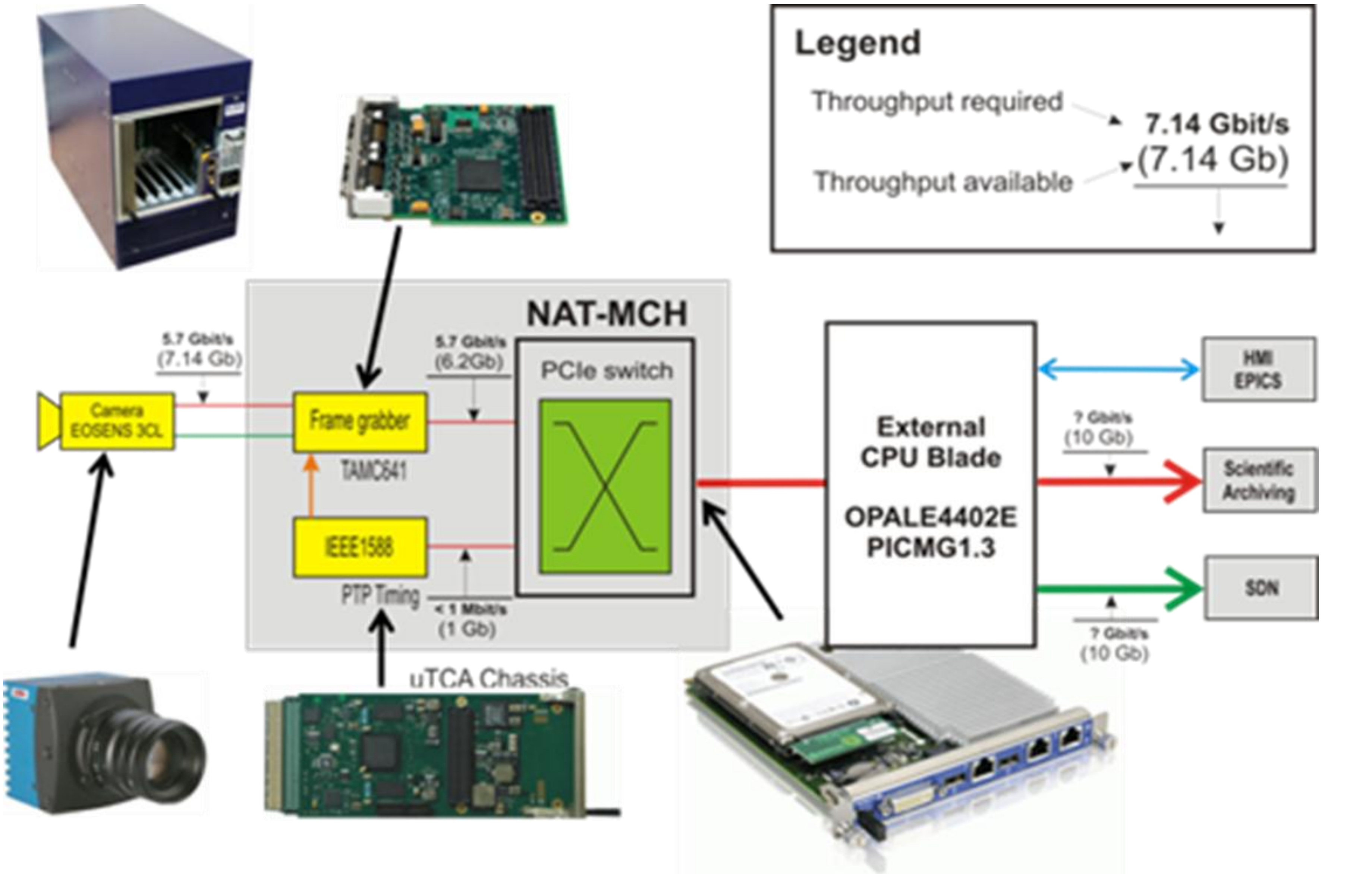
Implementation



Cubicles in Technical Room



Imaging Diagnostics UC



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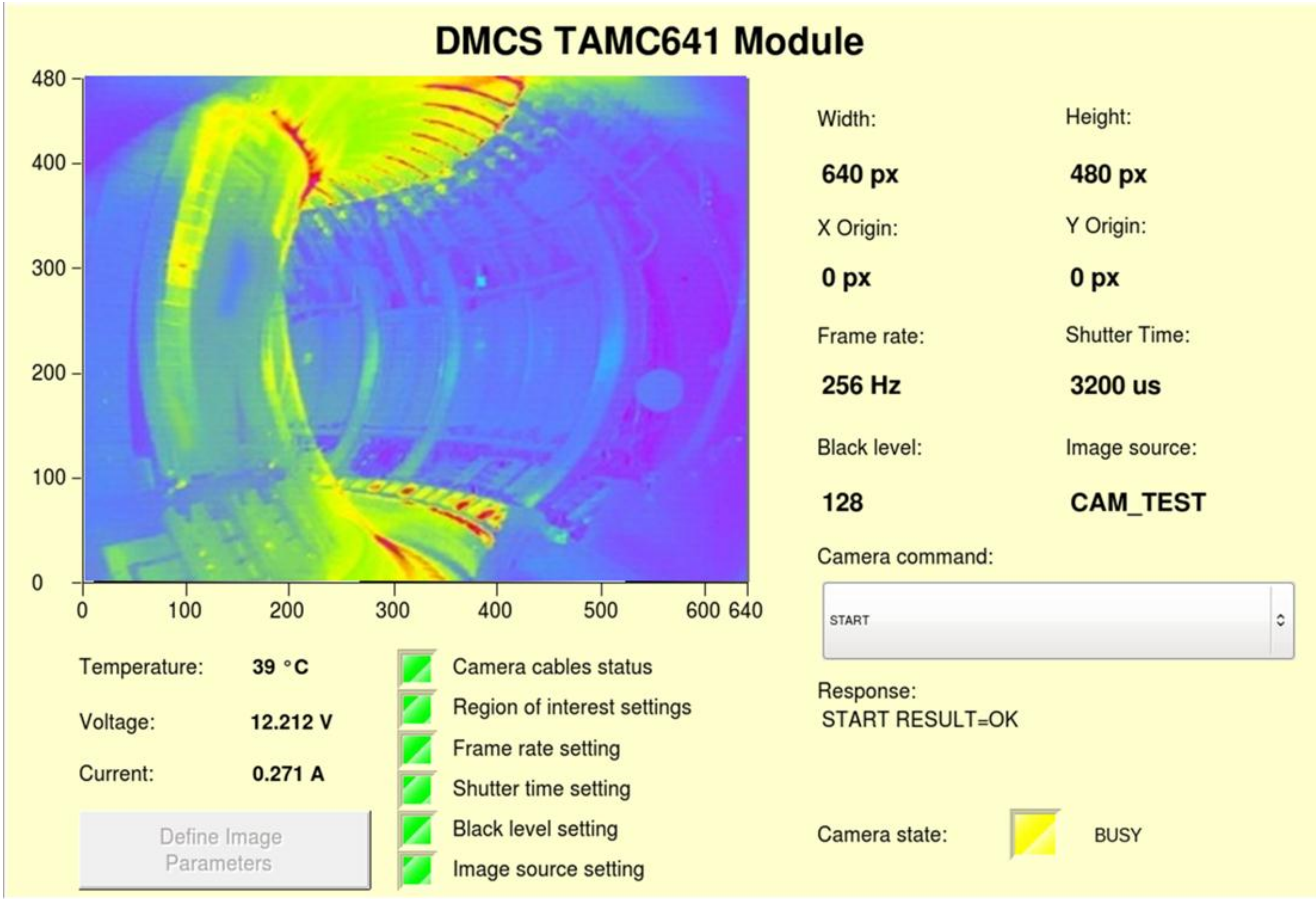
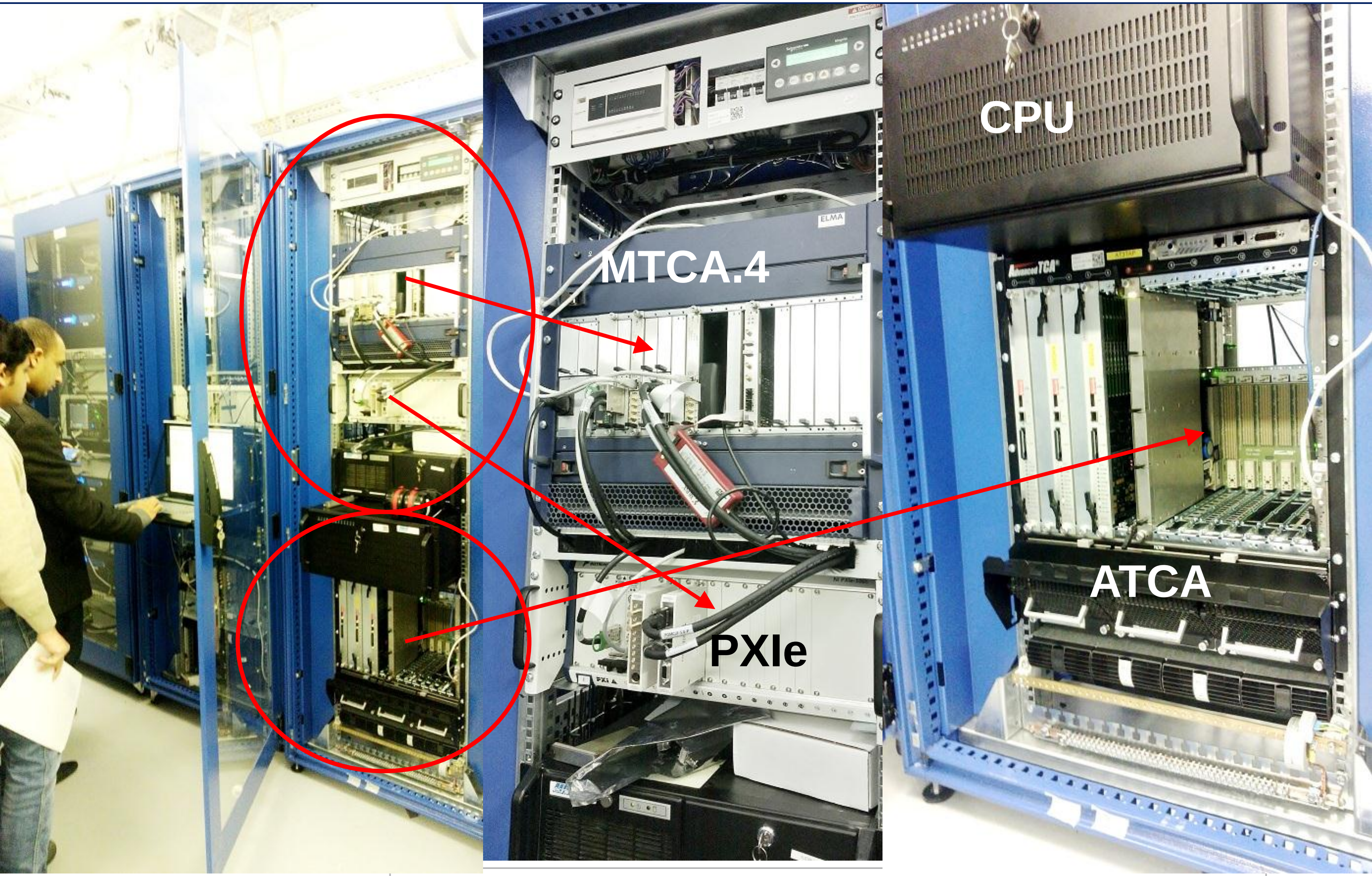
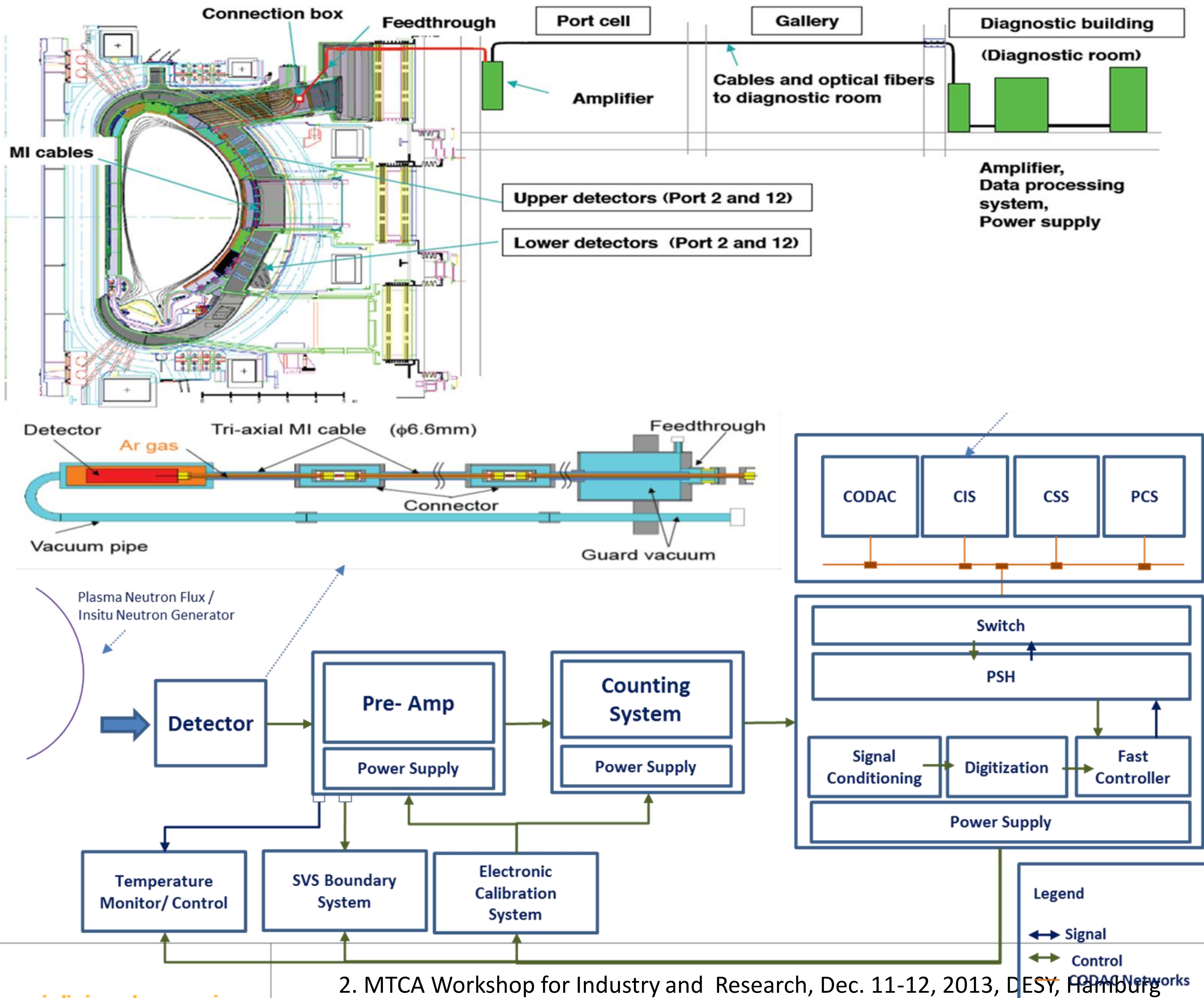


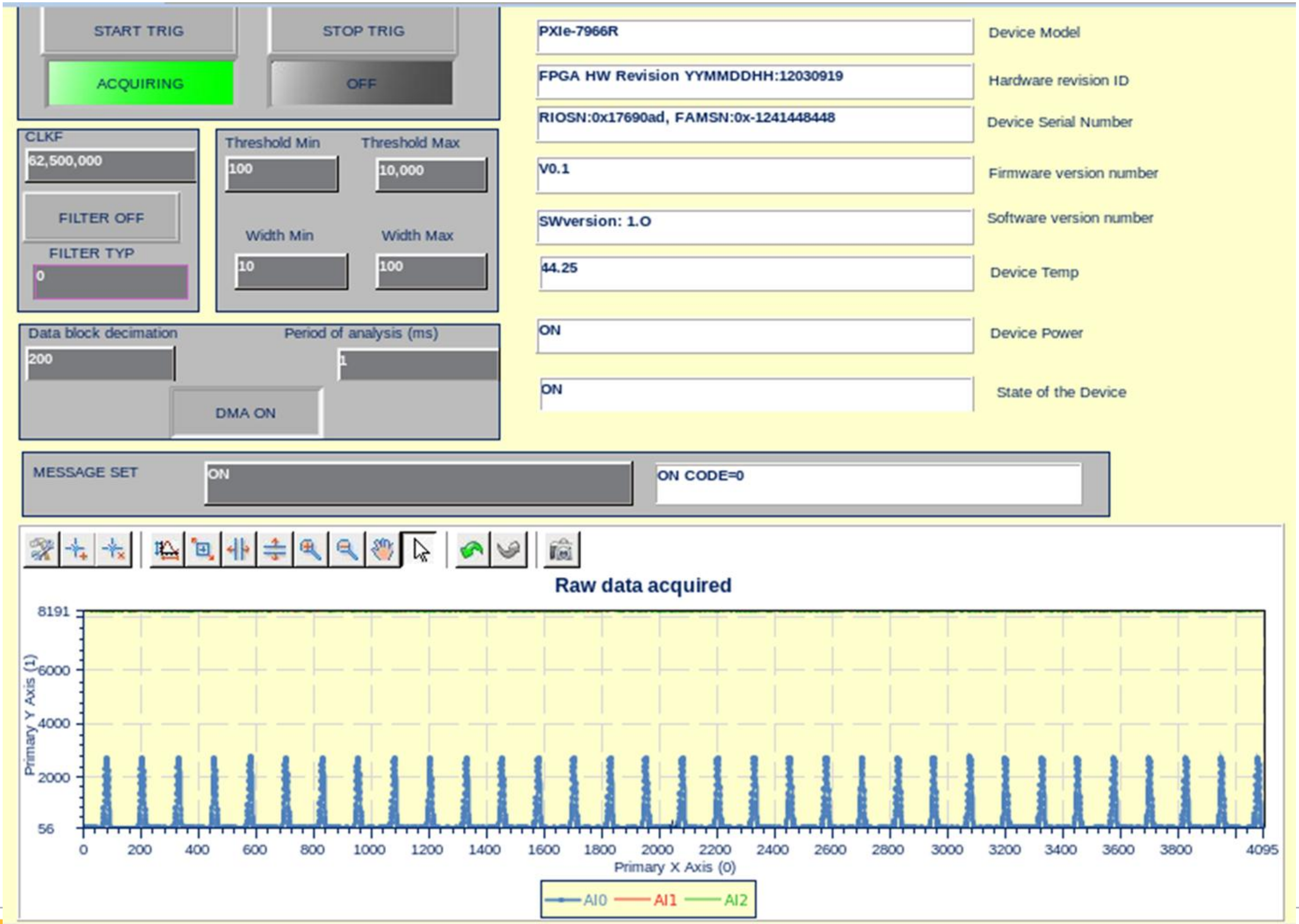
Imaging Diagnostics UC



Neutronic Diagnostics UC



Neutronic Diagnostics UC



NDS RIO device function implementation

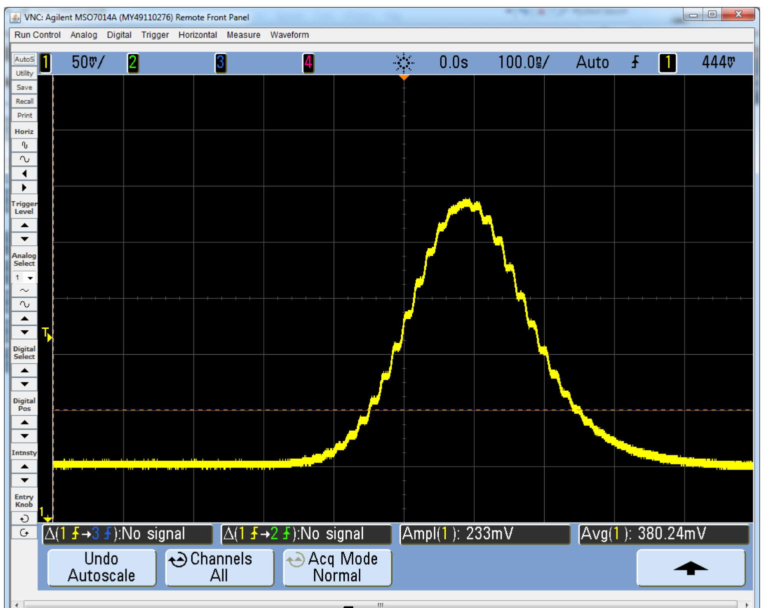
Function Description	NDM Function	Implemented	Notes
Get device state	getState	No	
Read FlexRIO temperat ure sensor		Yes	Board temperature in Celsius Deg
Read serial number	getSerial	Yes	String with FlexRIO card SN and and FAM SN
Read Hardware Revision	getHardwareRevision	Yes	FlexRIO Firmware identification label
Read firmware version	getFirmwareVersion	Yes	Mayor and minor number version of LabVIEW VI for programming the FPGA
Read Software verison	getSoftwareVersion	Yes	String with mayor and minor identificatio of NDS RI O (1.0)
Read input coupling	setCoupling	Yes	NI 5761 could be AC or DC coupled. Products with different part numbers, software cannot det ect this.
Read channel state	setChannelState	No	
Set/Read sample rate	setClockFrequency	Yes	Same rate for 4 AI channels
Configure trigger		No	Digital trigger (start trigger)
Configure filter	setFilter	No	3 dB point, lowpass filter only
Calculate mean		No	
Read raw data	getBuffer	Yes	Waveforms PVs for 4 analog inputs channels
Start point		No	
Number of elements	BufferSize	No	Set the NELM field. Now, constant to 4096
Set decimation factor	setDecimationFactor	Yes	

NDS RIO device function implementation

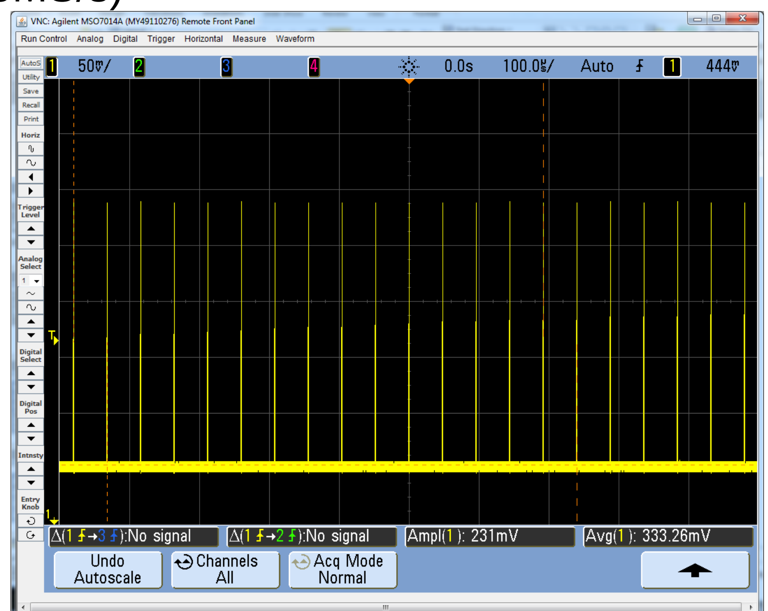
Function Description	NDM Function	Implemented	Notes
Read events/s	N/A		Every 1 ms – Various counting mod es
Read events/s array	N/A		1000 values every 1 s - Various cou nting modes
Read calibrated count s/s	getValueInt32	Yes	Pulses detected in 1 ms
Read calibrated count s/s array	N/A		1000 values every 1 s - Various cou nting modes
Read (electronic) cali brated counts/s	N/A		Every 1 ms – Various counting mod es
Read (electronic) cali brated counts/s array	N/A		1000 values every 1 s - Various cou nting modes
Read (energy) calibrat ed counts/s	N/A		Every 1 ms – Various counting mod es
Read (energy) calibrat ed counts/s array	N/A		1000 values every 1 s - Various cou nting modes
Provide calibration co nstants to FPGA	N/A		Various counting modes

Using NDS in Neutronic Diagnostics Use Case

- NI FPGA design v1.0
- Starting NDS RIO:
  - EPICS st.cmd:
    - ndsCreateDevice "ndsRIO", "RIO0", "N_AI=4,N_AO=0,N_DI=0,N_DO=0,N_DIO=0,N_auxDI=3, N_auxDO=3, N_auxAI=1, N_auxAO=2, RIOMODEL=PXIe-7966R, RIOSERIAL=0177A2AD, RIOVI=TESTCOUNTMFCV2“
- Test signal applied to AI0 (NI5761)
  - Generated with NI PXIe 5442 (62.5MS/s)



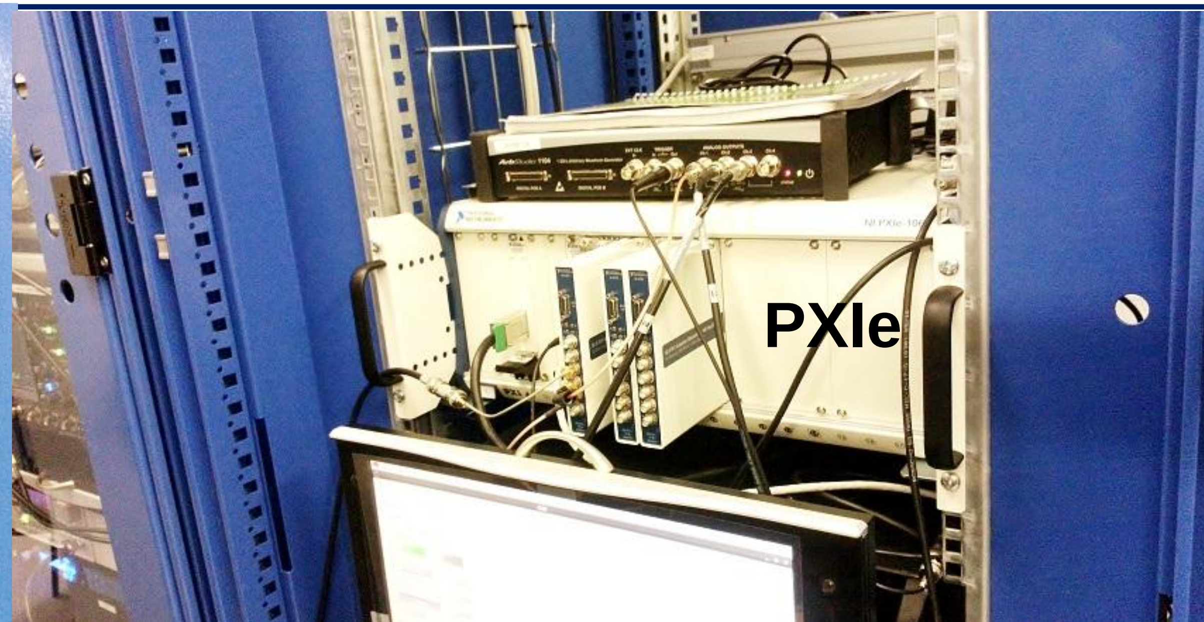
1us

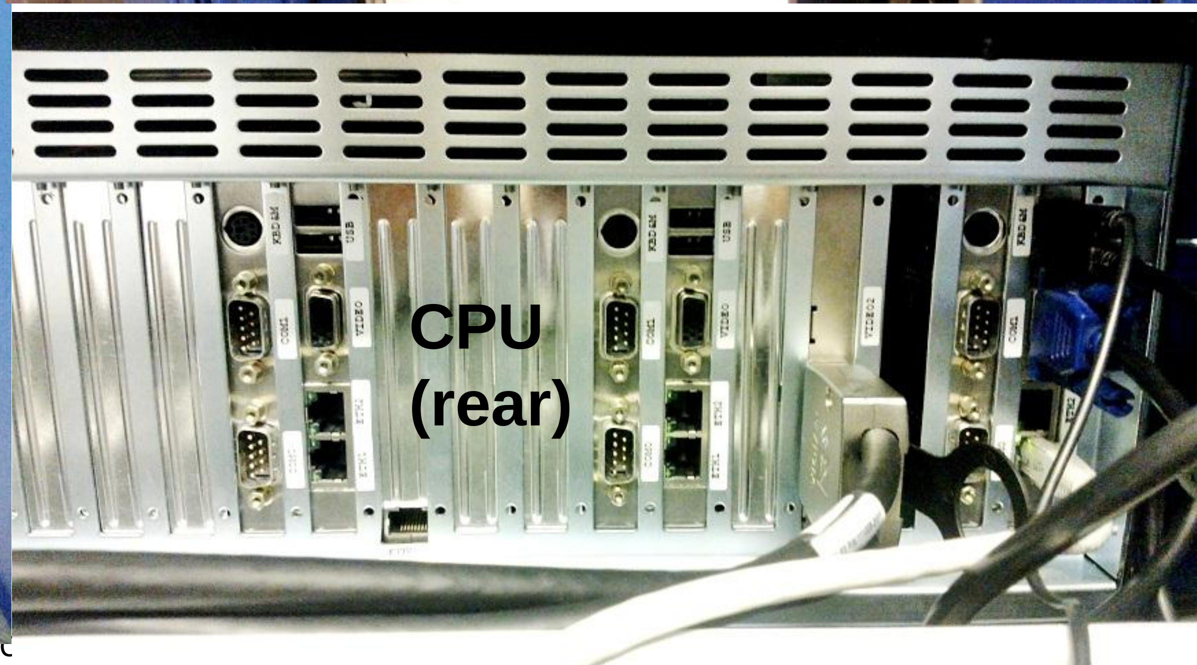


1ms

21 pulses/1 ms

Neutronic Diagnostics UC





What Industry must provide

- Commercially available hardware
- Linux Driver (with function required by diagnostics)
- EPICS Device support (according to NDS)
- Help Desk (all IO countries, all languages)
- Marketing in domestic agencies
- Alternative solutions
- Good documentation
- Compliance with standards

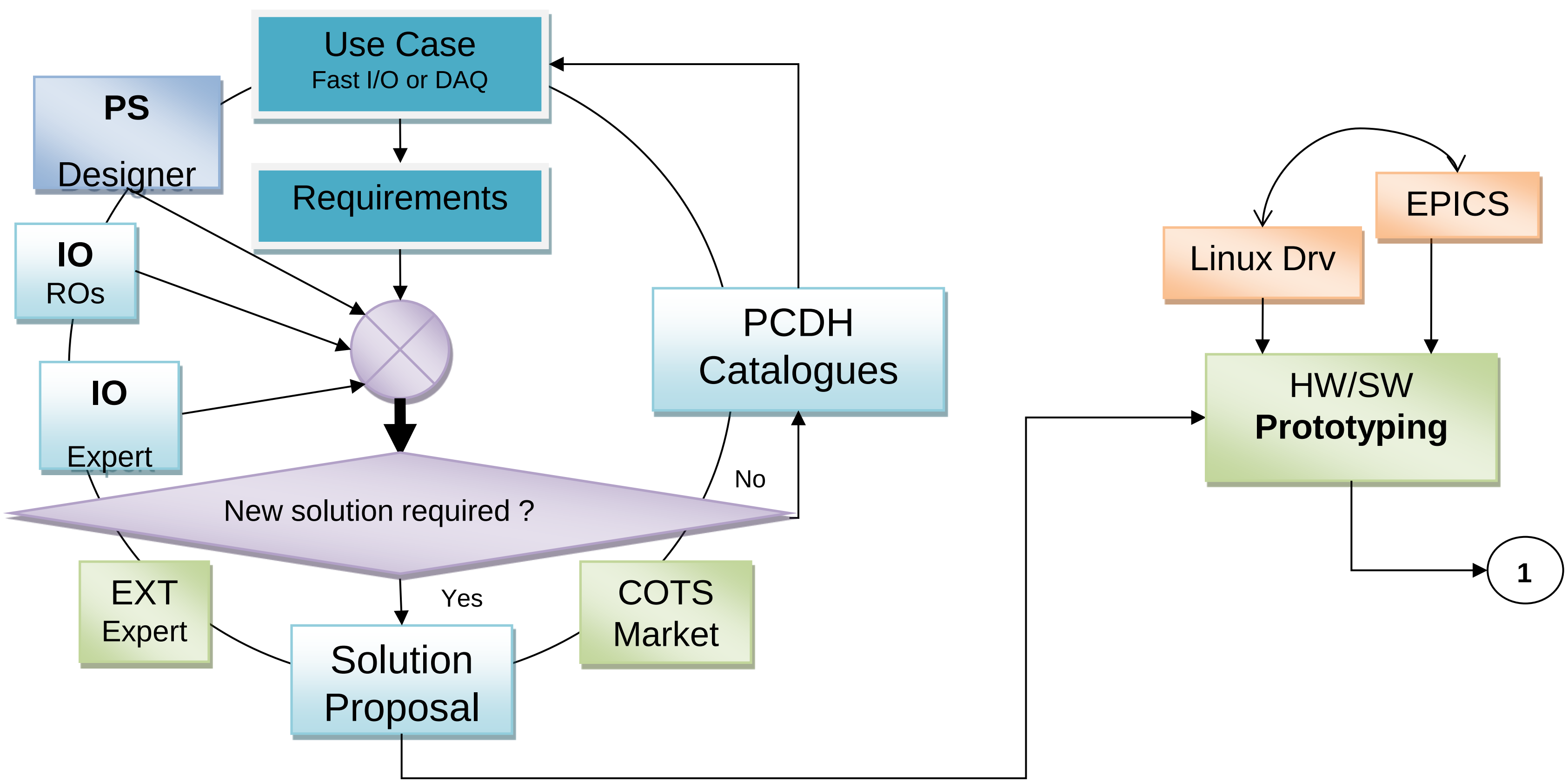
Ability to deliver integrated systems with CODAC Core System and use case examples installed and tested

Summary

- ITER's instrumentation needs are identified
  - Data acquisition
  - Data Processing
  - Real time control
  - Data Streaming
- Most fast controllers are required by diagnostics
- PXIe, ATCA, MTCA.4 platform technically adequate for these needs
- Diagnostics use case implementation help to promote the standards
- Commercial availability of MTCA.4 still limited
- Only minimal software support

Back-up Slides

Fast Controller Catalog – New items needed



Fast Controller Catalog – Total Cost of Ownership