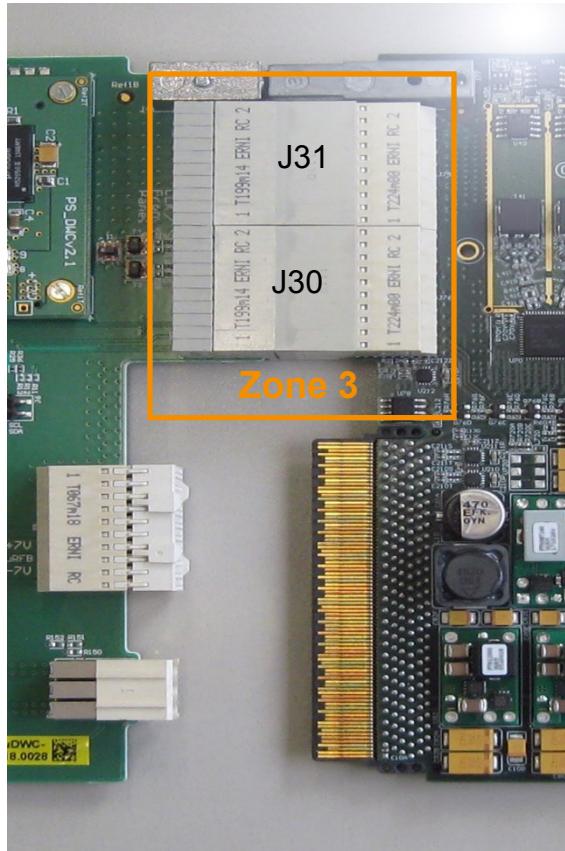


2nd MTCA Workshop for Industry and Research



Ratified Zone 3 classes to achieve
enhanced AMC – RTM modularity

Dr. Frank Ludwig
for the LLRF Team
Hamburg, 12.12.2013

Zone 3 Classes Recommendations in MTCA.4

FIL

- > Class A1.x mainly for analog signal transmission over Zone 3
- > Class D1.x for digital signal transmission over Zone 3
- > Recommendation – no standardization to be open for future signal types

- > Requires
 - AMC FPGA module based,
 - 2 ADF 30 pair (Mid-size) connectors
 - Class A1.x and D1.x needs not to be compatible



- > Supports
 - LVDS, LVCMOS, OC, CML, analog differential
 - Digital signals (single-, diff.-ended, bi-directional)
 - Analog signals
 - High-speed links
 - non-FPGA low-jitter clock signals
 - non-FPGA signals with fixed direction
 - ps-stable timing signals

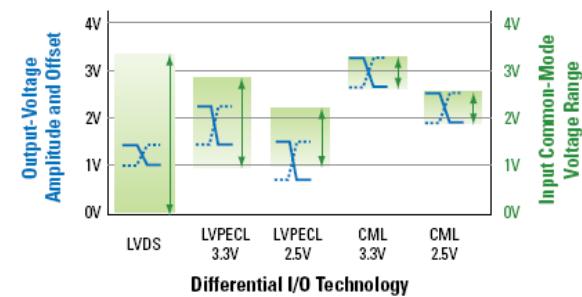
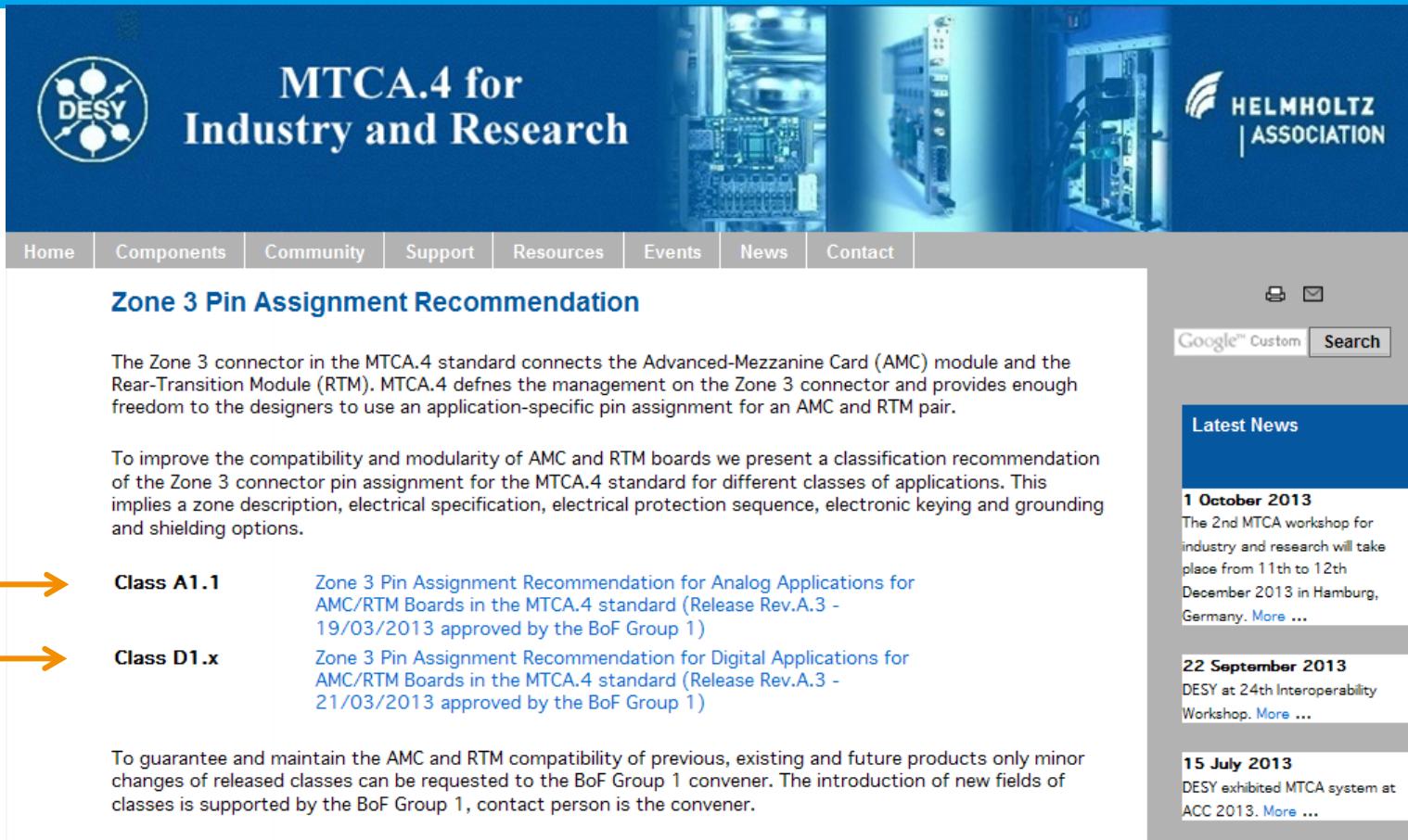


Figure 4-8. Differential Technologies

Ratified Zone 3 Class Recommendations <http://mtca.desy.de/>



The screenshot shows the MTCA.4 for Industry and Research website. At the top, there's a header with the DESY logo, the text "MTCA.4 for Industry and Research", and the Helmholtz Association logo. Below the header is a navigation menu with links to Home, Components, Community, Support, Resources, Events, News, and Contact. The main content area features a section titled "Zone 3 Pin Assignment Recommendation". It includes a text block about the Zone 3 connector, two orange arrows pointing to specific class recommendations, and a text block about maintaining compatibility. On the right side, there's a sidebar with "Latest News" sections for October 2013, September 2013, and July 2013.

Zone 3 Pin Assignment Recommendation

The Zone 3 connector in the MTCA.4 standard connects the Advanced-Mezzanine Card (AMC) module and the Rear-Transition Module (RTM). MTCA.4 defines the management on the Zone 3 connector and provides enough freedom to the designers to use an application-specific pin assignment for an AMC and RTM pair.

To improve the compatibility and modularity of AMC and RTM boards we present a classification recommendation of the Zone 3 connector pin assignment for the MTCA.4 standard for different classes of applications. This implies a zone description, electrical specification, electrical protection sequence, electronic keying and grounding and shielding options.

→ **Class A1.1** [Zone 3 Pin Assignment Recommendation for Analog Applications for AMC/RTM Boards in the MTCA.4 standard \(Release Rev.A.3 - 19/03/2013 approved by the BoF Group 1\)](#)

→ **Class D1.x** [Zone 3 Pin Assignment Recommendation for Digital Applications for AMC/RTM Boards in the MTCA.4 standard \(Release Rev.A.3 - 21/03/2013 approved by the BoF Group 1\)](#)

To guarantee and maintain the AMC and RTM compatibility of previous, existing and future products only minor changes of released classes can be requested to the BoF Group 1 convener. The introduction of new fields of classes is supported by the BoF Group 1, contact person is the convener.

Latest News

1 October 2013
The 2nd MTCA workshop for industry and research will take place from 11th to 12th December 2013 in Hamburg, Germany. [More ...](#)

22 September 2013
DESY at 24th Interoperability Workshop. [More ...](#)

15 July 2013
DESY exhibited MTCA system at ACC 2013. [More ...](#)

> 03/2013 Ratification BoF Group 1:
Rev.A.3

Thank
You!

Niels Koll NKoll@tews.com
Prof. Matthew Jones mjones@fnal.gov
Dr. Dariusz Makowski dmakow@dmcs.pl
Thomas Holzapfel thomas.holzapfel@powerbridge.de
Dr. Petr Vetrov petr.vetrov@desy.de
Samer Bou Habib samer.bou.habib@desy.de
Brian Ulskov Sørensen bus@recab.com
Saeed Karamoza saeed@vadatech.com
Dr. Frank Ludwig frank.ludwig@desy.de



Class A1.1 (Analog signal transmission)

FIL



Zone 3 Connector Pin Assignment Recommendation for Analog Applications for AMC/pRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:

- Power, I_C, optional JTAG support

Analog signal transmission zone:

- 10 channel AC-coupled differential input signals
- 10 channel DC-coupled differential input signals
- 5 channel DC-coupled differential output signals

Digital clock signal transmission zone:

- 6 AC-coupled differential inputs for low-jitter clock signals

User signal transmission zone:

- 6 LVDS inputs / outputs for user-configuration
- 3 LVDS outputs with fixed output direction
- Optional dual high-speed link

Zone shielding:

- Supports ground shielding between zones

APPLICATIONS

- AMC / pRTM board design in MTCA.4 standard
- High-precision multi-channel analog-to-digital converters
- High-speed multi-channel analog-to-digital converters
- Multi-channel high-frequency down/up-converters
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-jitter clock signal sampling and clock recovery

GENERAL DESCRIPTION

This Class A1.1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and pRTM boards transferring analog signals over the Zone 3 connector. This analog class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and pRTM boards.

This Class A1.1 pin assignment requires a common pRTM management implementation to make AMC and pRTM boards compatible. Appropriate management interface templates for this Class are available on <http://mtca.desy.de>.

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

Class A1.1 / Zone	a	b	c	d	e	f
J30	1 PWRA1	PWRB1	PS#	SDA	TCK	TDO
	2 PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link	3 SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX	SFP-TX+	SFP-TX-
User-configuration	4 D3+	D3-	D4+	D4-	D5+	D6-
Digital fixed I/O	5 D6+	D6-	D7+	D7-	D8+	D8-
Shielding	6 AMC_TCLK+	AMC_TCLK-	OUTD+	OUTD-	OUT1+	OUT1-
Digital clock inputs	7 gnd	gnd	gnd	gnd	gnd	gnd
	8 RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5-
	9 RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
Shielding	10 gnd	gnd	gnd	gnd	gnd	gnd
J31	1 CH0_PA+	CH0_PA-	DAC0+	DAC0-	CH0_TF+	CH0_TF-
	2 CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-
	3 CH1_PA+	CH1_PA-	DAC1+	DAC1-	CH1_TF+	CH1_TF-
	4 CH1_TF+	CH1_TF-	gnd	gnd	CH1_PA+	CH1_PA-
	5 CH2_PA+	CH2_PA-	DAC2+	DAC2-	CH2_TF+	CH2_TF-
	6 CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
	7 CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
	8 CH3_TF+	CH3_TF-	gnd	gnd	CH3_PA+	CH3_PA-
	9 CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
	10 CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-
Analog signals						

Table 1 : Pin assignment of Class A1.1, AMC side view

ZONE DESCRIPTION

As depicted in Table 1, the zones in the analog Class A1.1 consists of a management zone, user zone, digital clock zone and a zone for analog differential signals. The signal placement and filling sequence is done such, that the most sensitive signals have to be filled-up from connector J31 row 10) to (J30 row 3) and signals emitting high distortions filled-up vice versa.

The management zone (J30 row 1-2) is reserved for the pRTM management in the MTCA.4 standard. The user zone (J30 row 4-5) houses input and output signals in LVDS, CMOS or open collector (OC) level, which can be used for general purpose, e.g. I_C communication for slow board diagnostics. To achieve a high compatibility between AMC and pRTM boards, these inputs and outputs should be programmable in direction and signal type, preferable by an FPGA located on the AMC side.



Existing Class compatible AMC and RTMs

FIL

> Class A1.1 :

- AMCs:
- SIS8300 (Class A1.1, ADC, Struck)
 - SIS8300L (Class A1.1, ADC, Struck)
 - **SIS8325 (Class A1.1, ADC, Struck)**
 - **AMC520 (Class A1.1, ADC, Vadatach)**
 - DAMC-DS800 (Class A1.1, ADC , DESY)
 - TAMC532 (Class A1.2, ADC, TEWS)



RTMs:

- DRTM-DWC10 (Class A1.1, Down-Converter, DESY)
- DRTM-DWC8VM1 (Class A1.1, Down-Converter, DESY)
- DRTM-DS8VM1 (Class A1.1, Direct-Sampling, DESY)
- BPM (Class A1.1, DESY)
- SIS8900 (Class A1.1, Feed-through, Struck)
- **TAMC532-TM (Class A1.2, Shaper, TEWS)**

> Class D1.x :

- AMCs:
- DAMC-TCK7 (Class D1.2, Signal processing, DESY)
 - DAMC-FMC20 (Class D1.0, FMC carrier, DESY)
 - DAMC-FMC25 (Class D1.1, FMC carrier, DESY)
 - DAMC2 (Class D1.0, FMC carrier, DESY)
 - **IC-FEP-TCAa (Class D1.2, FMC carrier, IC)**
 - **IFC_1410 (Class D1.2, FMC carrier, IO&OS)**



RTMs:

- DRTM-AD84 (Class D1.0.1, ADC/DAC, DESY)
- DRTM-VM2 (Class D1.1, Up-Converter, DESY)
- DRTM-PZT4 (Class D1.0.1,2 HV-Board, DESY)
- MPS (Class D1.0, MPS- Board, DESY)
- **HV-PANDA (Class D1.1, CAEN)**
- **uRTM_1411 (Class D1.2, FMC carrier, IO&OS)**



. . . and more boards will be compatible . . .

Class A1.1 (Analog signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class A1.1 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1 2 PWRA2	PWRB1 PWRB2	PS# MP	SDA SCL	TCK TDI	TDO TMS
Standard Gbit-Link		3 SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
User-configuration		4 D3+ 5 D6+	D3- D6-	D4+ D7+	D4- D7-	D5+ D8+	D5- D8-
Digital fixed I/O		6 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Shielding		7 gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8 RTM_CLK4+ 9 RTM_CLK0+	RTM_CLK4- RTM_CLK0-	RTM_CLK2+ RTM_CLK3+	RTM_CLK2- RTM_CLK3-	RTM_CLK5+ RTM_CLK1+	RTM_CLK5+ RTM_CLK1-
Shielding		10 gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1 CH9_PA+ 2 CH8_TF+ 3 CH7_PA+ 4 CH6_TF+ 5 CH5_PA+ 6 CH4_TF+ 7 CH3_PA+ 8 CH2_TF+ 9 CH1_PA+ 10 CH0_TF+	CH9_PA- CH8_TF- CH7_PA- CH6_TF- CH5_PA- CH4_TF- CH3_PA- CH2_TF- CH1_PA- CH0_TF-	DAC0+ gnd DAC1+ gnd DAC2+ gnd DAC3+ gnd DAC4+ gnd	DAC0- gnd DAC1- gnd DAC2- gnd DAC3- gnd DAC4- gnd	CH9_TF+ CH8_PA+ CH7_TF+ CH6_PA+ CH5_TF+ CH4_PA+ CH3_TF+ CH2_PA+ CH1_TF+ CH0_PA+	CH9_TF- CH8_PA- CH7_TF- CH6_PA- CH5_TF- CH4_PA- CH3_TF- CH2_PA- CH1_TF- CH0_PA-

- MTCA.4 management
- 10 analog AC-coupled differential inputs
- 10 analog DC-coupled differential inputs
- 5 analog DC-coupled differential outputs

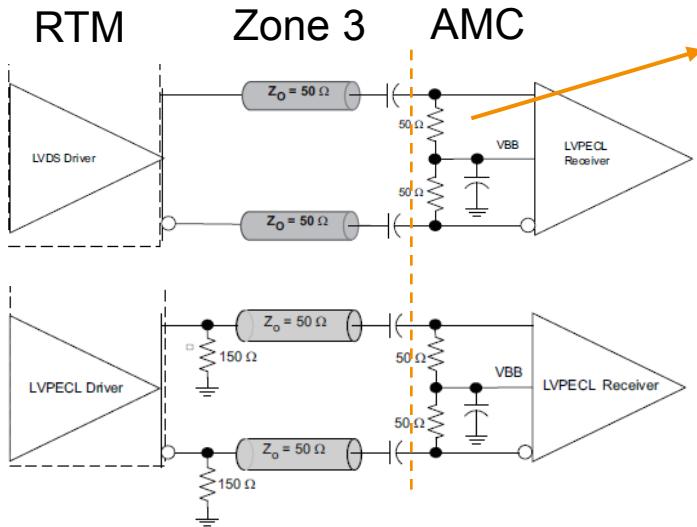
- 6 LVDS inputs for low-jitter clock signals
- 6 LVDS inputs / outputs
- 3 LDVS outputs
- Dual high-speed link support

Class A1.1 (Analog signal transmission)

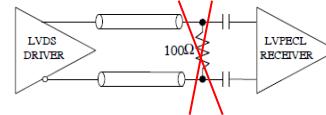
FIL

> Low jitter clocks termination refinement (AMC side, Rev.A.3.): TBD

Class A1.1 / Zone	a	b	c	d	e	f
MTCA.4 management	J30 1 PWRA1 2 PWRA2	PWRB1 PWRB2	PS# MP	SDA SCL	TCK TDI	TDO TMS
	3 LVDS - I 4 LVDS / LVCMOS / OC - I/O 5 LVDS / LVCMOS / OC - I/O 6 LDVS - O 7 gnd	LVDS - I LVDS / LVCMOS / OC - I/O LVDS / LVCMOS / OC - I/O LDVS - O gnd	CML - I LVDS / LVCMOS / OC - I/O LVDS / LVCMOS / OC - I/O LVDS - O gnd	CML - I LVDS / LVCMOS / OC - I/O LVDS / LVCMOS / OC - I/O LVDS - O gnd	CML - O LVDS / LVCMOS / OC - I/O LVDS / LVCMOS / OC - I/O LVDS - O gnd	CML - O LVDS / LVCMOS / OC - I/O LVDS / LVCMOS / OC - I/O LVDS - O gnd
Standard Gbit-Link						
User-configuration						
Digital fixed I/O						
Shielding						
Digital clock inputs	8 Differential AC-coupled, ±350mV...±1V / I, 100Ω 9 Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω Differential AC-coupled, ±350mV...±1V / I, 100Ω	
Shielding	10 gnd	gnd	gnd	gnd	gnd	gnd
J31	1 Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω			Differential 0 - ±1V / I, 100Ω
	2 Differential 0 - ±1V / I, 100Ω	gnd	gnd			Differential 0 - ±1V / I, 100Ω
	3 Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω			



> Termination and level adjustment after AC-coupling at the „end“.



e.g. on-chip termination ...

HMC988LP3E
 Hittite
MICROWAVE CORPORATION

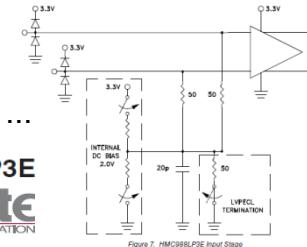


Figure 7. HMC988LP3E Input Stage

Class D1.0 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.0 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2 PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		1 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3 P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-

- D1.0 Subclass :
 - MTCA.4 management
 - 48 LVDS inputs / outputs

- (+) High compatibility, also to existing boards
- (-) No High-speed link support
- (-) No support of low-jitter clocks
- (-) No support of non-FPGA output signals

Class D1.1 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.1 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2 PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		1 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3 P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
User Configuration		4 P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO+ / CC
		6 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO+ / CC
		7 P31_IO+ / CC*	P31_IO+ / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8 P31_IO+ / CC*	P31_IO+ / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		9 GTP0-1_CLK_IN+	GTP0-1_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10 GTP0-1_CLK_OUT+	GTP0-1_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

- D1.1 Subclass :
- MTCA.4 management () Moderate compatibility
 - 42 LVDS inputs / outputs
 - 2 High-speed links (+) High-speed link support
 - 2 LVDS signals for low-jitter clocks (+) Support of low-jitter clocks
 - 4 LVDS outputs (+) Support of non-FPGA output signals

Class D1.2 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.2 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2 PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		1 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3 P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
User Configuration		4 P31_IO+ / CC	P31_IO+ / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO+ / CC
		6 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO+ / CC
		7 P31_IO+ / CC*	P31_IO+ / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8 P31_IO+ / CC*	P31_IO+ / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9 GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10 GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

- D1.2 Subclass :
- MTCA.4 management () Moderate compatibility
 - 38 LVDS inputs / outputs
 - 4 High-speed links (+) High-speed link support
 - 2 LVDS signals for low-jitter clocks (+) Support of low-jitter clocks
 - 4 LVDS outputs (+) Support of non-FPGA output signals

Class D1.3 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.3 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2 PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6 P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8 P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10 P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		1 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2 P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3 P31_IO+ / CC	P31_IO- / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
Standard Gbit-Links		4 P31_IO+ / CC	P31_IO- / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5 GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6 GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7 P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8 P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9 GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10 GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

- D1.3 Subclass :
- MTCA.4 management () Moderate compatibility
 - 28 LVDS inputs / outputs
 - 8 High-speed links (+) High-speed link support
 - 2 LVDS signals for low-jitter clocks (+) Support of low-jitter clocks
 - 4 LVDS outputs (+) Support of non-FPGA output signals

Class D1.4 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.4 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2 PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3 AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Standard Gbit-Links		5 P30_IO+ / CC *	P30_IO+ / CC *	GTP15_RX+	GTP15_RX-	GTP15_TX+	GTP15_TX-
		6 P30_IO+ / CC *	P30_IO+ / CC *	GTP14_RX+	GTP14_RX-	GTP14_TX+	GTP14_TX-
		7 GTP12-15_CLK_IN+	GTP12-15_CLK_IN-	GTP13_RX+	GTP13_RX-	GTP13_TX+	GTP13_TX-
		8 GTP12-15_CLK_OUT+	GTP12-15_CLK_OUT-	GTP12_RX+	GTP12_RX-	GTP12_TX+	GTP12_TX-
		9 P30_IO+ / CC*	P30_IO+ / CC*	GTP11_RX+	GTP11_RX-	GTP11_TX+	GTP11_TX-
		10 P30_IO+ / CC*	P30_IO+ / CC*	GTP10_RX+	GTP10_RX-	GTP10_TX+	GTP10_TX-
		1 GTP8-11_CLK_IN+	GTP8-11_CLK_IN-	GTP9_RX+	GTP9_RX-	GTP9_TX+	GTP9_TX-
		2 GTP8-11_CLK_OUT+	GTP8-11_CLK_OUT-	GTP8_RX+	GTP8_RX-	GTP8_TX+	GTP8_TX-
		3 P31_IO+ / CC	P31_IO- / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4 P31_IO+ / CC	P31_IO- / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5 GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6 GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7 P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8 P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9 GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10 GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

- D1.4 Subclass :
- MTCA.4 management () Moderate compatibility
 - 16 LVDS inputs / outputs
 - 16 High-speed links (+) High-speed link support
 - 2 LVDS signals for low-jitter clocks (+) Support of low-jitter clocks
 - 4 LVDS outputs (+) Support of non-FPGA output signals

High-Speed Links over Zone 3: Tx, Rx AC-coupling

FIL

- > Are we prepared for the next generation of high speed links over Zone 3 ?

AMC/ATCA	AC-coupling	Remark
	Receiver (Rx)	
	Transmitter (Tx)	
PCIe	Tx	AMC.0
	Tx (and Rx)	AMC.1 (Rev. 2.0), Gen 2, C=[76nF, 265nF]
	Tx (and Rx)	AMC.2 (Rev. 2.0), Gen 3, C=[176nF, 265nF]
GbE	Rx	
10GBase-BX4	Rx	
Serial Rapid IO	Rx (and Tx)	(Rx and Tx coupling allowed ? see Part 6, section 8.5.13: " ... Receivers and transmitters shall support AC coupling...")
Infiniband	Rx	
Fibre Channel	Rx	or 1:1 transformer on Rx
Compact PCI		
Serial Rapid IO	Rx	or 1:1 transformer on Rx

- > AMC.1: PCIe, Gen 2, 1.25Gbps, 2.5Gbps, 5Gbps



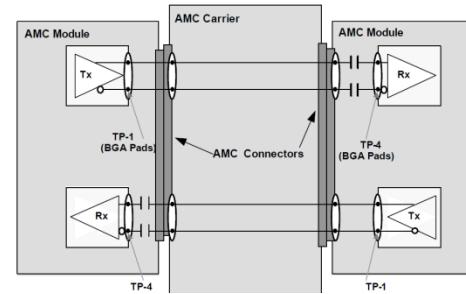
5 Gbps "DOUBLE CAP" PCIe
EXPRESS SIMULATION AND
ANALYSIS

The optimized passive channel with $1.0\mu F$, $0.68\mu F$ or no cap yielded nearly identical frequency domain performance.

6.2.1 Fabric Interface electrical requirements for LVDS

Modules are directly connected. The example shows the case where optional receive interface capacitors are used.

Figure 6-2 Channel test points – Module to Module routing model example

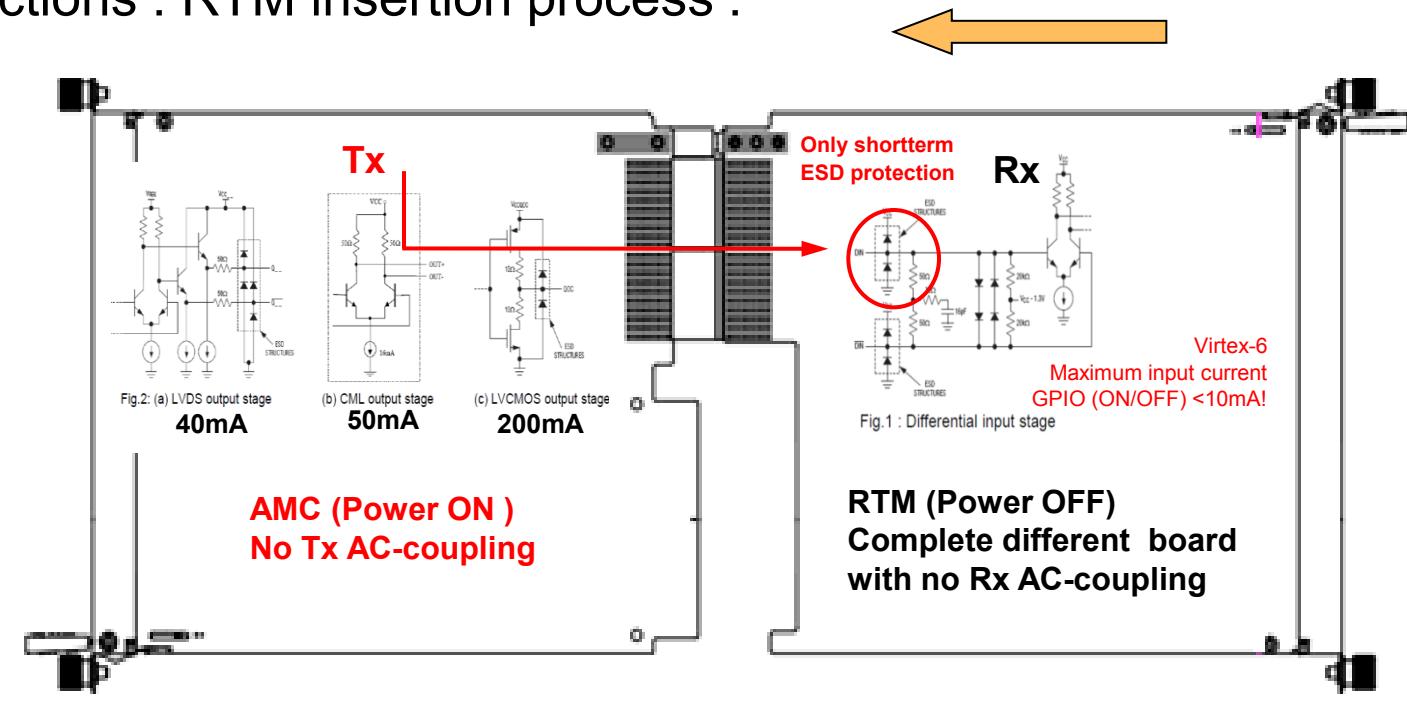


- > Rx AC-coupling -> Rx input protection

MTCA.4 : Electrical Protection during RTM Insertion

FIL

- > Quiesce actions : RTM insertion process :



- > Class A1.1, Class D1.2 → GTP Tx AC-coupling over Zone 3 is a must.

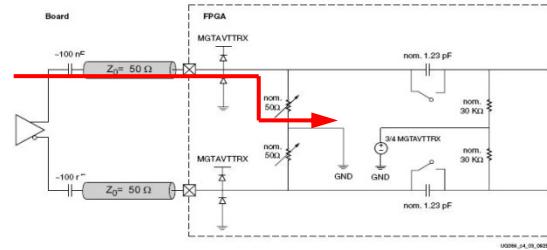
	7 Disabling via FPGA	Disabling via FPGA	
Standard Gbit-Links	8 Disabling via FPGA	Disabling via FPGA	
	9 Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled
10 Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	

Class D1.x (Digital signal transmission)

FIL

> Should we make 0201 placeholders for Rx AC-coupling ?

- (Tx) : (-) Cable distortions were feed into the receiver system,
but Zone 3 is sufficient shielded for digital signals.



- (Tx + Rx) : (?) Floating lines (ESD), but no floating inputs
(+) Always AC-coupling between Boards
(-) High-speed signal degradation from package

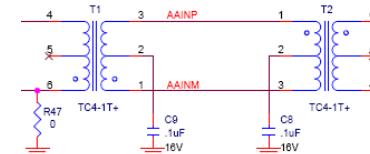


PCIe Gen 3, $C_{tot} = [176nF, 265nF] = C_{Tx} - C_{Rx} \rightarrow C_{Tx} = 220nF$, 0201 pack.

Capacitor value selection: Tradeoff

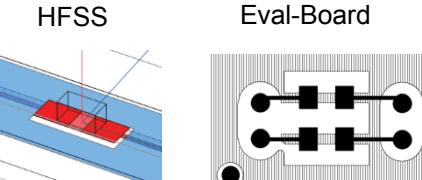
1. Capacitor lower cutoff for the coding scheme
2. Capacitor edges for the rate degradation

$C_{Rx} = 1\mu F$, 0402 pack. (AMC.2, R.2)



> Xilinx References:

V7-> UG483, V6-> UG373, V5-> UG196, V4-> UG076



- Gen. 2, Rx, ok
- Gen. 3 Tx 0201, 220nF
- (TCK7) Rx 0201, 0Ohm with no GND cutout
- Gen. 4 ? Rx seems a limitation
- > High-Speed Signal Integrity BoF Group DM + SIMULATION

Class A1.2 (Analog signal transmission – 32 ADCs - Draft)

FIL

> Backward compatible to Class A1.1 ?

	a	b	c	d	e	f
J30	1 PWRA1 2 PWRA2	PWRB1 PWRB2	PS# MP	SDA SCL	TCK TDI	TDO TMS
3 SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-	
4 D3+	D3-	D4+	D4-	D5+	D5-	
5 D6+	D6-	D7+	D7-	D8+	D8-	
6 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-	
7 gnd	gnd	gnd	gnd	gnd	gnd	
8 RTM_CLK4+	RTM_CLK4-	CH26+	CH26-	CH25+	CH25-	
9 RTM_CLK0+	RTM_CLK0-	CH28+	CH28-	CH27+	CH27-	
10 CH31+	CH31-	CH30+	CH30-	CH29+	CH29-	

Yes →

- 10 DC-Channels
- 5 DACs
- Low-jitter clocks
- IOs



	a	b	c	d	e	f
1 PWRA1 2 PWRA2	PWRB1 PWRB2	PS# MP	SDA SCL	TCK TDI	TDO TMS	
3 SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-	
4 AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-	
5 CH15+	CH15-	RTM_CLK4+	RTM_CLK4-	CH31+	CH31-	
6 CH30+	CH30-	RTM_CLK0+	RTM_CLK0-	CH14+	CH14-	
7 CH13+	CH13-	D3+	D3-	CH29+	CH29-	
8 CH28+	CH28-	D4+	D4-	CH12+	CH12-	
9 CH11+	CH11-	D5+	D5-	CH27+	CH27-	
10 CH26+	CH26-	D6+	D6-	CH10+	CH10-	

1 CH9+	CH9-	D7+	D7-	CH25+	CH25-	
2 CH24+	CH24-	D8+	D8-	CH8+	CH8-	
3 CH7+	CH7-	DAC0+	DAC0-	CH23+	CH23-	
4 CH22+	CH22-	DAC4+	DAC4-	CH6+	CH6-	
5 CH5+	CH5-	DAC1+	DAC1-	CH21+	CH21-	
6 CH20+	CH20-	DAC5+	DAC5-	CH4+	CH4-	
7 CH3+	CH3-	DAC2+	DAC2-	CH19+	CH19-	
8 CH18+	CH18-	DAC6+	DAC6-	CH2+	CH2-	
9 CH1+	CH1-	DAC3+	DAC3-	CH17+	CH17-	
10 CH16+	CH16-	DAC7+	DAC7-	CH0+	CH0-	

No





Convener BoF Group1
Dr. Frank Ludwig
frank.ludwig@desy.de

Thanks for
your attention!

Class A1.1 (Analog signal transmission)

FIL

> Zone 3 Electrical Specification (AMC side, Rev.A.3.):

Class A1.1 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 PWRA1 2 PWRA2	PWRB1 PWRB2	PS# MP	SDA SCL	TCK TDI	TDO TMS
Standard Gbit-Link		3 LVDS - I	LVDS - I				
User-configuration		4 LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O
Digital fixed I/O		5 LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O	LVDS / LVC MOS / OC - I/O
Shielding		7 gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8 Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω	
Shielding		9 Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω	
		10 gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1 Differential 0 - ±1V / I, 100Ω					Differential 0 - ±1V / I, 100Ω
		2 Differential 0 - ±1V / I, 100Ω	gnd	gnd			Differential 0 - ±1V / I, 100Ω
		3 Differential 0 - ±1V / I, 100Ω					Differential 0 - ±1V / I, 100Ω
		4 Differential 0 - ±1V / I, 100Ω	gnd	gnd			Differential 0 - ±1V / I, 100Ω
		5 Differential 0 - ±1V / I, 100Ω					Differential 0 - ±1V / I, 100Ω
		6 Differential 0 - ±1V / I, 100Ω	gnd	gnd			Differential 0 - ±1V / I, 100Ω
		7 Differential 0 - ±1V / I, 100Ω					Differential 0 - ±1V / I, 100Ω
		8 Differential 0 - ±1V / I, 100Ω	gnd	gnd			Differential 0 - ±1V / I, 100Ω
		9 Differential 0 - ±1V / I, 100Ω					Differential 0 - ±1V / I, 100Ω
		10 Differential 0 - ±1V / I, 100Ω	gnd	gnd			Differential 0 - ±1V / I, 100Ω

- Logic levels : LVDS, LVC MOS, OC, CML
- Signal direction : „I“=input (RTM to AMC) „O“=output (AMC to RTM)
- Any level clock input : AC-coupled and termination on AMC side (Rev. A.2 -> Rev. A.3)
- Fixed output direction : DACx outputs, AMC_TCLK, OUT1, OUT2, SFP

Quiescent Condition

Class A1.1 (Analog signal transmission)

FIL

> Zone 3 Quiescent condition (AMC side, Rev.A.3.):

Class A1.1 / Zone		a	b	c	d	e	f
MTCA.4 management	J30	1 2					
Standard Gbit-Link		3		Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
User-configuration		4 5 6	Disabling via FPGA Disabling via FPGA Disabling via Buffer	Disabling via FPGA Disabling via FPGA Disabling via Buffer	Disabling via FPGA Disabling via FPGA Disabling via Buffer	Disabling via FPGA Disabling via FPGA Disabling via Buffer	Disabling via FPGA Disabling via FPGA Disabling via Buffer
Digital fixed I/O		7					
Shielding		8 9 10					
Digital clock inputs							
Shielding							
Analog signals	J31	1 2 3 4 5 6 7 8 9 10		DAC quiescent condition DAC quiescent condition	DAC quiescent condition DAC quiescent condition		

- Idle-state, AC-coupled : Idle-stated by FPGA, AC-coupled transmitters on AMC and RTM
- Disabling via FPGA : Tri-stated initiated by MMC
- Disabling via buffer : Disabling via buffer controlled by MMC (-> MMC V1.0)
- DACx quiescence : Outputs to zero current or power down mode