Contribution ID: **55** Type: **not specified**

ATCA/MicroTCA based Compute Nodes in the Belle II Pixel Detector DAQ

Thursday 12 December 2013 10:30 (15 minutes)

In this talk we present the application of the MicroTCA based Compute Node in the Belle II experiment at KEK, Japan. The system comprise an ATCA carrier board and AMC board design based on Virtex-4 FX60 and Virtex-5 FX70T FPGAs. It is designed to perform data acquisition of 22 GB/s and data reduction by a factor <10 at the Belle II pixel detector. The firmware programming comprises buffer management with pointer lookup tables, DDR2 memory access using NPI (native port interface), optical link data transfer using GTX transceivers and Aurora 8B/10B, SERDES links and custom UDP and TCP/IP interfaces. A parallel region-of-interest (ROI) algorithm performs data reduction of the PXD data based upon charged track extrapolation from the high level trigger and silicon strip vertex detector, arriving with a large latency and out of order. First test of the full DAQ readout chain with a scaled down system, using a uTCA shelf instead of the carrier boards, have been performed recently at DESY as preparation for a beam test in January 2014.

Primary author: Dr SPRUCK, Bjoern (University Giessen)

Presenter: Dr SPRUCK, Bjoern (University Giessen)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities