MTCA.4 Fast Digitizer

+applications for LLRF systems @ DESY

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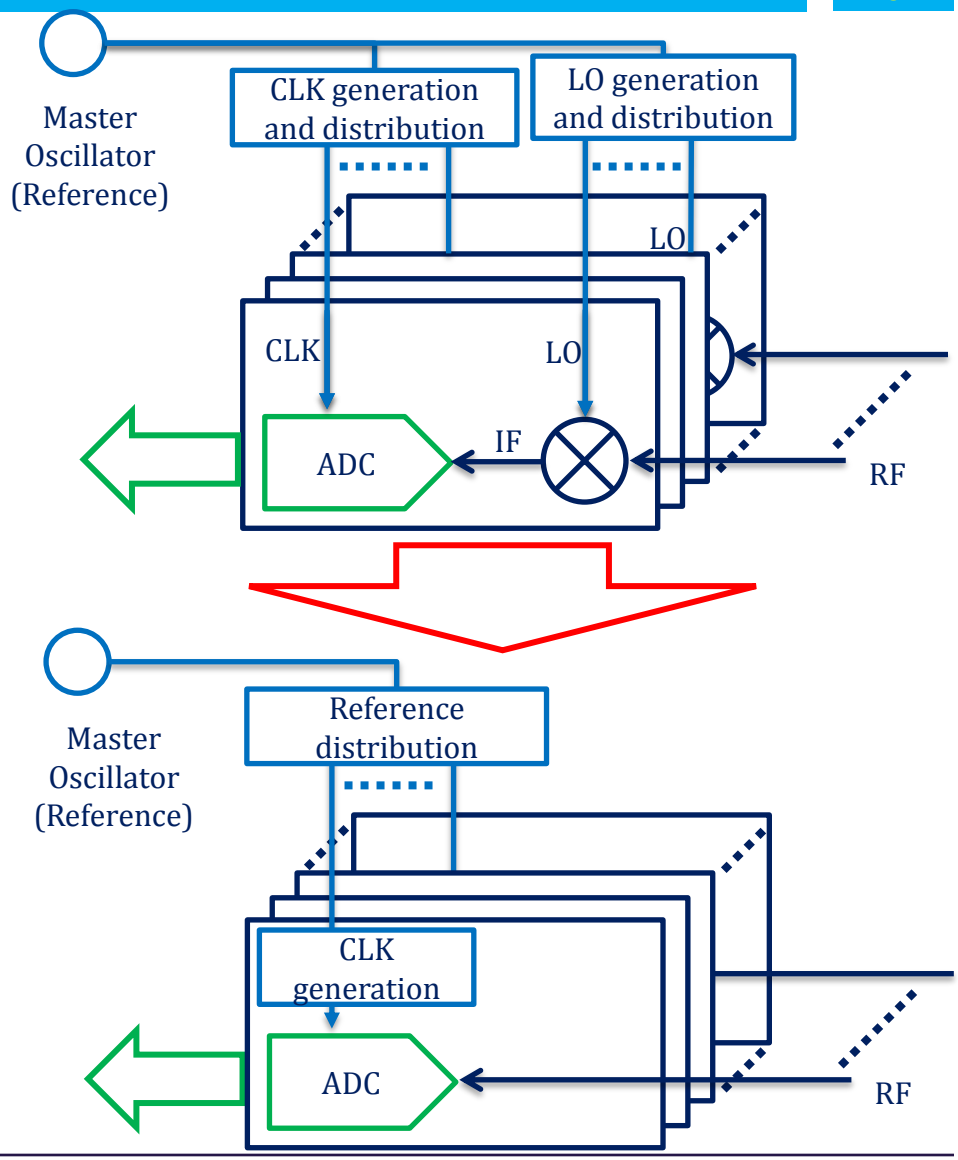
Agenda

- Introduction
- DAMC-DS800 digitizer
- ADC measurements
- Applications
- Summary

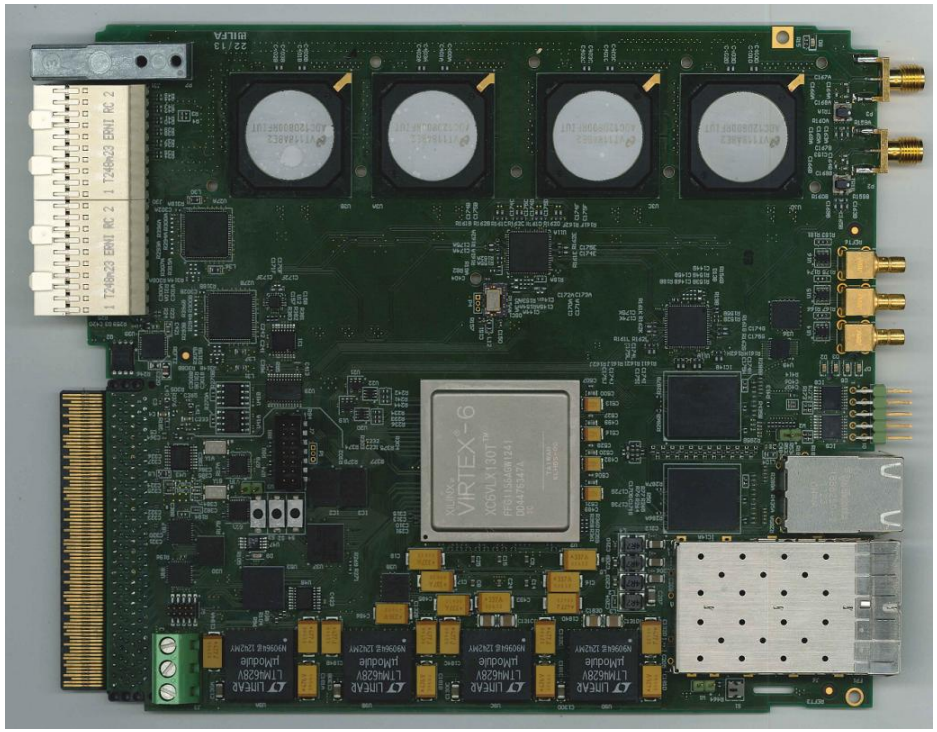
Introduction

- Direct sampling of signals of frequencies ≥ 1.3 GHz
  - No DWC
  - No LO generation
- Very high sampling rates (>500 MSPS) ⇒ very low latencies
- Using undersampling to obtain information on amplitude, phase, and shape of signals
- Different Applications

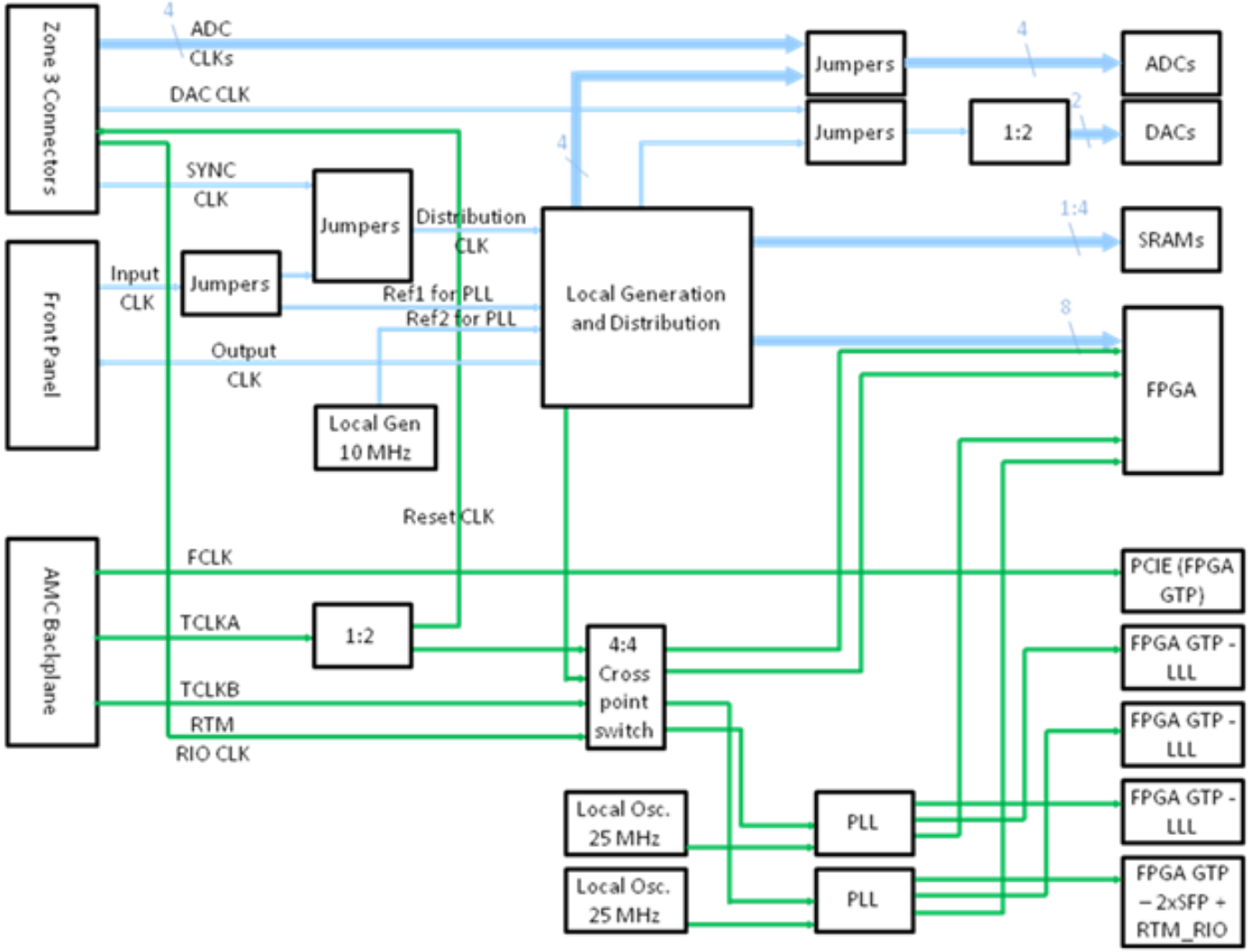


DAMC-DS800

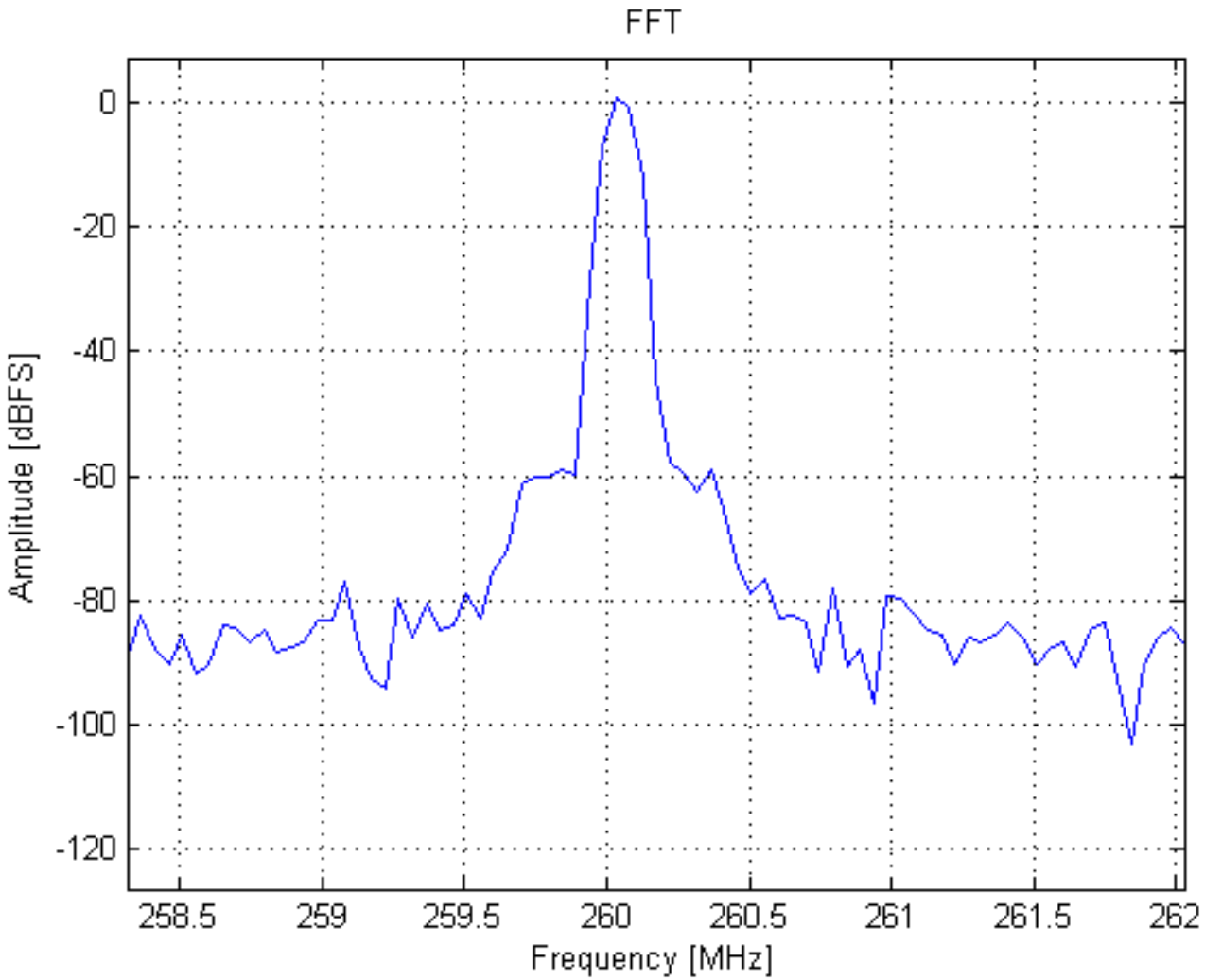
- AMC Fast Digitizer Card
- MTCA.4 Analog A1.1 class compliant
- 8 analog channels (AC or DC) up to 2.7GHz @ 800 MSPS 12-bit ADCs OR 4 channels @ 1600 MSPS
- 4 16-bit DACs up to 250 MSPS
- Very complex low noise/jitter CLK generation and distribution System
- Triggers, SRAM, communication interfaces…



DAMC-DS800

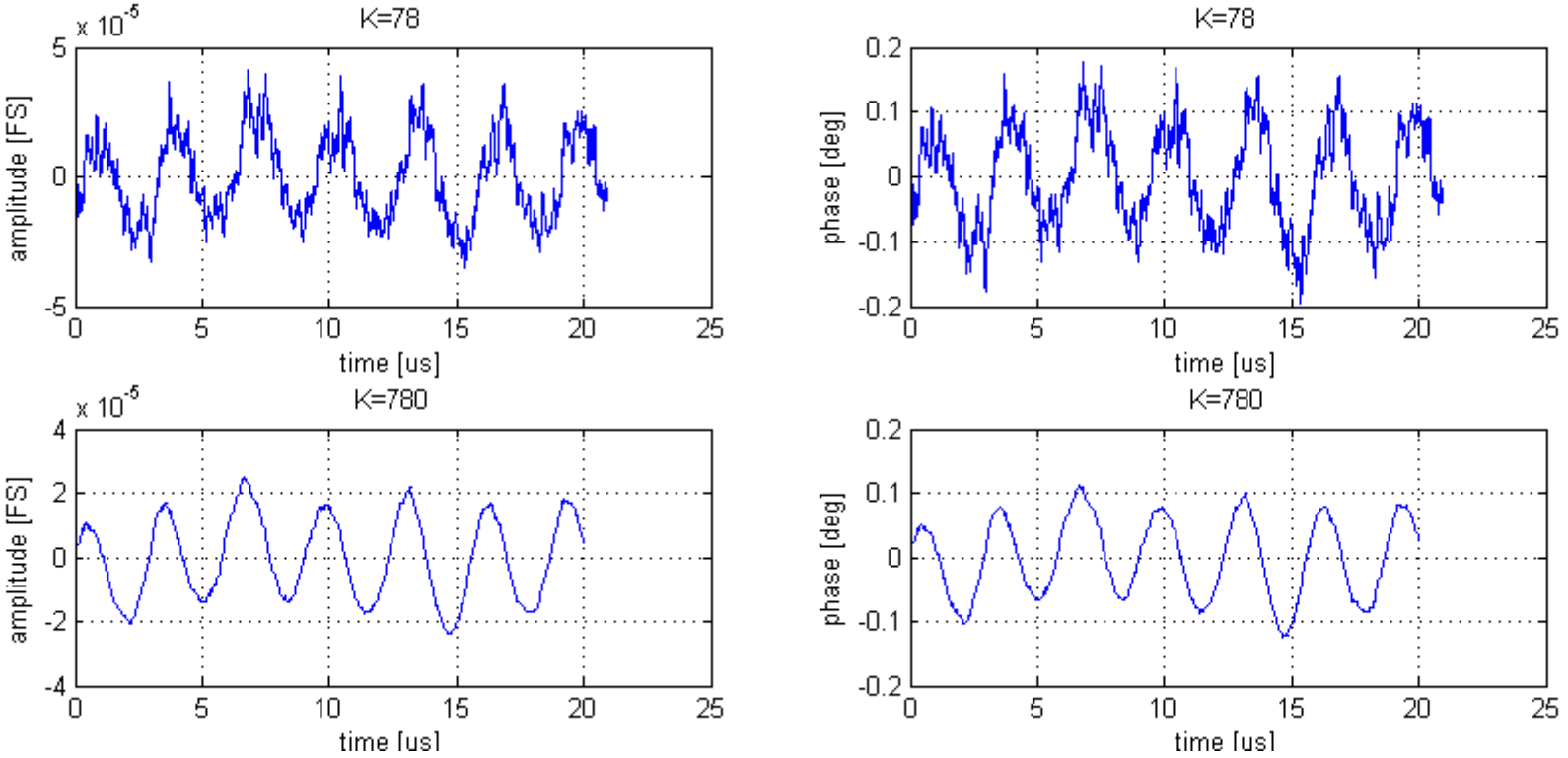

Zone 3 Connectors
Front Panel
AMC Backplane
4
ADC
CLKs
DAC CLK
SYNC
CLK
Input
CLK
Output
CLK
Jumpers
Jumpers
Distribution
CLK
Ref1 for PLL
Ref2 for PLL
Local Gen
10 MHz
Reset CLK
FCLK
TCLKA
TCLKB
RTM
RIO CLK
1:2
4:4
Cross
point
switch
Local Osc.
25 MHz
Local Osc.
25 MHz
PLL
PLL
Jumpers
Jumpers
1:2
Local Generation
and Distribution
ADCs
DACs
SRAMs
FPGA
PCIE (FPGA
GTP)
FPGA GTP -
LLL
FPGA GTP -
LLL
FPGA GTP -
LLL
FPGA GTP
– 2xSFP +
RTM_RIO

Sampling 1.3GHz at 780 MSPS



- SNR : ~55 dB
- ENOB : ~8.75

First ADC tests



Rms resolution from demodulation (10 MHz BW)		Rms resolution from demodulation (1 MHz BW)		Rms resolution from demodulation (100 kHz BW)	
Amplitude	Phase	Amplitude	Phase	Amplitude	Phase
0.0016%	0.077°	0.0013%	0.062°	0.0001%	0.0045°

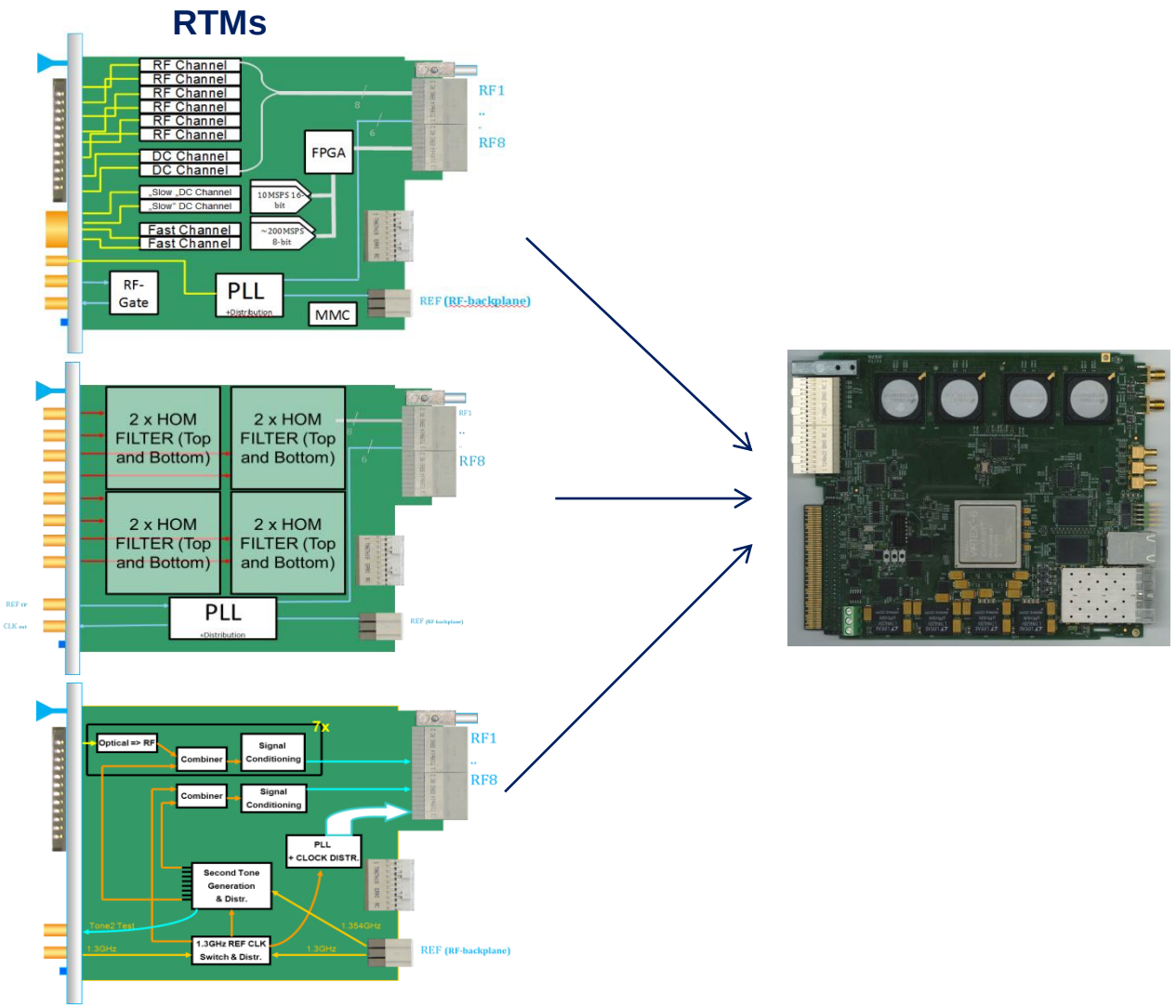
DAMC-DS800 + RTMs

Application examples:

Klystron life-time Management

High-Order Mode measurements (1.3/1.7/2.4GHz)

Femtosecond Fiberoptic Synchronisation

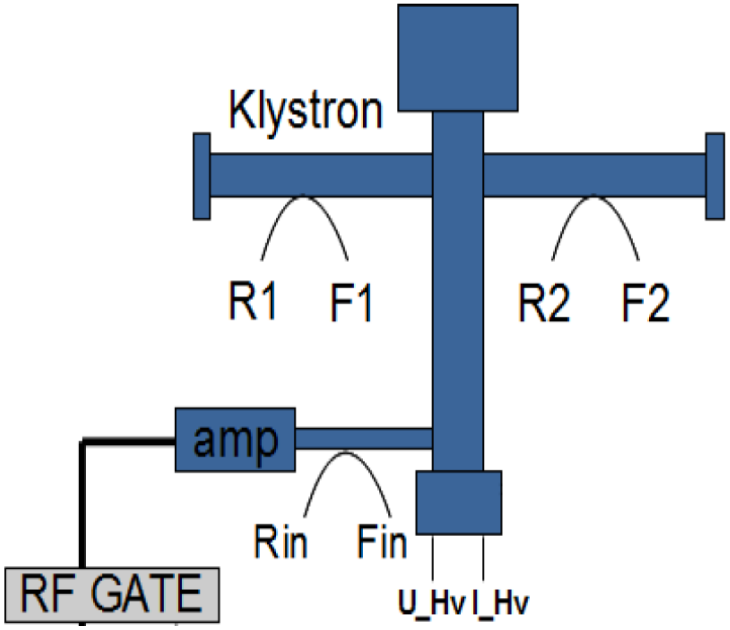


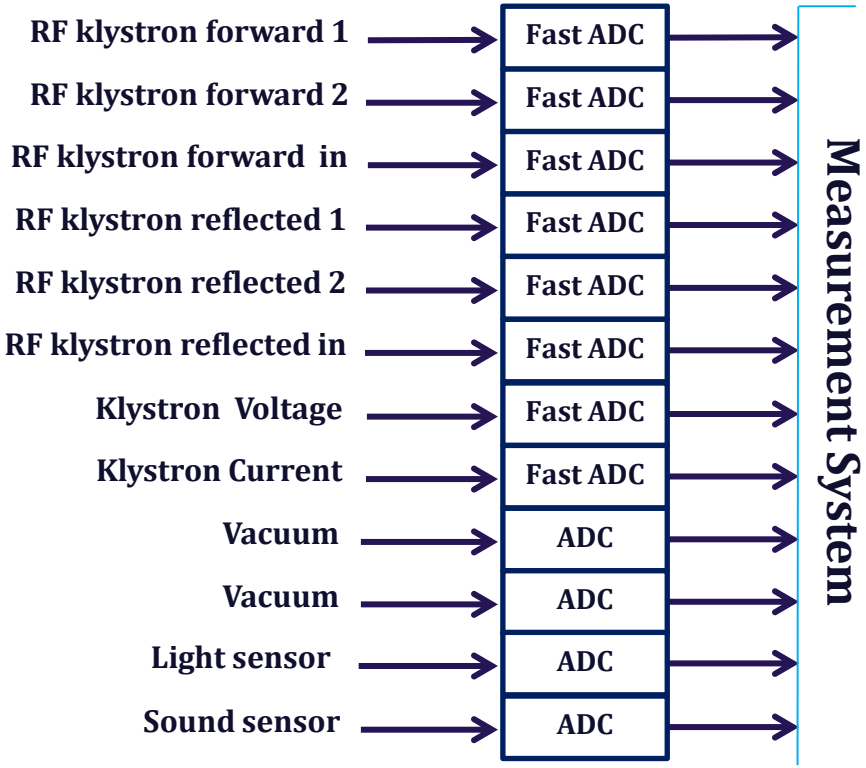
Klystron Lifetime Management

- Measurements of klystron parameters
- Detection of exceptional events
- Fast reaction to „abnormal" activity
- Tube recovery procedure according to detected event

⇒ Fast interlock and measurement system with reaction time < 250 ns

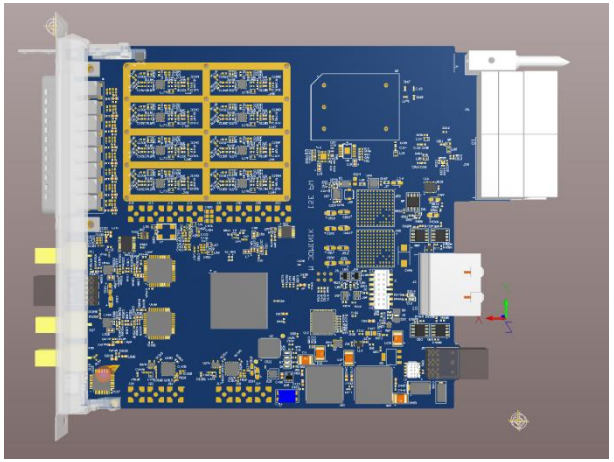
Klystron Lifetime Management

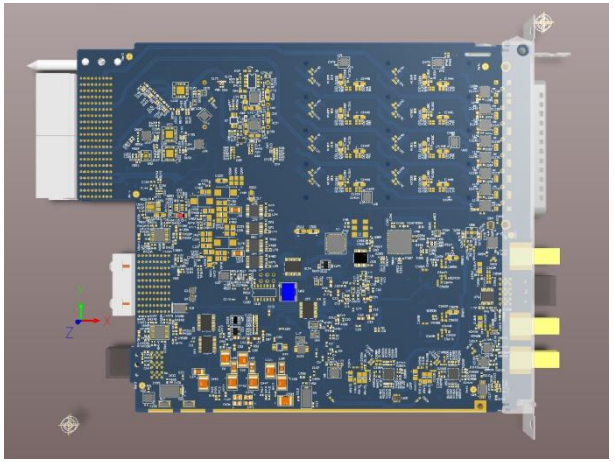




Applications – KLM/GP RTM

- 8 Channels
  - AC coupled: 400-2700 MHz BW
  - DC coupled: DC-2700 MHz BW
  - Possible filter implementation
- 2 x 8-bit ADC @ 250 MSPS
- 2 x 16-bit @ 10MSPS with very high ENOB >15 bits
- 2 Output channels (e.g. 2x VM) with RF-Gates
- Very Low Noise PLL and CLK distribution system
- For KLM: ADC + Calculations delay <55ns vs 168 ns in current system

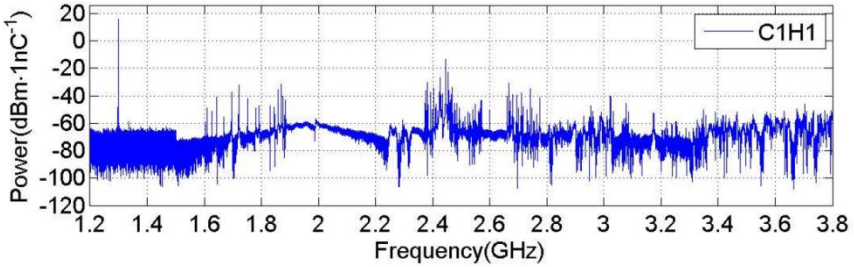


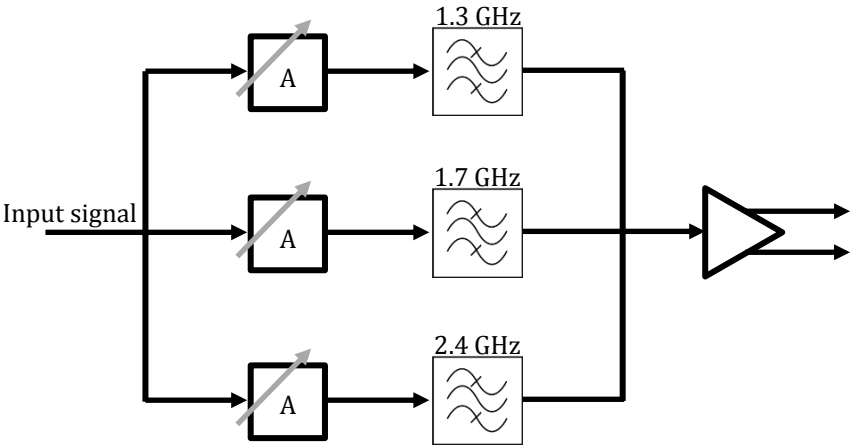


High Order Modes Measurements

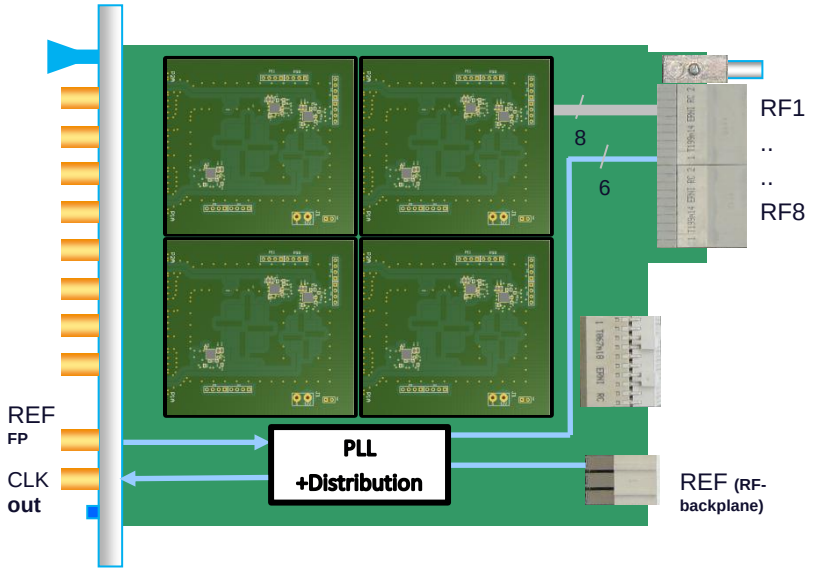
- Measurements of High Order Modes from couplers at cavities
- 3 frequencies filtered out:
  - 1.7 GHz – used for bpm and cavity allignment
  - 1.3 GHz – RF power
  - 2.4 GHz – from beam, for phase measurement w.r.t the 1.3 GHz

Applications – DRTM-HOM





- MTCA.4 A1.1 RTM designed
- 8 Channels each with a triple passband filter
- Very Low Noise PLL and CLK distribution system



Conclusion

- Very high speed AMC digitizer designed and being tested
- RTM designs/measurement in progress
- To be installed for LLRF (KLM and HOM)
- Implementations for other systems in progress

Thank you for your attention

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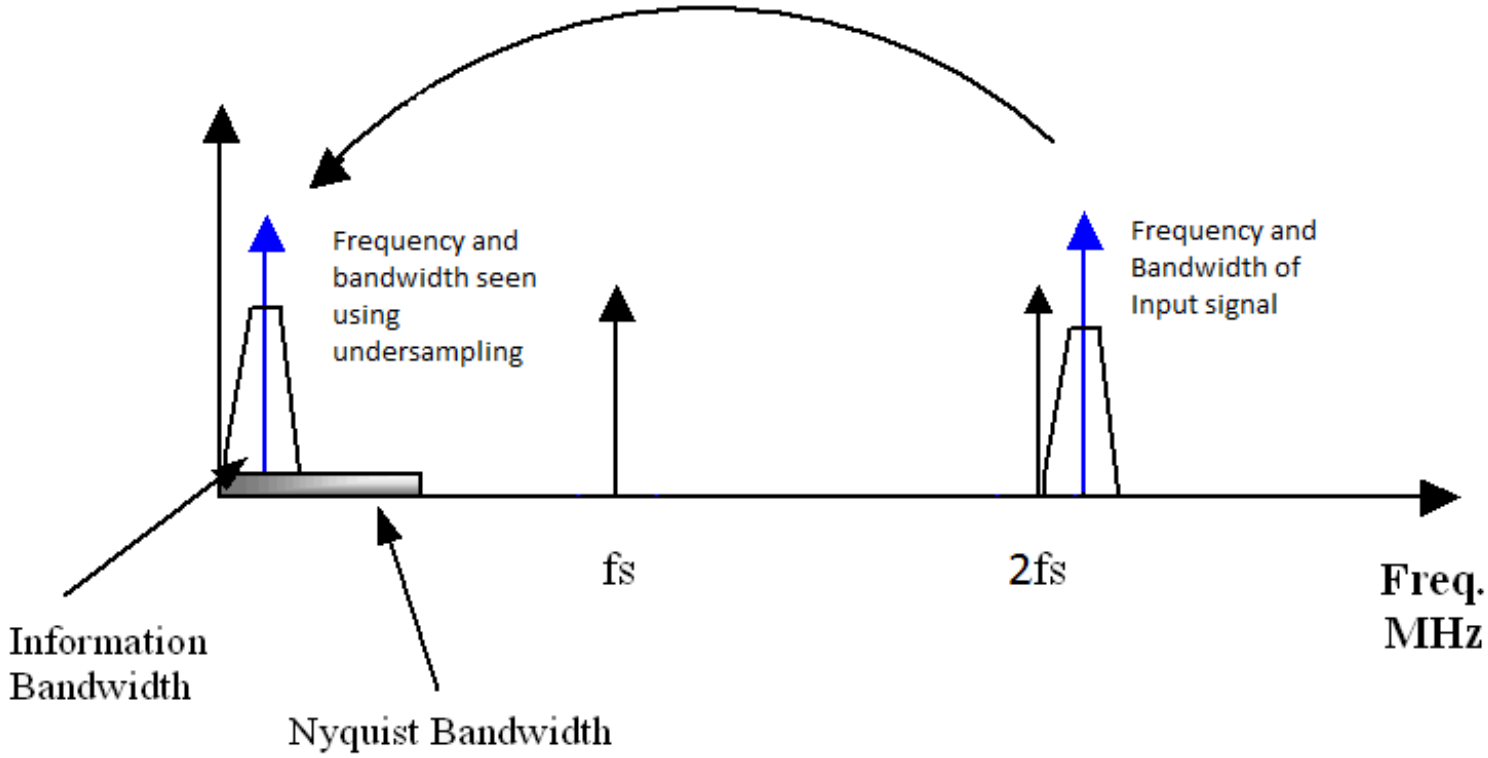
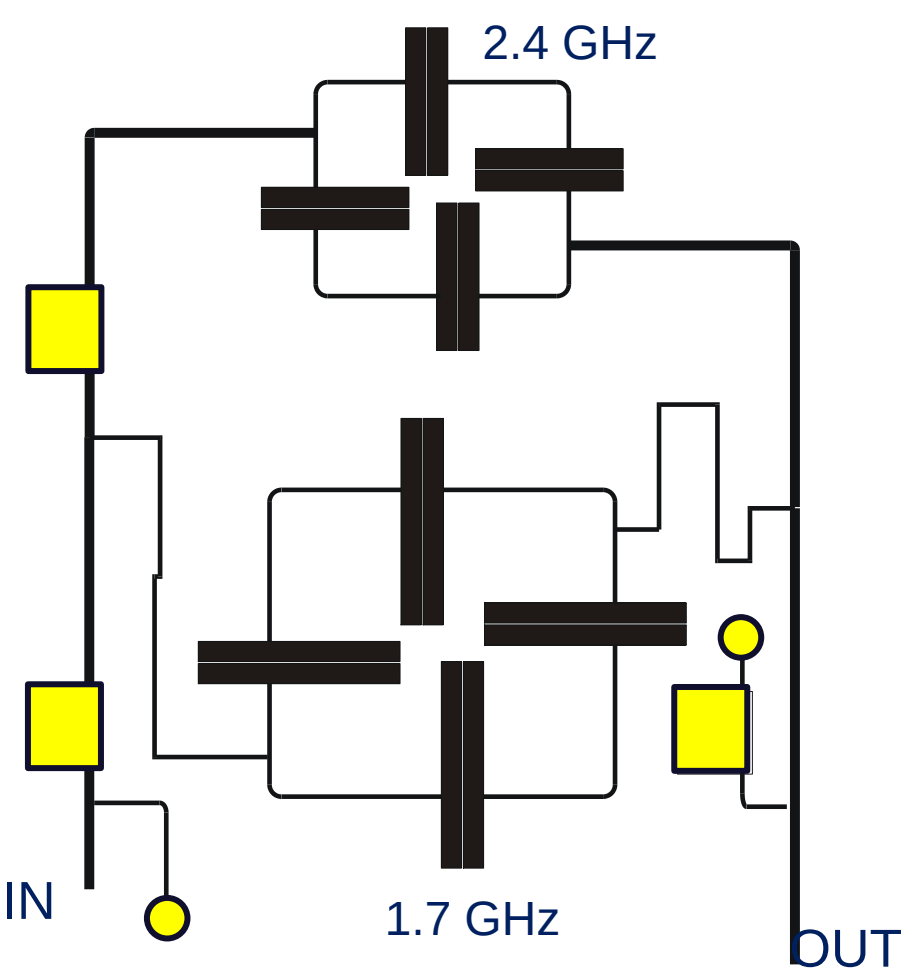
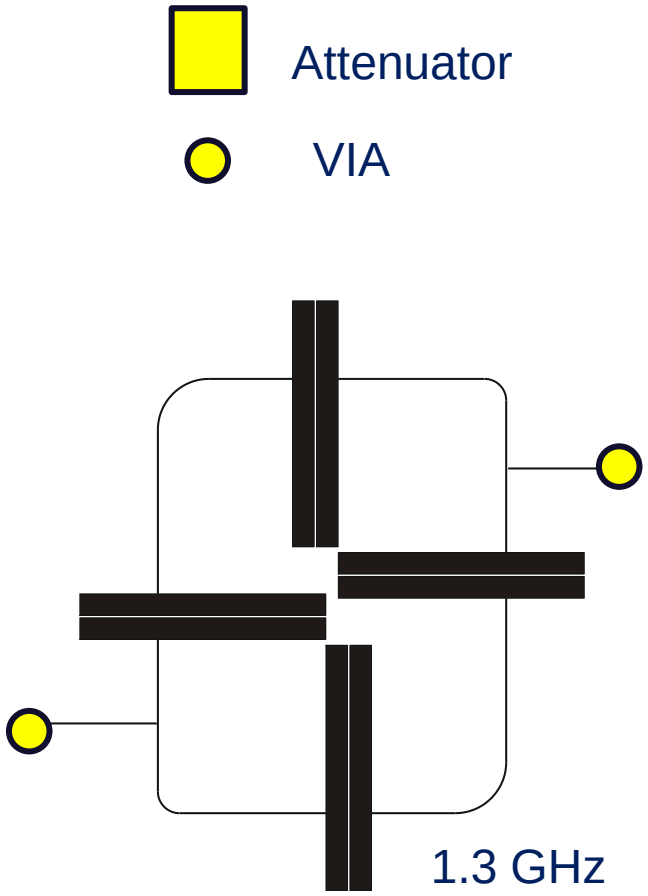
Undersampling



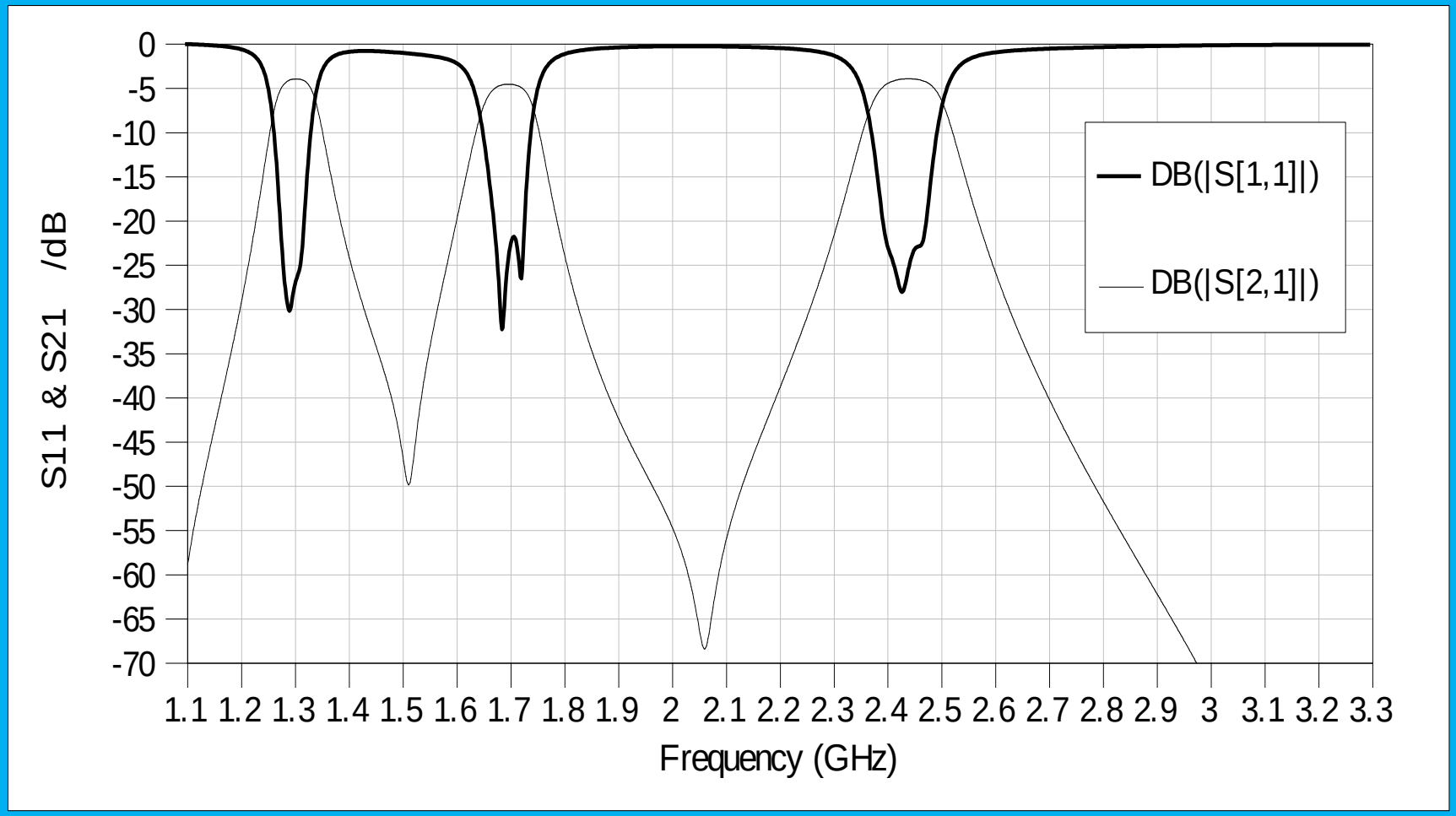
- ADC BW > Fin
- Fs > 2*Fin BW

HOM Filter Design





HOM Filter Characteristics

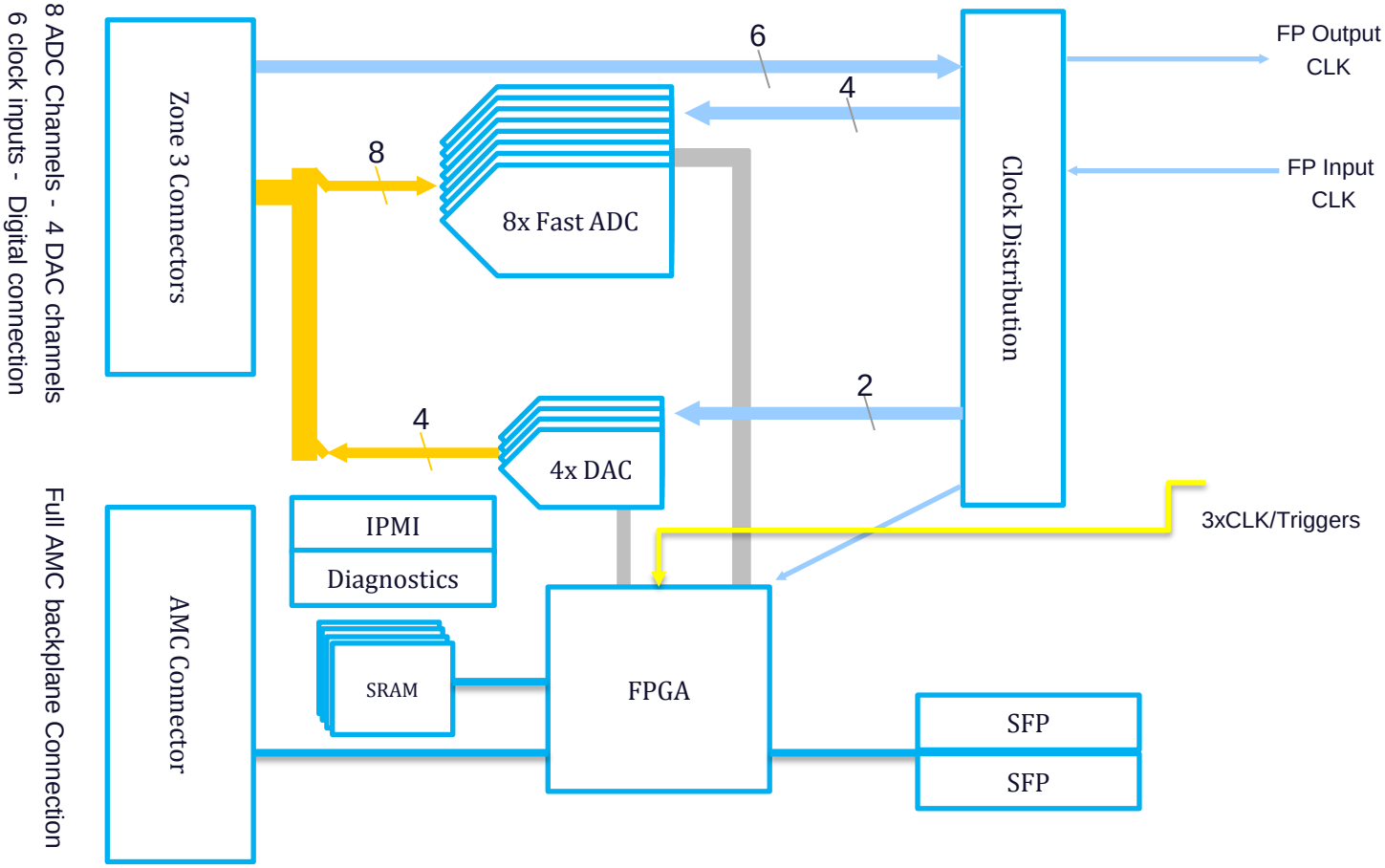


HOM Filter Design

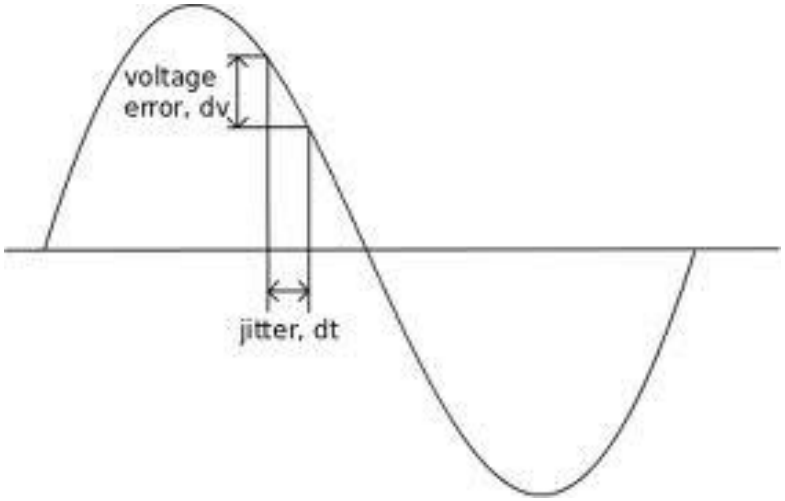
- f_1=1300 MHz, BW=37 MHz (at RL=-20 dB), IL_0=4 dB, n=4 stripline, substrate height 0.204 mm, size 35x35 mm
- f_2=1700 MHz, BW=55 MHz (at RL=-20 dB), IL_0=4.5 dB, n=4 microstrip, substrate height 0.204 mm, size 45x35 mm
- f_3=2400 MHz, BW=74 MHz (at RL=-20 dB), IL_0=4 dB, n=4 microstrip, substrate height h_1=0.204 mm, h_2=0.25 mm size 45x25 mm

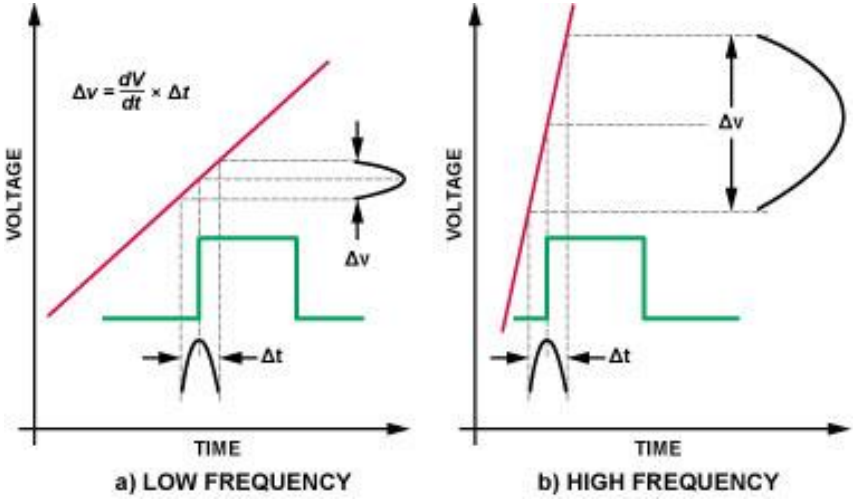
- (2 and 3 together on the same layer) size **45x60 mm**
- all filters (2 and 3 up, 1 down) size needed **55x70 mm - (max)**

DAMC-DS800 Block diagram

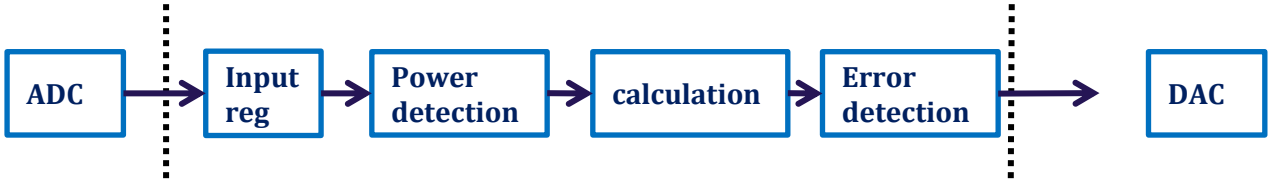


DAMC-DS800


voltage
error, dv
jitter, dt


$\Delta v = \frac{dV}{dt} \times \Delta t$
VOLTAGE
Δv
Δt
TIME
a) LOW FREQUENCY
VOLTAGE
Δv
Δt
TIME
b) HIGH FREQUENCY

Klystron Lifetime Management



ADC Delay + 2 clock +3 clock + 4 clock + 1 clock = 14 clock

27 ns + (26 ns) = 53 ns vs. 168 ns current system