Status of MTCA.4 Standards & SLAC Overview

2nd MTCA.4 Workshop for Industry & Research

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SLAC National Accelerator Laboratory

December 11, 2013

Outline

I. Brief Status of MTCA.4 Standards, Guidelines, Roadmaps, New Tasks

II. SLAC MTCA.4 New Developments & Goals

III. Conclusion

IV. Acknowledgments

V. Appendix: Additional Slides

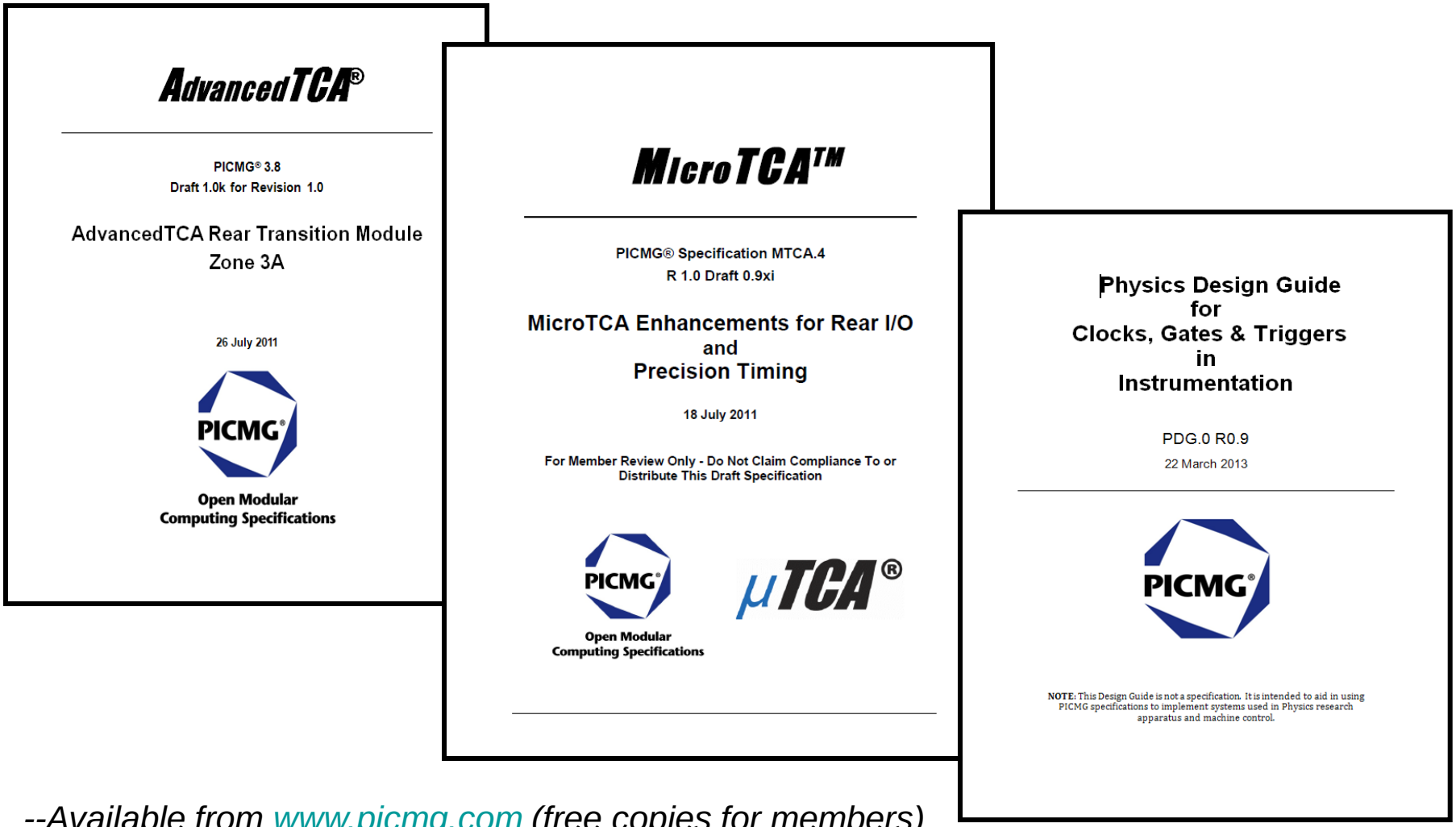
I. Status – xTCA for Physics TC's

- *Technical Committees: (KAVI PICMG members website)*
  - Physics Timing & Synchronization (HWG)
    - R. Downing, D. Somes, V. Pavlicek
  - Software Architecture & Protocols (SWG)
    - S. Simrock, A. Lowell, Zhen'An Liu
  - xTCA for Physics (CC, Coordinating Committee)
    - R. Larsen
  - *New*: Physics xTCA for Physics Roadmap Group (PICMG request)
    - R. Larsen
- *Workshops*
  - *2007 (FNAL), 2008 (NSS-MIC Dresden), 2009 (IHEP Beijing), 2010 (Real Time IPFN Lisbon), 2011 (NSS-MIC Valencia), 2012 (DESY MTCAWS 1), 2013 (DESY MTCAWS 2), 2014 (Real Time Nara Japan)*

Technical Committees (WGs)

- *Original Goals: Extend PICMG Standards*
  - ATCA RTM Standard: PICMG 3.8 √
  - ATCA Clocks, Gates & Trigger Guideline: PDG0 R09 √
  - MTCA Rear I/O & Precision Timing: MTCA.4 √
  - Develop guidelines for Software-Firmware systems WIP
- *Progress*
  - 2 Standards, completed, reviewed, issued in 2011
  - Design Guide ATCA clocks, gates triggers in 2013
  - *HW Group finished Statement of Work; new group & SOW needed*
  - Significant progress on SW Guidelines; none issued to date
  - *SW now urgent to achieve interoperability goals – See Talk 44*

*MTCA.4 *PICMG 3.8 *PDG 0 R09



--Available from www.picmg.com (free copies for members)

xTCA Software Extensions for Physics

- Committee Purpose:
  - *Facilitate inter-operability/interchangeability between facilities and projects*
  - *Facilitate availability of COTS solutions, interoperability at applications level*
  - *Reduce software development time and cost*
- Goals:
  - *Define common techniques, interfaces, and modules for software development*
  - *Create guidelines and examples for those who must create/interact with module management software to make as easy as possible*
  - *Extend some standardization into the application space*
- Status
  - *See presentation 44, A. Lowell and D. Makowski, 17:30 Dec 12/13*.

Courtesy A. Lowell

Roadmaps – New Hardware Goals

- µRTM Interface management, I/O standards
  - Basic RTM IPMI, power interface defined but raise new management issues to be solved
  - Standardizing I/O connectivity for classes of modules, e.g. ADC-DAC, generic FPGA, for various adapter modules
  - Achieve complete interface *interoperability* between labs designs, vendor AMCs & RTMs
- Major Goals
  - Simplification of user implementation of IPMI interface with standard *Reference Designs, I/O configuration, COTS availability*
- Interoperability
  - *Achieve highest level of AMC-RTM interface standardization for most successful lab-industry interoperable products*
  - *Interface standardization does not compromise Intellectual Property of core vendor products (min. 2 COTS sources of key products PICMG rule)*

Interoperability Goals: Lab Infrastructure Workshops

- Reduce infrastructure startup complexity for all
  - Historically IPMI & Power Systems testing of COTS products
  - Heavily ATCA, AMC industry-driven
  - Success of xTCA collaboration lies in adapting IPMI as major tool; alleviating demanding startup complexity
  - New system-level collaboration needed (Rehlich-Simrock-Larsen)
- Proposed Actions xTCA Coord. Committee
  - Organize Lab-Industry Interoperability Workshops 2/yr. at Labs
  - Test COTS Physics products plus new lab designs
  - Full AMC-RTM IPMI management + clock/timing products, configurations
  - *Note: Test results private to participants!* (Identify, fix problems; re-test; claim PICMG compatibility for products)

Roadmaps –New Standards/Guidelines

- Hardware Examples
  - Basic HW *reference design* AMC, RTM with IPMI, FRU support
  - RF Backplane Distribution for Local Oscillator
  - RF Generator Module in Rear IO non-payload slot
  - Zone 3 I/O for Generic AMCs to Custom RTMs
    - *High speed ADC-DAC* to LLRF Down-mixer, BPM RTMs
    - *FPGA* to Analog Front End RTM, e.g. Toroid, Interlocks RTMs
    - *Industry Pack Adapter* to external Device Interface, e.g. Temperature, Digital I/O, Motor driver RTMs etc.
    - *I/O standards enhance HW/SW interoperability, do not threaten proprietary core circuitry or SW.*

Roadmaps – SW & Protocols Guidelines

- Software Examples – Pending, Proposed
  - Common Hardware API
  - Common Process Thread Model
  - Common I/O Device Model
  - Data Transport Protocol
  - Synchronization Protocol
  - Command Control Protocol
  - Component Management/Failover/Update Protocol
  - Common FPGA configuration register assignment
  - Common FPGA architecture/download protocol
    - *See talk 44- Lowell/Makowski*

Standards Summary: Collaboration

- Hardware Rear I/O & Precision Timing
  - Basic MTCA.4 specification working well; more challenges to fully demonstrate
  - New initiatives: Per PICMG rules group needs to be reformed around new statement of work, goals
- SW Architecture & Protocols
  - Much work done but committee needs more workers to complete, consider further extensions; more labs & industry partners needed
- Collaboration Essential to Grow
  - Labs, Industry have large investment which now needs completion of original goals, new extensions
  - Committees need new people, leadership to maximize return on investment, achieve ultimate interoperability HW, SW, FW

III. Collaboration Requirements 2

- Industry
  - Working to achieve next level of I/O compatibility at base level of IPMI interoperability mandatory
  - Compatibility at next level of RTM Zone 3 highly desirable; will increase market overall; reduce development costs for new designs
  - Standardizing I/O should not compromise vendor's Intellectual Property at embedded design or hardware device level

II. SLAC MTCA.4 Developments & Goals

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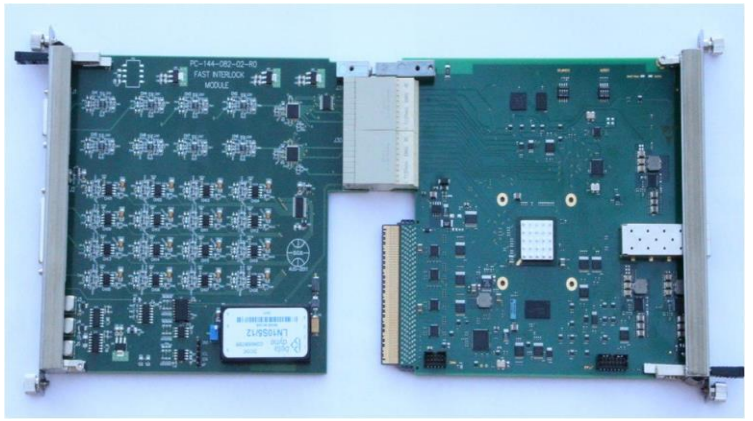
- LCLS-II Injector
  - LLRF System for 6 RF Stations; 15 BPMs lab-operational
  - *Program halted to switch to 1MHz CW Superconducting machine*
  - Injector systems to be installed later for High Energy machine R&D, Plasma Wakefield acceleration etc.
- New Superconducting CW Linac
  - 0.5 km high power beam, 1 MHz pulse rate, 1.3 GHz RF
  - No pulsed modulators; IOT RF sources
  - LLRF controls, BPMs very similar to xFEL requirements; higher continuous data rates (MTCA.4 Backplane bandwidth ideal)
- Upgrade SLAC Legacy CAMAC Controls
  - Plans submitted to replace all legacy CAMAC in Linac with MTCA.4

RTM-AMC Lab-Industry Family

A. SLAC RF RTM + Industry AMC ADC-DAC



C. Fast-Slow Interlock ADC RTM + Industry FPGA AMC

B. SLAC BPM RTM + Industry ADC-DAC

D. Industry AMC 3-Industry-Pack Adapter + Industry RTM

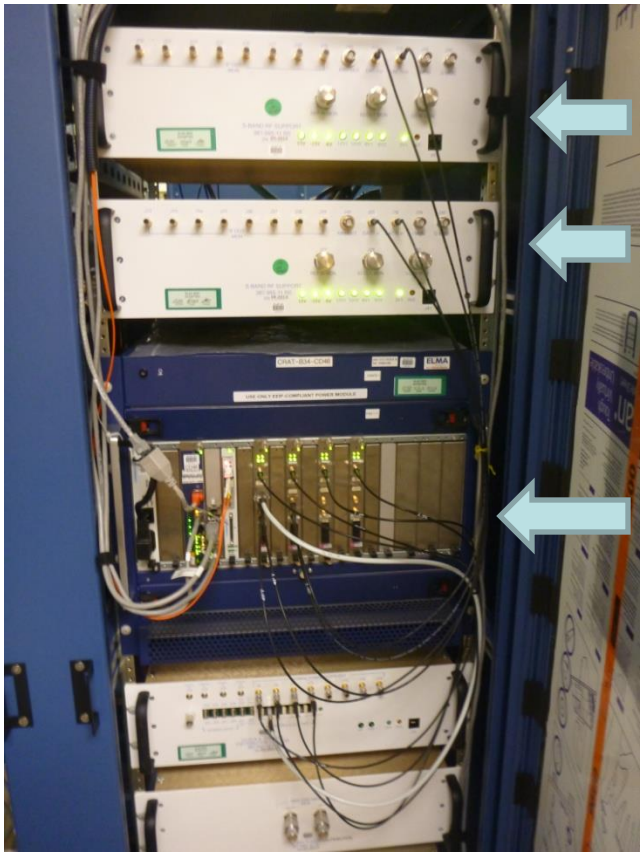
BPM Development

MTCA.4 12 Slot Crate
8 - SIS8300 Struck ADC-DAC AMCs
2 Crates in Injector System

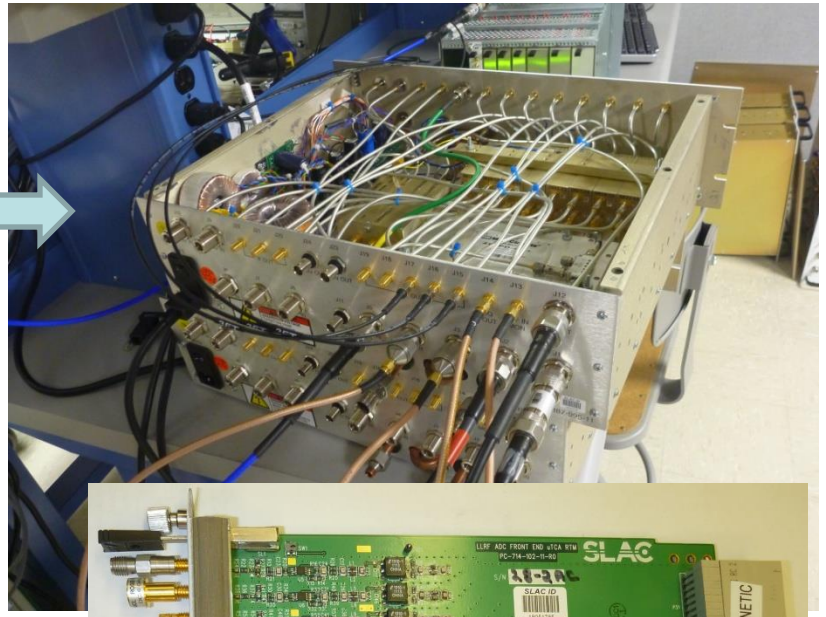
Stripline BPM RTM
4 Ch gain, BP Filter, Calibration Pulser

See A. Young et al Presentation

LLRF Development

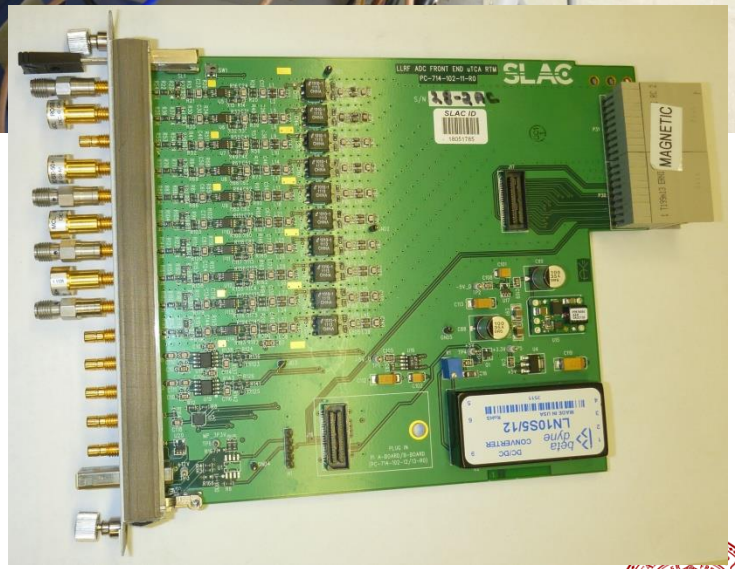


Legacy Down-Mixer Chassis



MTCA Chassis w/ 4 LLRF 10 Ch ADC-DAC's

LLRF 10 Ch RTM



SLAC Infrastructure Developments

- Major efforts on LLRF, BPMs, Infrastructure
  - Testing COTS Crates, Power & Cooling, MCH, Processors
  - Developed EPICS SW, IPMI, Firmware
  - Timing solution using DESY-Stockholm model – started testing, not yet implemented, workaround chassis for small systems to date
  - *See Appendix slides for more Infrastructure details*
  - *Also see talk 52 on Real Time Performance of Linux-MTCA, Dec 12 1715 hrs. by K. Kim, SLAC*.

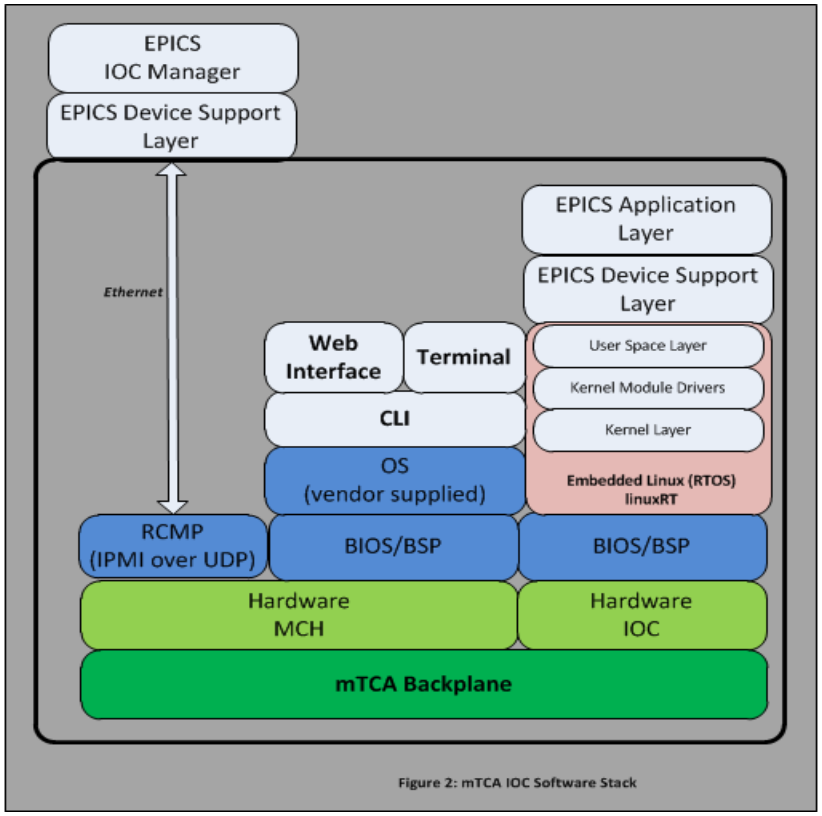


Figure 2: mTCA IOC Software Stack

III. Conclusions

- Laboratory interest in MicroTCA growing
  - Architecture proven to perform well in very low noise high accuracy LLRF, BPM applications
  - Few generic modules adaptable to multiple applications
  - Several new labs planning to use, collaborating with labs leading developments
  - Industry benefiting from lab programs esp. DESY MTCAWS initiative
- Infrastructure needs more collaboration work
  - IPMI learning curve is steep; more standard solutions needed to make it easy
  - Hardware-Software-Firmware standardization key to products easily adapted and shared among labs and industry, short time to market

IV. Acknowledgments

- xTCA for Physics Lab-Industry TC's

  Far too many to name! Special mention to Kay Rehlich & DESY team, R. Downing, S. Simrock, Gus Lowell, Dariusz Makowski, Vince Pavlicek, Zhen'An Liu, J. Sousa, J-P Cachemiche, Industry team members from Elma, Schroff, Struck, NAT, TEWS, Hytek, Vadatech, Wiener, Telkoor, others

- SLAC µTCA Team

  D. Anderson, S. Condamoor, J. Dusatko, T. Himel, B. Hong, S. Hoobler, K. Kim, D. Rogind, T. Straumann, T. Vu, D. van Winkle, E. Williams, C. Xu, C. Yee, A. Young

Appendix – Additional Slides

Lab Applications & Infrastructure Examples

Infrastructure – Hardware 1

- Hardware common to our control system platform:
  - 12-slot MTCA.4 Shelf
  - MCH
  - Power Modules
  - CPU AMC
  - QUAD Ethernet AMC
  - Timing/Event Receiver Card *{on an PMC Carrier}*
    - Still no timing on backplane :(

Infrastructure – Hardware 2

12-Slots mTCA 0.4 Shelf

WEINER PM

NAT MCH PHYSIC

Concurrent CPU AM310/302

Vadatech carrier & EVR-230

Ethernet card SB-AMC59M

Dec 11, 2013

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LELAND STANFORD JUNIOR UNIVERSITY

Infrastructure – Hardware 3

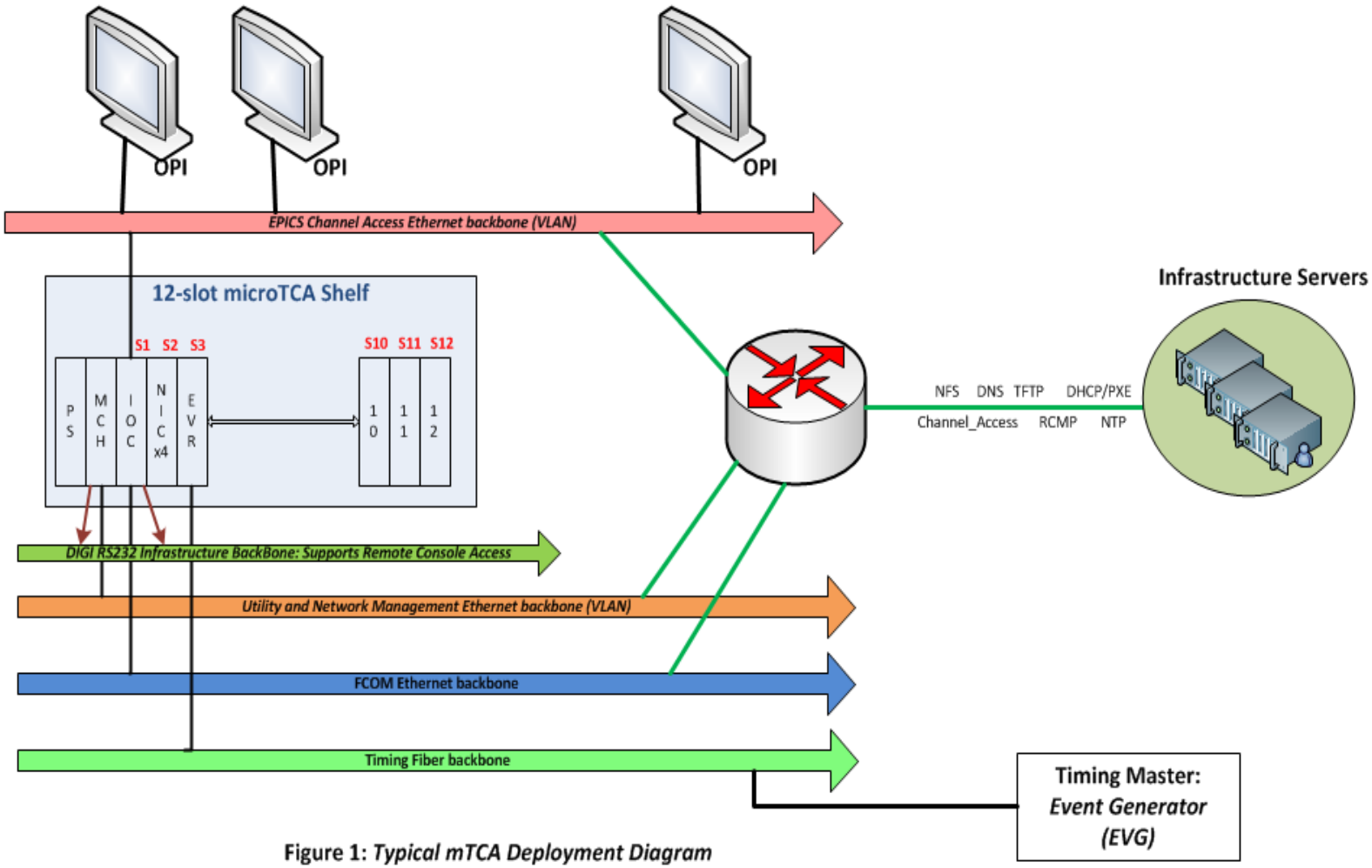
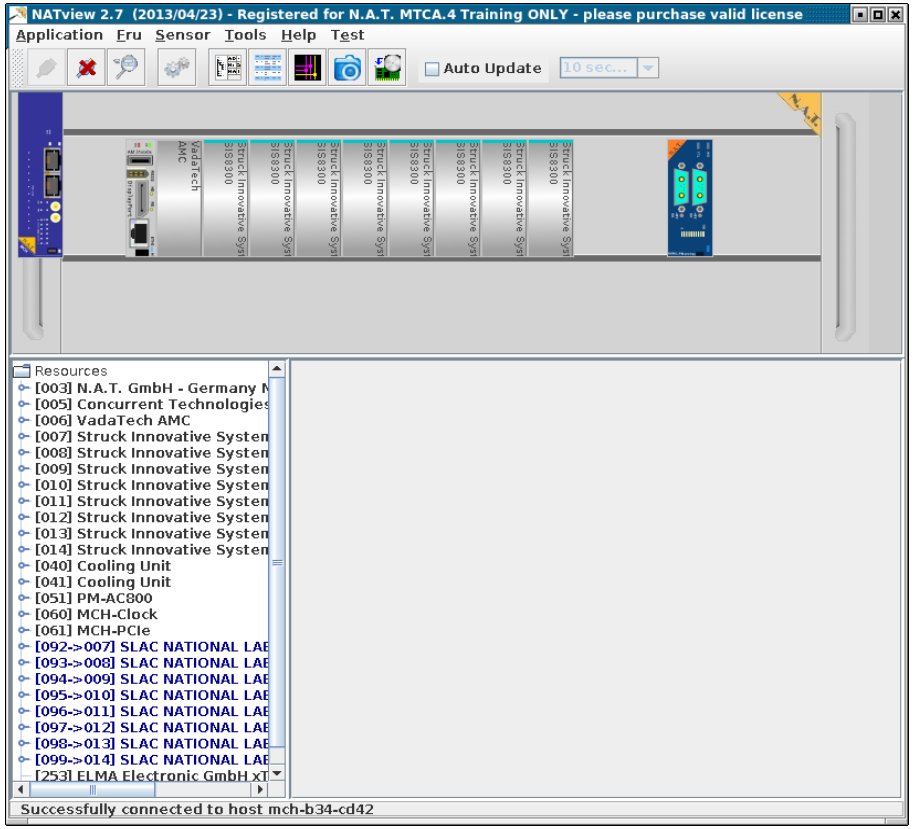


Figure 1: *Typical mTCA Deployment Diagram*

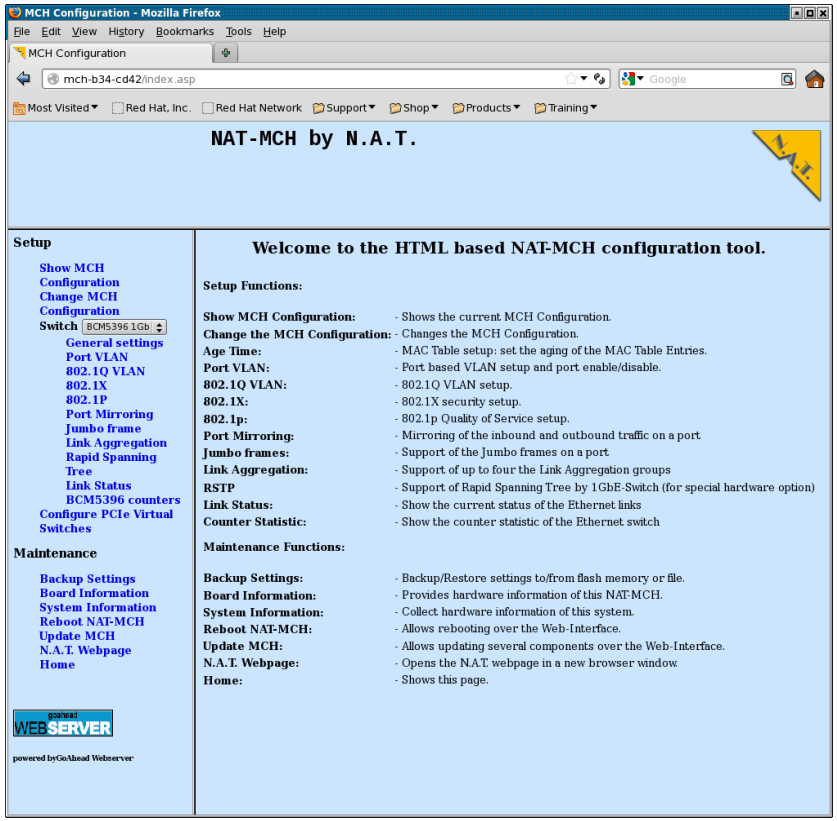
Infrastructure – Software 1

- Software for SLAC control system platform:
  - Real-time embedded Linux operating system
    - preempt_rt patch
  - EPICS
    - Control system applications
  - MCH Configuration software
    - Command-line tool
    - Web-based Tool.
    - Java-based viewer

Infrastructure – Software 2



Java-based Shelf Viewing Tool



Web-based Configuration Tool

Infrastructure – Software 3

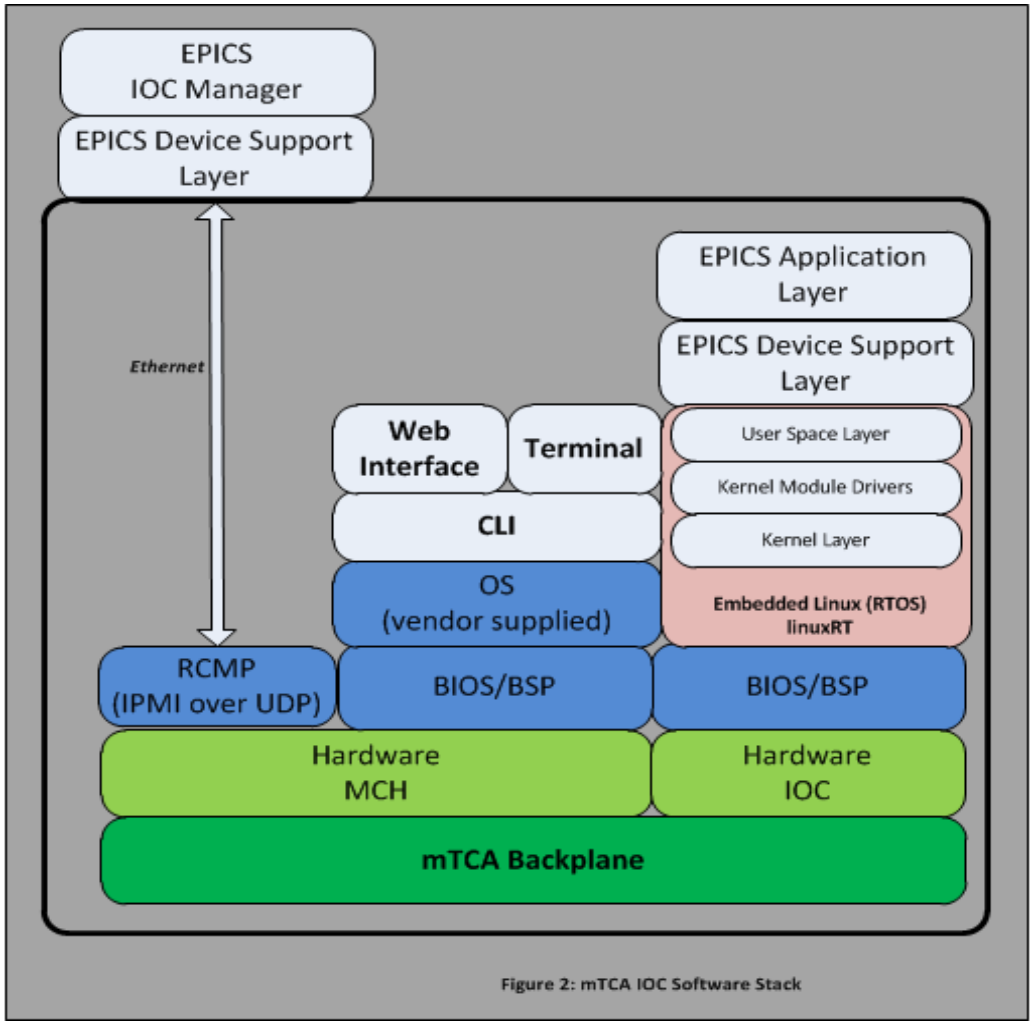
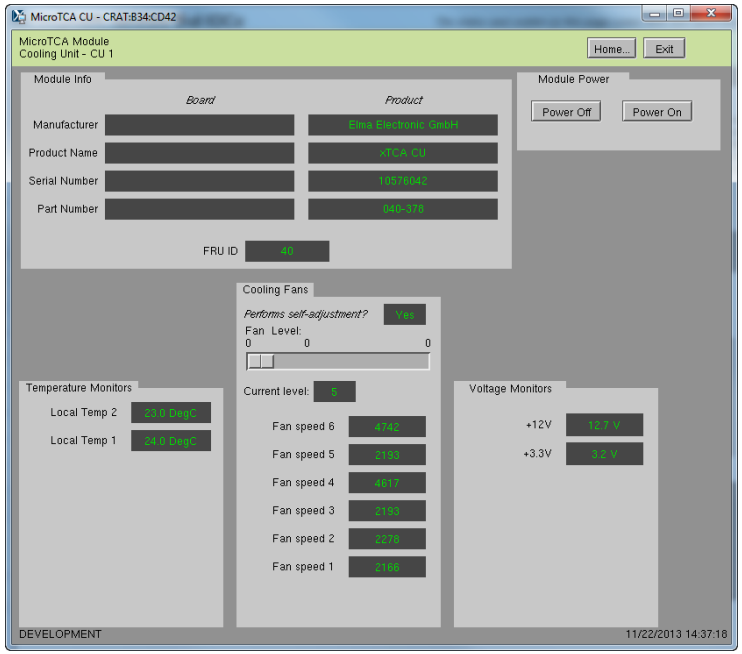
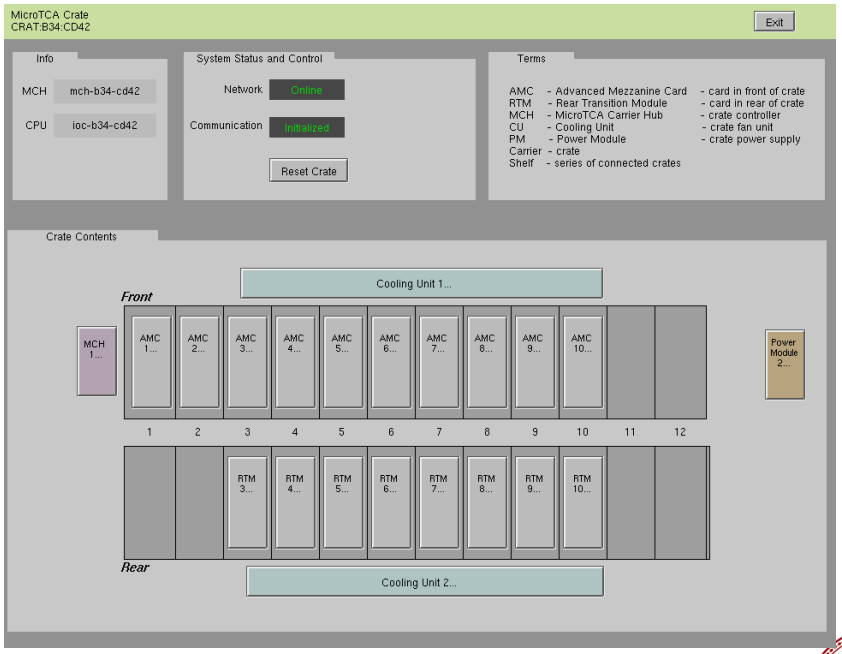


Figure 2: mTCA IOC Software Stack

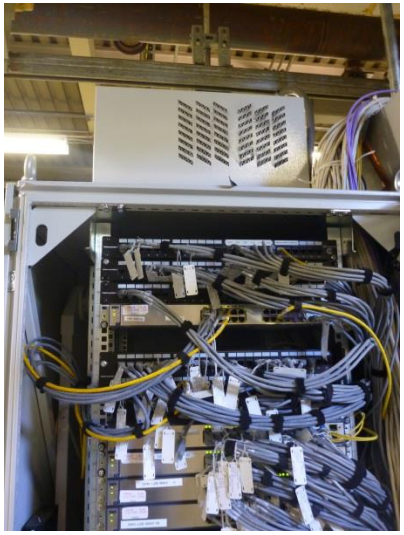
SLAC EPICS IPMI Monitoring

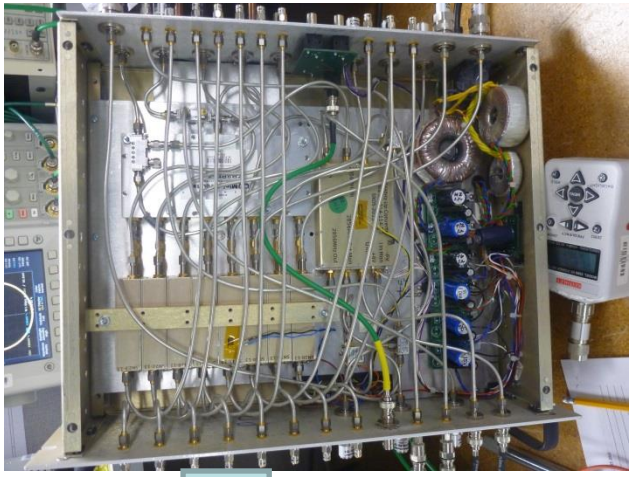
- Monitors & controls MicroTCA systems via MCHs.
- Temperature, voltage, current, fan speeds, system reset.
- Available to user via EPICS PVs.
- EPICS IOC process w/ list of MicroTCA systems to monitor.
- Discovers MCH vendor and uses appropriate message protocol

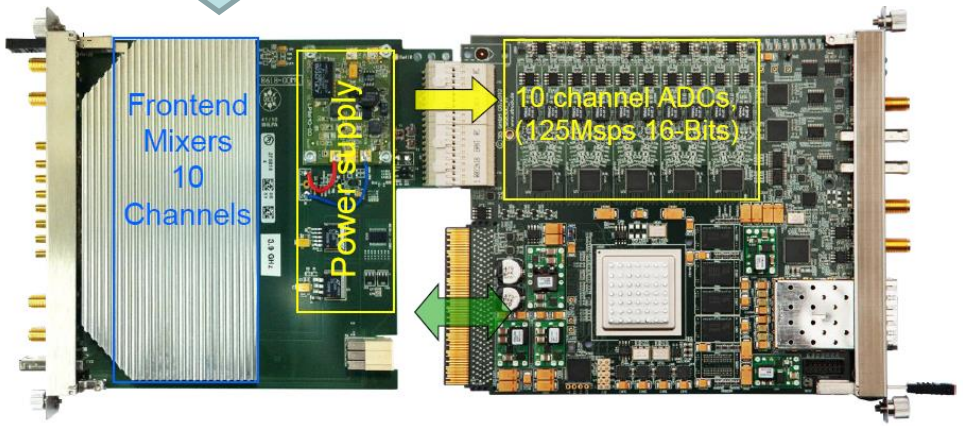




LLRF Development – Potential Transition to MTCA



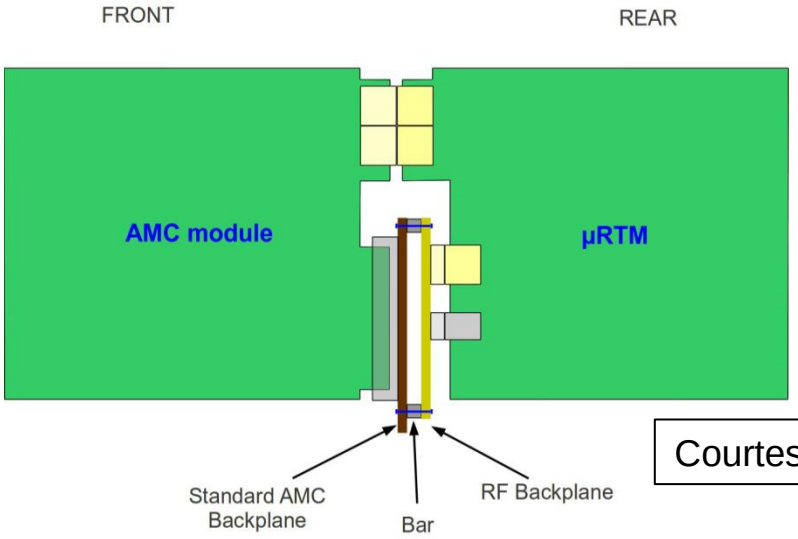




Legacy Down-Converters will transition to DESY-Struck RTM along with RF Local Oscillator distribution system; eliminate expensive chassis & cables.

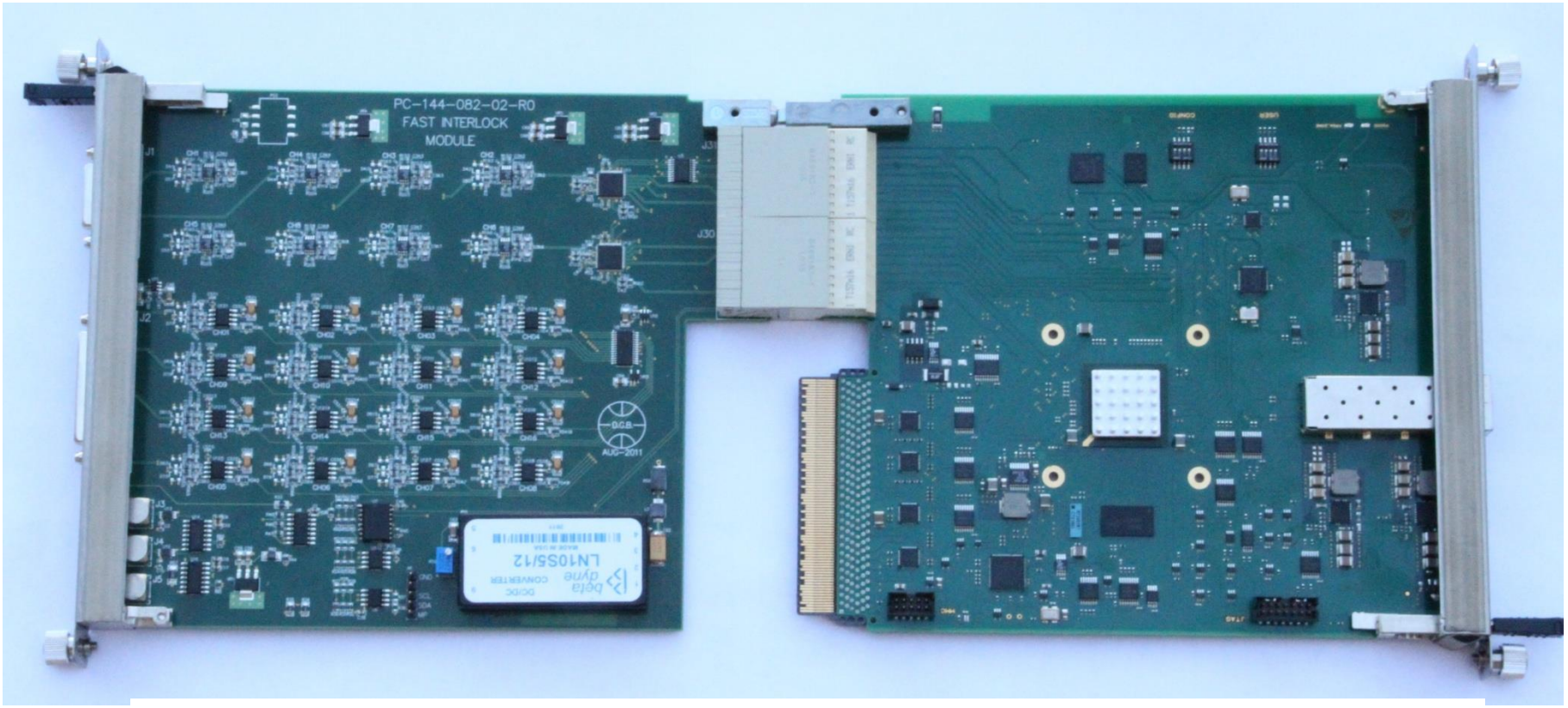
Typical LLRF Chassis vs. MCTA.4

SLAC LLRF
4 RF Stations



Courtesy DESY

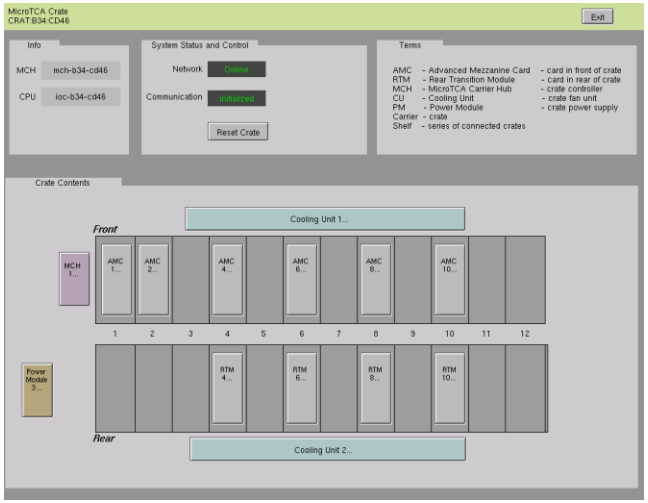
Klystron Interlock RTM, FPGA AMC

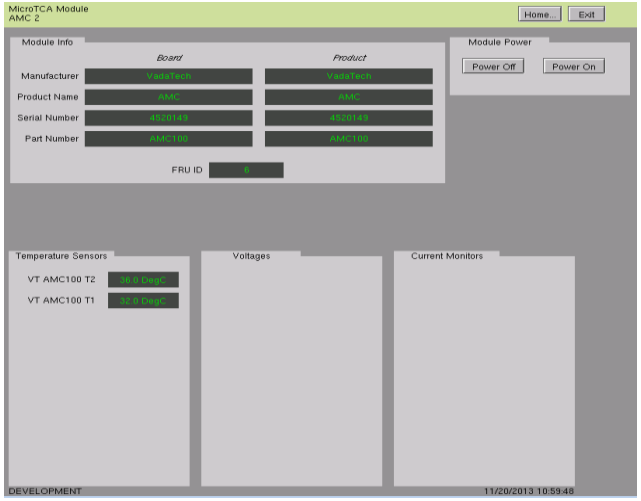


3 sets of RTM-AMC cards replace MKSUII klystron protection chassis.
Firmware to be ported from MKSUII.

RTM Fast-Slow ADC Board design by D. Brown
Layout by C. Yee
TAMC651 by TEWS company

IPMI Screen Shots – *S. Hoobler*





-Courtesy S. Hoobler