AGH University of Science and Technology

Readout electronics for LumiCal detector
Present status and new developments

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ECFA Detector Panel Meeting 10 June 2013, DESY in Hamburg, Germany

Agenda

- Present readout system for LumiCal and BeamCal detectors
  - Front-end electronics
  - 10b multichannel ADC
  - Detector module
- New ASIC developments for BeamCal
- New ASIC developments for LumiCal
- Conclusions

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- **Present readout system for LumiCal and BeamCal detectors**
  - Front-end electronics
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  - Detector module
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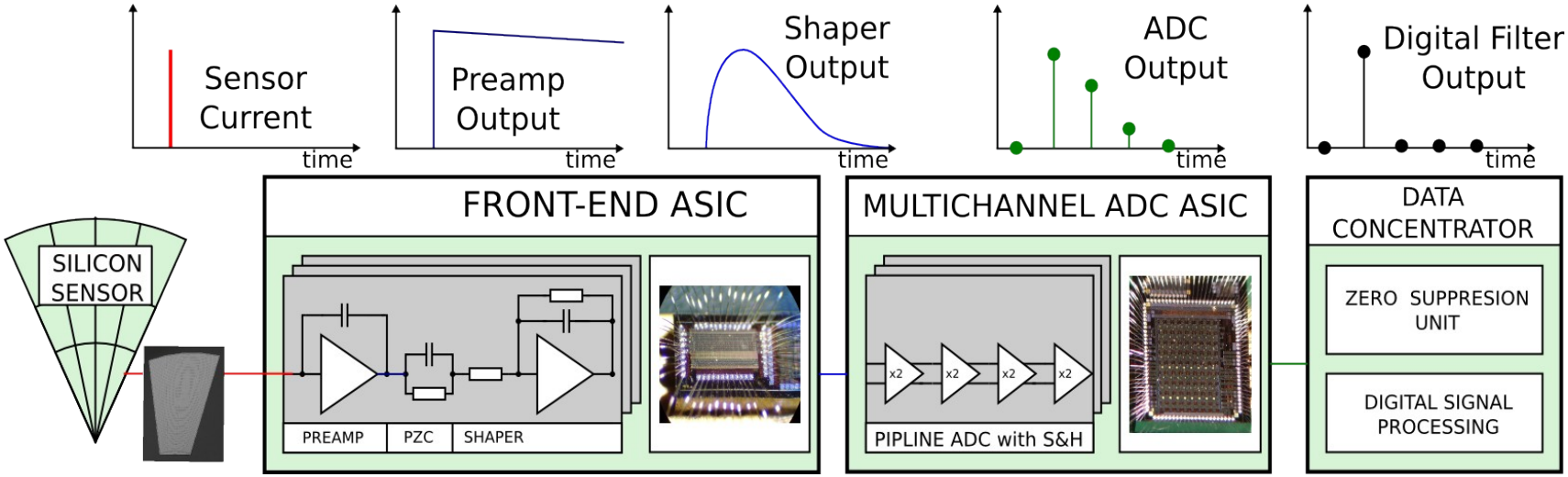
- New ASIC developments for LumiCal
- Conclusions

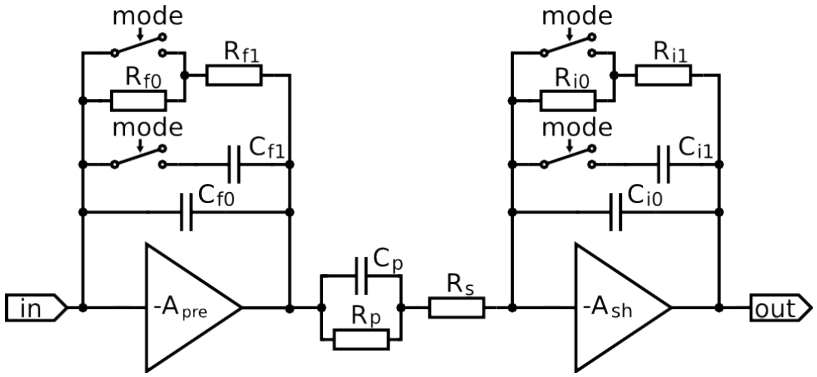
LumiCal (BeamCal) detector readout chain

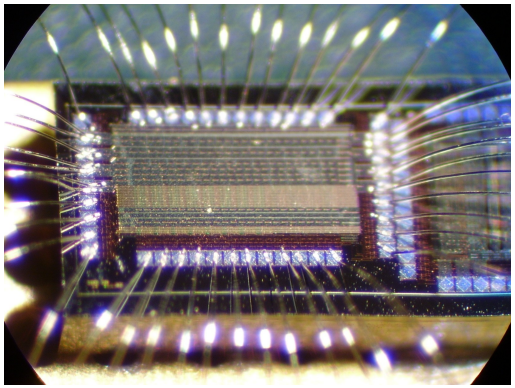


Components of LumiCal detector readout (used also for BeamCal)**:**

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (AMS 0.35um)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (AMS 0.35um)
- FPGA based data concentrator and further readout

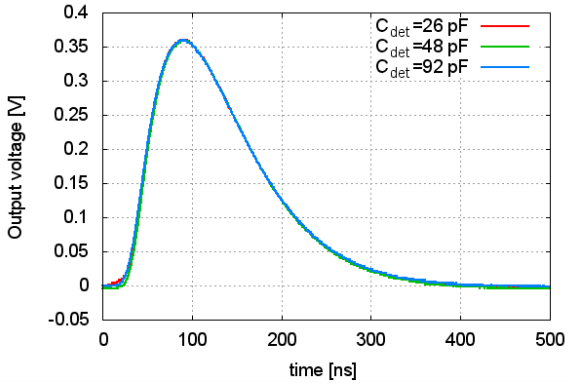
Front-end Electronics in AMS 0.35um





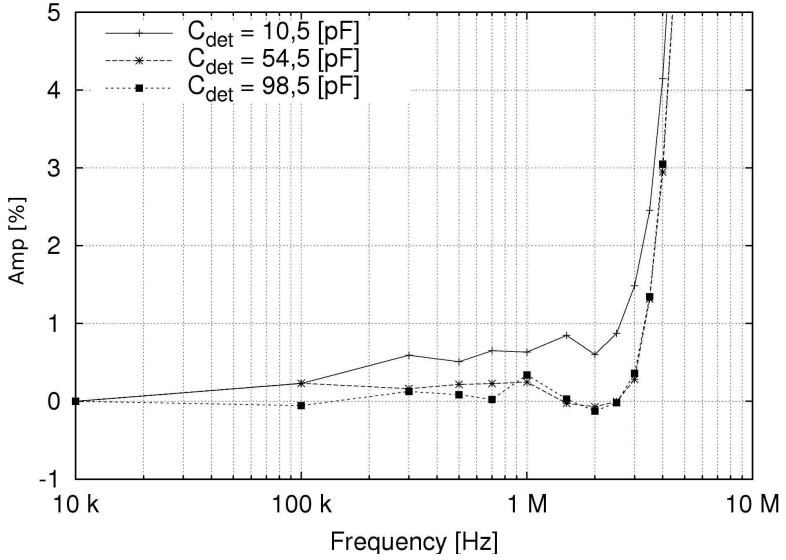
Existing prototypes:

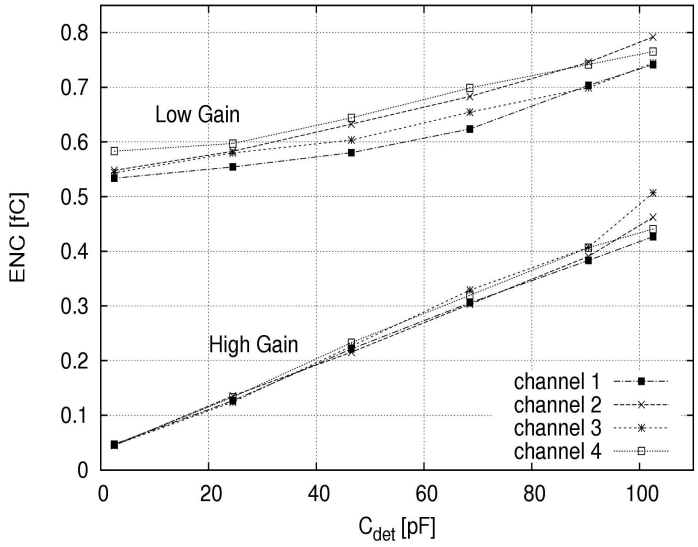
- 8 channels in AMS 0.35um
- Cdet ≈ 0 ÷ 100pF (in new specs: Cdet<50pF)
- 1st order shaper (Tpeak ≈ 60 ns)
- Variable gain:
  - calibration mode – MIP sensitivity (~4fC)
  - physics mode - input charge up to 10 pC
- Prototypes fabricated and tested
  - power consumption 8.9 mW/channel
  - crosstalk < 1%



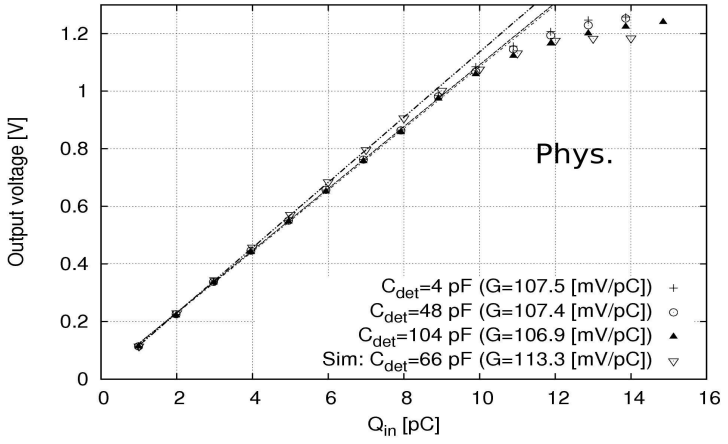
M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminosity detector at ILC", NIM A 608 p.169-174, 2009

Front-end ASIC measurement results



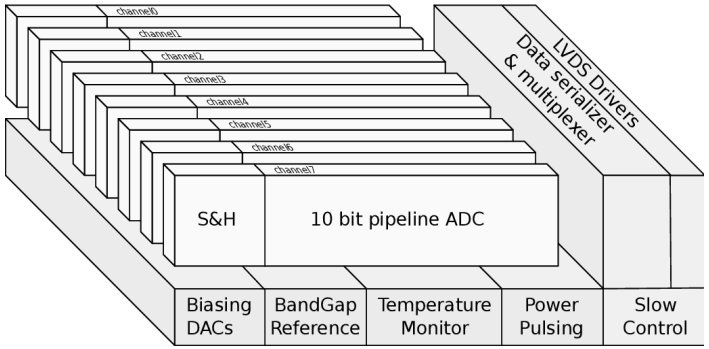


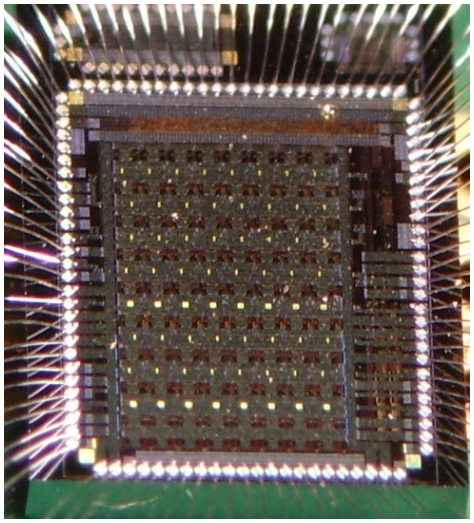
- Maximum event rate about 3 MHz
- In physics mode the ENC is about 0.6 fC and in calibration ~0.2 fC
- Linear range up to ~25 fC (calibration) and ~10 pC (physics)



Multichannel digitizer in AMS 0.35um architecture

- 8 channels of 10-bit pipeline fully differential ADC
- Technology AMS 0.35um
- Layout with 200um ADC pitch
- Multimode digital multiplexer/serializer:
  - Full serialization mode: one data link per all channels
  - Partial serialization mode: one data link per channel
  - Test mode: single channel output
- High speed LVDS interface (~1GHz)
- Power pulsing
- Low power DACs for internal settings
- BandGap reference source
- Temperature sensor

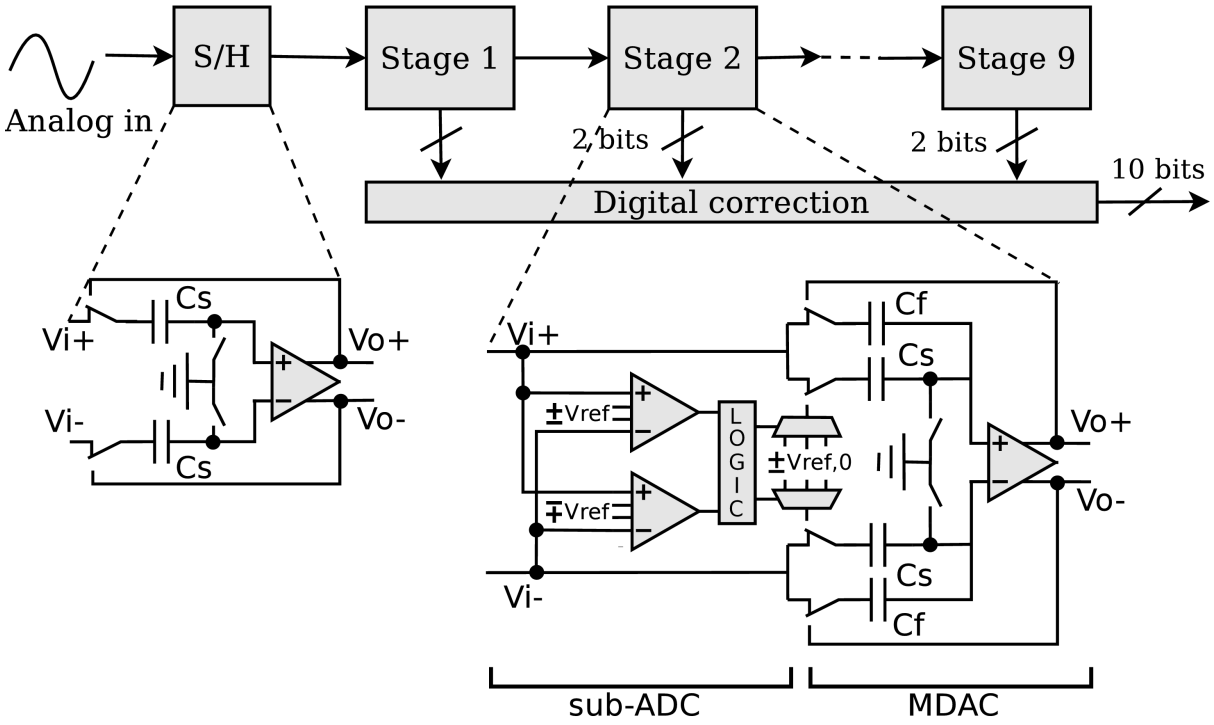




2.6mm x 3.2mm

M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. v.59 p.294-302 2012

Pipeline ADC architecture

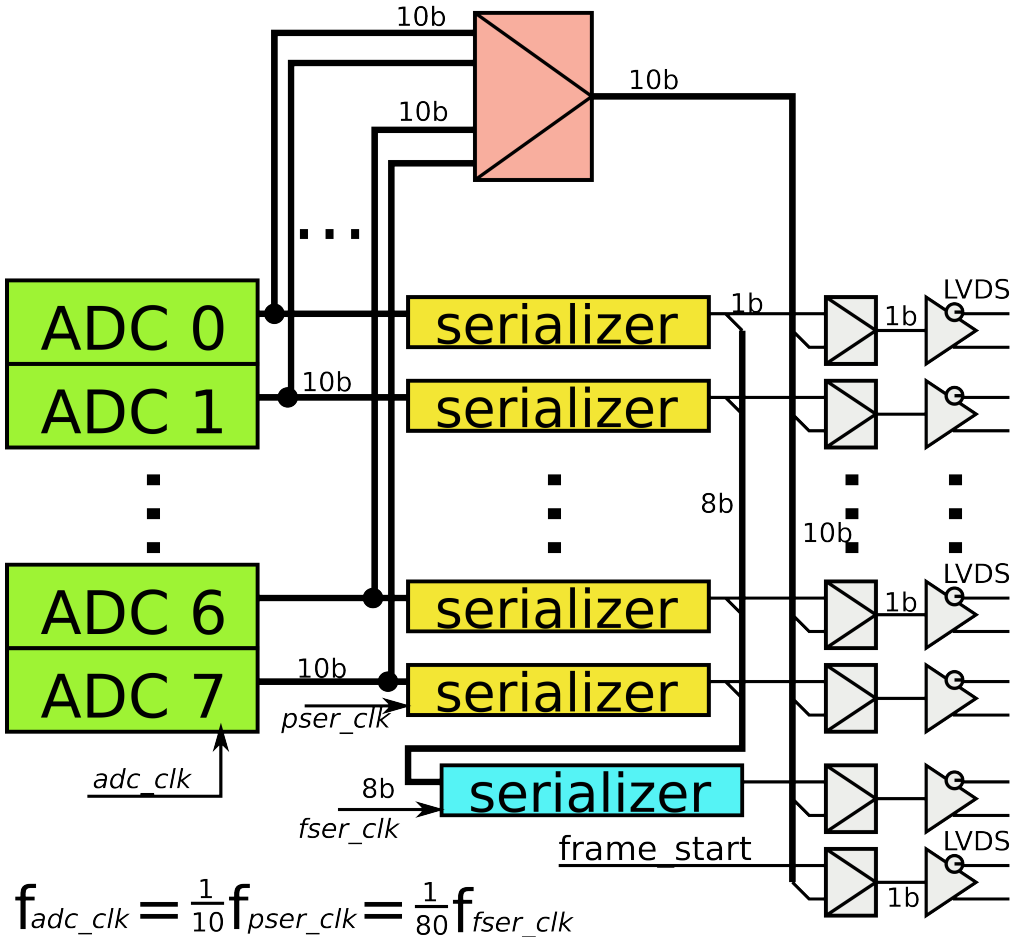


- 9 almost identical stages – capacitance scaling
- Stage – 1.5 bit architecture with digital correction – comparator requirements relaxed
- Bootstrapped S/H switches

Multichannel ADC ASIC readout

Three operation modes:

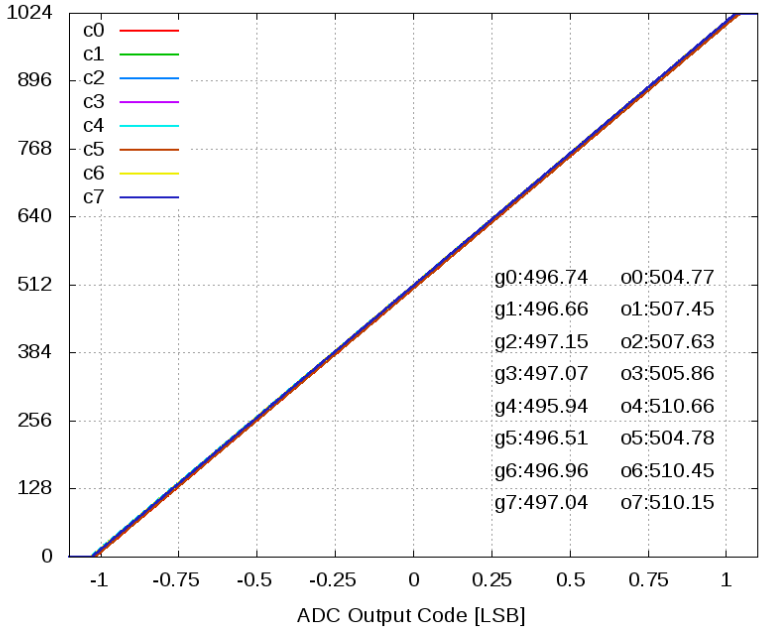
- **Full serialization:** one data link per all channels
  - up to ~250 MHz readout
  - up to ~3 Msps
- **Partial serialization:** one data link per channel
  - up to ~250 MHz readout
  - up to ~25 Msps
- **Test**: single channel output
  - up to ~50 Msps



Multichannel ADC - Static measurements

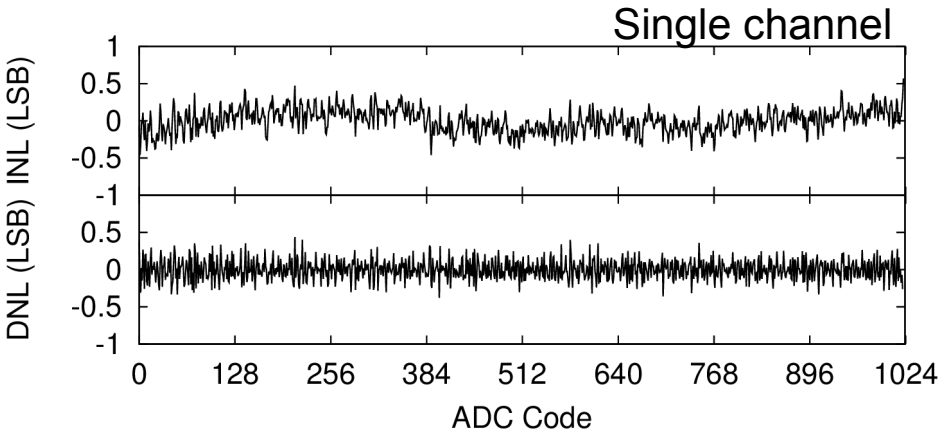
Transfer curves for 8 ADC channels (left)

- Good uniformity of offset and gain

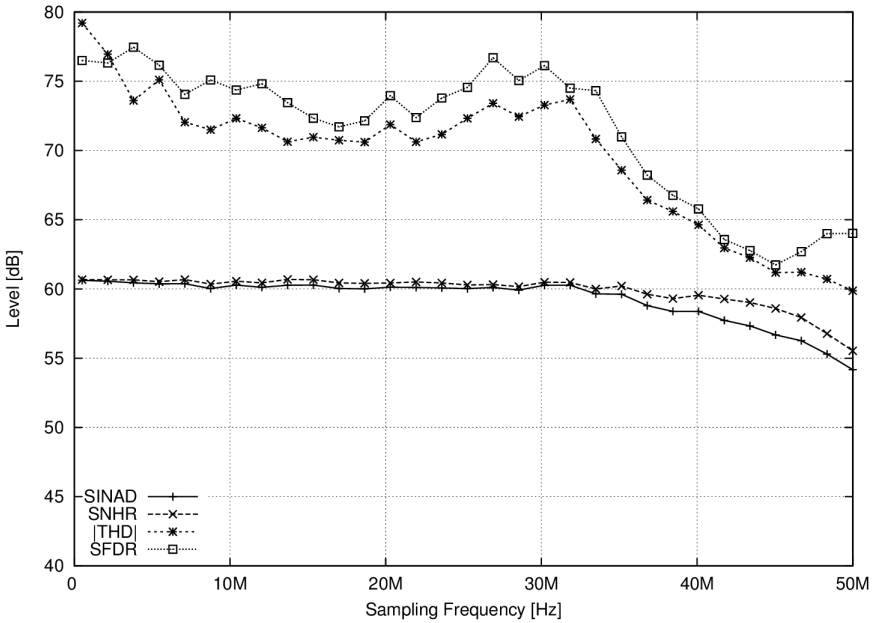


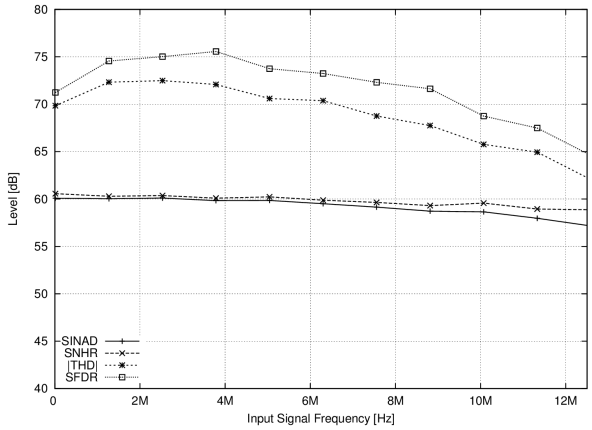
INL and DNL measured for ASIC at 25MS/s:

- INL < 0.7 LSB
- DNL < 0.6 LSB



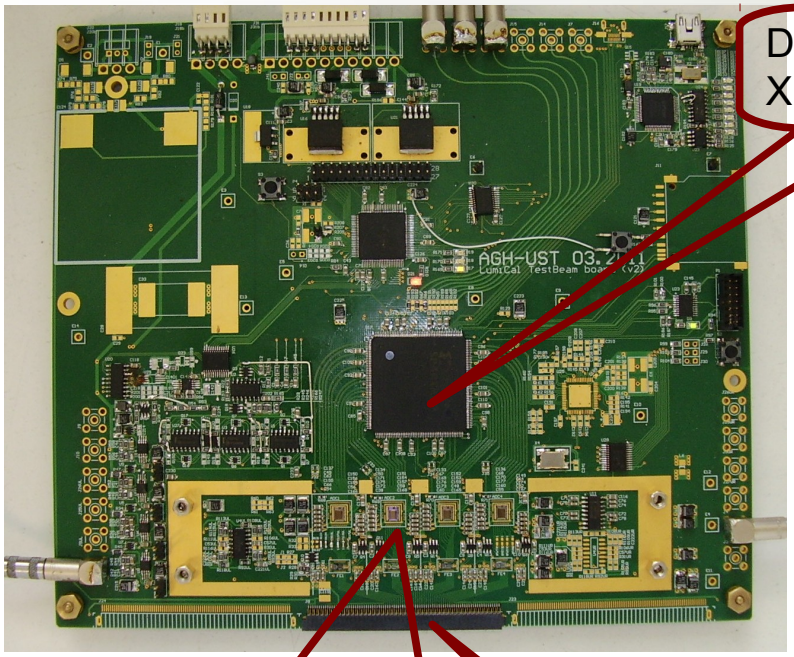
Multichannel ADC - Dynamic measurements





- Dynamic parameters vs sampling frequency (top) and vs input frequency (bottom)
- SINAD ~60 dB corresponding to ENOB ~ 9.7 bits for sampling rates below 35 MS/s
- In test mode ADC works up to ~50 MS/s but in multichannel system two practical configurations are:
  - serialization/channel up to ~25 MS/s
  - serialization/chip up to ~3 MS/s

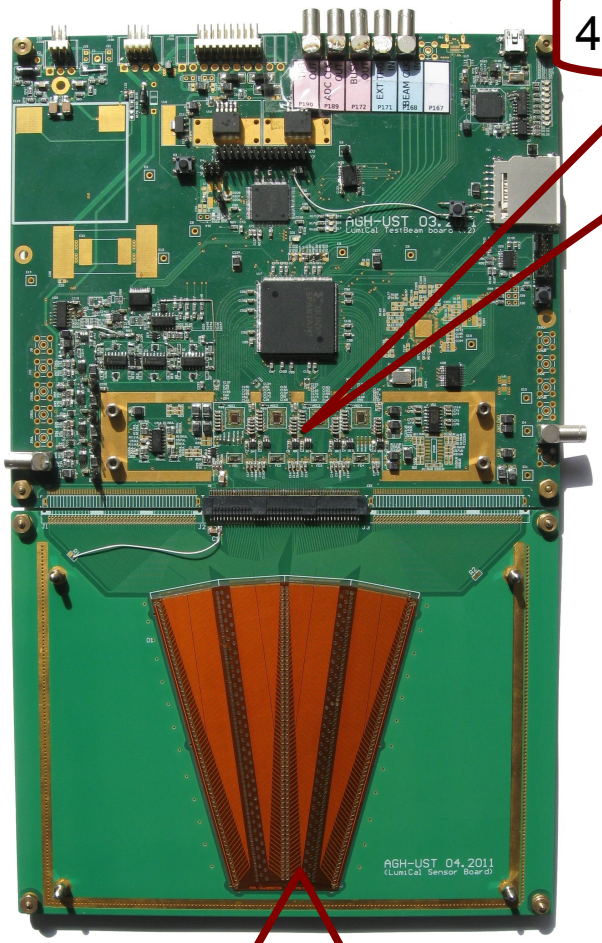
32 channels readout module
Final readout based on AMS 0.35um ASICs



- 32 channels fully equipped channels (Front-end +ADC)
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock usec for synchronization) ILC mode

Sz. Kulis, A. Matoga, M. Idzik, K. Swientek, T. Fiutowski, D. Przyborowski "A general purpose multichannel readout system for radiation detectors", Journal of Instrumentation JINST 7 T01004 2012

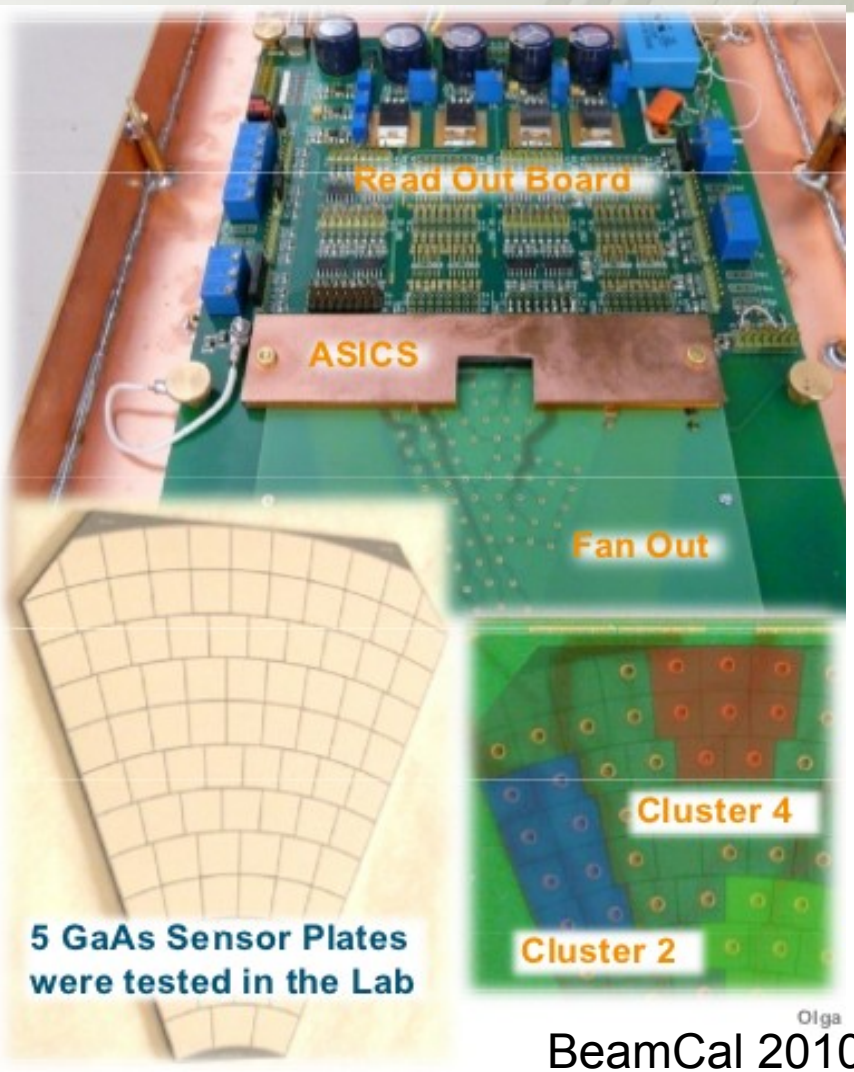
LumiCal detector readout module (ASICs in AMS 0.35um)



- LumiCal detector module with 32 fully equipped channels (Front-end +ADC ASICs) plus FPGA data concentrator is regularly used during testbeams
- Good performance of detector module verified on 2 testbeams in 2011
- Power pulsing: 1ms ON then 199ms OFF – ASICs Power ON/OFF >30
- Using deconvolution, tests for CLIC are performed with asynchronous readout

Readout module is used for BeamCal and LumiCal detectors

LumiCal in testbeam 2011



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- Present readout system for LumiCal and BeamCal detectors
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- **New ASIC developments for BeamCal**
- New ASIC developments for LumiCal
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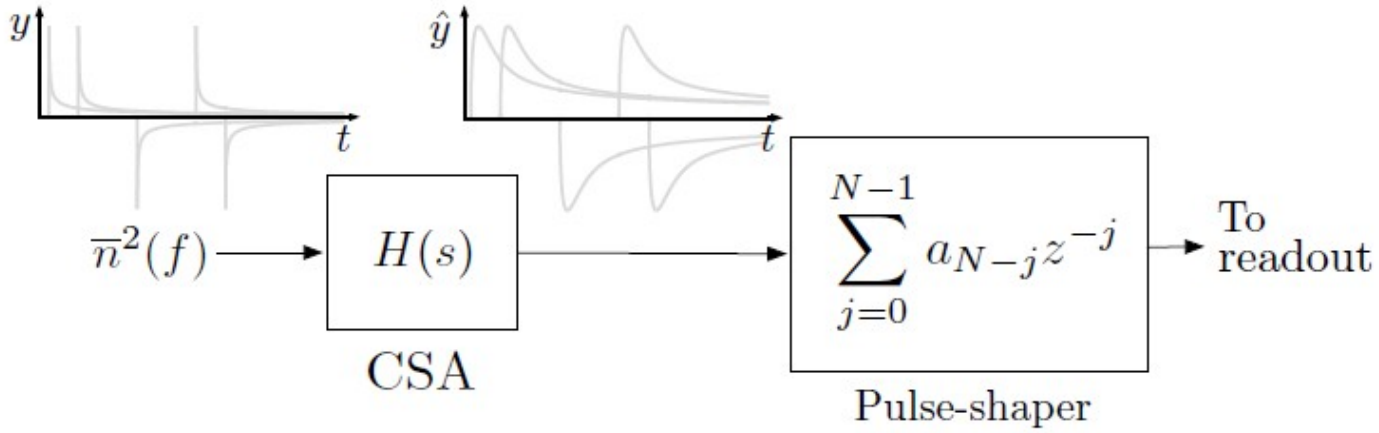
Noise analysis and optimization in front-end

Angel Abusleme

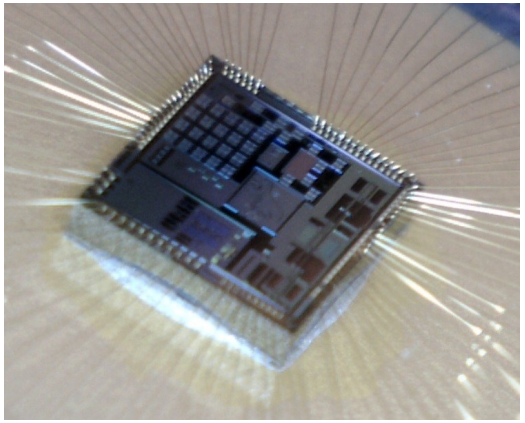
- Aims to understand and test how different weights in multiple sampling affects signal-to-noise ratio
- and therefore, how to optimize the weights
- Switched capacitor implementation is being designed



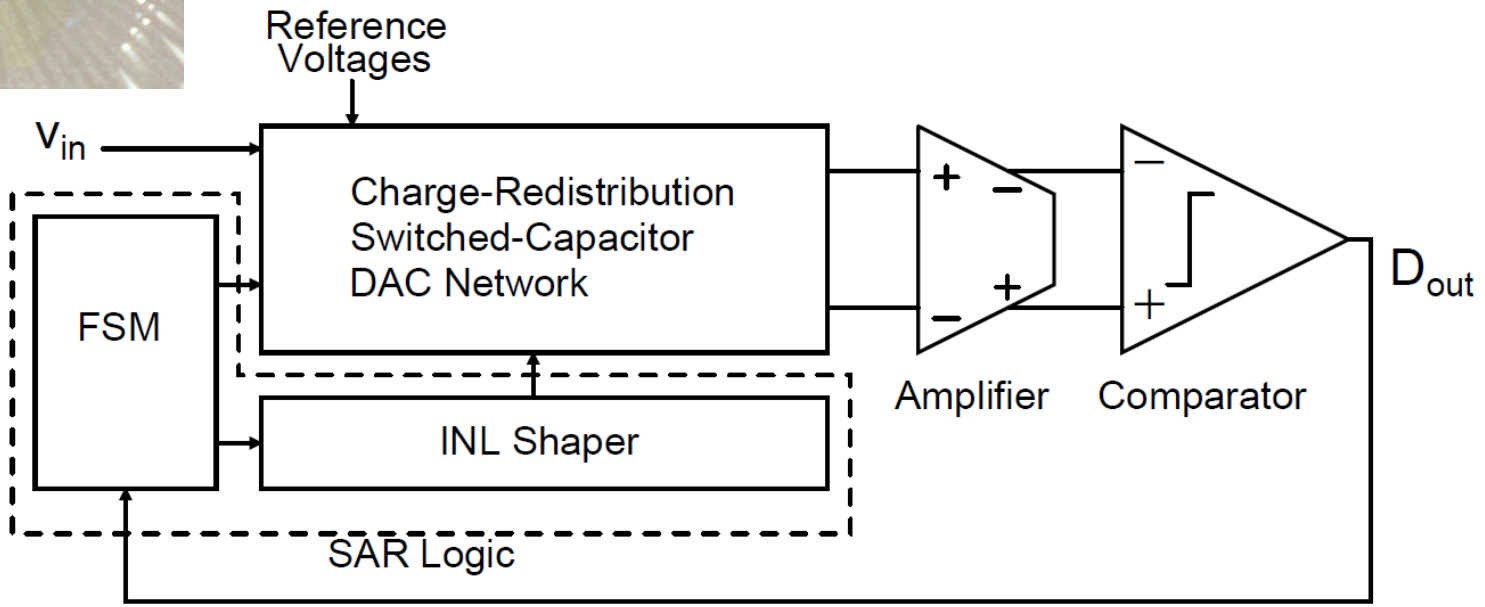
E. Alvarez, D. Avila, H. Campillo, A. Dragone, and A. Abusleme. Noise in Charge Amplifiers – A gm/ID Approach. IEEE Transactions on Nuclear Science, 59(5), Oct. 2012.

BeamCal SAR ADC architecture

Angel Abusleme



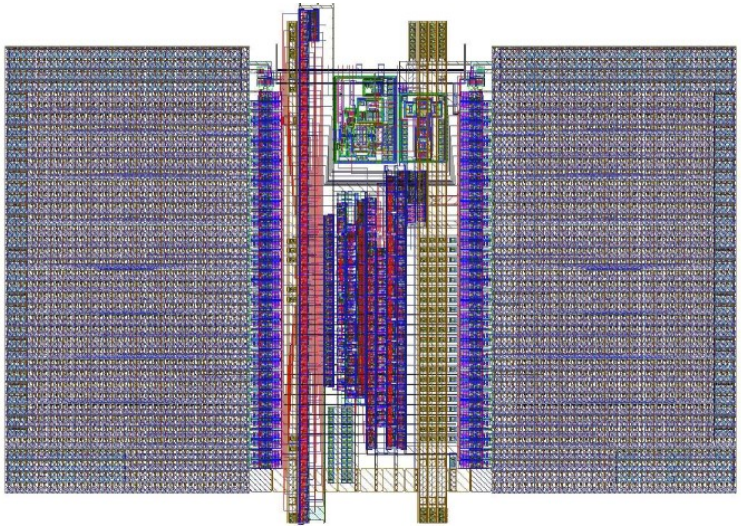
- ADC uses systematic process mismatch (radial gradients in array) to correct nonlinearity
- Test structures already produced

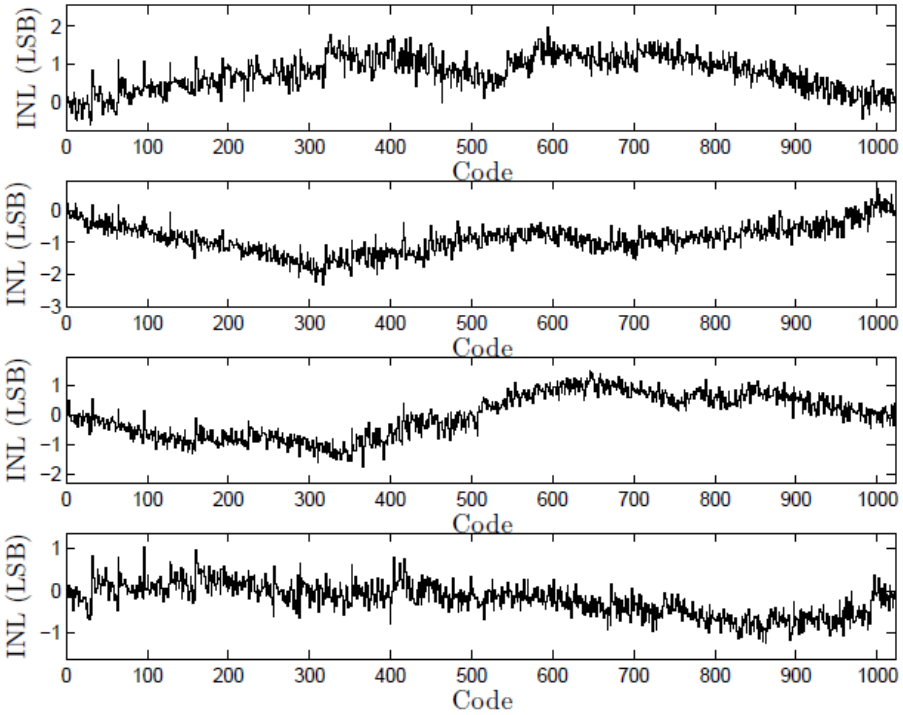


SAR ADC linearity correction

Angel Abusleme

- Recently tested in a 180 nm process
- INL can be shaped to correct nonlinearity of signal path





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- **New ASIC developments for LumiCal**
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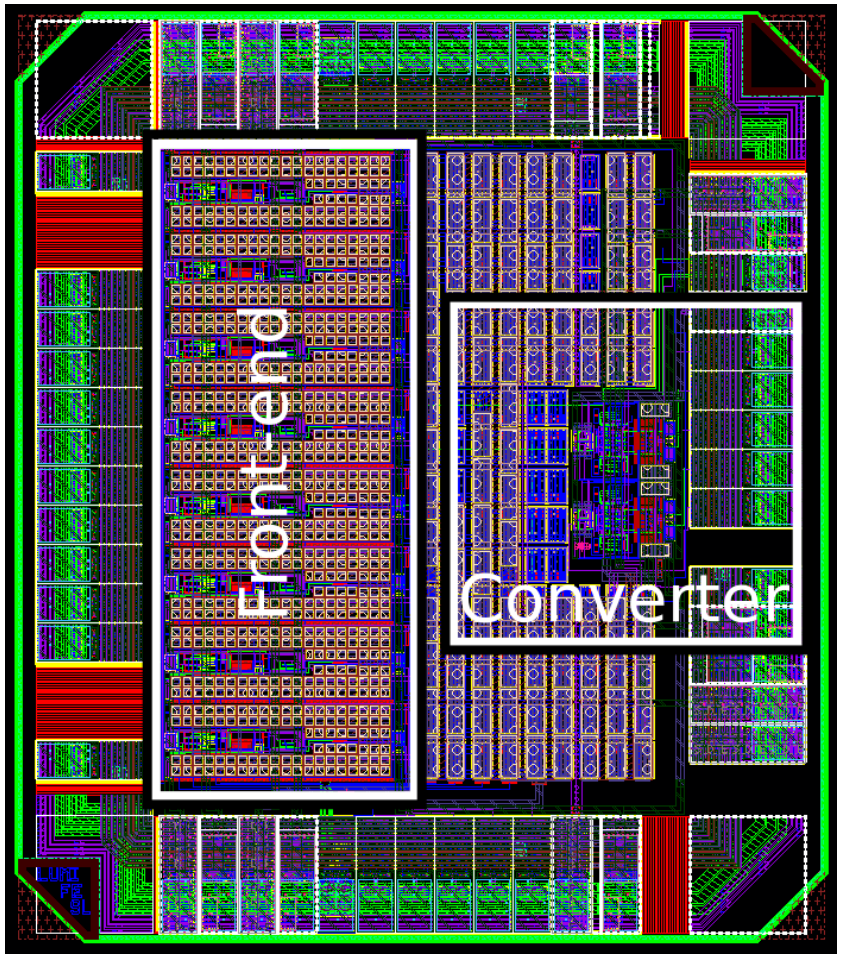
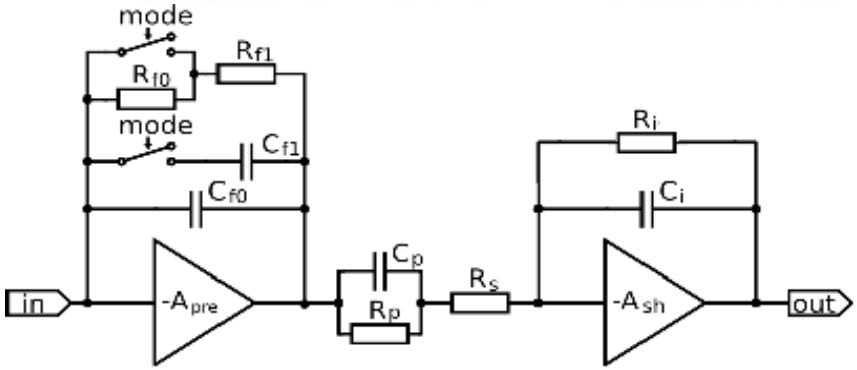
Front-end: Preamplifier & Shaper



IBM 130 nm

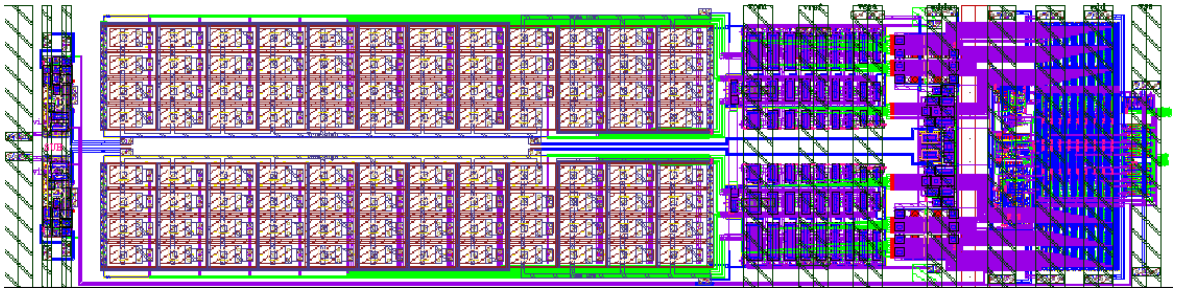


Design specs:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~6 pC
- Power pulsing implemented
- Simulated power consumption ~1.5 mW/channel

Design of 10-bit SAR ADC

SAR channel 600um x 146um

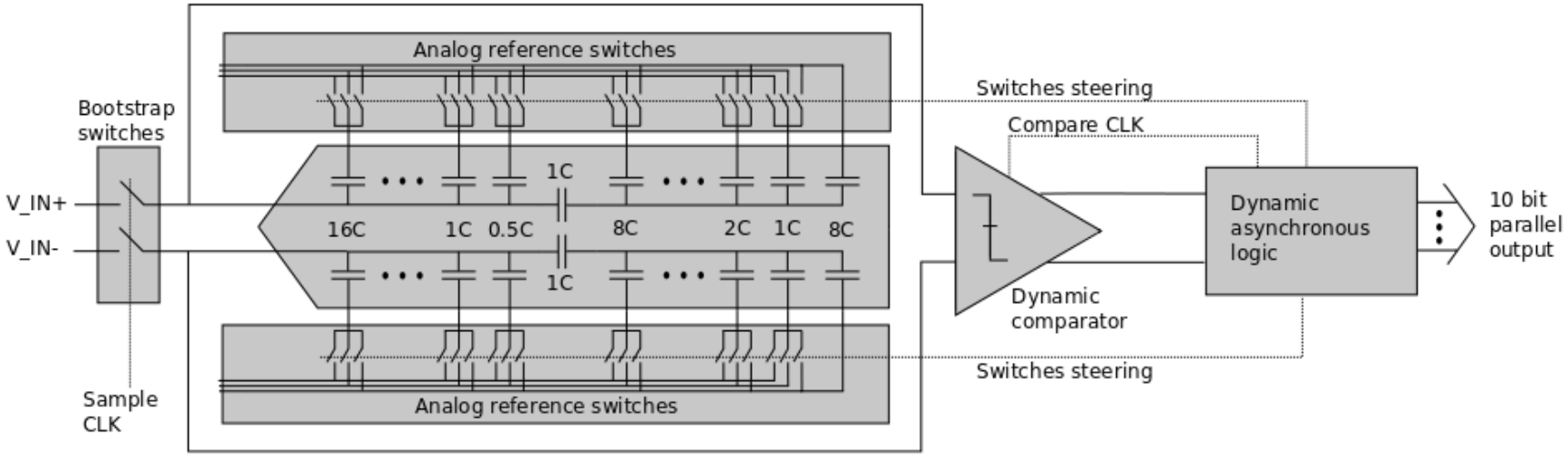


IBM 130 nm

Designs of 10-bit ADC

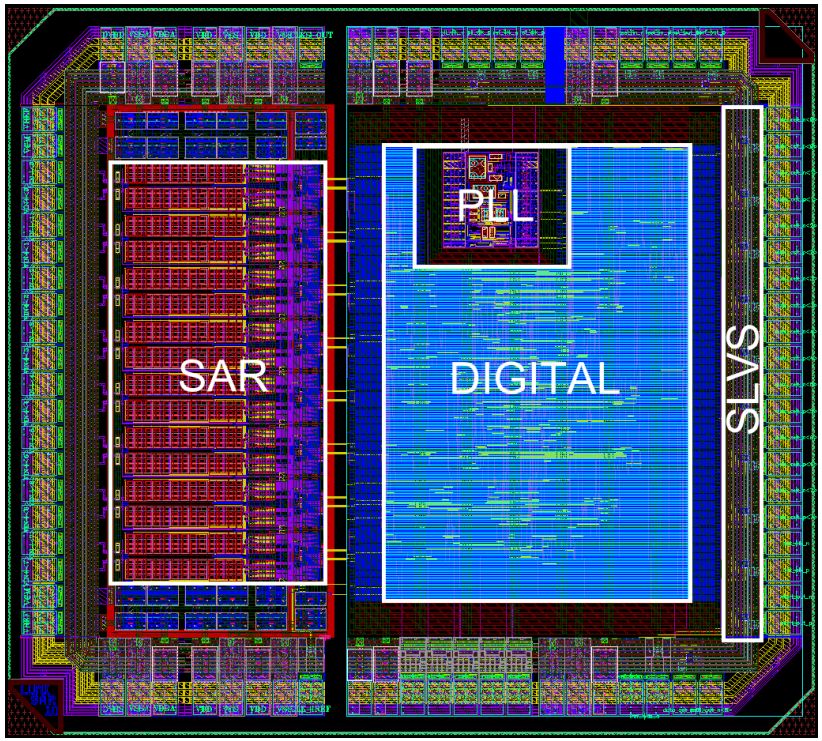
- Architecture: SAR ADC with segmented/split DAC
- Sampling frequency up to ~50 MS/s
- Power consumption scales with sampling frequency
- Asynchronous SAR logic – no fast clock

- 1-2 mW at 40 MS/s
- 146um pitch
- Fabricated in 2012 (2 prototypes)



Layout of 8 channel 10-bit SAR ADC

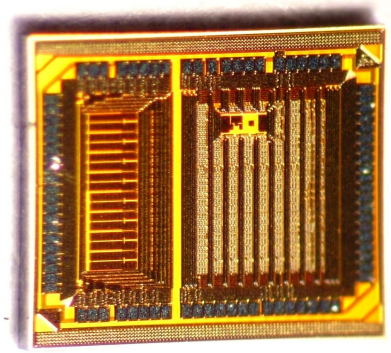
IBM 130 nm



2200um x 2000um

ASIC comprising

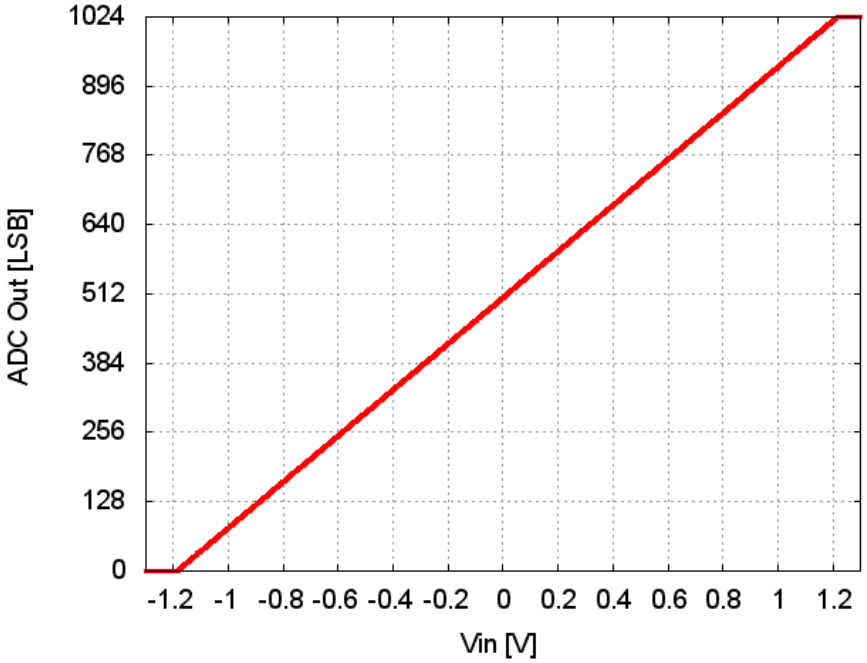
- 8 channels of 10-bit SAR ADC
- PLL for data serialization
  - Systematic tests are just starting
  - PLL output clock signal was observed with scope
- High speed SLVS interface
  - No dedicated tests of SLVS interface done yet
  - PLL differential outputs it was veryfied that SLVS driver operates at least up to 700 MHz.



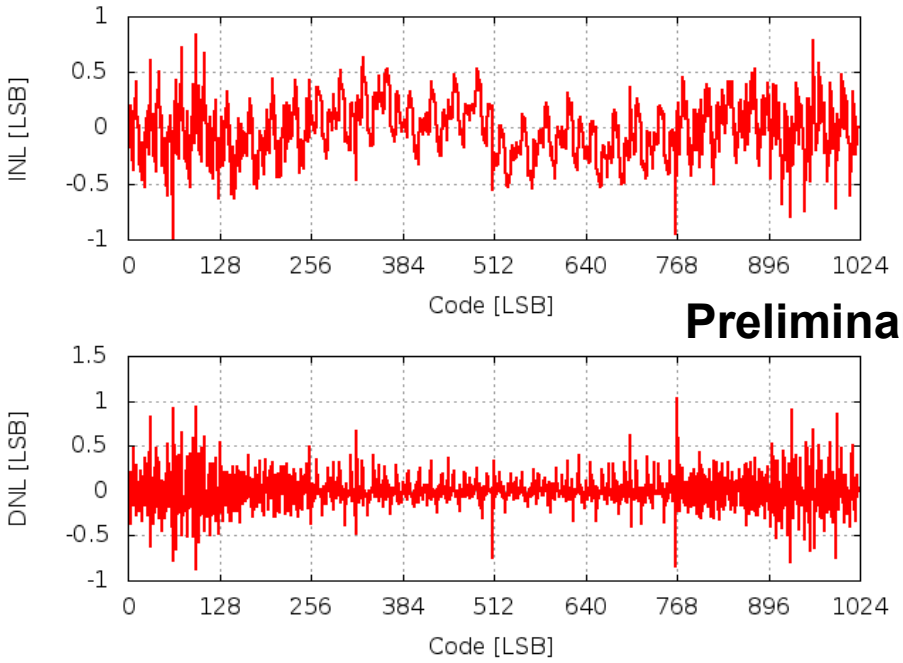
Design submitted and fabricated in 2012

10-bit SAR ADC - Static measurements

Transfer function

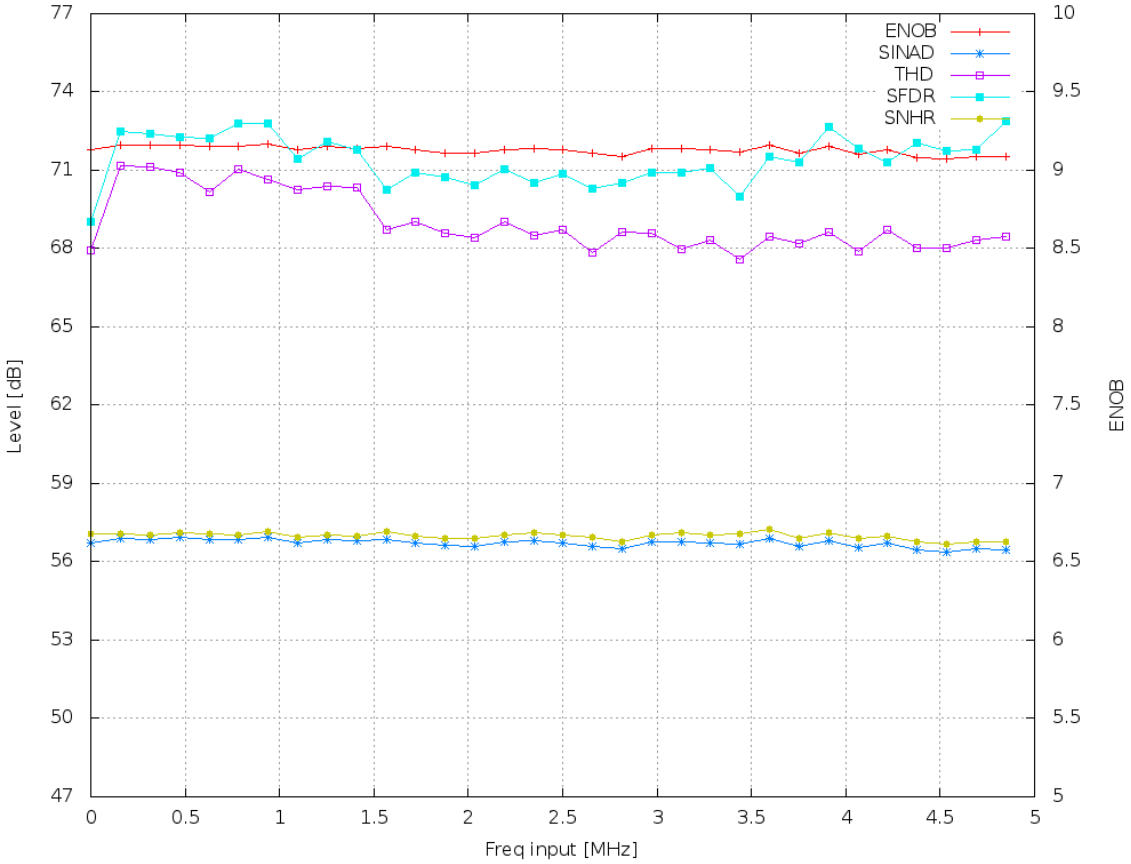


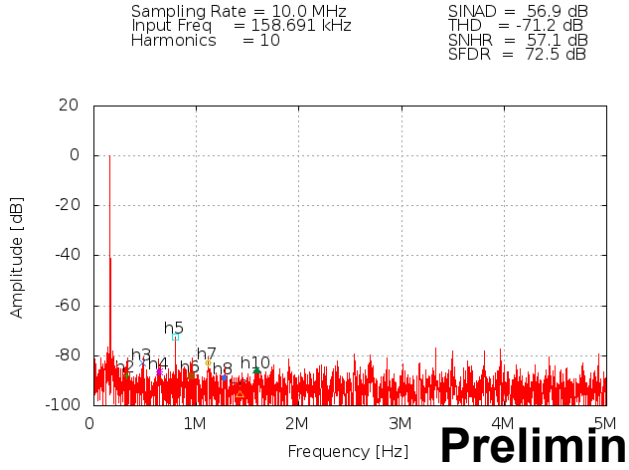
INL/DNL measurements



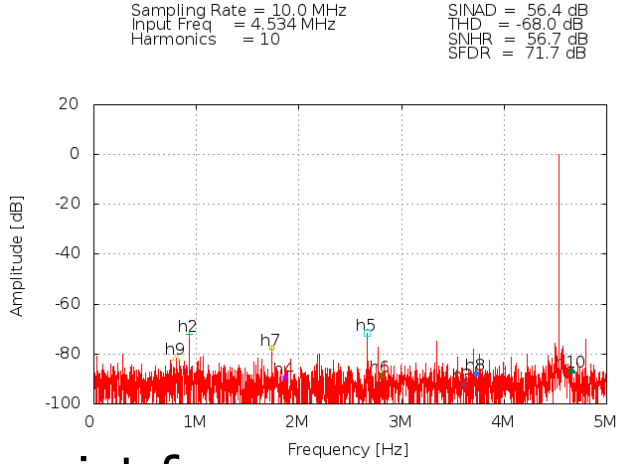
- ADC works in the whole input signal range
- There are some codes with worse linearity (under investigation...)

10-bit SAR ADC - Dynamic measurements





Preliminary



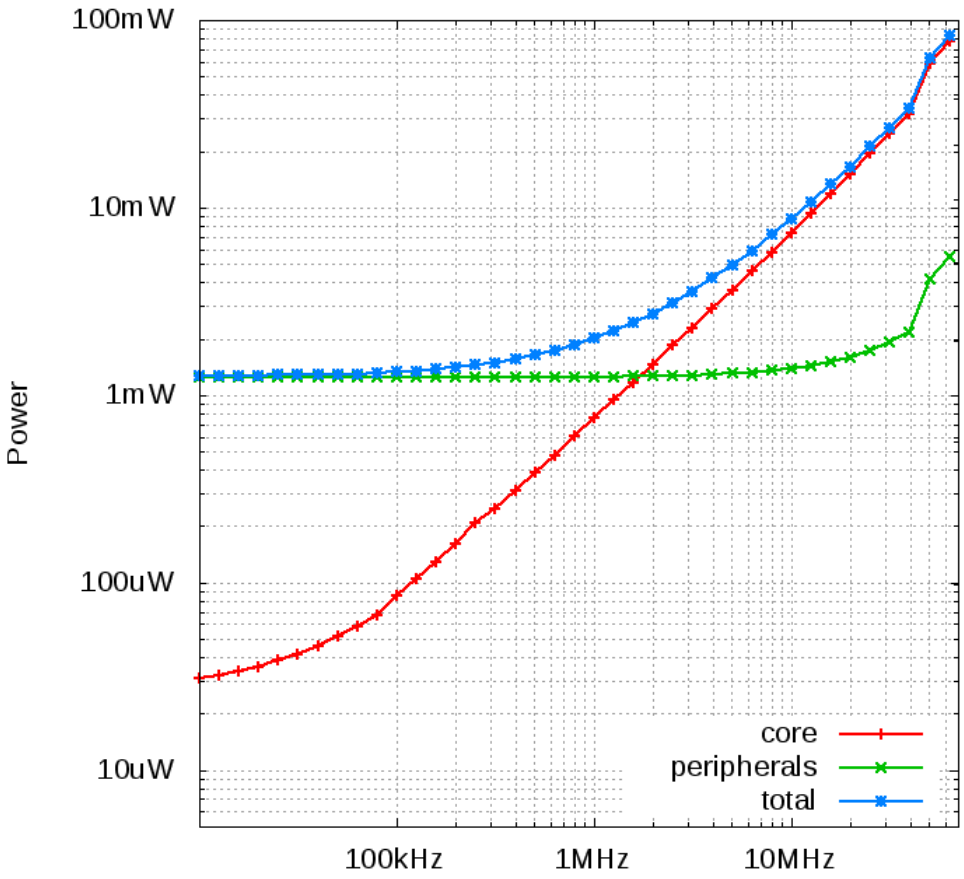
- ENOB of >= 9.2 was measured up to Nyquist frequency after improving test setup – more improvement needed?

Summary and Plans

- Presently FCAL uses in test-beams the readout modules based on developed at AGH-UST ASICs in CMOS AMS 0.35um
- Development of new ASICs for BeamCal readout in 180 nm in progress – next front-end submission planned at the end of 2013
- Development of new ASICs for LumiCal readout in IBM 130 nm in progress:
  - First prototype of front-end electronics submitted and should be available in June 2013
  - First prototypes of 10-bit SAR ADC, PLL, SLVS already produced and presently under test:
    - 10-bit SAR ADC: first results show its functionality, the effective resolution slightly less than simulated - quantitative measurements in progress..
    - PLL tests just started...
    - SLVS interface works well
  - Depending on test progress and results we plan next submission at the turn of 2013/2014

Backup slides

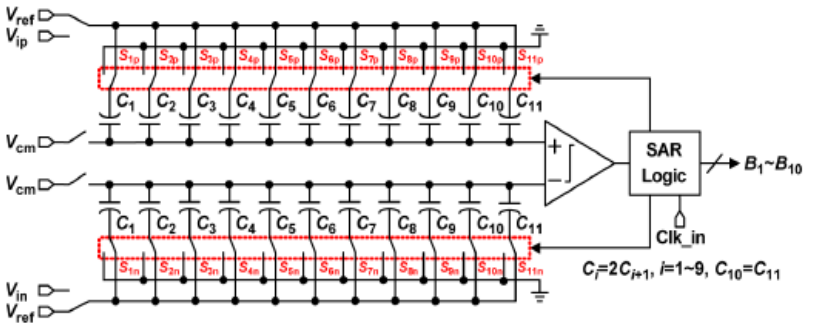
Developments in AMS CMOS 0.35um
Power consumption in pipeline ADC



- Power scales lineary in frequency range 3 kHz – 10 MHz:
  - ADC (core) – **0.8 mW/channel/MHz**
  - serializer in partial serialization mode – **0.35 mW/channel/MHz**
  - serializer in full serialization mode – **0.85 mW/channel/MHz**

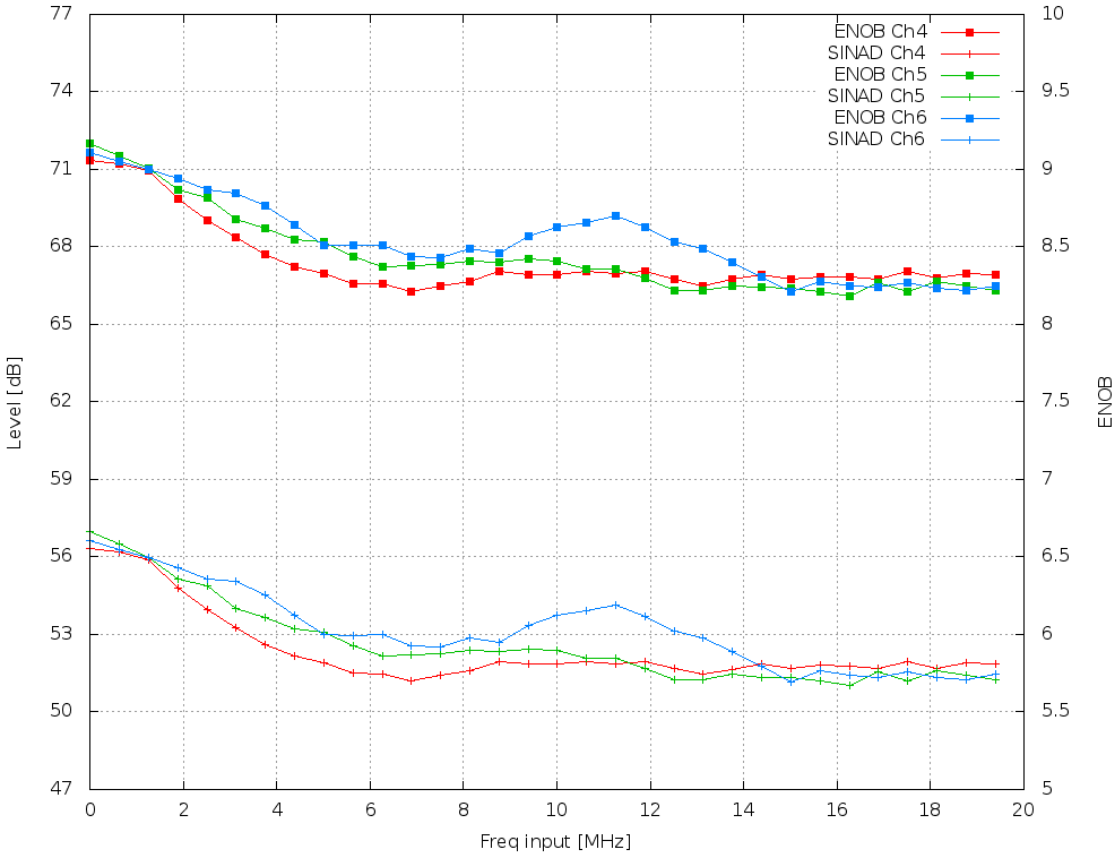
Developments in IBM CMOS 130nm
SAR ADC: General features & design considerations

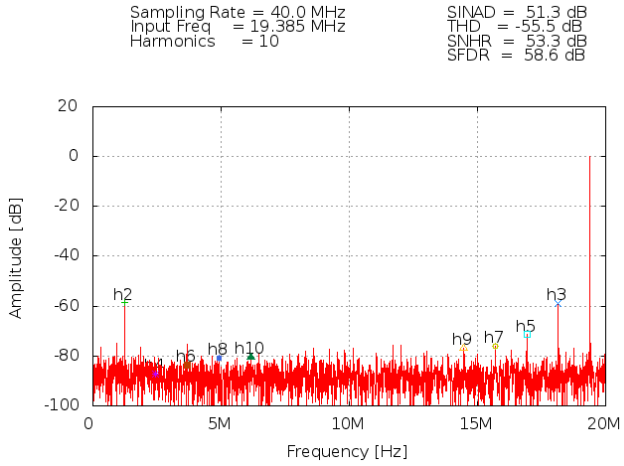
- Power and area-efficient architecture – the same circuitry is used N-times (for N-bit ADC) to approximate the input voltage
- Only one comparator, two DACs and SAR logic needed – fits well to modern digital CMOS
- Limited sampling rates - but with modern CMOS technology (~100nm) up to ~100MSps 10-bit ADCs were reported
  - next conversion cannot be started before completion of previous one
  - sampling time adds to conversion time (not like in pipeline)



- Comparator – the only analog block
- DAC network serves as sampling capacitance
- Simple digital logic
- Fully differential implementation increases the resistance to disturbances

Preliminary measurements
10-bit SAR ADC - Dynamic measurements – different channels

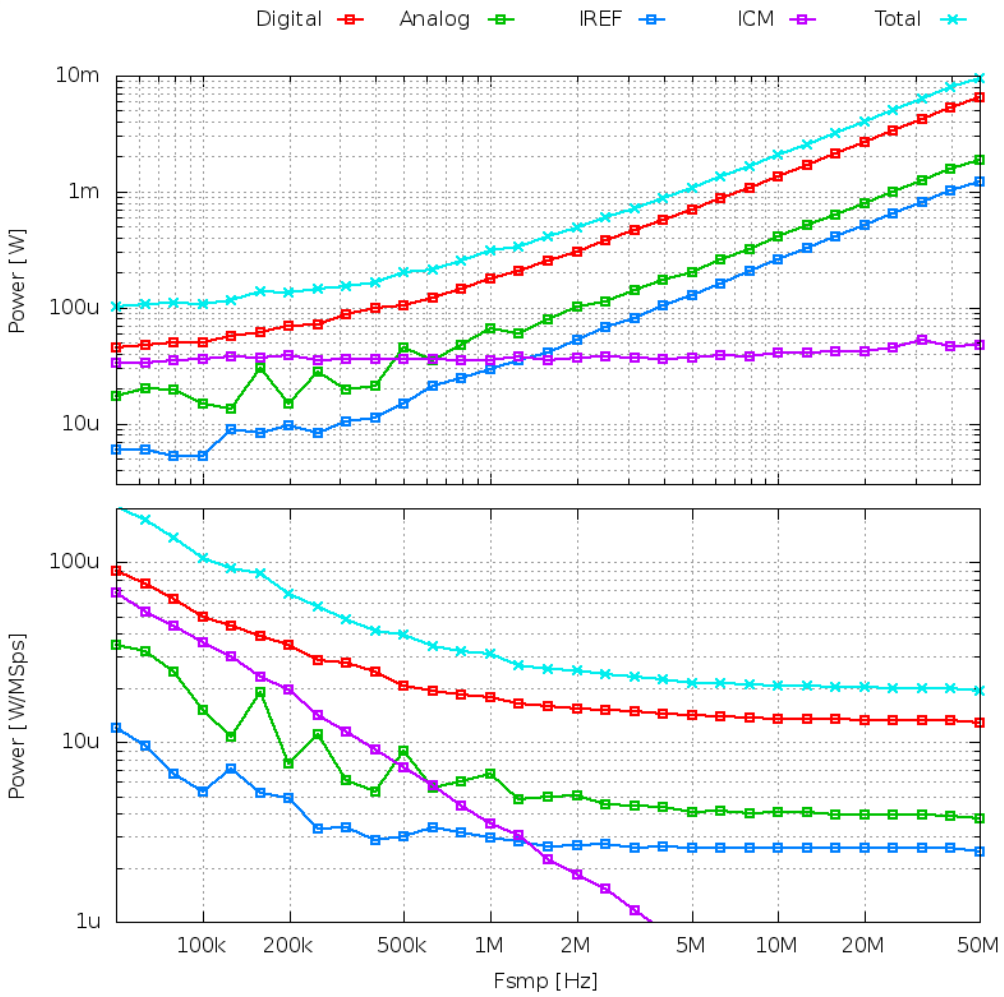




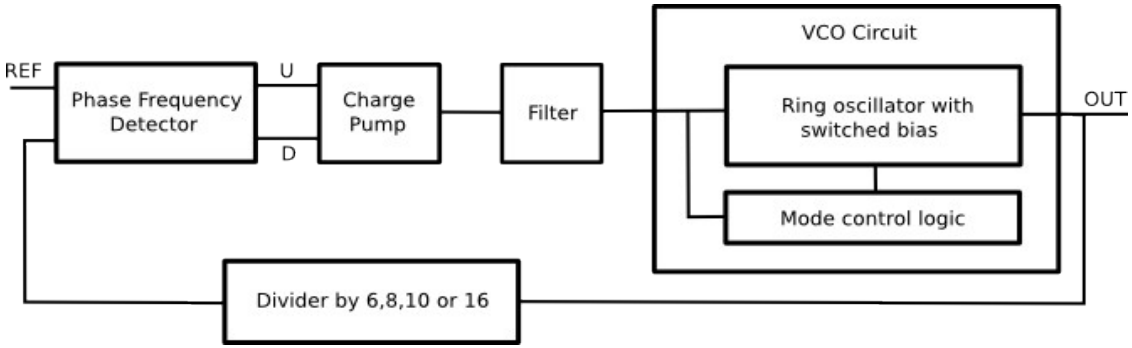
- Results for different channels (only one channel ON during measurements) are similar
- It was suspected that ENOB decrease with f_{in} is partially/mainly due to setup

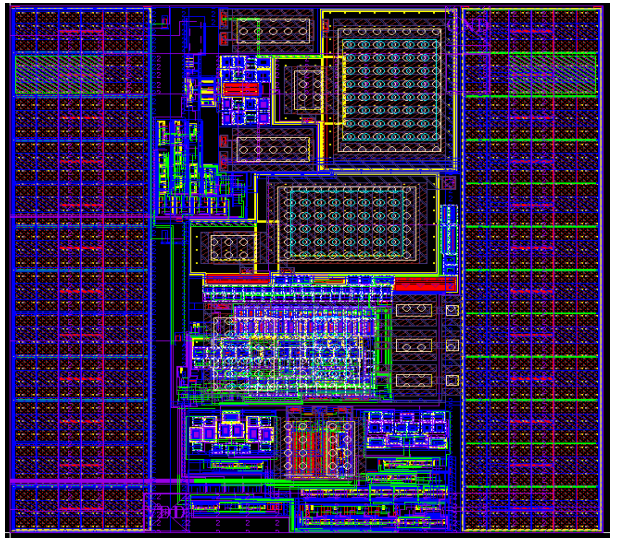
Preliminary measurements
10-bit SAR ADC - Power consumption vs sampling frequency

- Power measured for 8 ADC channels
- At 40MS/s power consumption is about 1 mW per channel – in agreement with simulations



Developments in IBM CMOS 130nm
Design of PLL for data serialization





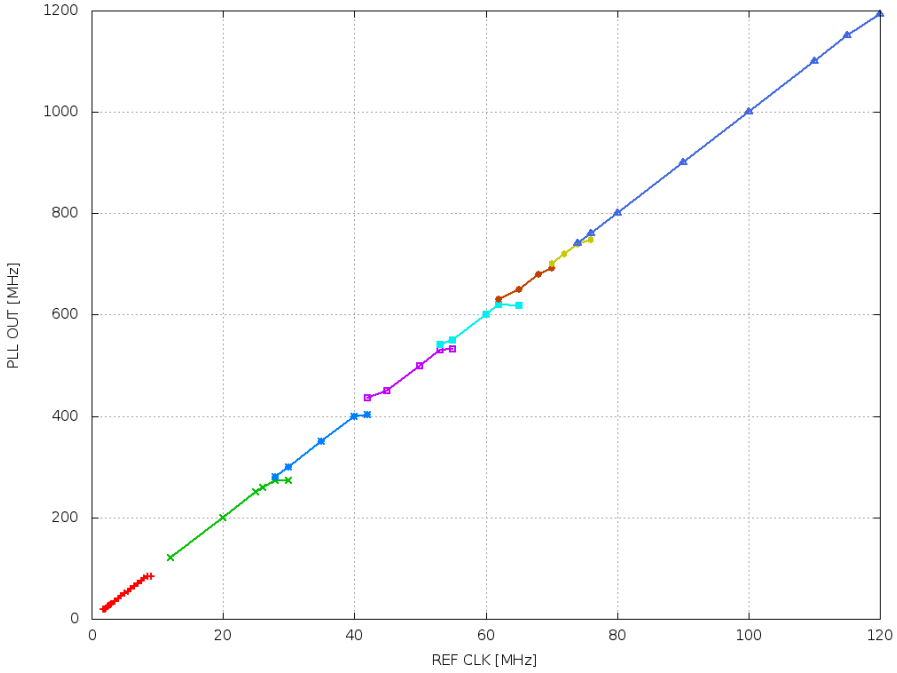
300 x 300 um

Design specs:

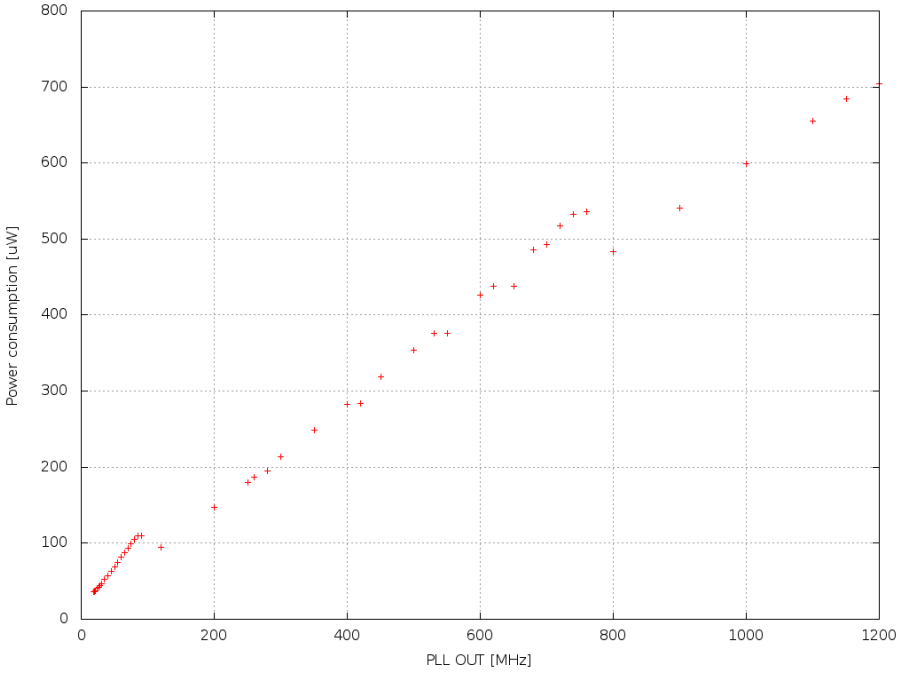
- Architecture: type II PLL with 2nd order filter
- Scalable frequency & power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- ***Submitted and fabricated in 2012, the tests have just started…***

Preliminary measurements
PLL – Transfer function, power consumption

PLL transfer function – CLK out vs CLK in



Power consumption measurements

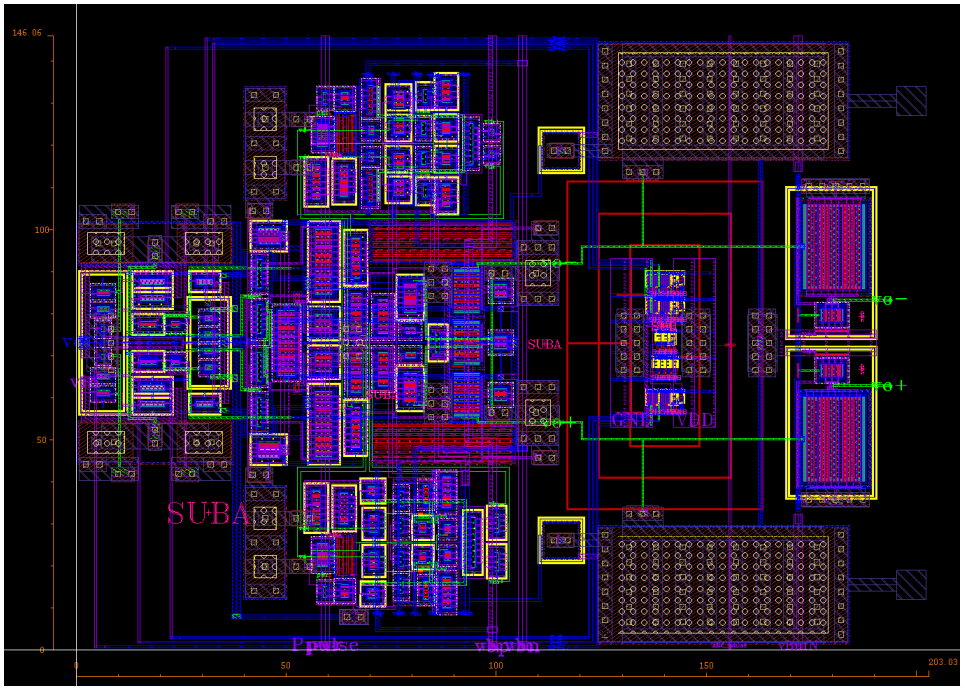


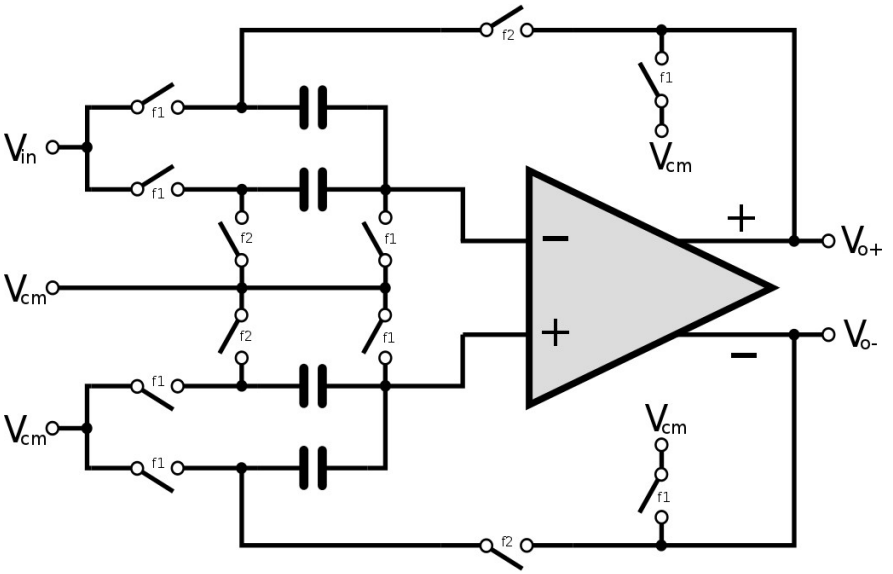
- PLL measurements have just started (~ 2 days) and are in progress...
- PLL output CLK in frequency range 15MHz-1.2GHz already observed
- There are some gaps between frequency ranges...
- Automatic mode detection looks promising
- SLVS driver works at least up to 1.2 GHz (used for PLL output)

Developments in IBM CMOS 130nm
Single Ended-to-Differential converter

Single Ended to Differential converter (in front-end ASIC)

- Dynamic input range ~600 mV
- Differential output range ~1.2V
- Maximum frequency ~ 50 MHz

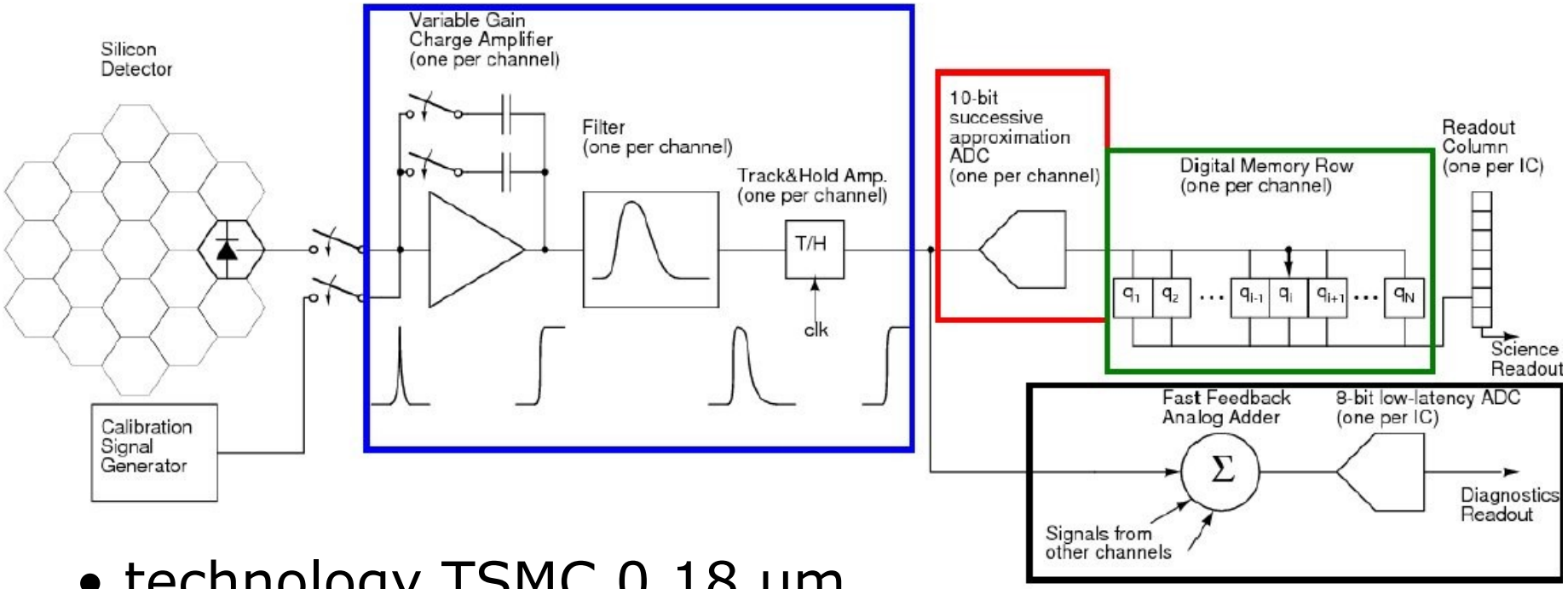




Design submitted February 2013

Old BeamCal readout ASIC

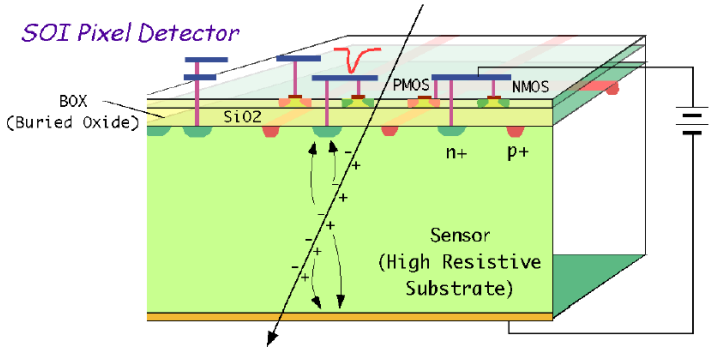
Angel Abusleme



- technology TSMC 0.18 um
- 32 channels
- memory: 2820 words (10 bits + parity) per channel
- analog addition of 32 channels for fast feedback

Pair monitor

- First readout ASIC
  - CMOS process: **0.25 µm TSMC**
  - Chip size : 4 x 4 mm^2, **6 x 6** pixels (36)
  - Test setup based on KEK-VME 6U module was prepared
  - Sensor needs to be bound bonded



- Silicon On Insulator (SOI) technology – first readout prototype
  - The sensor and readout electronics are integrated in the SOI substrate. (monolithic)
  - **SOI 0.2 µm** CMOS process
  - Chip size : 2.5 x 2.5 mm^2, **3 x 3** pixels (9) (only readout)
  - The noise level (260 e$^-$+130 e$^-$/pF) is much smaller than typical signal level (20000 e$^-$)
  - All the ASIC components work correctly.