# Pixel high rate pulse test, 3

Daniel Pitzl, DESY

Hamburg CMS Pixel Upgrade meeting, 3.5.2013

- update from DPIX 26.2.2013
- highly irradiated psi46digtrig 214:
  - 113 MRad

# Data Rate Estimations

- Simulation with Pythia Z2 tune and GEANT4
- Assuming 24 bits per hit, 100 kHz level 1 trigger rate
- Peak luminosity = $2x10^{34}cm^{-2}s^{-1}$, $\sigma_{tot}$=80mb, $\sigma_{signal}$=1.5mb, 25 ns BC

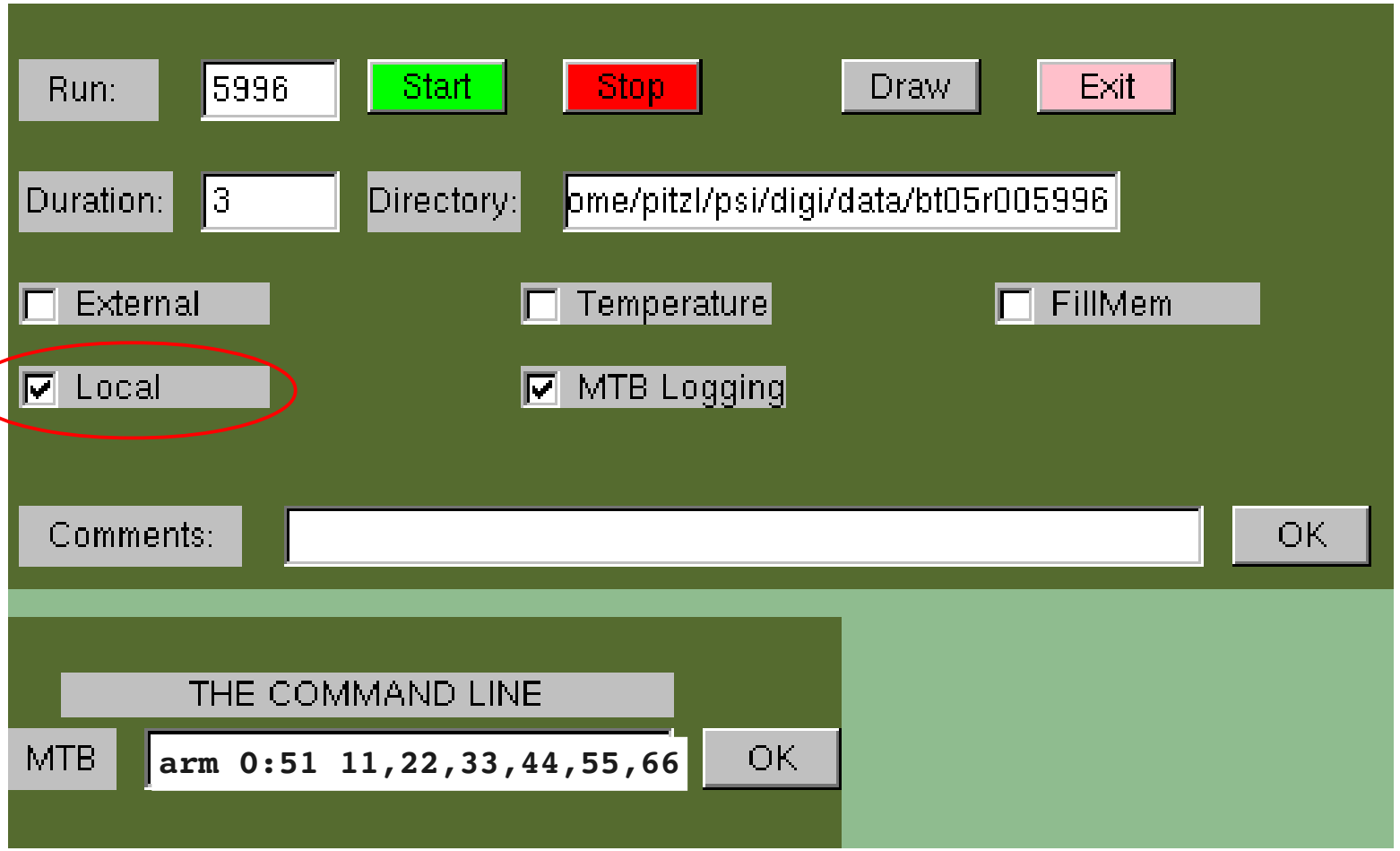
| Layer | 1 @ 2.9cm | | 2 | 3 | 4 |
|---|---|---|---|---|---|
| Pixel fluence [MHz/cm$^2$] | 520 | | 119 | 52 | 27 |
| Hits / trigger / module | 190 | | 40 | 18 | 8.4 |
| MBit/link/sec | 435 | | 118 | 66 | 45 |

1 ROC = 0.65 cm$^2$

Hans-Christian Kästli,
CMS Upgrade plenary,
20.7.2011

# takeData with test pulses

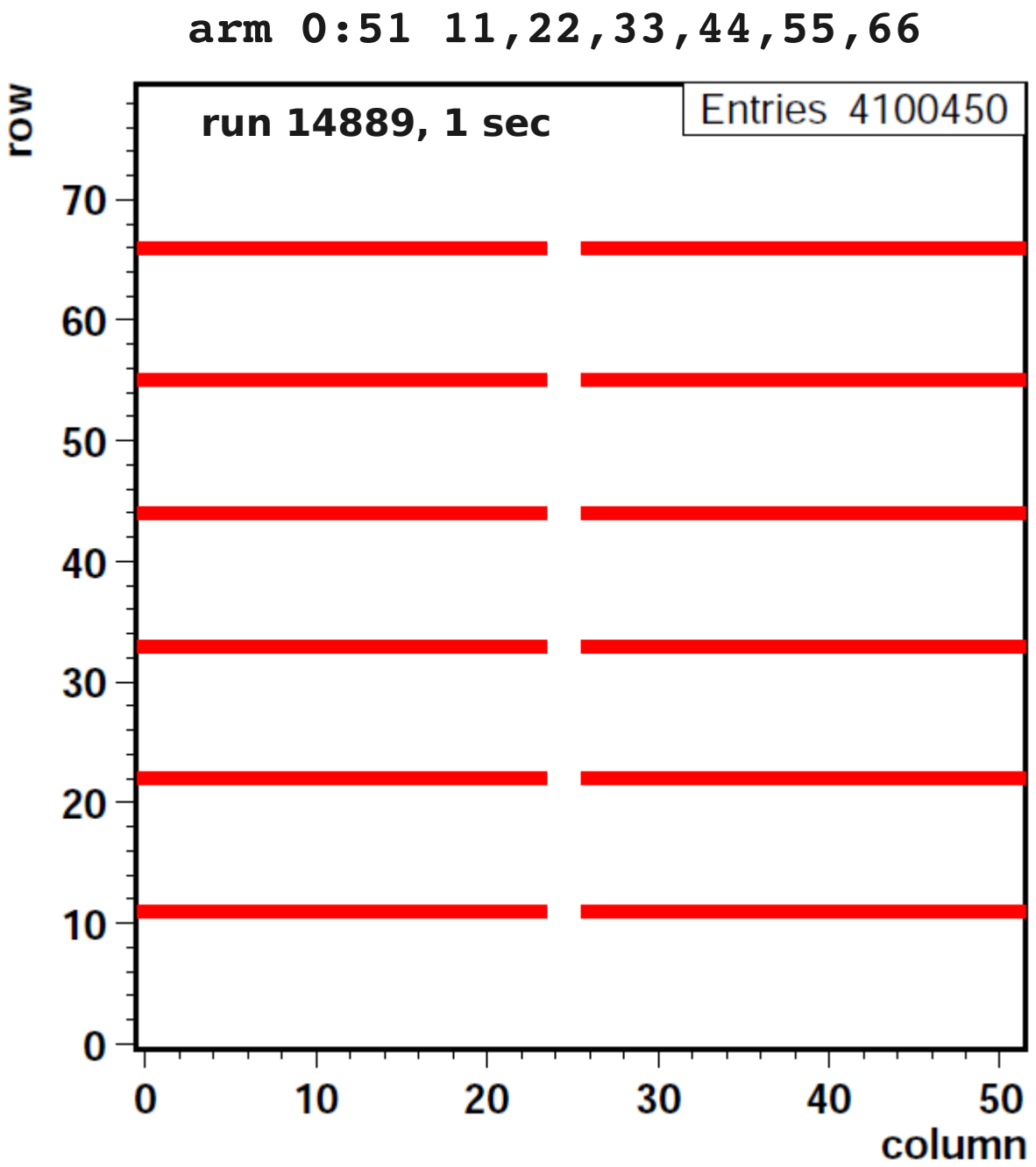
internal pulse trigger




**arm: activate test pulse for columns 0..51 in 6 rows**

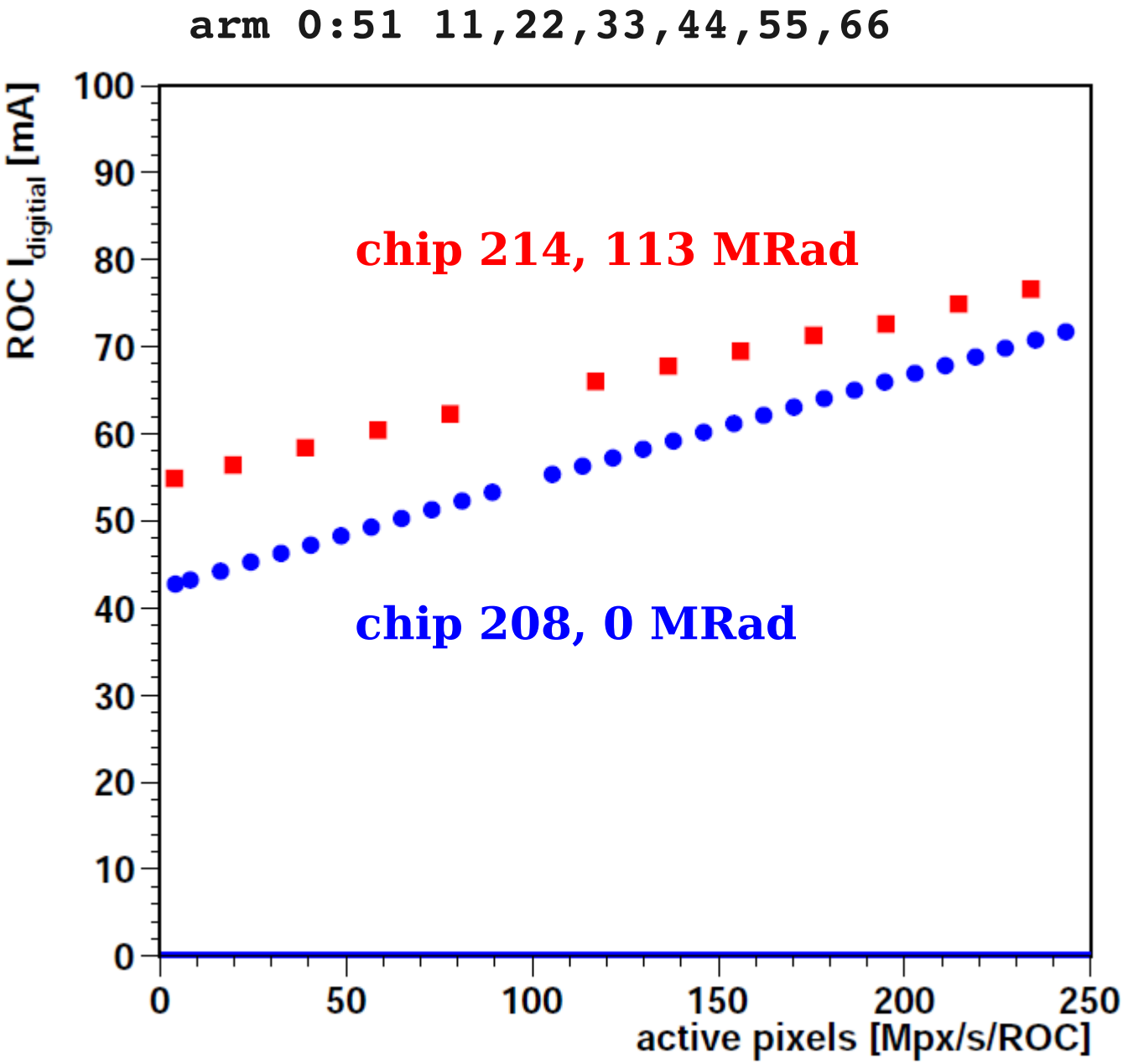
use FPGA firmware atb5 with compact data format,
extended event buffer

# high rate test pulse run




- psi46digtrig chip214
  - **113 MRad**
  - (1 dead DC)
- 300 pixels pulsed
- 13 kHz trigger rate (`trep 12`):
  - 4 Mpx/s read out
  - 19.6 MB/s
- 20 calibrate pulses:
  - **81 Mpx/s active.**
- 100% efficiency
- no data errors

# ROC digital current vs activity



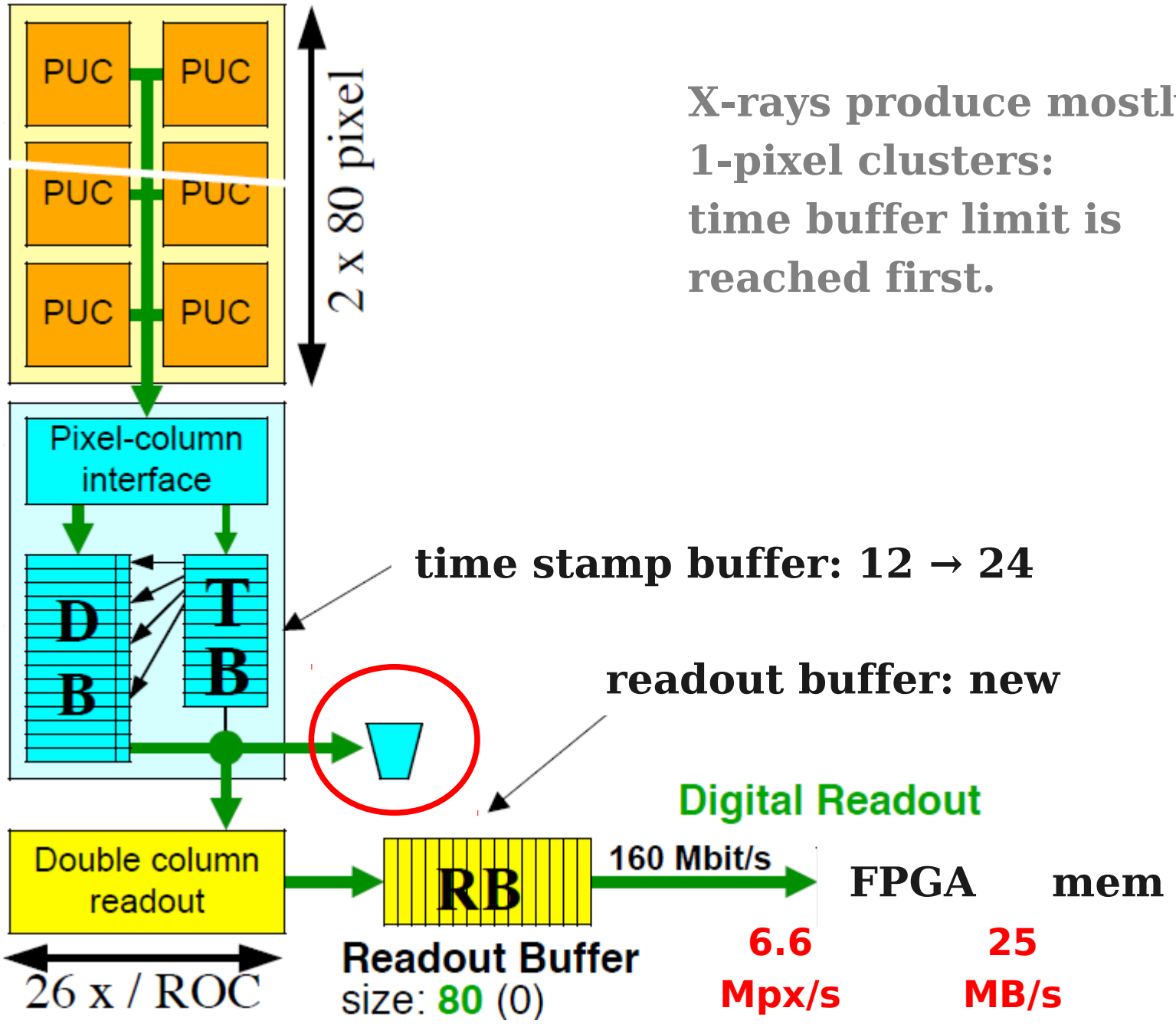

- 300 pixels pulsed
- 13 kHz readout
- vary number of calibrates: 1..60
- measure current by DVM at test board
- current increases linearly with ROC activity:
  - 1 mA / 8 Mpx/s
- Irradiated:
  - +12 mA offset
  - 1 mA / 10 Mpx/s

# Summary

- High rate test pulse test
  - error-free readout of up to 4 Mpx/s (300 pixels at 13 kHz)
  - ROC activity up to 240 Mpx/s simulated with multiple test pulses
  - digital ROC current rises linearly with activity: 1 mA / 8 Mpx/s
- Highly irradiated psi46digtrig (113 MRad):
  - needs 12 mA (28%) more digital current at low activity
  - current increase is smaller: 1 mA / 10 Mpx/s
  - error-free readout at 4 Mpx/s

# Back up

# double column readout




**X-rays produce mostly 1-pixel clusters: time buffer limit is reached first.**

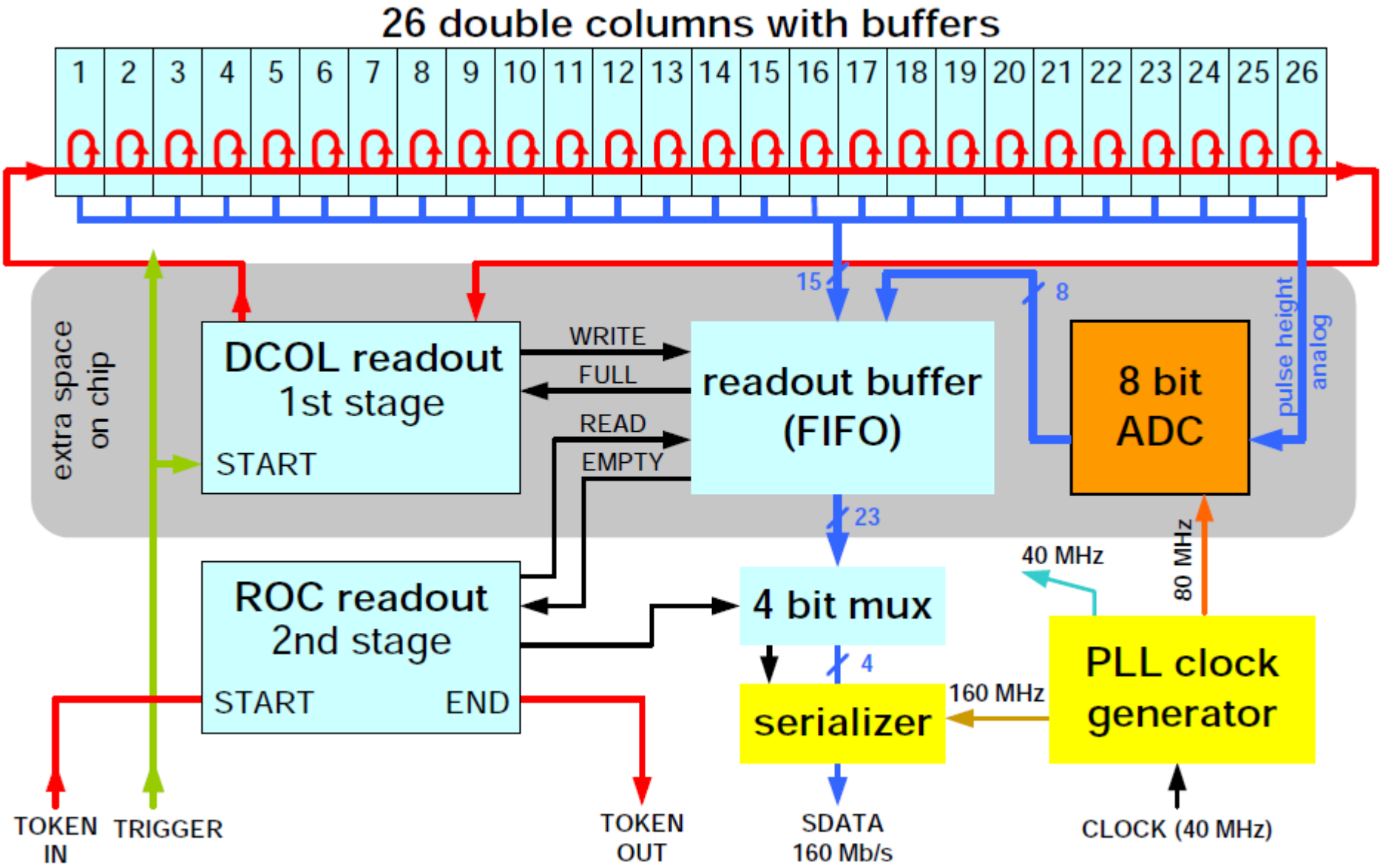
**data buffer: 32 → 80**

**auto clear when full**

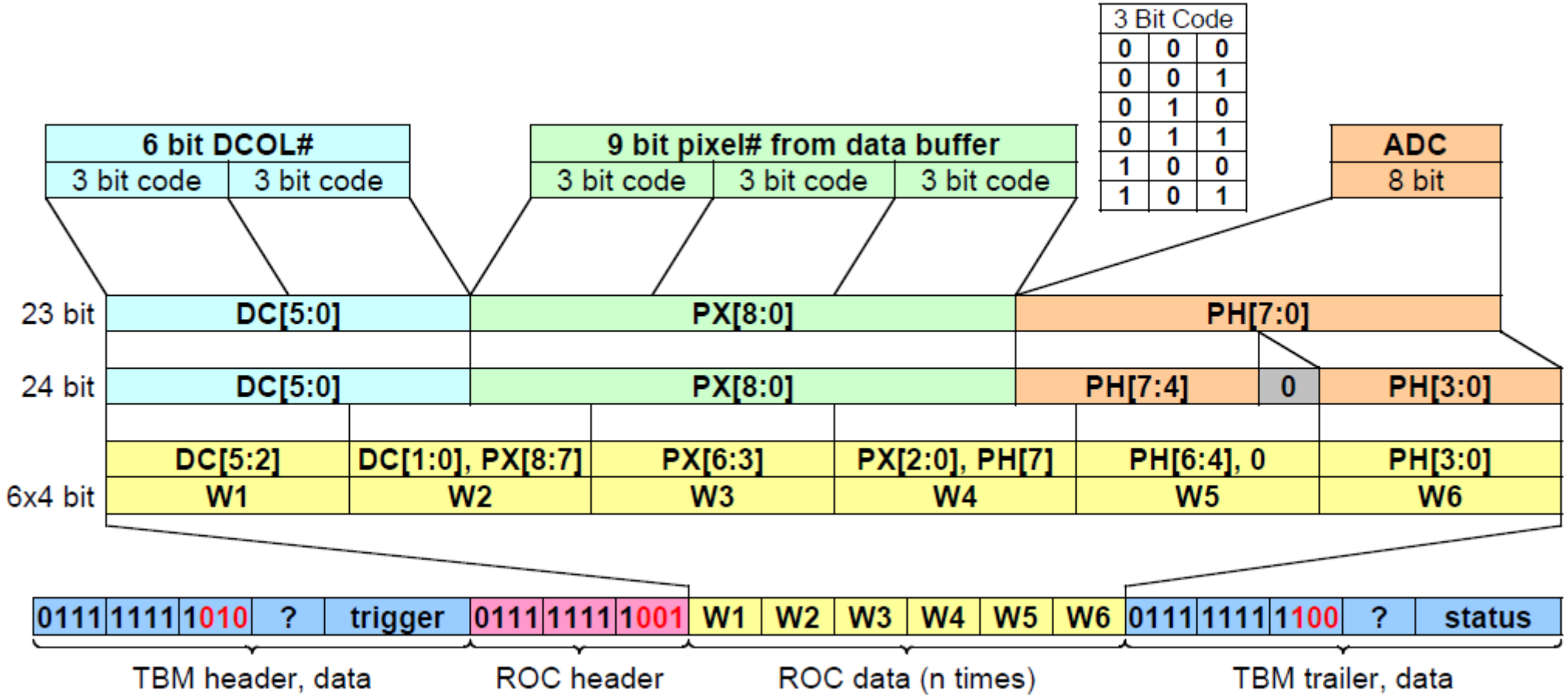
**time stamp buffer: 12 → 24**

**readout buffer: new**

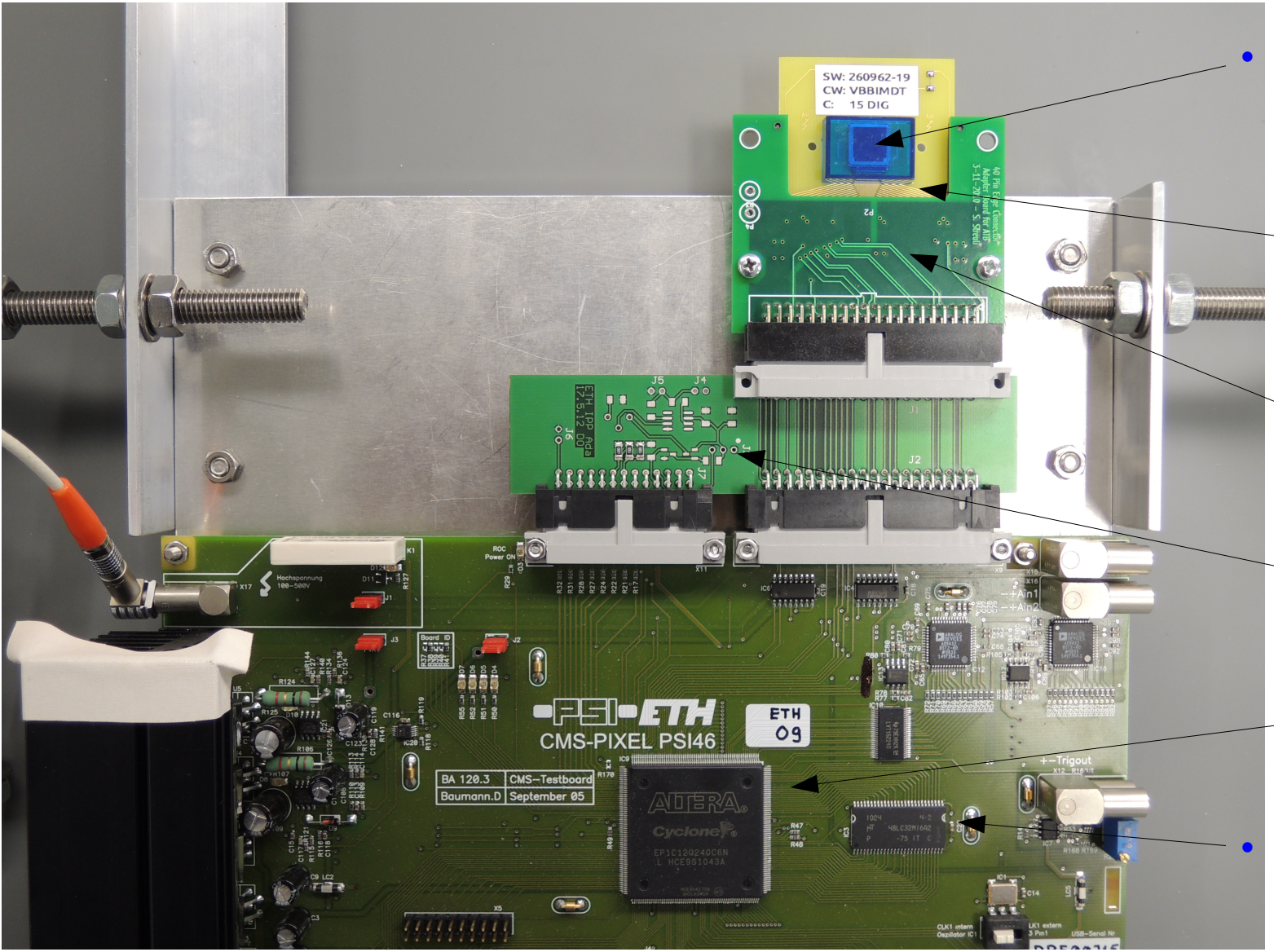
# psi46dig periphery



# digital ROC data format



# psi46 test board with digital ROC




- Single chip module:
  - Indium bump bonded at PSI
  - Glued and wire bonded to carrier printed circuit board
  - Interface card to psi46 TB with edge connector
  - ETH adapter card for digital 160 MHz differential signal directly into FPGA (LCDS into LVDS)
- 64 MB memory

# tbParameters.dat

```
 8   clk    0  # delay of ROC clock [ns] w.r.t. TB ADC
 9   sda   22  # delay of I2C send data [ns]
10   ctr    0  # delay of cal trig reset [ns]
11   tin   13  # delay of token in  = start readout [ns]
12   rda    3  # delay of token out = end of read [ns]

17   trc   18  # time between reset and cal [BC]
18   tcc   38  # time between multiple calibrates [BC]
19   tct  104  # time between cal and trig [BC]
               #  daqFrame.cc: WBC = tct - 5 for Vcal
20   ttk   18  # time between trig and token [BC]
21  trep   12  # trig rep = time between triggers [many BC]
22    cc   20  # number of calibrates

77   spd    0  # 0 = 40 MHz
```

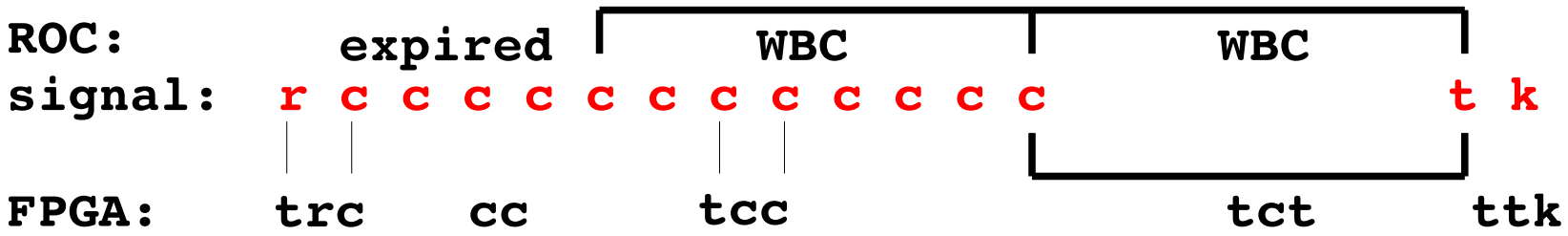
# test board signals and steering

## signal sequence from FPGA to ROC:

**reset  *n*×calibrate  trigger  token = r c(ccc) t k**

**tbParameters.dat:**

| | | |
|---|---|---|
| trc | 18 | time between reset and cal [BC] |
| cc | 20 | calibrate counter *n* |
| tcc | 38 | time between calibrates [BC] |
| tct | 167 | time between calibrates and trigger |
| | | WBC = tct – 5 = 162 |
| ttk | 18 | time between trigger and readout token [BC] |
| trep | 12 | time between triggers [many BC] |



# High rate ROC test

**pixels read out:**

$$f_{read} = f_{trig}\ n_{pix/DC}\ n_{DC}$$

**pixels active:**

$$f_{act} = f_{trig}\ n_{cal}\ n_{pix/DC}\ n_{DC} = n_{cal}\ f_{read}$$

**limit:**

$f_{read}$ **: write < 25 MB/s into memory, < 6.6 Mpx/s ROC rate**

**reached:**

$n_{cal} = 20,\ f_{read} = 4$ Mpx/s => $f_{act} = 80$ Mpx/s/ROC