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Data Handling Processor Development
Status of the First Production Version DHPT 1.0

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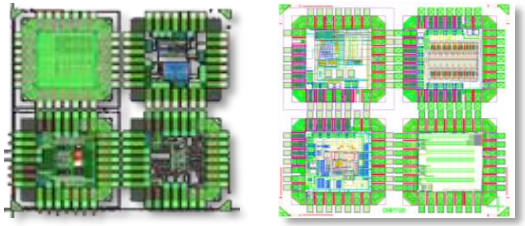
PXD/SVD Worksop, DESY, October 21-24, 2013

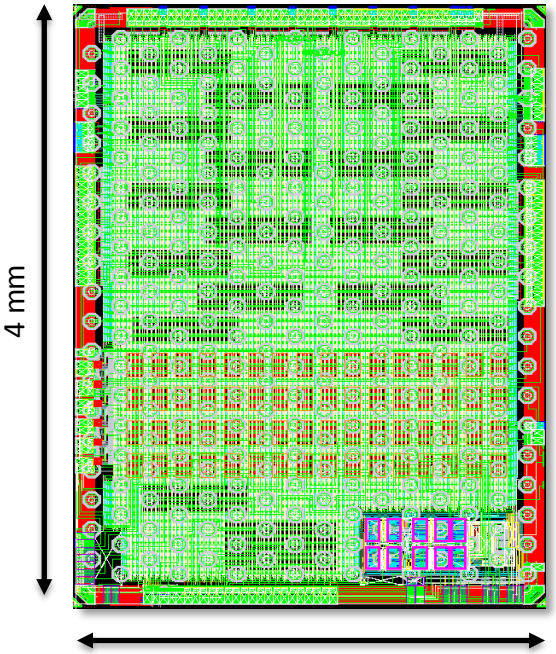
DHP Implementation in TSMC 65nm

- Test chips for **custom IP verification**
  - Two mini@sic submissions in 2011 and 2012
  - 1.6GHz PLL
  - Gigabit link driver
  - LVDS transmitter & receiver
  - Pixel matrices with analog front-ends (CSA + comp.)



DHPT 0.1 and DHPT 0.2 test chips

- DHPT 1.0, **first production version**
  - MPW submission in Aug. 2013
  - 12 mm^2 area, C4 bumps (SAC 305), 200µm pitch
  - Mainly digital with analog IP blocks (PLL, serializer, Gbit link, LVDS …)



Data handling processor DHPT 1.0

DHPT 1.0 New Features & Improvements

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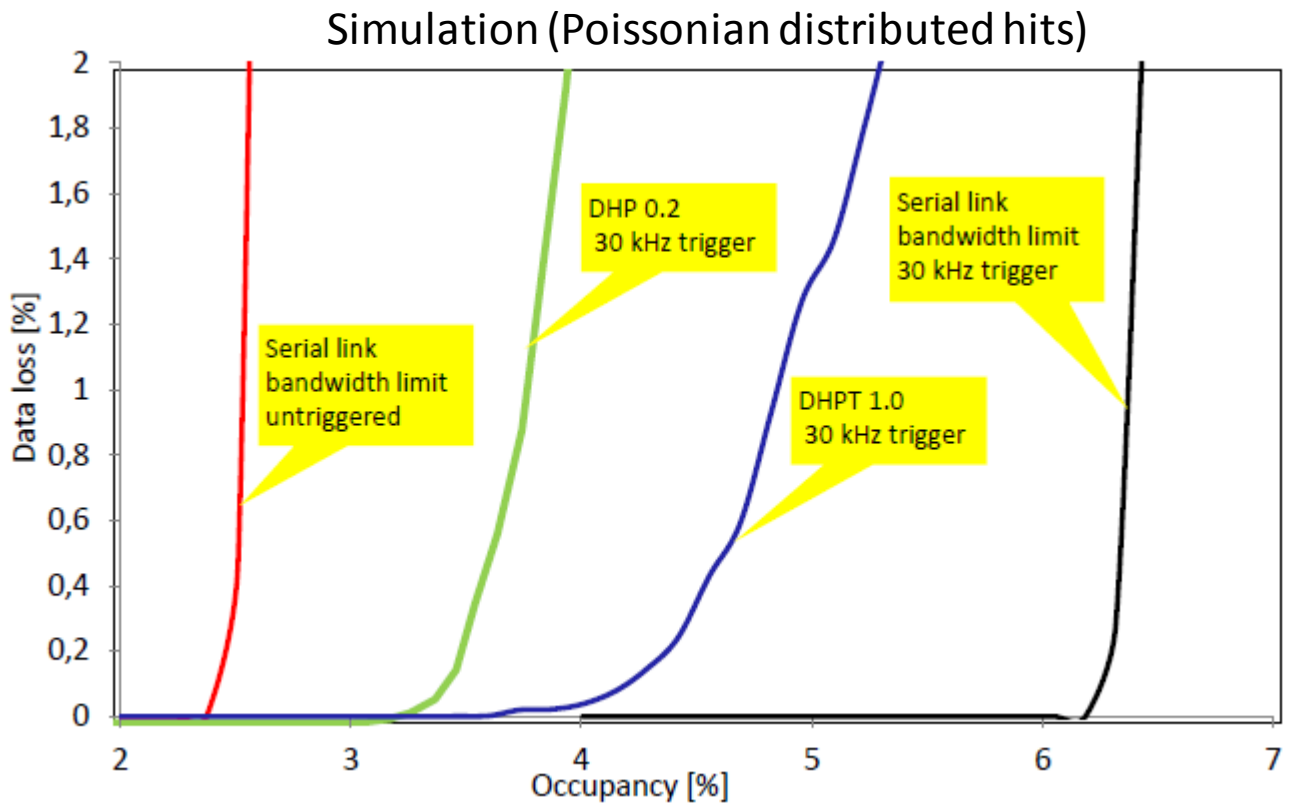
- Fully programmable Switcher Sequencer ➔ Gated Mode support
- Fast commands now encoded on trigger line (4 bit Manchester coded):
  - TriggerOn, TriggerOff: selects frame(s) to be processed and read out
  - Veto: selects Gated Mode Switcher sequence
  - DataDump: initiates transfer of raw (non 0-soppressed) data
- Increase of FIFO buffer depth ➔ improve data efficiency at high occupancies
- More raw data memory
  - Up to four frames, use for calibration
  - Double buffer scheme for pedestal storage (one buffer active while the other buffer gets updated in the background)
- Differential DCD clock output

Occupancy Dependent Data Loss



- Larger FIFO buffers lead to some improvement of the data handling capabilities
- Data losses start to become critical at 4%

Status & Outlook

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- Samples expected end of November (100 chips, C4 bumps)
- Test bench currently being upgraded from DHP 0.2 to DHPT 1.0
  - Software (trigger command scheme, gated mode sequencer control) ➔ in progress
  - Hardware (Test PCB, needle card) ➔ compatible
  - Test procedures for needle card testing ➔need to improve coverage
- Silicon verification
  1. Start tests with DHPT 1.0 mounted on PCB with WB adapter
  2. If successful continue with needle card testing

- Only a few old DHP 0.2 left (~9 pcs., refurbished)

➔ Decide what to do with them until we have verified the new DHPT 1.0

  - Best case scenario: new DHPT 1.0 chips available for E-MCM / PXD6 assemblies by end of this year
  - Worst case scenario (DHPT 1.0 needs re-design): New chips not available before mid 2014

Outlook

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- MPW submission details
  - Cost (12 mm^2, one wafer included): 59 TUSD + 12 TUSD for bumping ➔ 52 TEUR
  - Extra 12“ wafer (100 chips): 9 TUSD
  - Two MPW runs per month, turn-around ~12 weeks

- PXD production
  - Can be done with MPW production + extra wafers, no engineering run needed
  - 160 chips for 40 modules + overhead for E-MCM, test assemblies, production contigency etc.
  - How many „green“ chips do we need?

- DHPT (65nm only) production costs
  - 2x test chip (mini@sic DHPT 0.1 & DHPT 0.2) ➔ 45 TEUR
  - 2x MPW (DHPT 1.0 & possible redesign DHPT 1.1) + 5 extra wafers ➔ 140 TEUR