LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

LMU München - Excellence Cluster Universe

PS & Services

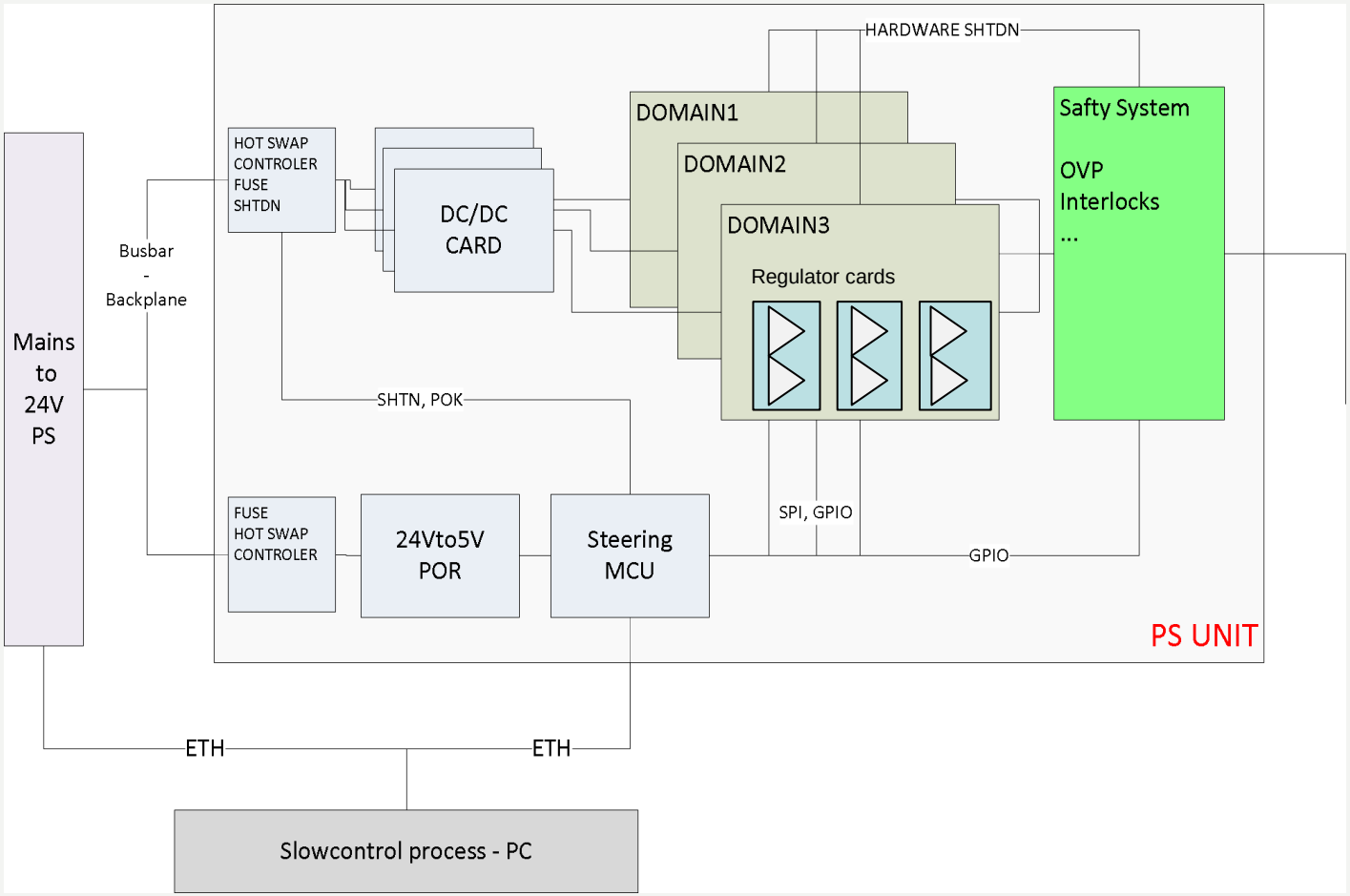
Stefan Rummel

DEPFET Collaboration Meeting
Hamburg
21.10.13-23.10.13

Overview

- Preproduction
  - Status
  - OVP Status - Cracow
- Services
  - Kapton development
  - Dock Box
  - Patch Panel
- Test Beam preparation
- Outlook

PS System Layout



Demonstrator vs. Preproduction PS

	Demonstrator	Preproduction PS
# Channels	16 (up to 24)	24
Mechanics	21TE	28TE
Power distribution	37 pin D-SUB	Mixed Layout D-Sub, final cable
Output Power	DEPFET + 1 pair DCD/DHP	DEPFET + 4 pairs DCD/DHP
Slow control	Chromosome + EPICS	Chromosome + EPICS

Preproduction

- Goal: 10 Units, 24 Channels, full output power → Final designs specifications
- Output connectors suitable for final cables (mixed layout D-Sub)
- Final DC/DC converter cards → Full output power
- Bug fixing / optimizing
  - MCU card finalized (Interlocks)
  - Regulator cards finalized (Temperature measurement on regulators, opt. SNR of ADC's)
  - Breakout boards adapted
  - OVP substitute

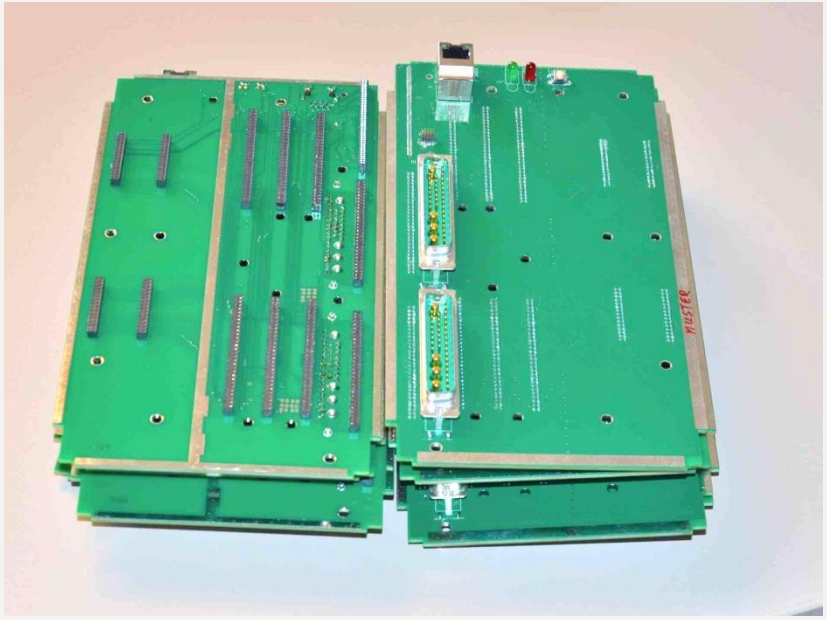
Preproduction status

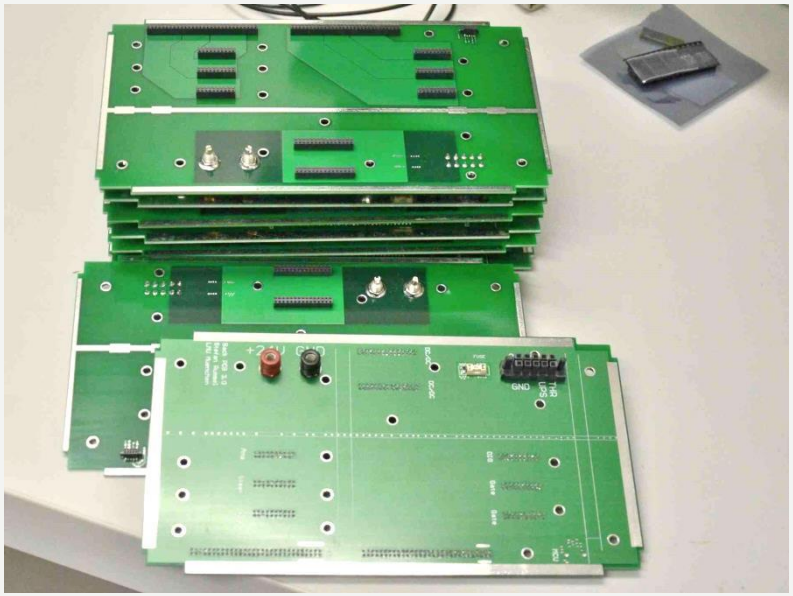
- PCB's are delivered
- Components provided by us ordered 80%

→ Production is under way – see the following slides

Preproduction status

- Several items are produced - Front PCB, Back PCB, empty OVP Card

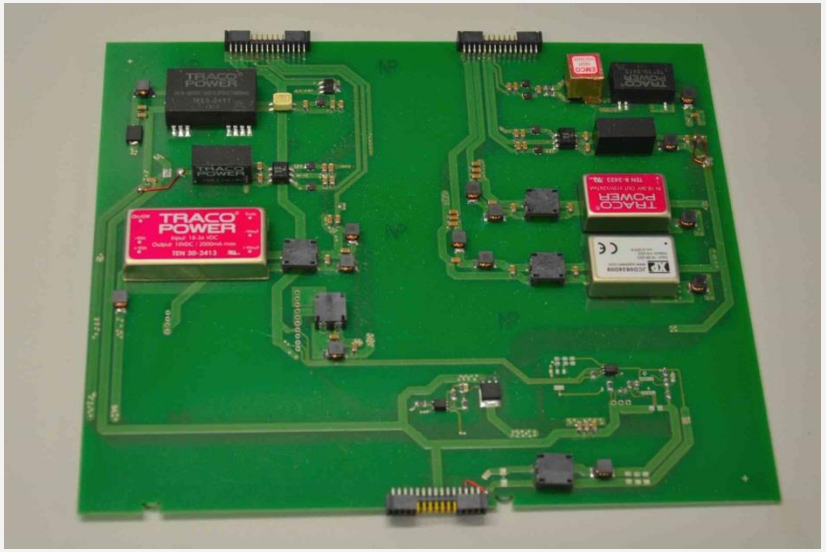


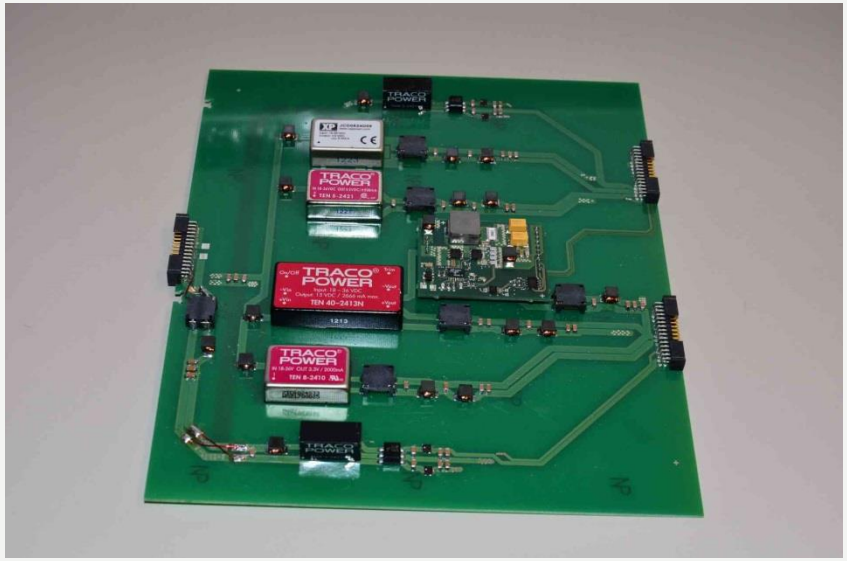


Preproduction status

- Final DC/DC converter cards are tested, manually produced in two sets
- Step-down converter is finalized and successfully tested

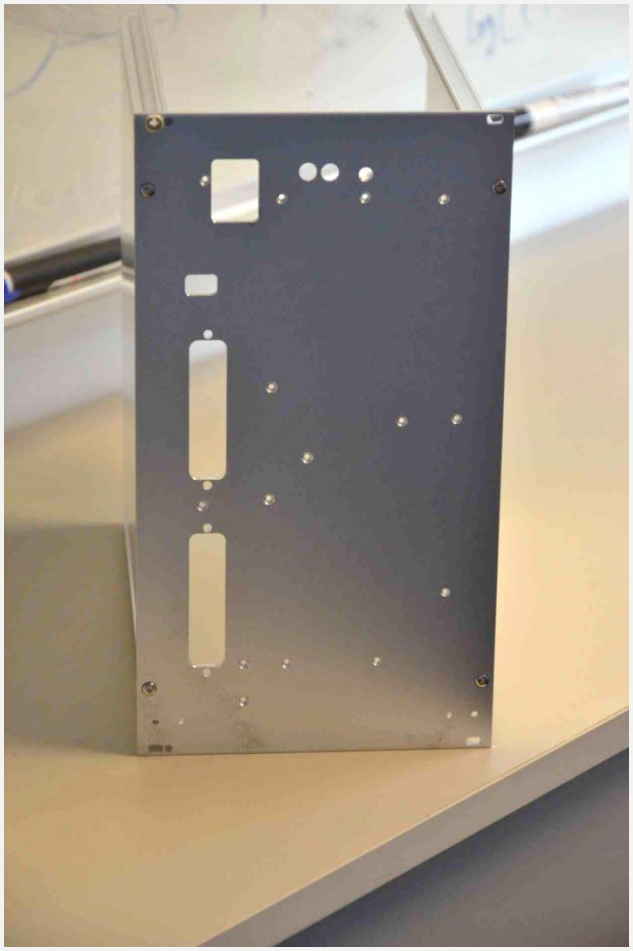
→ Ready for production





Preproduction status – Mechanics

- Box designed and first sample produced
- Extra wide crate received



Overvoltage Protection

Overvoltage Protection Module – fixed ranges

Protected ranges of all voltages fixed by hardwired resistor networks is presented on next slides on yellow marked columms.

Voltage margin is bigger than nominal by +- 1 V or by +- 2 V.

In case of over-voltage conditions all voltages in the domain will be switched off by hardwired machanism.

Please check proposed values and send us comments to:

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All voltages will be fixed by resistor networks !!!

	TMMH2						Voltage	Protection	Relative to:
							Min [V]	Max [V]	
MCU_GND	1	31	OVP_IO.STATUS						
OVP_IO.MUX_OUT	2	32	OVP_IO.A5						
OVP_IO.A3	3	33	OVP_IO.A4						
OVP_IO.A1	4	34	OVP_IO.A2						
5V_MCU	5	35	OVP_IO.A0						
I2C.SCL	6	36	SHTDN1						
I2C.SDA	7	37	SHTDN2						
GGND	8	38	GGND						
SENSE_ST12	9	39	ST12	Gate Domain					
GND_SENSE_ST12	10	40	SENSE_ST10						
GND_SENSE_ST10	11	41	ST10	CCG2	(-10V)-(+1V)	10mA	-12	3	
GND_SENSE_ST9	12	42	ST9	CCG1	(-10V)-(+1V)	10mA	-12	3	
SENSE_ST9	13	43	GND_SENSE_ST11						
SENSE_ST11	14	44	ST11	CCG3	(-10V)-(+1V)	10mA	-12	3	
GGND1	15	45	GGND1						
SENSE_ST16	16	46	ST16	Steering Domain					
GND_SENSE_ST16	17	47	SENSE_ST14						
GND_SENSE_ST14	18	48	ST14	SW_SUB	lowest				
SENSE_ST16	19	49	ST13	Depletion/VBP	(-80V)		-100	0	
SENSE_ST13	20	50	GND_SENSE_ST15						
SENSE_ST15	21	51	ST15	SW_SUB_REF		0.06mA			
DGND	22	52	DGND						
DV4	23	53	DV4	SW_DVDD	3.3V	24mA		4.5V	
SENSE_DV4	24	54	GND_SENSE_DV4						
GND_SENSE_DV2	25	55	SENSE_DV2						
DV2	26	56	DV2	DHP_IO	1.2V			1.5V	DGND
DV1	27	57	DV1	DCD_DVDD	1.8V	1A		2.5V	DGND
GND_SENSE_DV1	28	58	SENSE_DV1						
SENSE_DV3	29	59	GND_SENSE_DV3						
DV3	30	60	DV3	DHP_CORE	1.2V	580mA		1.5V	DGND
				Digital Domain					

Piotr Kapusta, Bartlomiej Kisielewski

21-23 Oct. 2013
DESY

All voltages will be fixed by resistor networks !!!

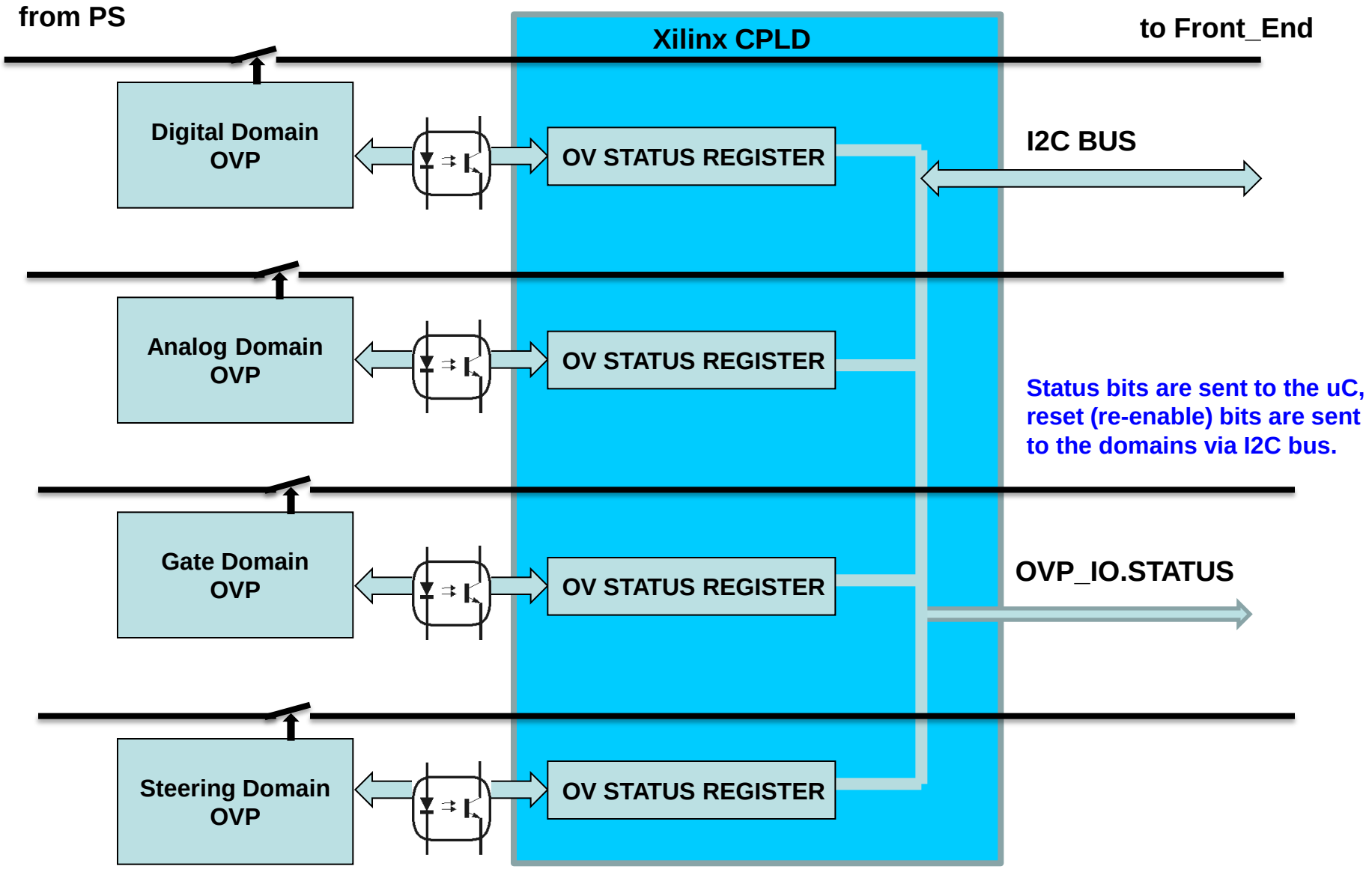
	TMMH4				Voltage/Range	Current	Voltage	Protection	Relative to:
							Min [V]	Max [V]	
T5V	1	31	Bm5V						
Tm5V	2	32	B5V						
TGND	3	33	BGND						
Gate_5V	4	34	STEER.m5V						
Gate_m5V	5	35	STEER.5V						
Gate_GND	6	36	STEER_GND						
STGND	7	37	STGND						
SENSE_ST4	8	38	ST4	VGUARD	(-7V)-(0V)		-8	1	
GND_SENSE_ST4	9	39	SENSE_ST2						
GND_SENSE_ST2	10	40	ST2	Clear Off	(0V)-(+5V)	60mA	-1	6	
GND_SENSE_ST1	11	41	ST1	Clear On	(+7V)-(+25V)	60mA	5	27	
SENSE_ST1	12	42	AGND_SENSE_ST3						
SENSE_ST3	13	43	ST3	Bulk/VBULK	(+5V)-(+15V)	10mA	3	17	
STGND1	14	44	STGND1						
SENSE_ST8	15	45	ST8	GateOFF	(-3V)-(+5V)	60mA	-5	7	
GND_SENSE_ST8	16	46	SENSE_ST6						
GND_SENSE_ST6	17	47	ST6	GateON2	(-13V)-(-3V)	60mA	-15	-1	
GND_SENSE_ST5	18	48	ST5	GateON1	(-13V)-(-3V)	60mA	-15	-1	
SENSE_ST5	19	49	AGND_SENSE_ST7						
SENSE_ST7	20	50	ST7	GateON3	(-13V)-(-3V)	60mA	-15	-1	
MCU_GND	21	51	MCU_3.3V						
AGND	22	52	AGND						
AV4	23	53	AV4	REF_IN	1.1V	360mA		1.5V	
SENSE_AV4	24	54	AGND_SENSE4						
AGND_SENSE2	25	55	SENSE_AV2						
AV2	26	56	AV2	VSOURCE	(0V-7V)	100mA	-1	8	
AV1	27	57	AV1	DCD_AVDD	1.8V	2.3 A		2.5V	AGND
AGND_SENSE1	28	58	SENSE_AV1						
SENSE_AV3	29	59	AGND_SENSE3						
AV3	30	60	AV3	AMP_LOW	0.35V	(-1A)	-1	1	

Steering Domain

Gate Domain

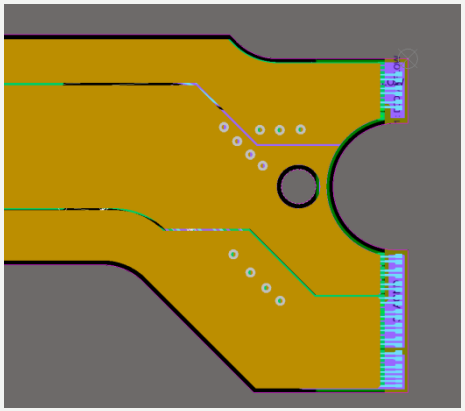
Analog Domain

Digital Control of the Over Voltage Protection Board



Services

Services - Kapton



- Design of Kapton transferred to MPI
- Design has been transferred to “Pads” and successfully finished
- Gerber Data transfered to Taiyo, delivery of first prototypes by November this year
- 5 working Kapton Flexes are expected

Next steps:

- Incorporate Capacitors into design
- Design of 4 types (Forward,Backward,Inner,Outer)

Services – Dock Box

- Design man power kindly provided by MPI
- Layout according to our design rules
  - 100 Ohm
  - Resistance of power traces adapted to expected current
  - CMD filter capacitors

- Design is finished, received Gerber data last week
- Lead time ~12WD

Services – Patch Panel

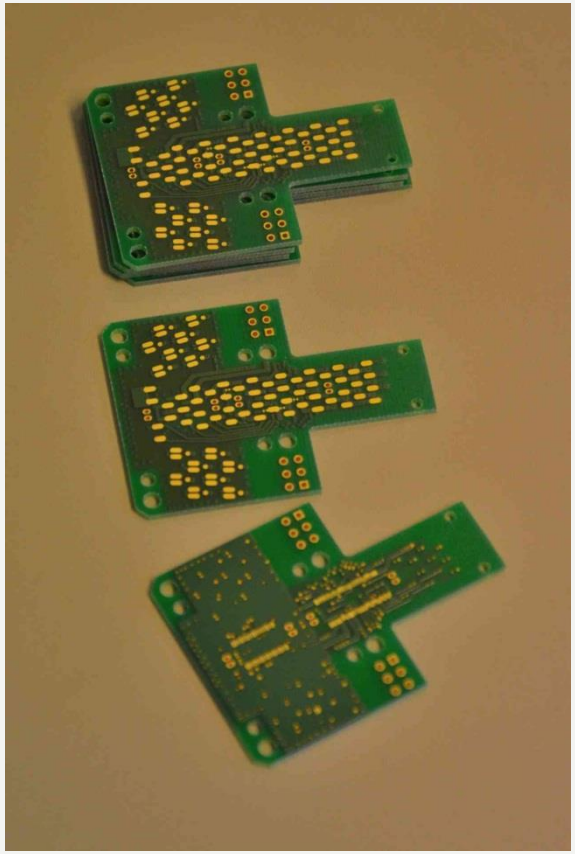
- Design of latest PP done

- Features:
  - Incorporates latest mechanical requirements
  - Solder pads for ALL cables
  - Samtec SS4/ST4 towards Kapton

- Design finished (8 Layers, Blind Vias)

- Mechanical Dummy for solder tests has been produced
- Expected lead time 12WD for full production

→ Testing of assembly procedure crucial!

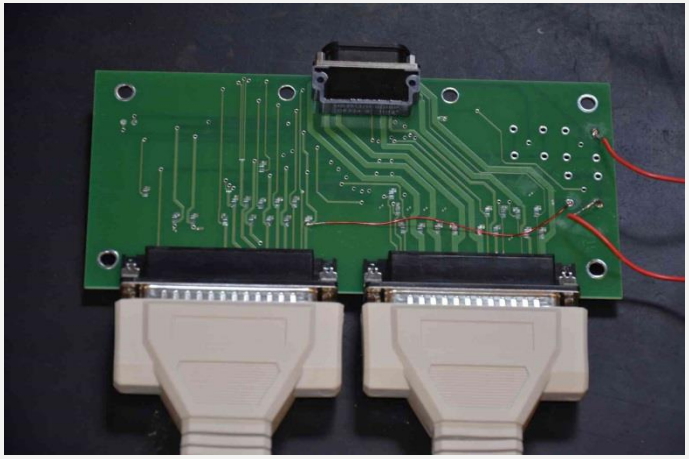


PS for TB status

PS for TB Status

- Demonstrator and Adapter to EMCM electrically tested with dummy EMCM module at HLL
- Hardware ready for commissioning phase
- Software is running, detailed testing after this meeting, Thorsten will present details on Software integration

→ Expected delivery to DESY next week



Summary

- Preproduction is ongoing, first items are produced
- OVP development is ongoing
- Kapton development is continued at MPI, first samples from Taiyo expected in November
- Design of Dock box and Patch Panel, mechanical PP dummy produced
- PS and EMCM-Demonstrator adapter successfully tested with EMCM

Backup