The 2nd Prototype of the SVD FTB
Recent Status and Plans

for
SVD Electronics session on Tuesday
at
4th Belle II PXD/SVD Workshop
and
14th International Workshop on DEPFET Detectors and Applications
in DESY Hamburg, Germany
21-23 October 2013

I. Status of Hardware
II. Plans and final production
III. Status of Firmware
IV. Firmware
V. DESY Test
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I. Status of Hardware

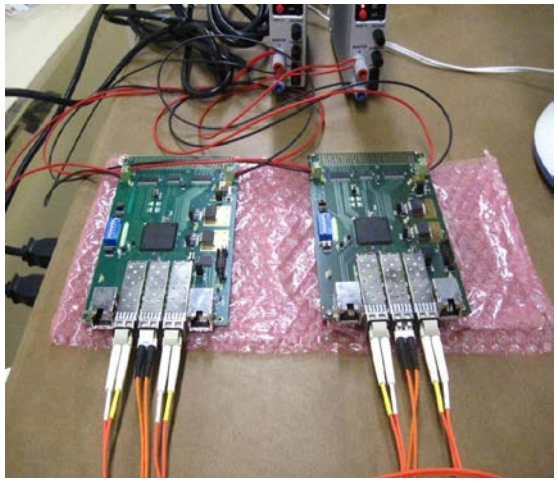
PCB Design version2

After many tests performed by Katsuro (thank you a lot for your effort) conclusions are as follow:

- PCB design is correct and may be send to final production
- No difference between FR4 and FR408 -> FR4 will be used for final production

from SVD meeting minutes by Koji Hara:

- FTB test (Katsuro) PRBS-7 tests finished without error for 8 days at 3.175Gbps.



result

•3.175 Gbps PRBS-7 data check
–no error is observed for 8-days running
–corresponding to error-less operation of the whole FTB system (48 FTBs) for 3.3-hours
–and also corresponding to error-less physics data for 11-days
•assuming 256word event size and 30kHz trigger rate.

II. Plans and final production

List of changes

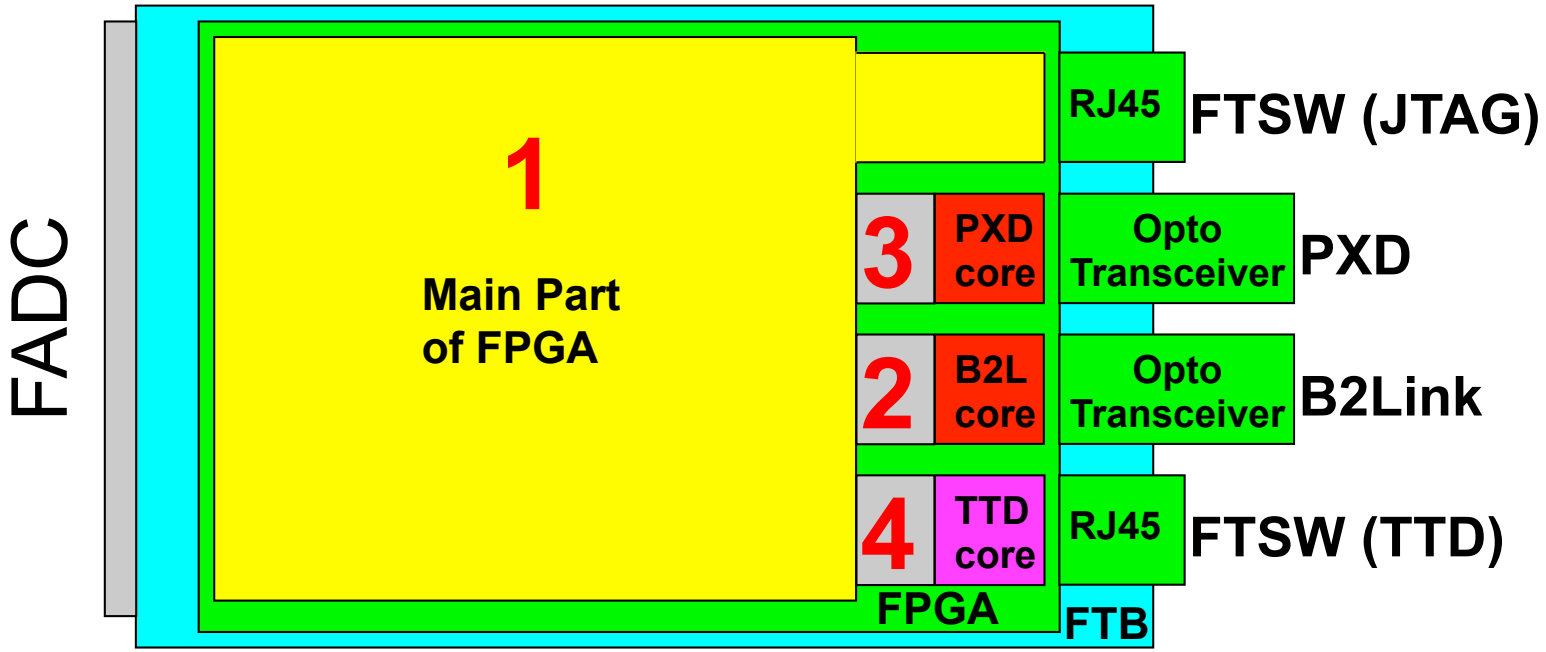
- one LED diode per OptoLink should be added on Front Panel. The best location is on bottom side of PCB. Under investigation.
- Two RJ-45 changed to different type with LEDs in front – not decided yet.

- Final PCB design finished to the end of 2013
- Even though the tests have been passed successfully we will wait for DESY tests results before we send the PCB to final production. Initial discussions have been held with the company.
- Most components are bought. The rest will be bought in December and beginning of January.

III. Status of Firmware

Main part of firmware is ready and works well.

Nb	Description	made by	responsible
1.	PCB design and Main Firmware	wacek	wacek
2.	Interface between FTB core and B2Link core	Katsuro	Katsuro
3.	Interface between FTB core and PXD core	Michael	Michael
4.	Interface between FTB core and TTD core	Nakao	Katsuro?



IV. Firmware

What has to be done:

1. Final version of the Interface to Registers – wacek, Katsuro. Temporary version is made by Katsuro
2. Interface for external (on board) Serial PROM which keeps content of some Mandatory Registers – wacek (in progress)
3. After suggestion by Nakao san:
‘FTB CRC’ is included in output Event from FTB . Should be changed to ‘FADC CRC’ – wacek (in near future)
4. In configuration as follows: FADC – FTB – DATCON but without B2Link final FIFO is not readout and transmission is blocked. Simple circuit to empty the final FIFO should be add – wacek (in near future)
5. Implementation of the new Belle2link and trigger/timing interface – Katsuro

V. DESY Test

1. Format of FTB Event

2. Equipment has to be taken to DESY

V. DESY Test - 1. Format of FTB Event

Nakao san wrote (06 Jul 2013) :
In my understanding the conclusion of the May/31 meeting is

- B2L does/should not care what is in FEE
- B2L adds two word header in addition to one word trailer
- Two word header info will be available from B2TT core in FEE
- HSLB adds two more word header and one word trailer

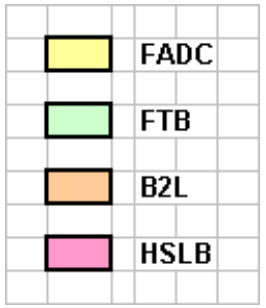
So, after adding the HSLB header and footer, it should be like this:

```
-------------------------------------------------
HSL: 0xFFAA(16) --- B2L header  |     reserved(16)
HSL: HSLB event count(24)       |     TTRX-tag(8)
-------------------------------------------------
B2L: TT-tag(16)                 |     TT-utime(16)
B2L: TT-stime(28)               | TT-type(4)
-------------------------------------------------
FEE: Data #0 (32)                 may be [ 0xFFAA(16) --- header of FEE  | reserved(16) ]
FEE: Data #1 (32)                 may be [ FEE event count(24)                | TTD-ev(8) ]
FEE:    ....
FEE: Data #n (32)                 may be [ 0xFF55(16) --- trailer of FEE | Checksum of FEE(16) ]
-------------------------------------------------
B2L: TT-tag-copy(16)            |  B2L checksum(16)
-------------------------------------------------
HSL: 0xFF55(16)                 | HSLB checksum(16)
-------------------------------------------------
```

FEE may be attaching header and trailer in the data, but B2L does not need to know.

V. DESY Test - 1. Format of FTB Event (cont.)

bit	HSLB Header		B2L Header		FTB Header		FADC Main Header	Input Header	FADC DATA	FADC Trailer	FTB Trailer	B2L Trailer	HSLB Trailer
31	F	HSLB Event Count	TT-tag	TT-stime	F	FTB Event Number	1	1	0	1	F	TT-tag-copy	F
30							1	0	FADC DATA	1			
29							0	FADC Channel Header DATA		1			
28							FADC Main Header DATA			0			
27	F				F					FADC Trailer	F		F
26													
25													
24													
23	A				A						5		5
22													
21													
20													
19	A				A						5		5
18													
17													
16													
15	Reserved	TTRX-tag	TT-utime	TT-type	0	Errors Field	FADC Event Number			FTB Flags Field	FTB CRC16 out	B2L checksum	HSLB checksum
14													
13													
12													
11					0								
10													
9													
8													
7					0								
6													
5													
4													
3					0								
2													
1													
0													



1. FFAA and FF55 as Magic Numbers are used by HSLB and FTB – is it correct?

2. Who is the right person to decide about format of FTB Header and Trailer?

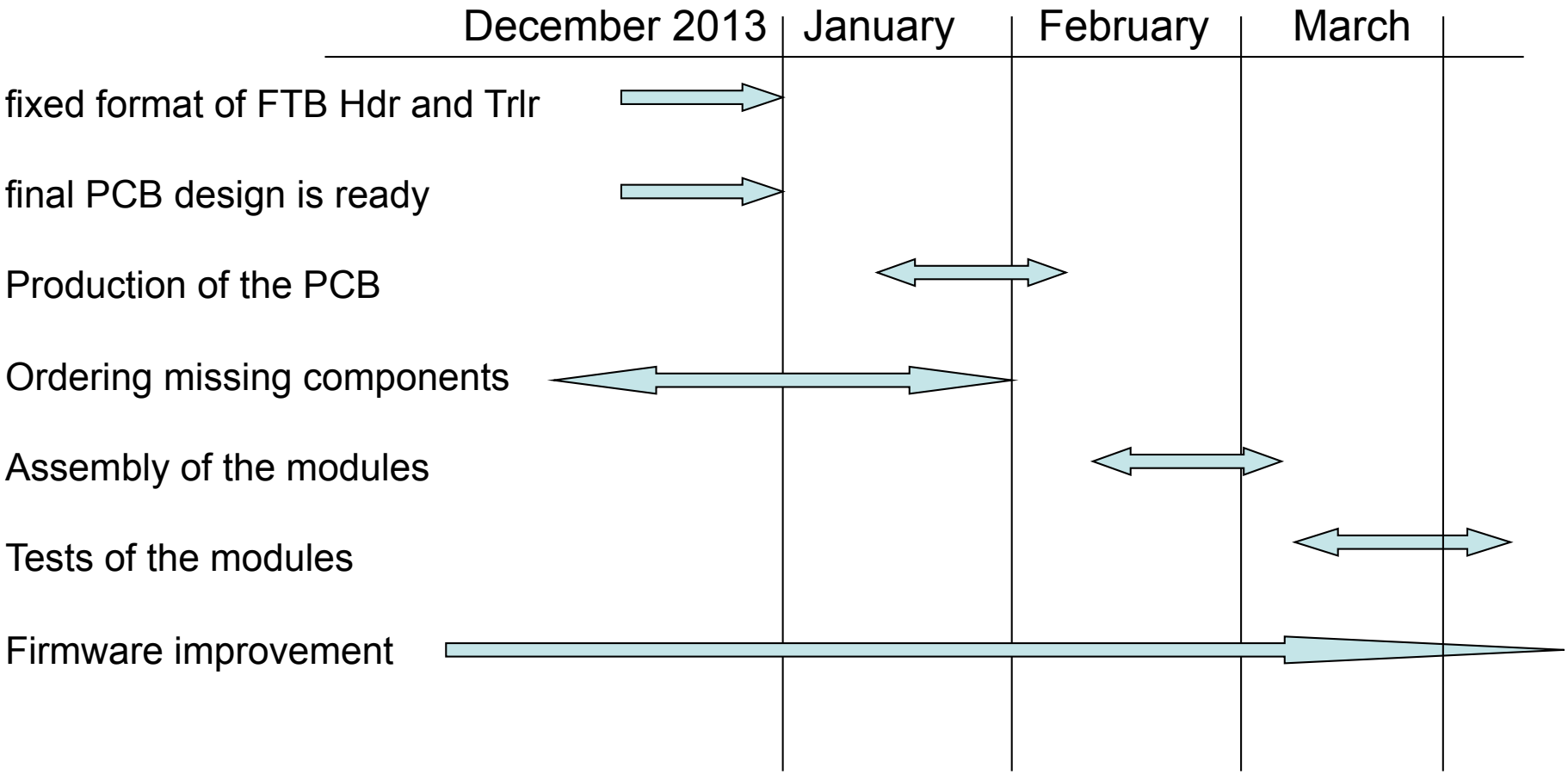
V. DESY Test

2. Equipment has to be taken to DESY

- Two FTB modules. There are:
two at KEK
one at CERN to middle of the December
one at HEPHY – partially tested during June migration test
one at Bonn – useless for DESY tests.
Suggestion to use two modules from KEK. They were tested.
Four Opto Drivers.
- Two for B2Link and two for DATCON (the same type?)
For B2Link should be taken from KEK.
For DATCON should be taken from Bonn
- Fiber optical patch cords LC/LC

IV. Schedule

Production of 55 modules of the FTB module ver2.



VII. Summary

1. Layout of the PCB are ready for mass production.
2. Decision about mass production will be taken after DESY test
3. Before DESY test decide the final format of header and trailer
4. All 55 modules should be ready to long term tests in May 2014

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main goals of FTB cont…