



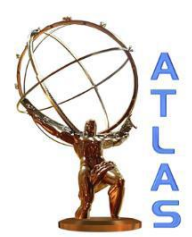
ITIM



Upgrading the ATLAS Tile Calorimeter electronics

**Gabriel Popeneciu, *on behalf of the
ATLAS Tile Calorimeter System***

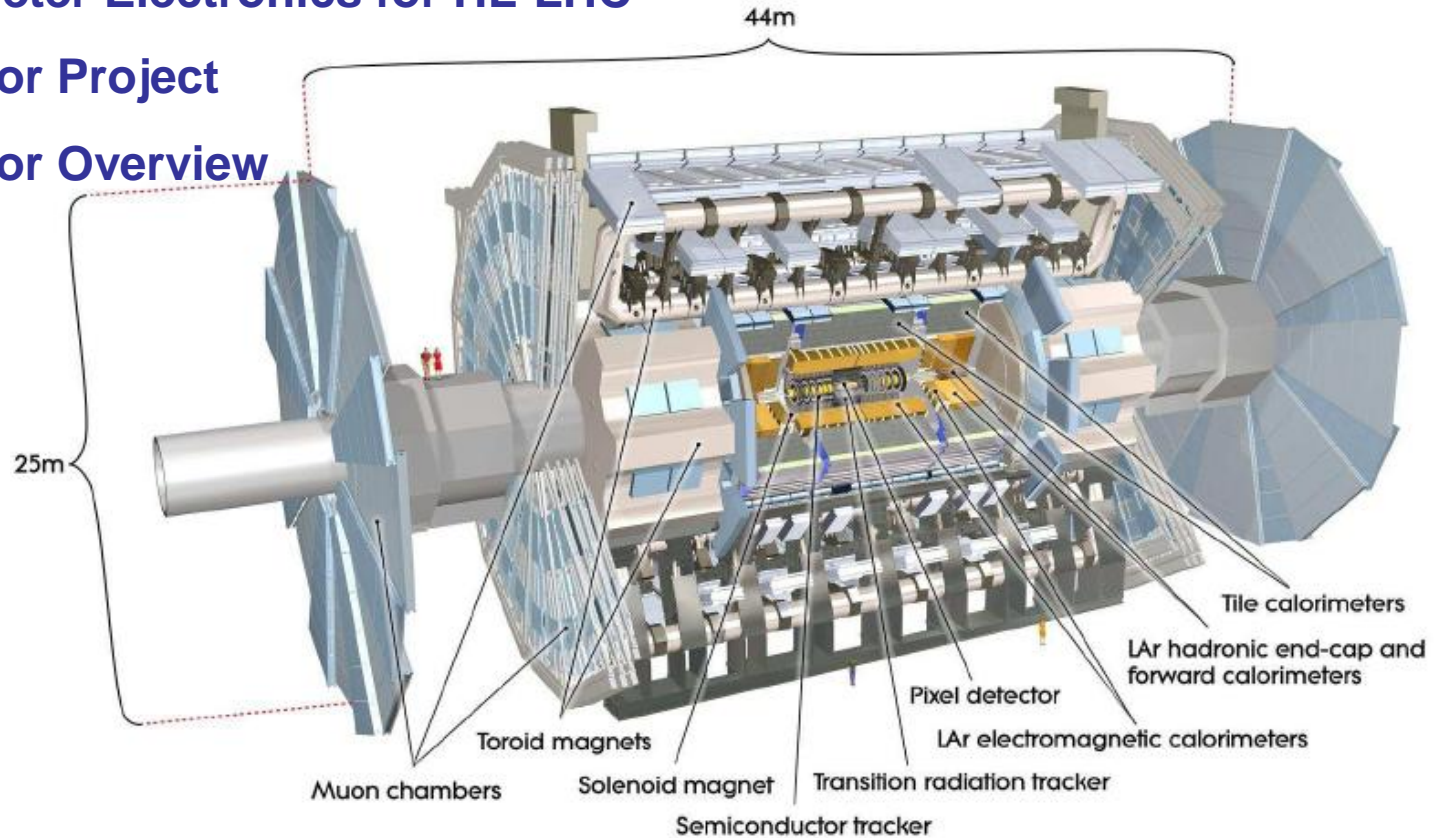
INCDTIM Cluj Napoca, Romania



Outline



- ❑ Tile Calorimeter Detector
- ❑ Tile Calorimeter Upgrade program
- ❑ Tile Calorimeter Electronics for HL-LHC
- ❑ Demonstrator Project
- ❑ Demonstrator Overview
- ❑ Summary

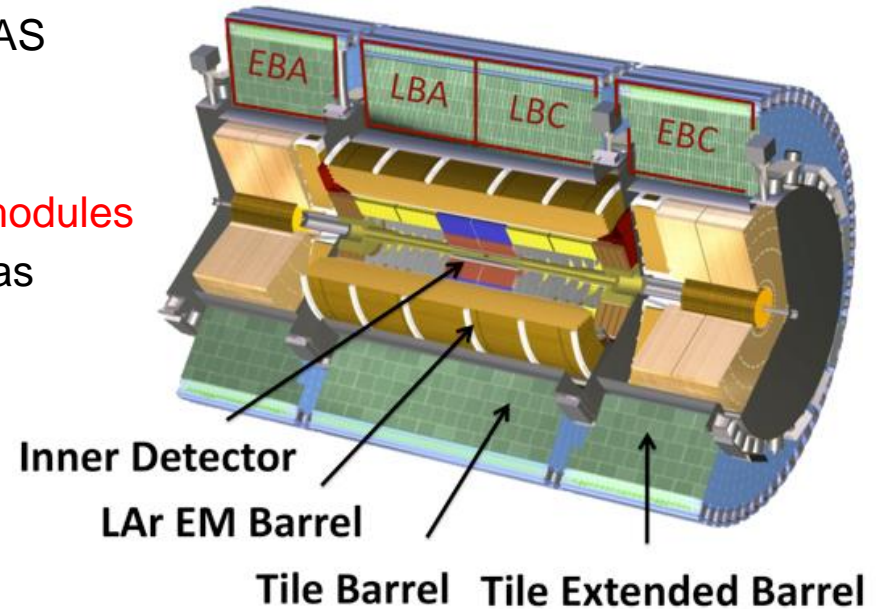
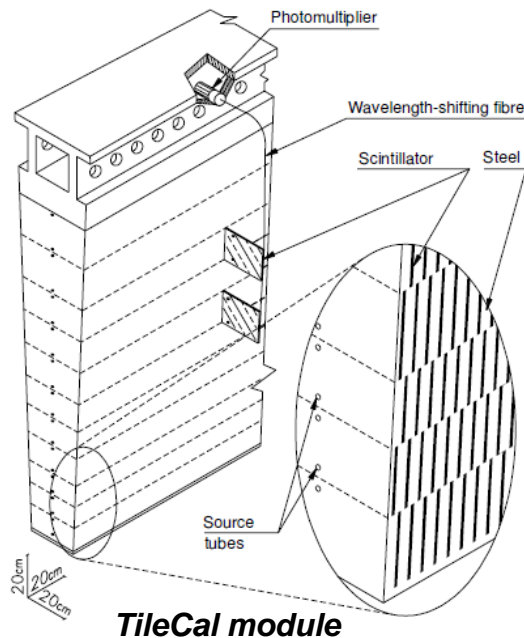


Tile Calorimeter



Tile Calorimeter (TileCal) is a scintillating hadronic calorimeter

- positioned in the most central region of ATLAS
- mechanically divided in 3 hollow cylinders
- 4 partitions: EBA, LBA, LBC, EBC
- each partition has 64 modules; in total **256 modules**
- sampling calorimeter, based on steel plates as absorber and plastic scintillating tiles



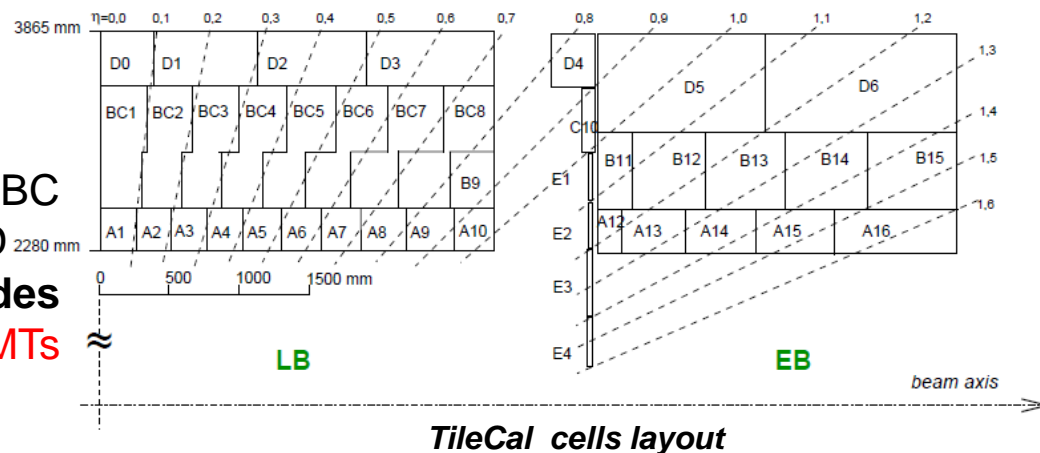
PhotoMultiplier Tubes (PMTs) and **Front-end (FE) electronics** are located in the outermost region of the module and situated in extractable „**super-drawers**”



Tile Calorimeter

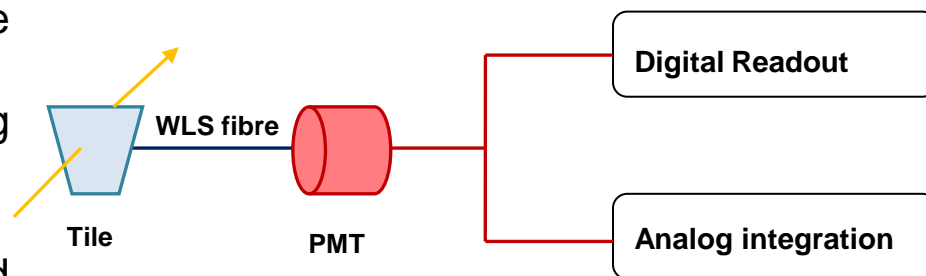


- **Each module is divided into cells**
 - in total 5,182 cells
 - three radial layers
 - cell granularity $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ for A, BC
0.2 \times 0.1 for D
- **Each cell is readout from two sides by 2 different PMTs**; in total **9852 PMTs**
- **More than 10,000 readout channels**



Readout scheme

1. Scintillation light produced by a charge particle in plastic scintillating tile
2. Light is collected by wavelength shifting fiber (WLS)
3. Electric pulse is produced by PMT
4. Signal is integrated, sampled and stored in the FE electronics
5. Stored data is transferred to back-end (BE) electronics (selected events after Level-1 trigger System acceptance)



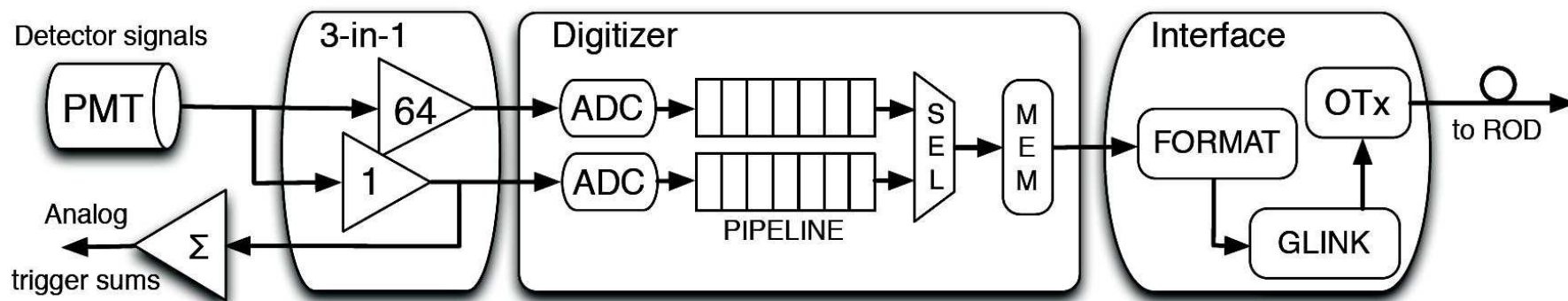


Tile Calorimeter

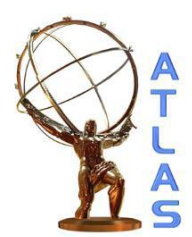


Data readout

- Signal pulse is shaped and amplified with two gains (1: 64)
- Both gains are digitized at 40 MHz by 10 bit sampling Analog to Digital Converters (ADCs)
- Digitised samples are stored in pipeline up to level-1 trigger latency
- Upon the first level trigger decision: readout of 7 samples of best gain
 - Analog summation for trigger
- Samples are merged and formatted into packages in the Interface Boards and sent to BE electronics in the counting room
- Signal from 7 samples is reconstructed using an optimal filtering algorithm



Tile Cal front-end electronics data flow



TileCal Upgrade plans



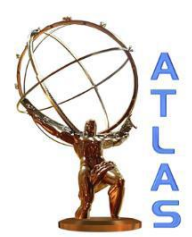
➤ **Advanced physics goals and LHC upgrade plans create new challenges for ATLAS detectors**

1. LHC upgrade program (High Luminosity **HL-LHC Phase-II**) aims to increase the peak luminosity by a factor of 5 compared to the design value ($10^{34} \text{ cm}^{-2}\text{s}^{-1}$) around 2024 → **higher levels of radiation** → can lead to **single point failures** or **permanent failures of electronics** → required better radiation tolerance

2. **Higher event rates** → required **more efficient trigger algorithms**

➤ **Upgrade concept: a multi-phase program (Phase-0, Phase-I, Phase-II)**

1. TileCal mechanics and optics together with their PMTs will be kept
2. Ageing electronics → existing designed for 10 years of operation
3. TileCal Readout electronics require major replacement for the Phase-II
 - **complete redesign for front-end and back-end electronics**



Tile Calorimeter Electronics for HL-LHC



Tile Cal Electronics requirements for HL-LHC

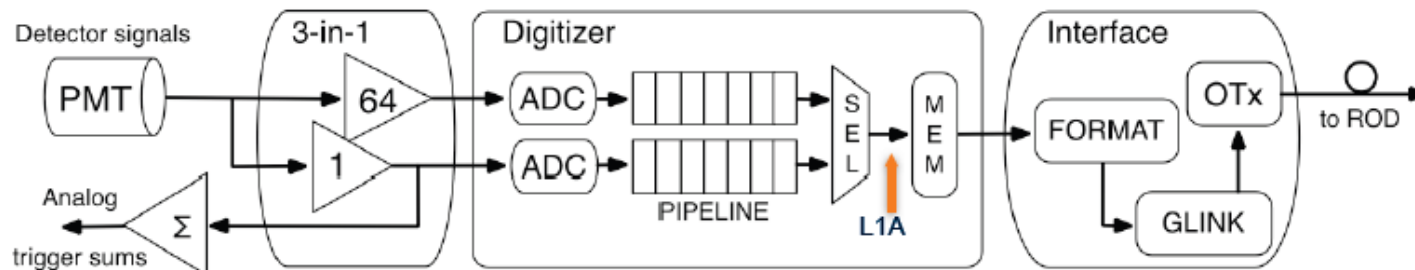
- **More events accepted** → **new full-digital trigger system**; raise the bandwidth up to 80 Tb/s (current 165 Gb/s)
 - Make all information available to the trigger and with minimum latency
- **Transfer all data to counting room** → **higher data rates between FE and BE**
- **Higher reliability** →
 - full redundant readout from cells to BE electronics
 - increase modularity in the FE electronics
 - redundant Power distribution
- **Higher robustness to reduce single point failures** → **higher radiation tolerance of electronics** (using Commercial Off-The-Shelf COTS components)
- **Better conditions for servicing due to future high radiation environment** → **implementation of the “mini-drawers” concept**

Tile Calorimeter Electronics for HL-LHC

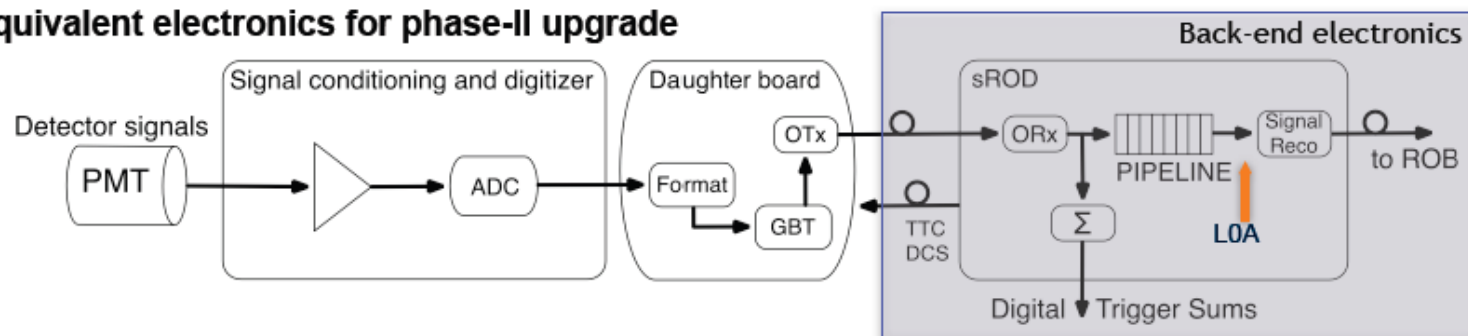
Tile Cal Electronics new concept

- ❑ **Full digital readout** - FE electronics transmit **digital data from all the channels** to BE electronics **for every bunch crossing**, with minimum latency
 - Completely new FE and BE electronics
 - New high speed links – high speed fiberoptic cables(40 Gb/s)
 - digitization of data at 40 MHz and transmission to BE electronics with 40Gb/s
 - digital trigger using sampled signal

Present front-end electronics



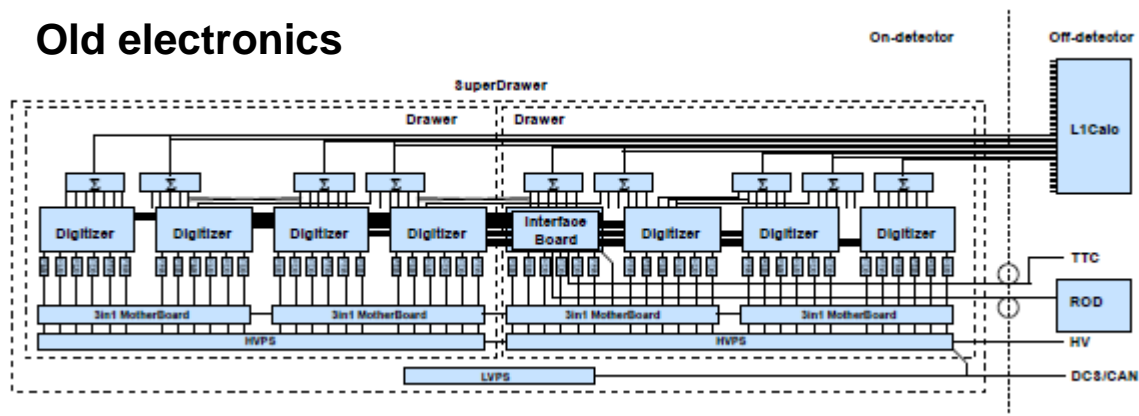
Equivalent electronics for phase-II upgrade



Tile Calorimeter Electronics for HL-LHC

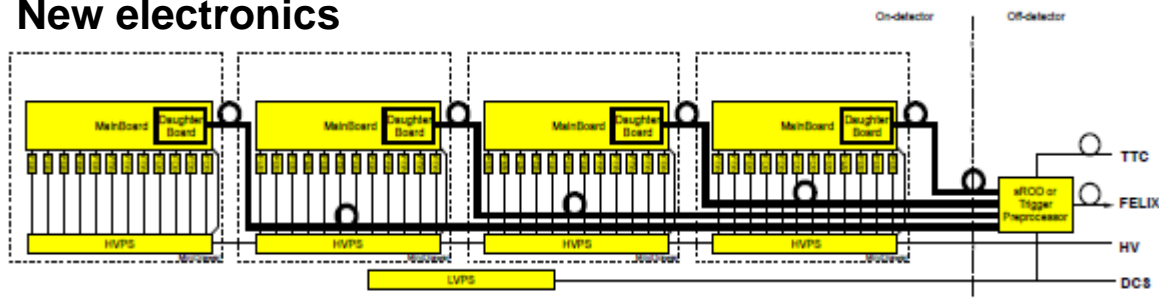


Old electronics



Total data rate	165 Gb/s
Number of links	256
Data rate per link	640 Mb/s
Links per SD	1
Data rate per SD	640 Mb/s

New electronics



Total data rate	80 Tb/s
Number of links	4096
Data rate per link	10 Gb/s
Links per SD	4X4
Data rate per SD	160 Gb/s

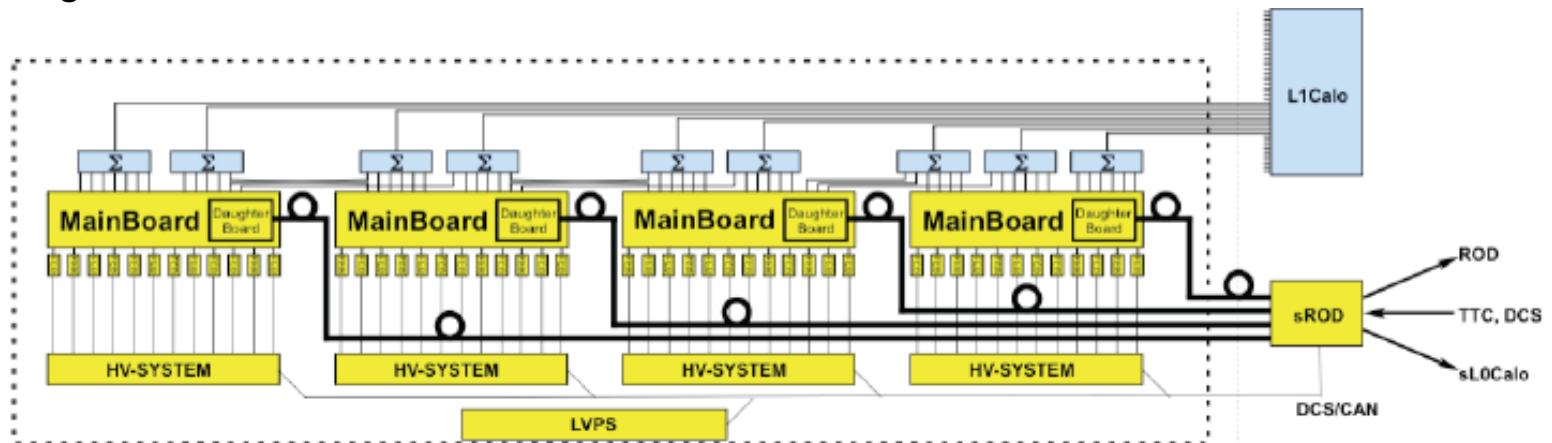
- Reduce the complexity and connections inside the FE electronics
- Moving from dependent drawers to independent mini-drawers (readout and power)
- Use a complete redundant readout from cell to BE electronics
- Redundant Power supply system introducing Point-of-Load regulators

Tile Calorimeter Demonstrator Project



Hybrid Demonstrator super-drawer

- The new Readout architecture needs tests for evaluation and qualification of the new technology before the replacement of FE and BE electronics for Phase-II upgrade
- Aimed to test new electronics under sharp conditions
- Upgraded electronics intended to be deployed as a **demonstrator prototype** inside TileCal during first shutdown in Run 2



- **Demonstrator** must be compatible with existing electronics

Hybrid Demonstrator: still using analog trigger readout

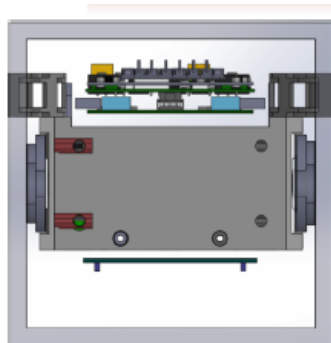
sROD system will interpret the Trigger Timing Control (TTC) and Detector Control System (DCS) commands and translate new detector data into a form acceptable for present ROD

Demonstrator Overview

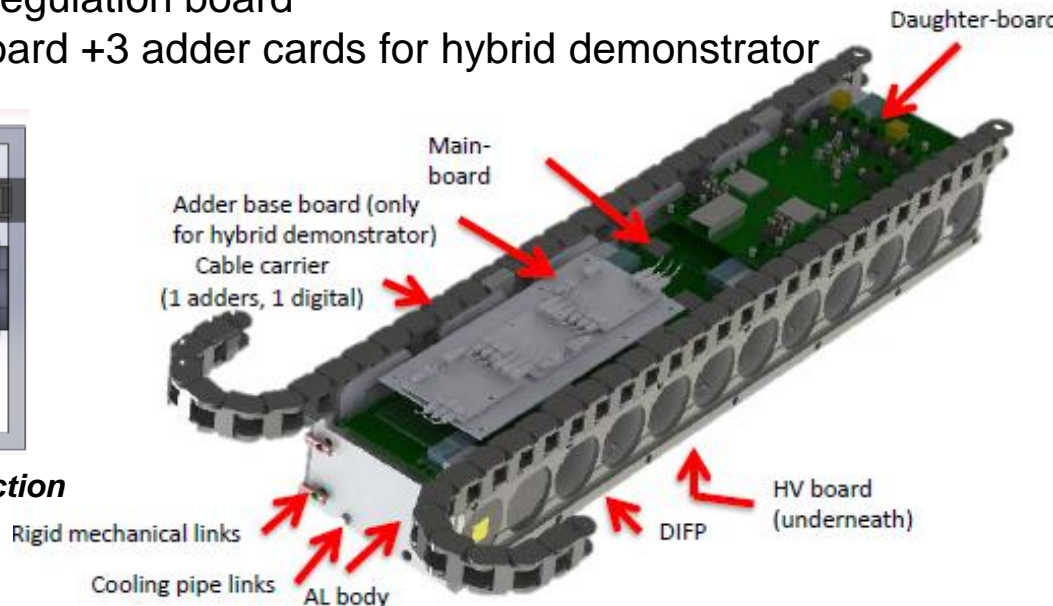


Mini-drawers

- Super-drawer demonstrator: composed of **4 mini-drawers** (MD) (half-size existing drawer), each one equipped with:
 - 12 Front-End Boards (FEB) with 3 alternative versions:
 - *Modified 3-in-1 card (modification of existing FEB)*
 - *QIE Charge integrator and encoder (4 gains, 6-bit ADCs)*
 - *FATALIC front-end ASIC (3 gains, TACTIC 12-bit ADCs)*
 - 1 Main Board: adapted to the 3-in-1 FEB
 - 1 Daughter Board: FPGA radiation tolerance
 - 1 High Voltage regulation board
 - 1 Adder base board +3 adder cards for hybrid demonstrator



Mini-drawer cross section

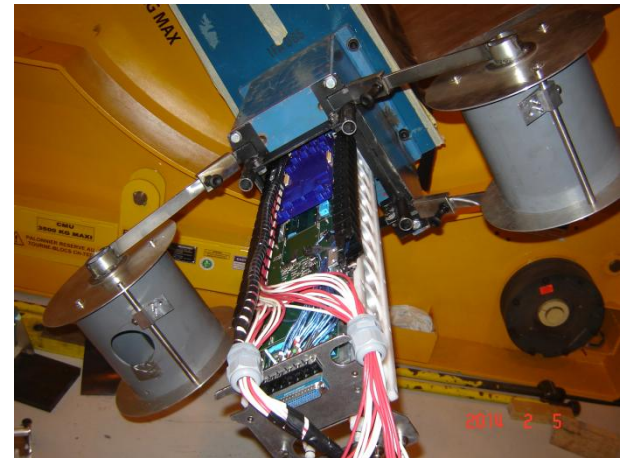
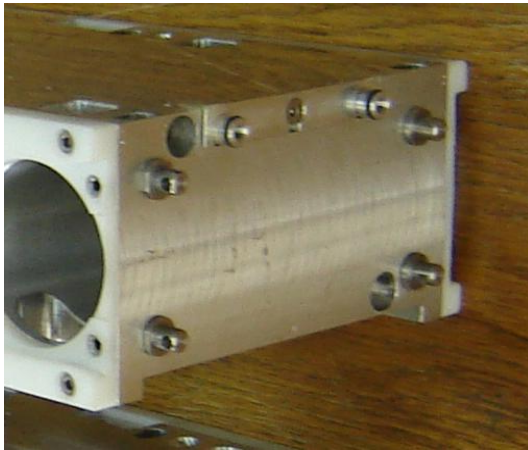
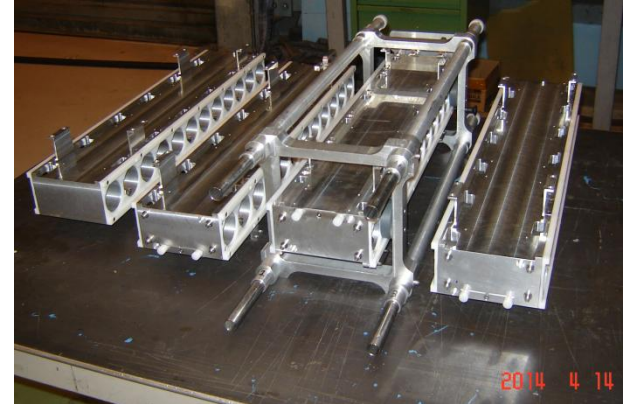


Demonstrator Overview



Mini-drawers mechanics

- Easier access - required smaller detector opening (1 m)
- Easier to handle
- Easier to replace – reducing radiation exposure of the maintenance personnel
- Improved mechanical links between mini-drawers
- More efficient internal cooling
- Internal flexible cable trays for electrical services





Demonstrator Overview



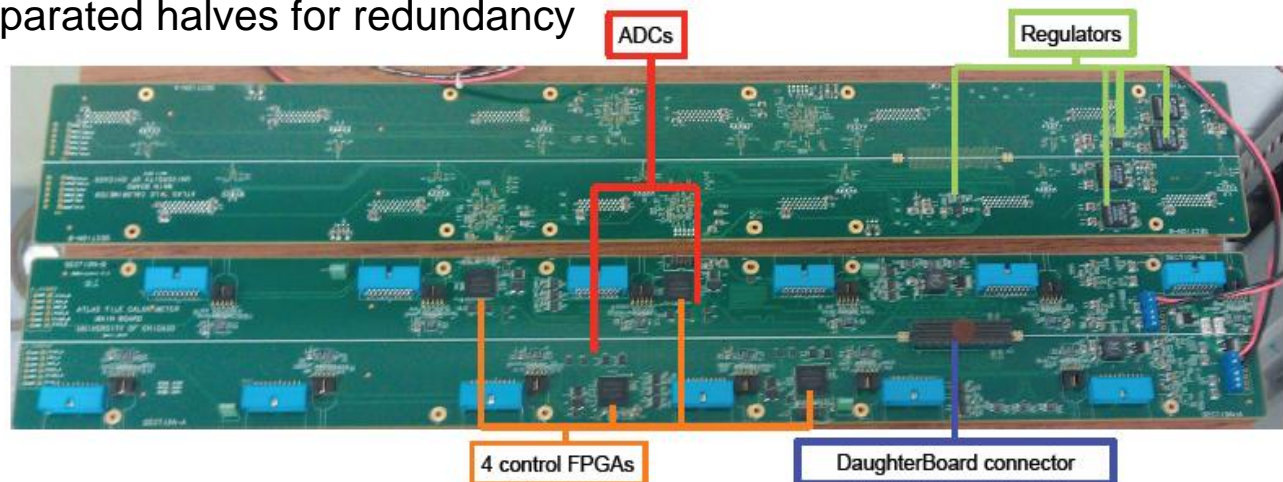
Front-End Board: new 3-in-1 cards

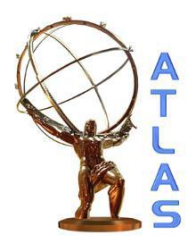
- **Reception and shaping of PMT signals**
 - provides analogue output in 2 gains (1:32)
 - charge injection calibration
 - integrator for physics calibration
- Design based on current 3-in-1 cards
 - COTS components
- Better linearity and lower noise than previous version
- Higher radiation tolerance



Main Board for new 3-in-1 cards

- **Digitizes signals from 12 new FEBs with new 12 bits ADCs via safe 5 Gb/s down link**
 - each cell will be readout by two PMTs, one on each side of MB
 - samples are transferred serially to the Daughter Board at 600 MHz
 - commands are sent in parallel to 2 control FPGAs on each side
 - MB is split into 2 separated halves for redundancy



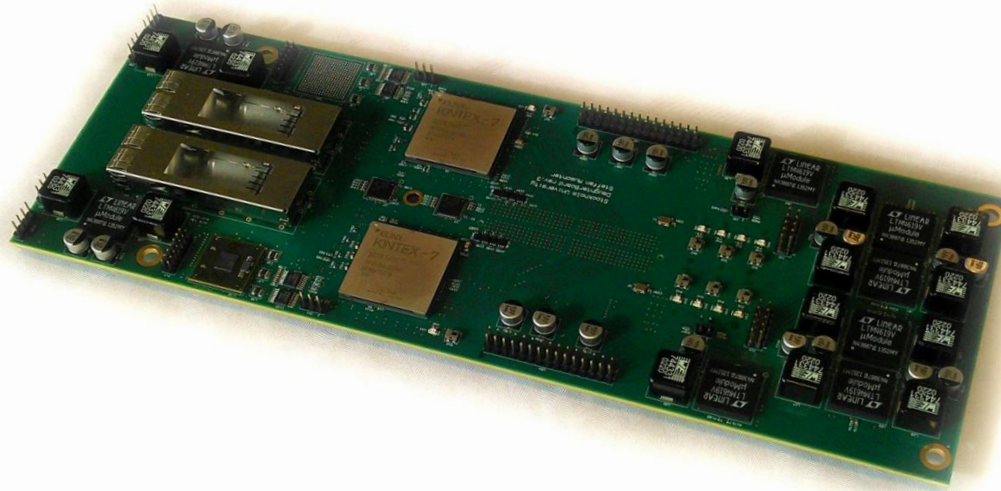


Demonstrator Overview



Daughter Board

- **Provides the high speed communication between front-end and back-end electronics**
 - DB collects, formats and transmits the data using high speed links (10Gb/s data rate)
 - DB implements slow control functionalities – distribution of Detector Control System (DCS) commands needed for the control and monitoring of the MB and HV power supplies
 - DB is split into 2 separated halves for redundancy, each includes 1 Kintex 7 FPGA and 1 QSFP modulator at 40Gb/s, 1 GBTx chip
- **Can be remotely configured from BE electronics via safe path using tolerant GBTx** and will in turn be able to configure Main Board FPGAs



Demonstrator Overview

Low Voltage power distribution

▪ Based on a three stage power distribution system

Stage 1: bulk 200VDC PS in counting room (USA15)

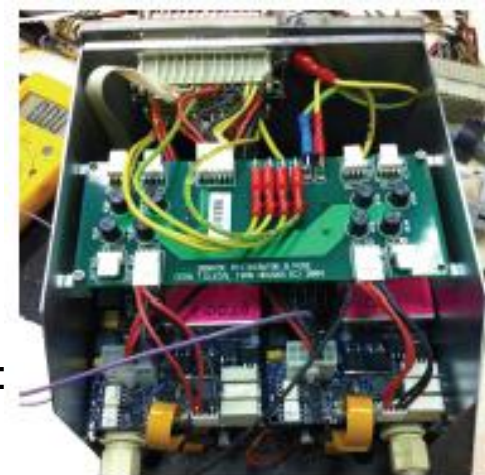
- provide power to 4 super-drawers

Stage 2: LVPS boxes - new design , serving 4 mini-drawers

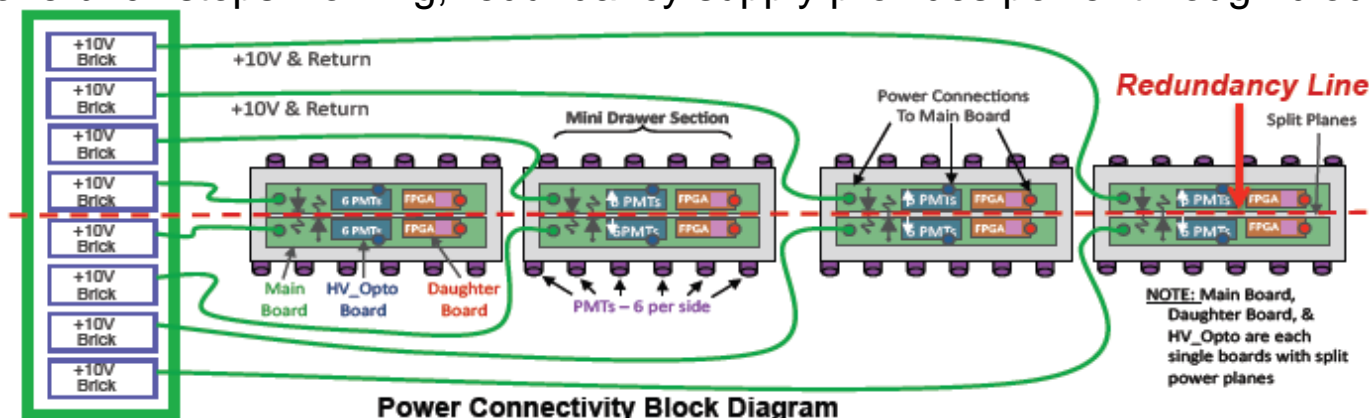
- providing only +10V in 8 separate bricks
- each brick serving half a mini-drawer
- require a factor 2 in the current output for redundancy:
(diode bridge between MB halves for redundancy)

Stage 3: Point-of-Load regulators

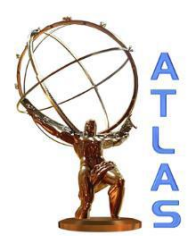
- locally produce the required voltages
- Point to point connection from brick to Main Boards
- If one brick stops working, redundancy supply provides power through diode on the MB



LVPS with two V8.0.1 bricks



Power Connectivity Block Diagram

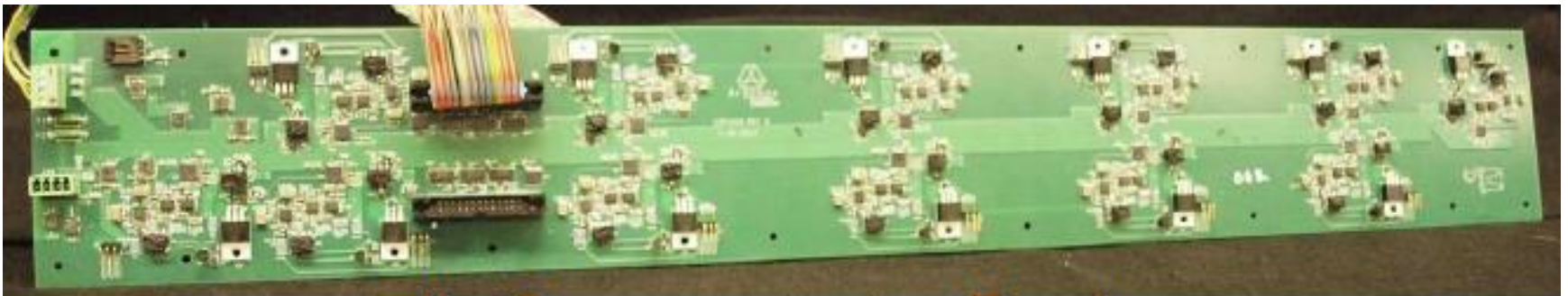


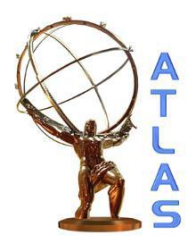
Demonstrator Overview



High Voltage power distribution

- **Two solutions are under evaluation, voltage regulation in USA 15 versus front-end (HV_Opto Board)**
- **For Demonstrator is implemented second version**
 - similar to previous HV PS but with individual PMTs on/off control
 - for a better PMTs stability passive dividers have been replaced by active dividers (better linearity)



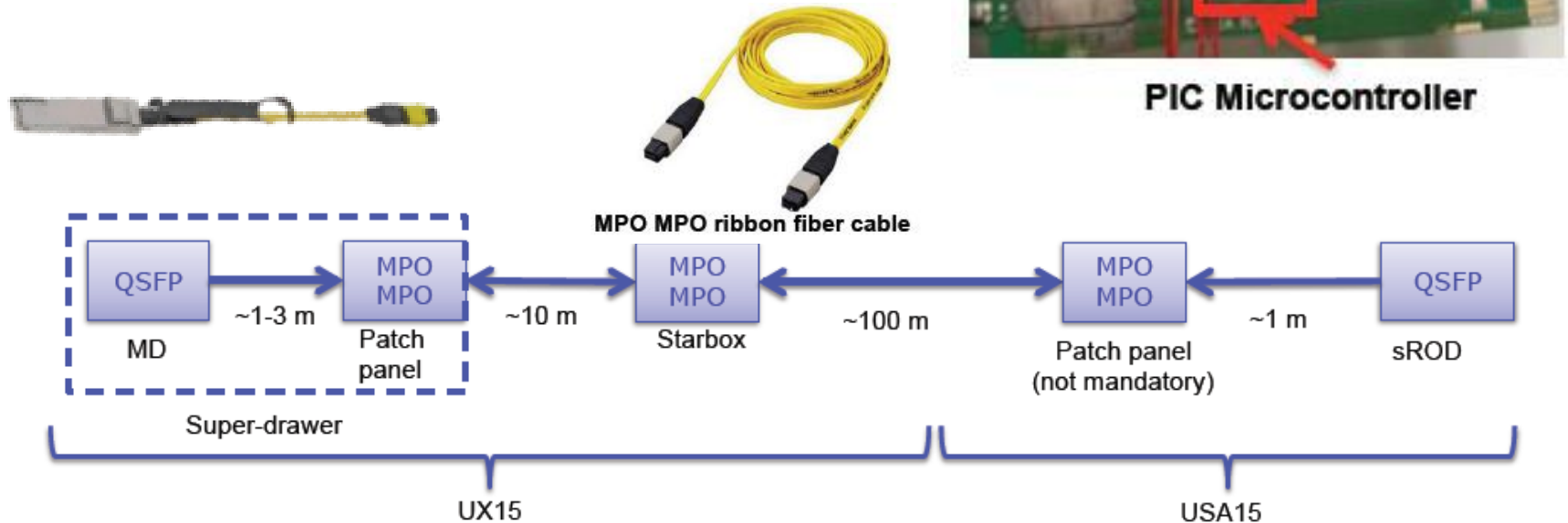


Demonstrator Overview



Readout links

- **Demonstrator require 8 readout links**
 - each DB equipped with 2 links:1+1 (redundancy)
 - cross section per ribbon $4 \times 2.5 \text{ mm}^2 = 10 \text{ mm}^2$
- **Using QSFP Active Optical Cable (Modulators)**
 - operate above 40 Gb/s with Bit Error Rate $< 10^{-18}$
- **Good results from radiation tests**
 - no Single Event Upset (SEU) at $8 \times 10^{11} \text{ p/cm}^2$



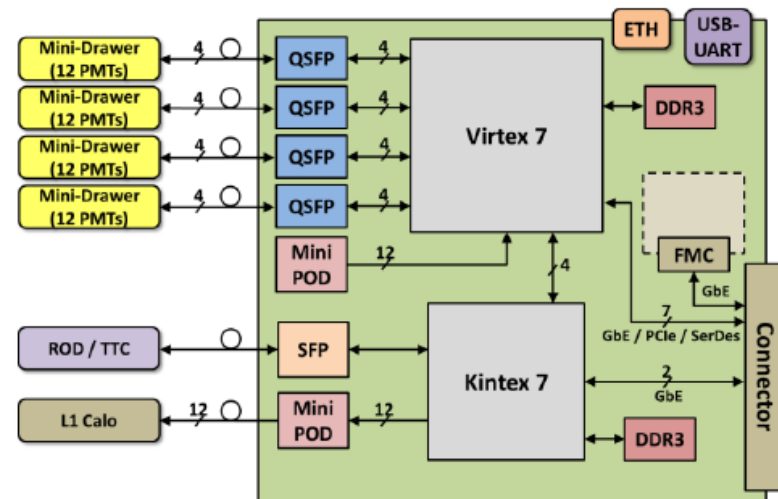


Demonstrator Overview



Super Read Out Driver

- **sROD is interface with FE electronics and L0/L1 Trigger system for Phase-II**
 - Processing Readout data
 - Interfacing Detector Control System (DCS) and FE electronics
 - Distributing Timing Trigger and Control (TTC) information towards detector
- **Readout of a complete new super-drawer (4 MD)**
- **Features:**
 - 4 QSFP, 1 MiniPOD RX, 1 MiniPOD TX
 - 1 Xilinx Virtex 7 FPGA with 48GTX@10Gb/s Interface with front-end electronics
 - 1 Xilinx Kintex 7 FPGA with 28GTX@10Gb/s; Interface with L0/L1 trigger system and keep compatibility with present system
 - 512 MB DDR3 SDRAM and 1Gb flash per FPGA



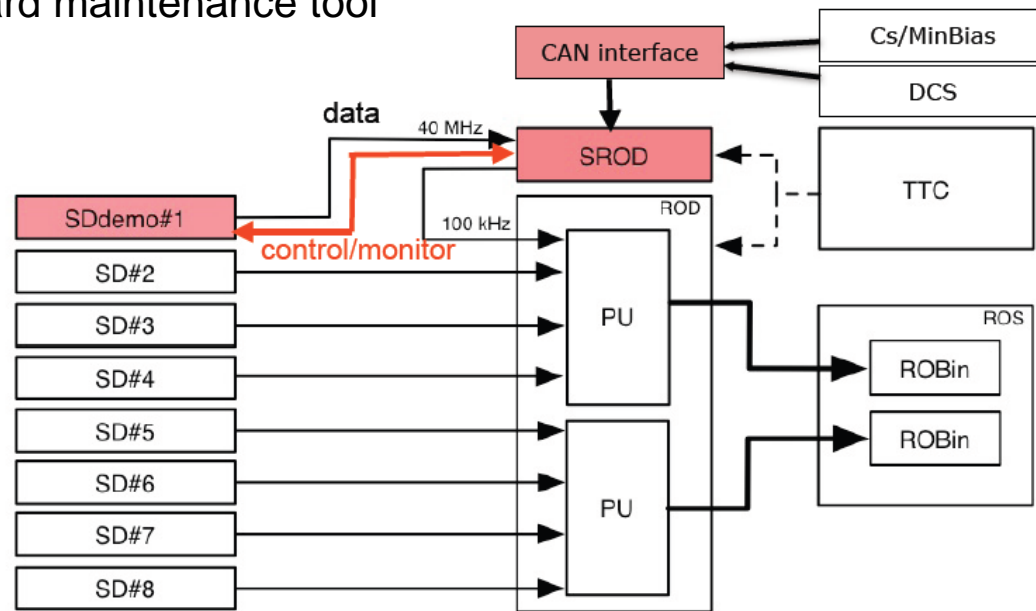
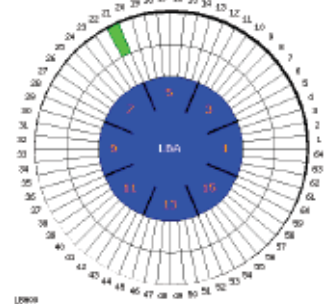
Conceptual design of the sROD



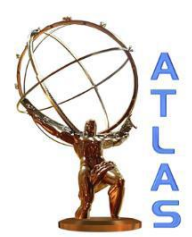
sROD prototype

Integration of the Demonstrator prototype

- **Very ambitious goal:** to build and install a hybrid demonstrator prototype at the next ATLAS opening in Run 2, followed by the certification of the system
 - Demonstrator must be equipped with proper interfaces modules that implement the functionalities required by ATLAS
- Installation is foreseen on LBA position 21
 - Demonstrator should pass the test for standard drawer readiness for insertion using standard maintenance tool



Scheme of the Demonstrator prototype integration



Summary



- ❑ R&D projects for Tile Calorimeter electronics upgrade for HL-LHC are well progressing
 - New readout architecture
 - Complete redesign of the FE and BE electronics for Phase-II Upgrade
- ❑ Tile Calorimeter Demonstrator project
 - In order to test the technology a hybrid demonstrator, compatible at the functional level with current design, was developed
 - Now we have four fully equipped mini-drawers
 - One super-drawer (4 mini-drawers) was completely assembled and first tests are starting
 - Procedures were developed for full validation of the design and for the installation in ATLAS
- ❑ The plan is to have a hybrid demonstrator ready to be installed at the next ATLAS opening in Run 2.

Intended schedule

