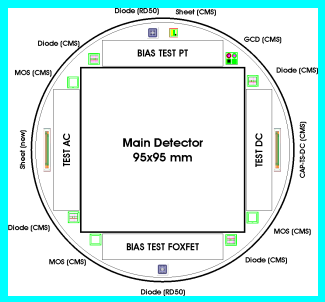
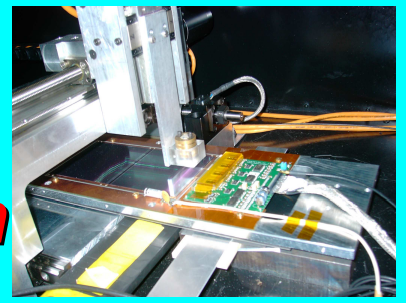
SiLC R&D: STATUS REPORT

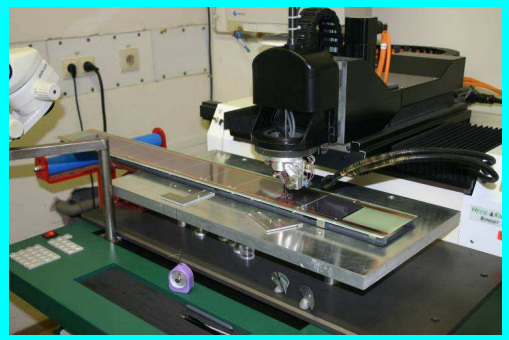


PRC-DESY, April 1st, 2008

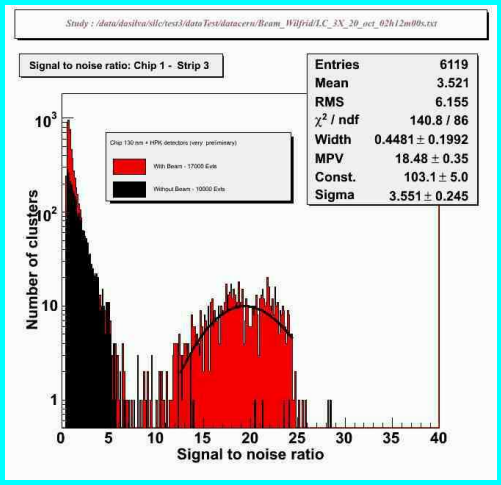
on behalf of SiLC Collaboration

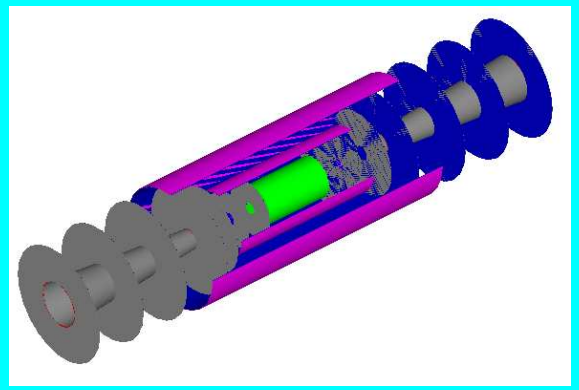
Aurore Savoy-Navarro, LPNHE/CNRS-IN2P3

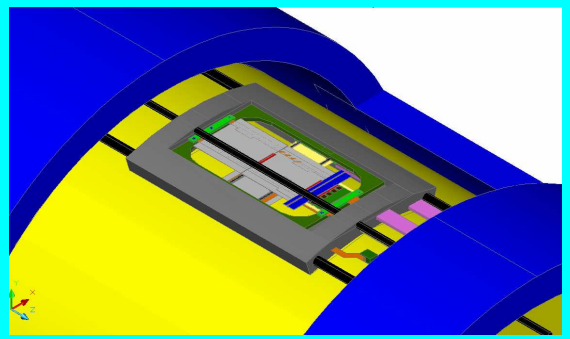


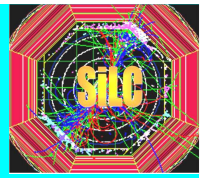


R&D sensors
R&D Electronics
Mechanics
Simulations
Tests
What's next





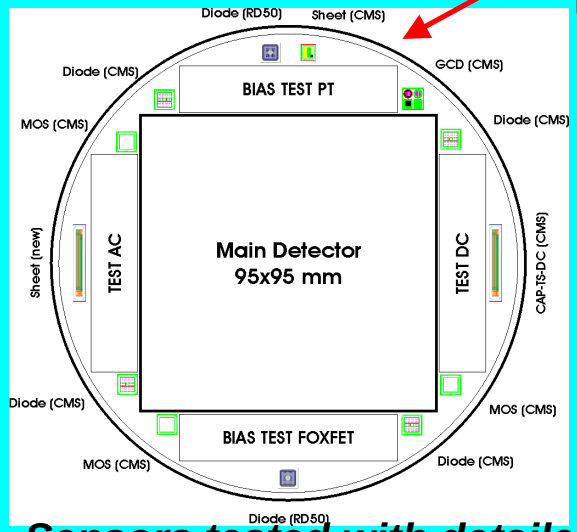


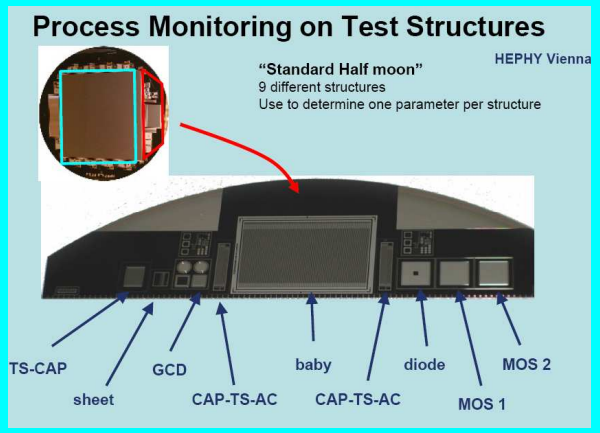


- R&D on sensors
  - R&D on baseline µstrip sensors, novel technologies,
  - Quality Test Control (QTC)
  - Development of collaboration with Industries
- R&D on electronics
- Mechanics developments
- Simulation
- Tests

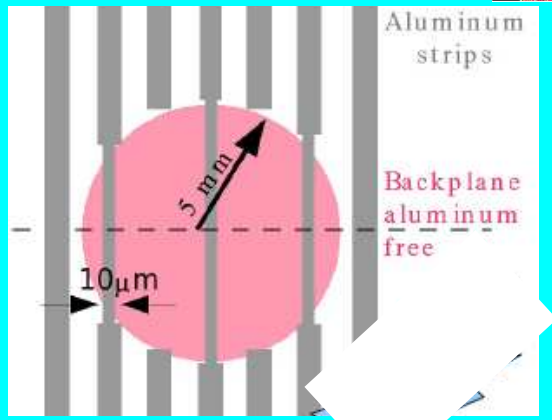
SENSORS R&D

NEW in 2007: HPK μstrips, **6'' wafer, but:** pitch=50μm; thickness: 320μm; Length: 9.15cm,





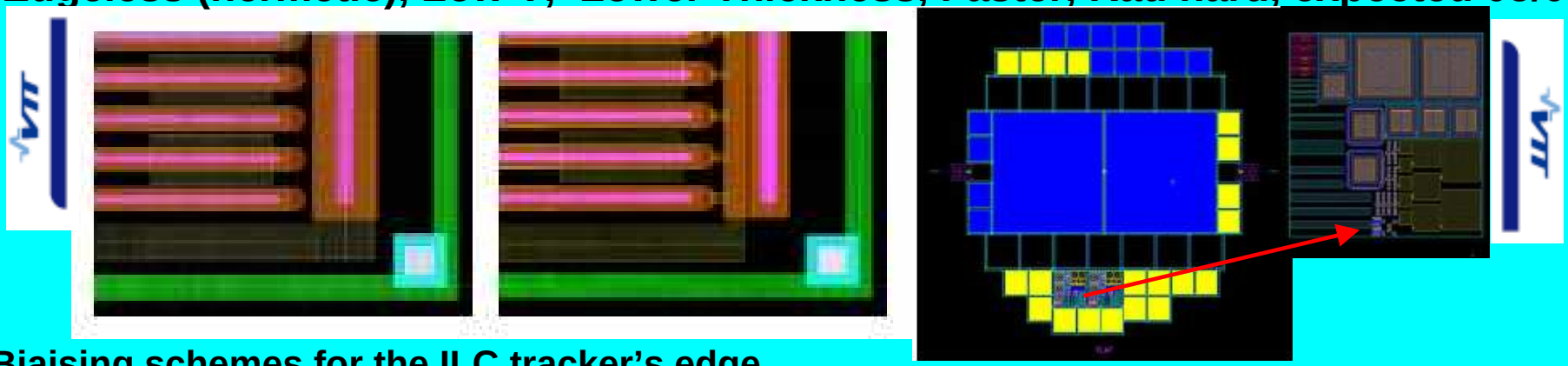
Test structures



5 sensors specially treated for laser alignment

Sensors tested with detailed QA control (HEPHY+IEKP)

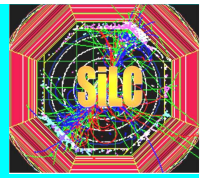
2007 (cont'd) **New technological approach: 3D Planar (6'') μstrips: Edgeless (hermetic), Low V, Lower Thickness, Faster, Rad hard, expected 05/08**



Biaising schemes for the ILC tracker's edge active strip detector (left) punch through, and (right) FOXFET . The detector is biaised from one corner of the active edge (green)

Test structures (not included this time)

And also pixels:



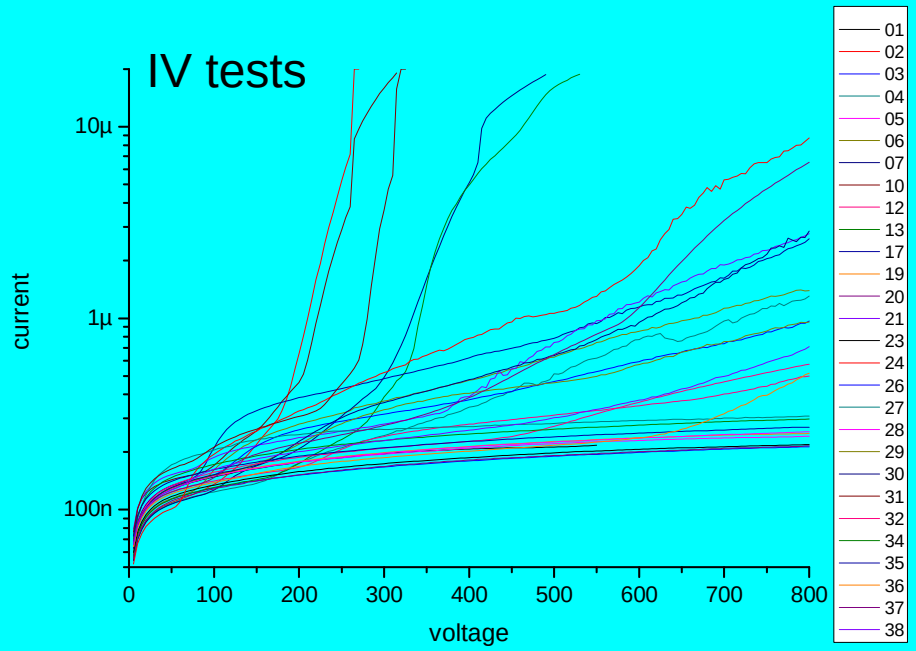
SiLC proposed since the beginning to use pixels in certain regions:

1) Pixels for the very forward zone nearby the vertex detector
2) Pixels in the overall internal region both central barrel and all very forward disk
   Not just an extension of the vertex region **but a new use of pixels (i.e. sensors f**
   large trackers (?))
3) Further on??? (i.e. an '' all-pixel tracker'')

The developments are currently done within the microvertex R&D collaborations.
The main emphasis is on DEPFET because of SiLC collaborators also in this R&D activity (IFIC-Valencia and CU Prague mostly)
There is a growing interest on the 3D pixel technology, starting with expertise at CNM-IMB/CSIC and VTT; other teams are now joining.

The possible use of pixels is being taken into account as an important issue in optimization studies. This R&D aspect is expected to evolve in these next years.

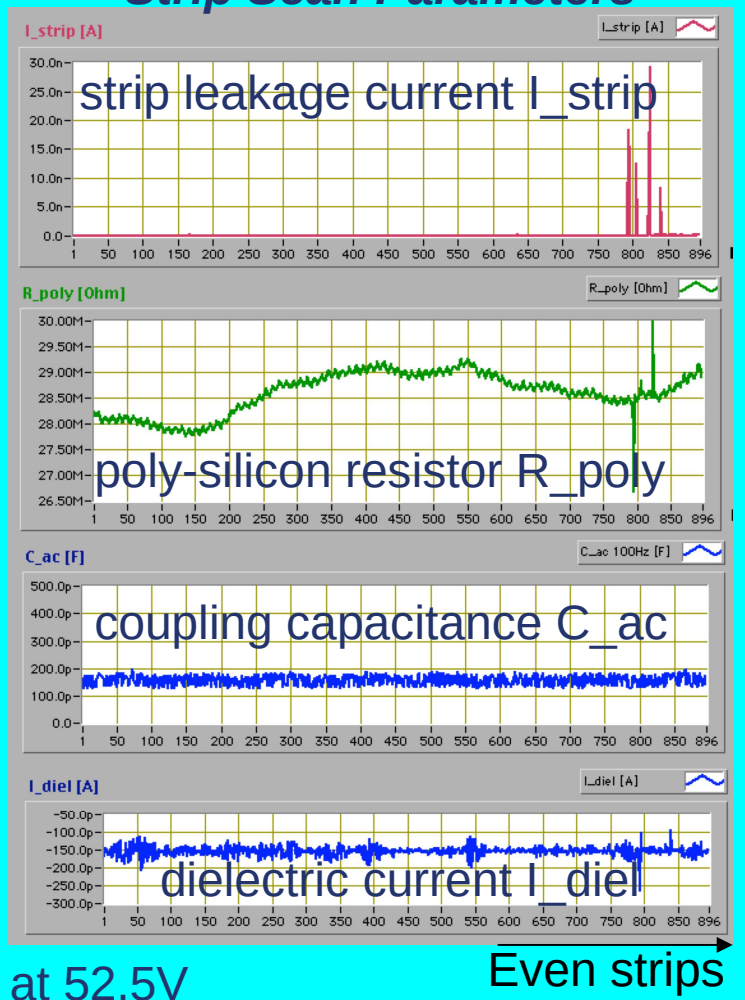
Quality control of sensors (IEKP & HEPHY)



IV tested up to 800V ; Breakthroughs:
3 sensors below 450V, 1 below 300V
No pb. since operating voltage<100V

CV tests: requested a resistivity such that depletion voltage is between 50 and 100V;
All sensors fully deplete between 47-58V, average at 52.5V

Strip Scan Parameters

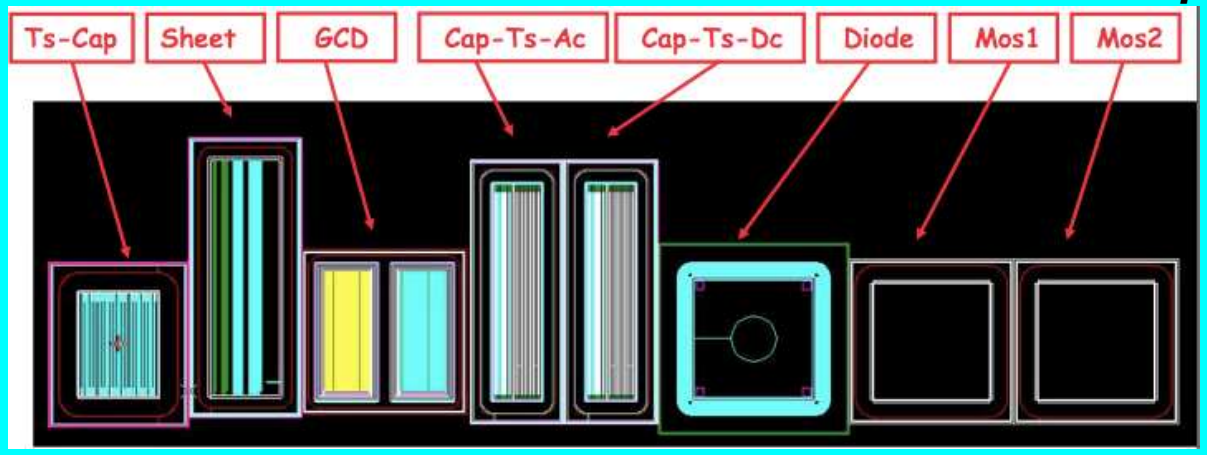


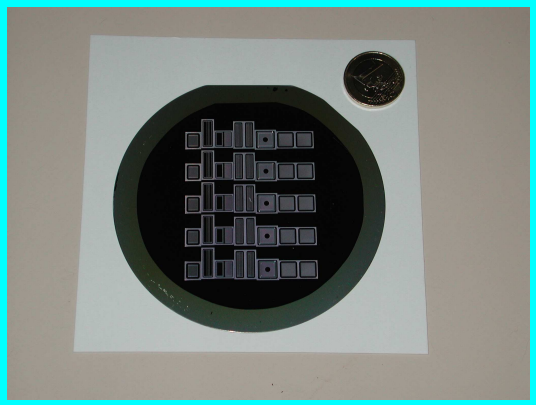
NEW HPK sensors look good.

Quality control of sensors (cont'd)

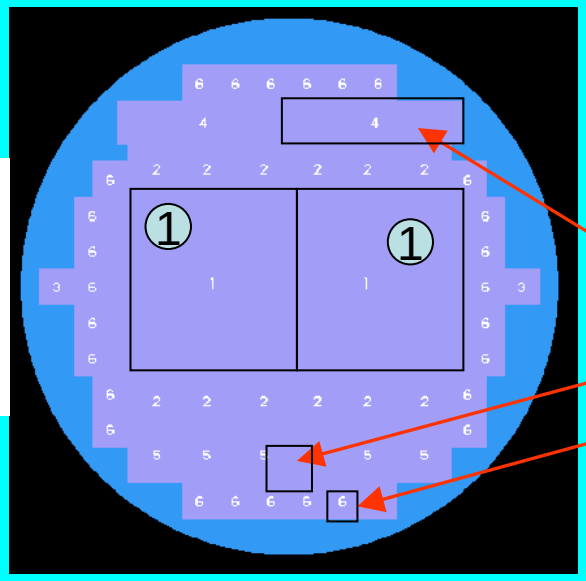
Test structures applied with further improvements wrt CMS to test new foundries or novel technologies or specific treatments (alignment sensors); As for example:

4'' wafers from IET Warsaw => new in the field of µstrips but looks promising





Next step: Design and production of test structures for dual metal layer

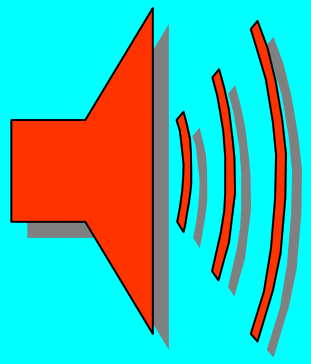


Test of novel technology: 3D planar µstrips from VTT

1. **MAIN DETECTOR, 5 X 5 SQCM**
2. *MEDIPIX2, 1.5 X 1.5 cm²*
3. ALIGNMENT MARKS, 1 X 1 *cm²*
4. **HALF MOON TEST STRUCTURE**
5. EDGELESS TEST STRUCTURES, 1.5 X 1.5 cm²
6. BABY DETECTORS, 1 X 1 cm²

And more to come ex: ON (CZ)…

Presently under test: test structures new HPK sensors

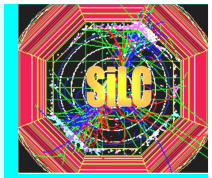


- R&D on sensors
- R&D on electronics:

HEAD ON THE NEW SiTR-130_96

- Mechanics developments
- Simulation
- Tests

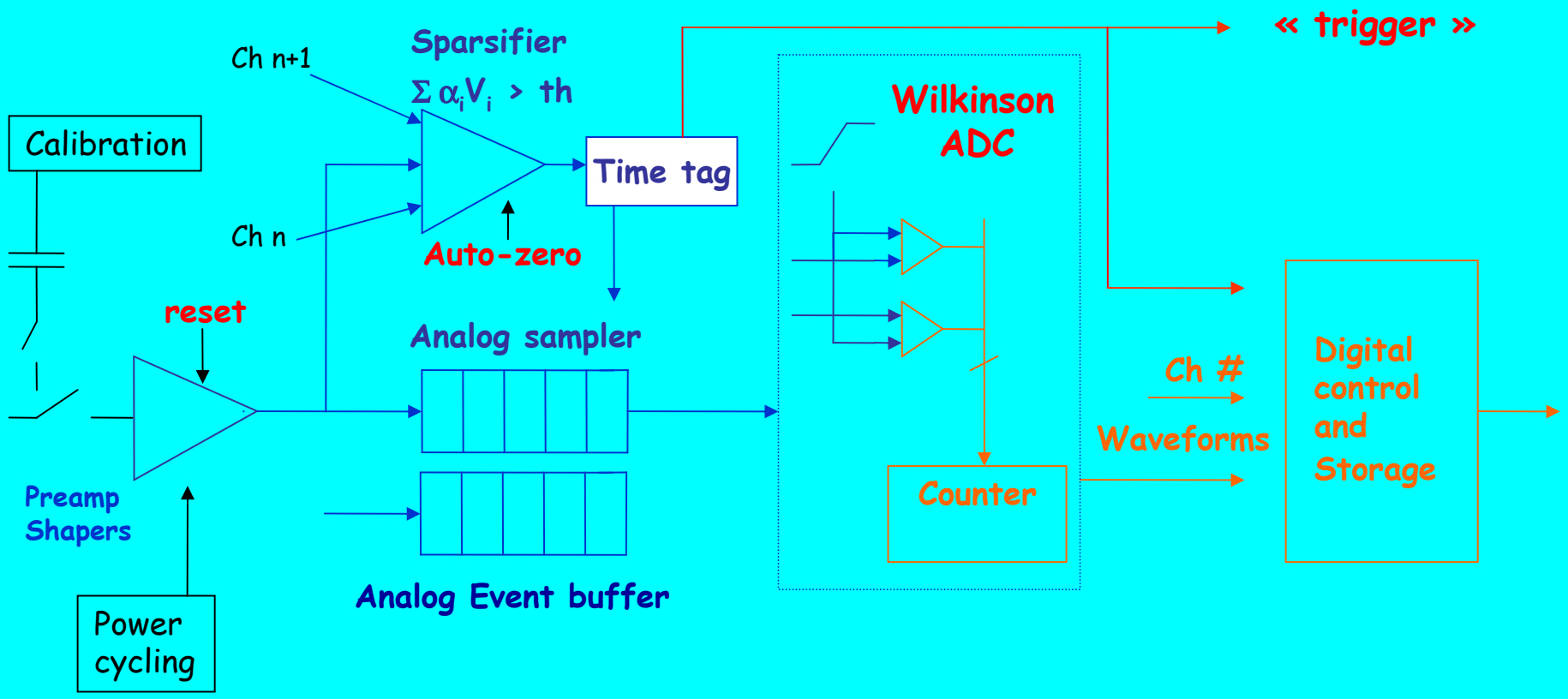
ELECTRONICS R&D:
FEE Functionalities to be integrated



- Full readout chain integration in a single chip, 512 or 1024 ch in 90nmCMOS
  - Preamp-shaper
  - Sparsification — Trigger decision on analog sums
  - Sampling — 8-deep sampling analog pipe-line
  - Analog event buffering: — Occupancy: 8-16 deep event buffer
  - On-chip digitization — 10-bit ADC
  - Buffering and pre-processing: Centroids, χ2 fits, lossless compression&error codes
  - Calibration and calibration management
  - Power switching (ILC duty cycle)

Amplifiers: - 30 mV/MIP over 30 MIP range
Shapers: - Two ranges: 500ns–1μs, 1μs-3μs
Sparsifier: - Threshold the sum of 3-5 adjacent channels
Samplers: - 8 samples at 80ns sampling clock period
- Event buffer 8 deep
Noise baseline: Measured with 180nm CMOS:
375 + 10.5 e-/pF @ 3 μs shaping, 210μW power dissipation
ADC: - 10 bits
Buffering, digital pre-processing
Calibration
Power switching can save a factor up to about 100

Front-end architecture



Charge 1-30 MIP, Time resolution: BC tagging 150-300ns
80ns analog pulse sampling

Technology: Deep Sub-Micron CMOS 130-90nm

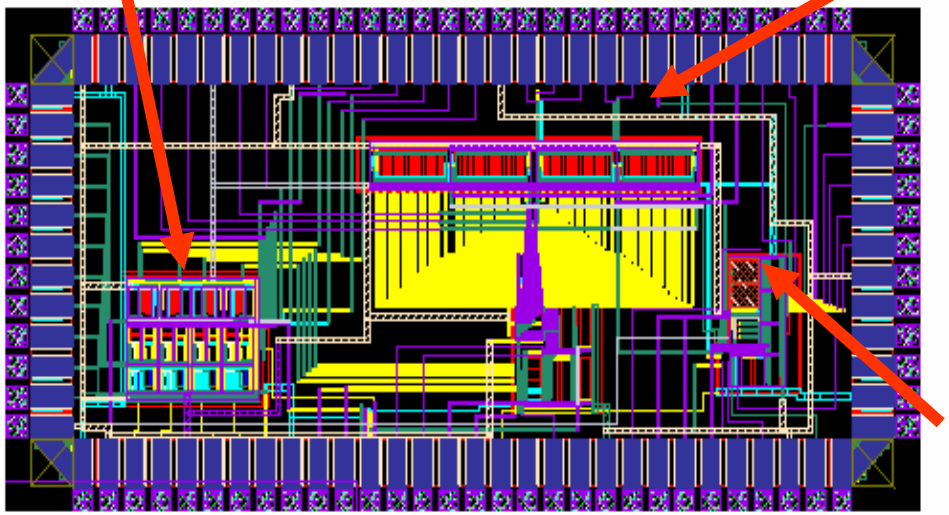
1 step: the 4-channel chip,SiTR-130_V1&2

(LPNHE-LAPP)

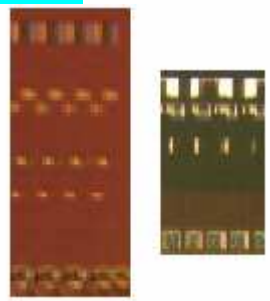
Amplifier, Shaper, Sparsifier 90*350 µm²

Analog sampler 250*100 µm²

layout



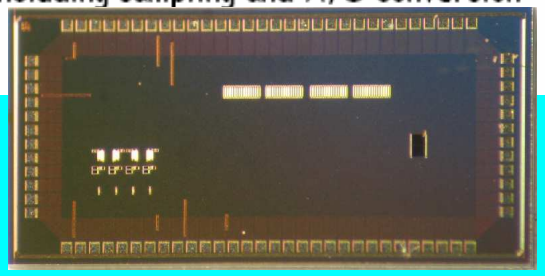
A/D 90*200 µm²



180nm 130nm

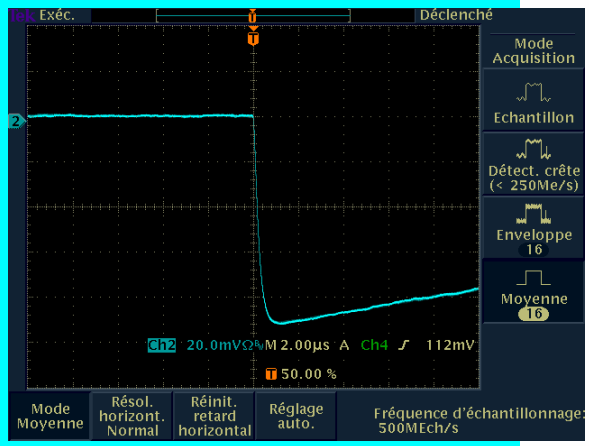
Layout of the 130nm chip including sampling and A/D conversion

Photo

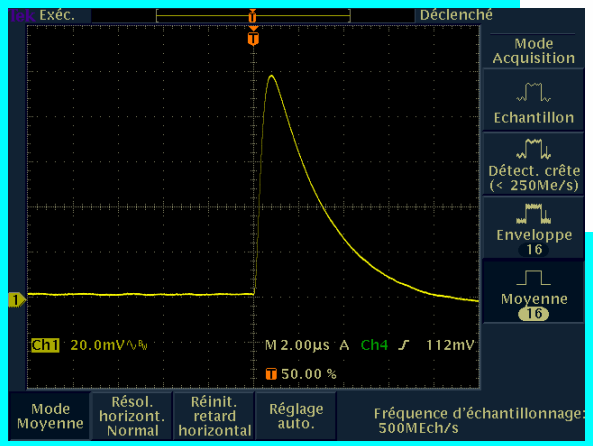


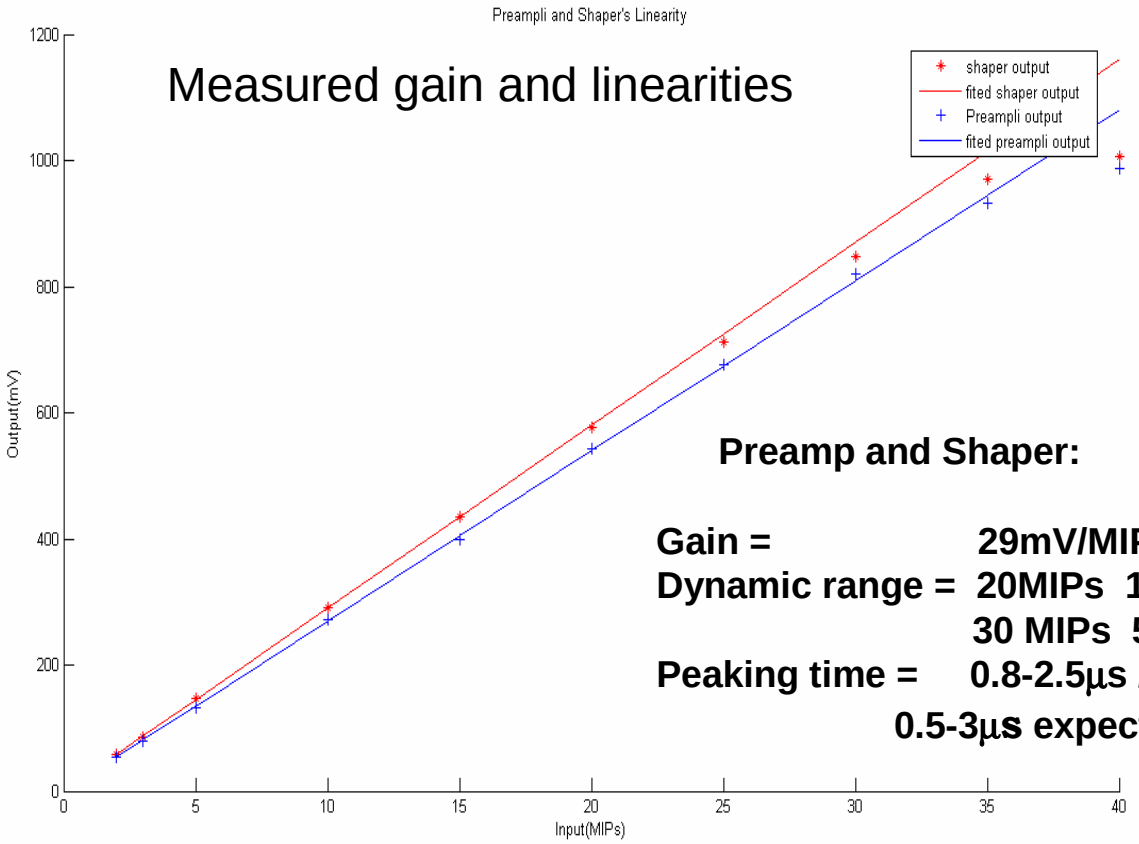
Preamplifier-shaper performances

Preamp output



Shaper output





Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs /
0.5-3µs expected

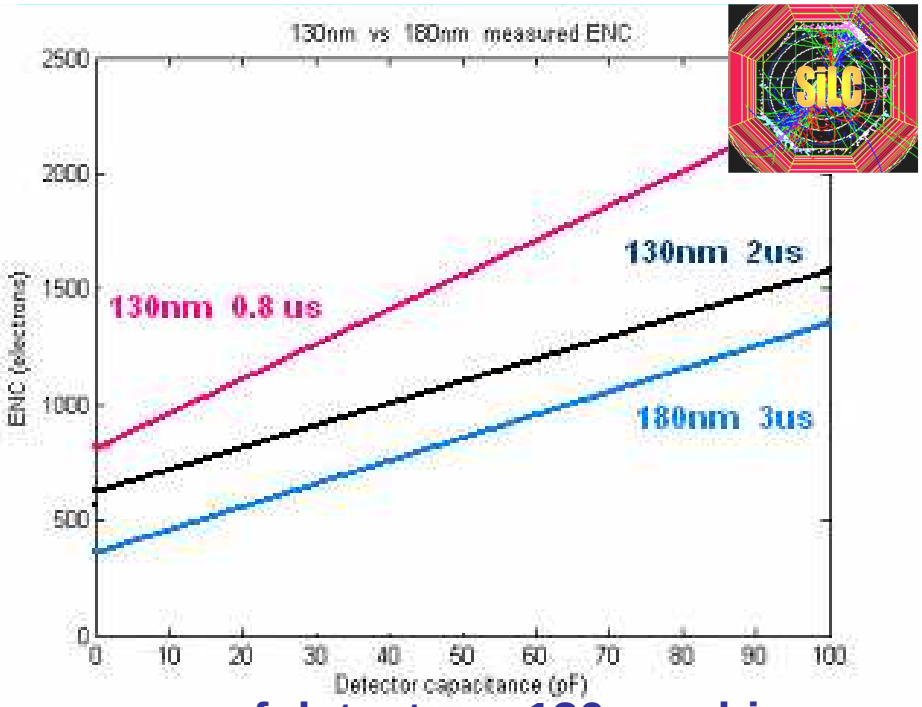
Test of the A/D converter: 9,7 bits (12 bits exp) in the worst case.

SiTR_130-V1 successfully tested both at Lab test bench snd test beam (realistic conditions (see next)

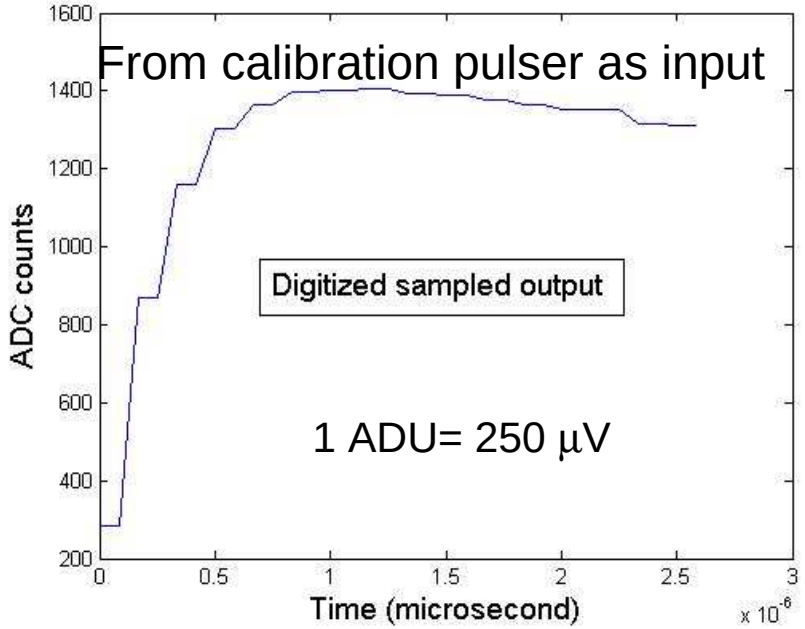
Measured Performances

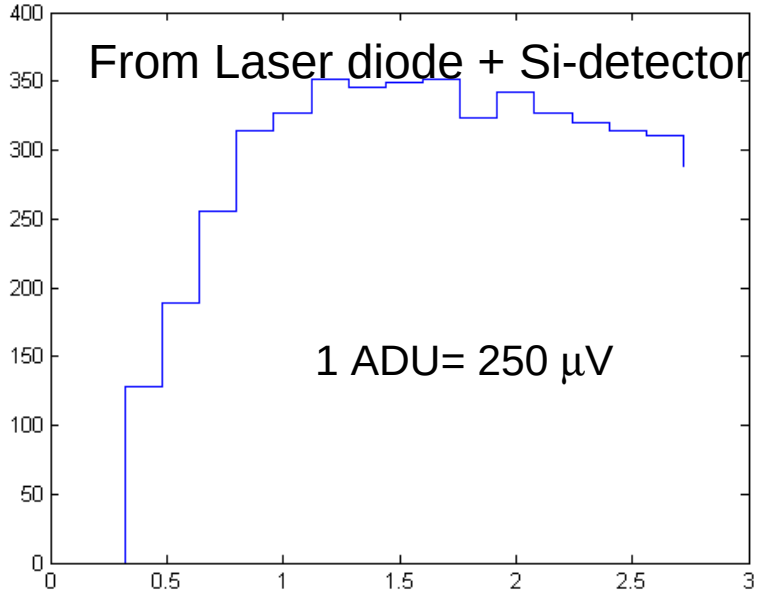
Noise:
130nm @ 0.8 µs: 850 + 14 e-/pF
130nm @ 2 µs : 625 + 9 e-/pF
180nm @ 3 µs : 375 + 10.5 e-/pF

Power (Preamp+ Shaper)
130 nm: 150+90= 245 µW
180 nm: 70+140= 210 **µW**



Digitized analog pipeline output Laser response of detector + 130nm chip



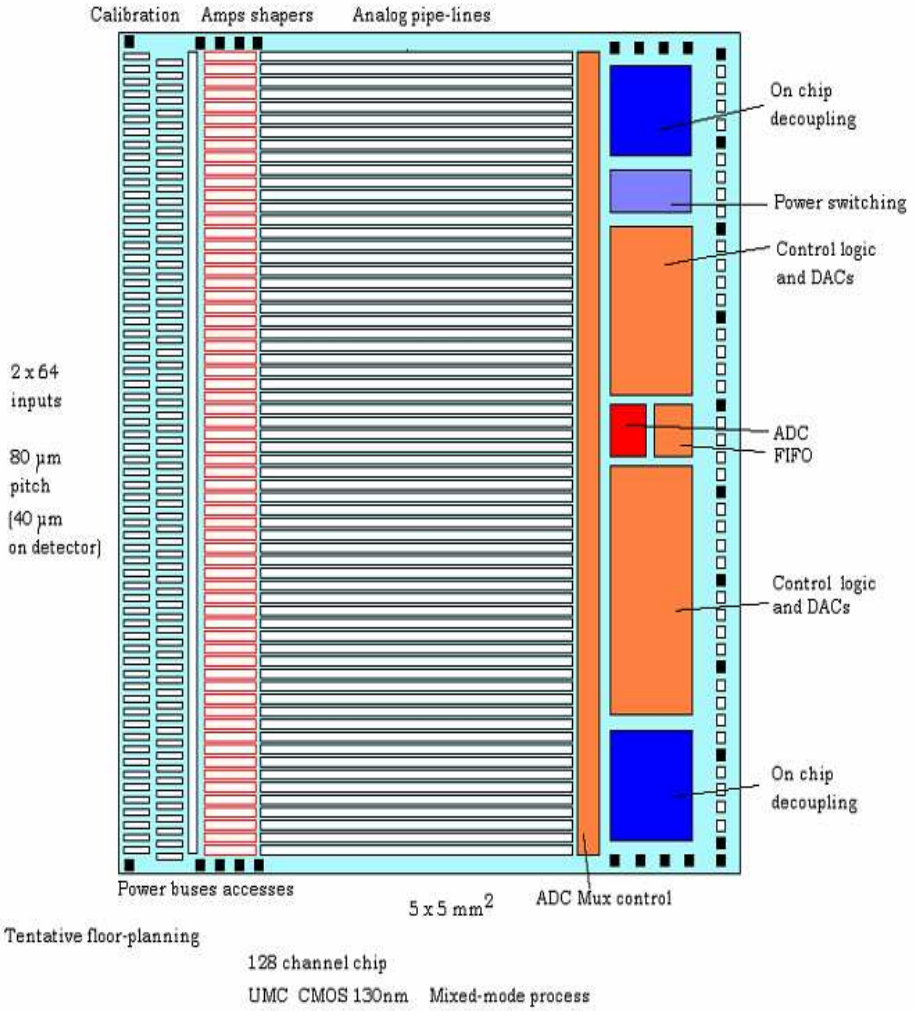


Sampling rate = 12 MHz; Readout rate = 10 KHz

New version: SiTR-130_96

LAPP, LPNHE, U.Barcelona

Floorplan

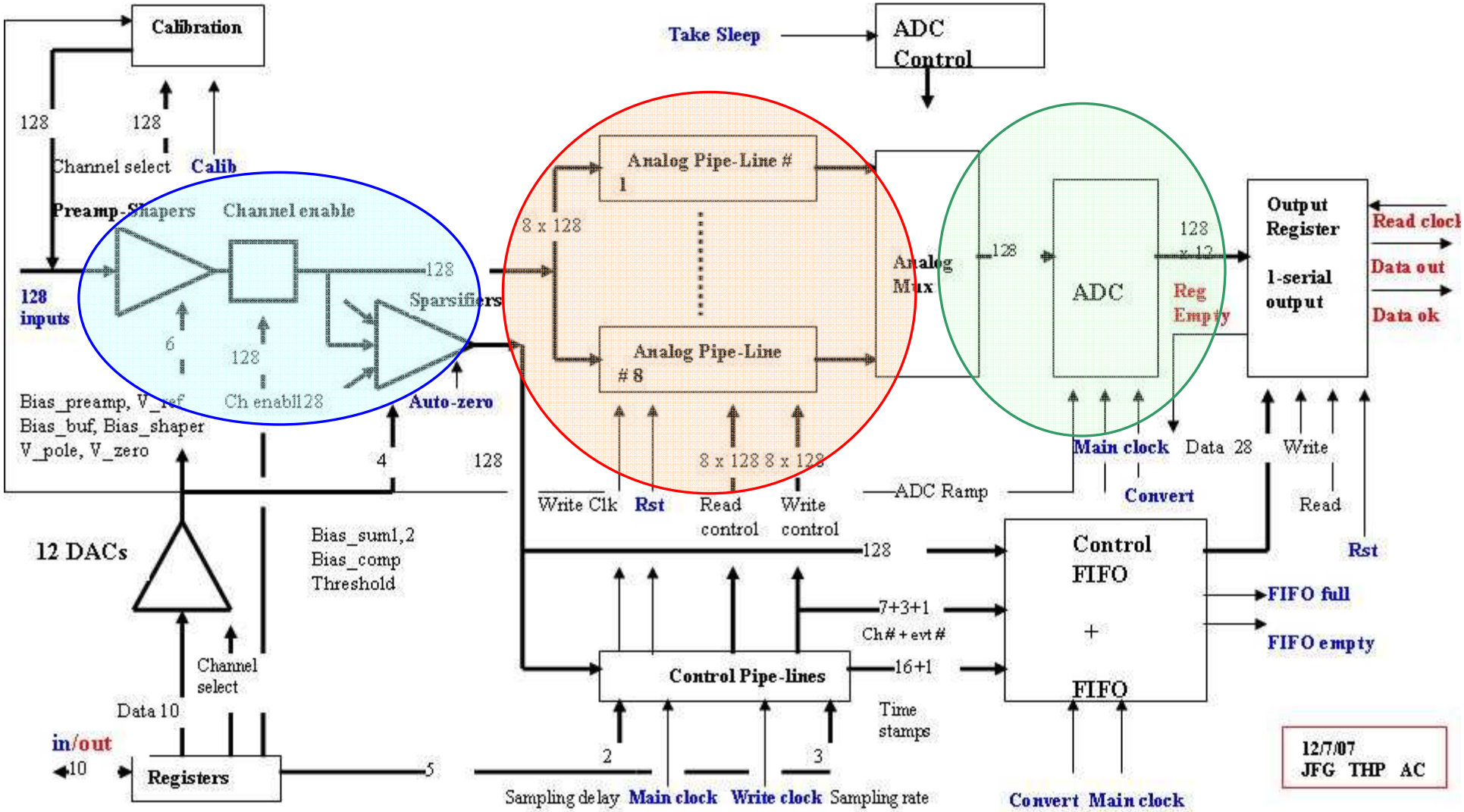


- 96 channels in 130nm CMOS
  - Improved shaper (reduced noise)
  - Improved pipeline
  - Chip control
  - Digital buffer
  - Processing for :
    - Calibrations
    - Amplitude,time χ2 estimate, centroids
    - Raw data lossless compression
  - Power cycling using DACs controlled current sources

- Tools
  - Cadence DSM Place and Route tool
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM
  - Some IPs: PLLs

Include mixed-mode simulator
AMS designer under installation at LPNHE

SiTR-130_96 block diagram
(*B.U., LPNHE, LAPP)*



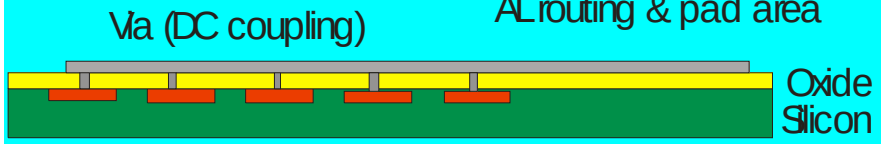
Simulation finished Mid March; Layout & Mix-mode simu undergoing

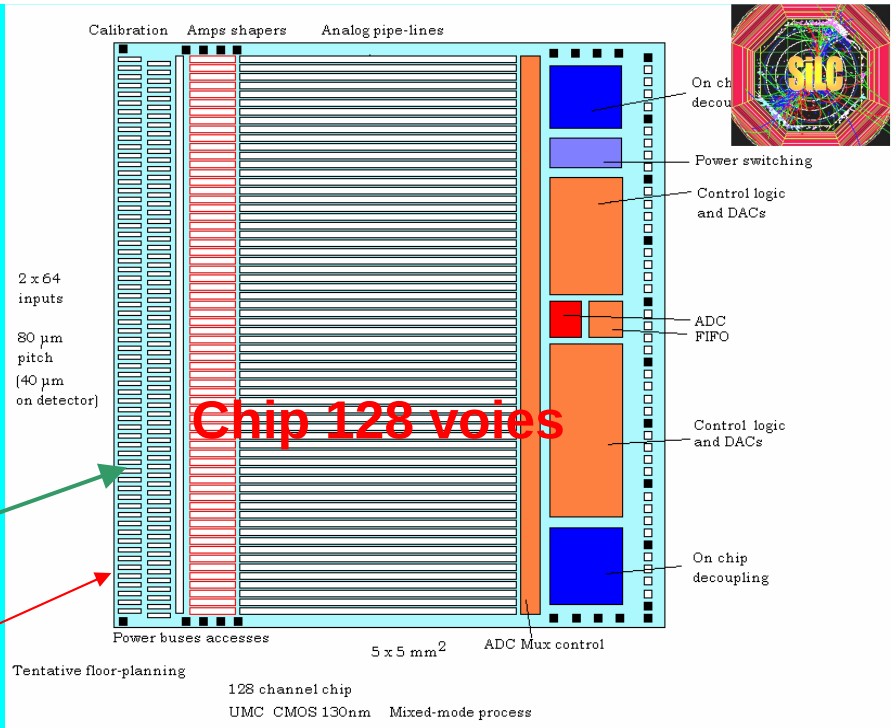
To be sent to foundry April 15

WIRING FEE CHIP ONTO µSTRIPS

Goal: developing new routing and inline pitch technology for FE chip onto the strips

1st try: SiTR_130-96 chip + new HPK sensors





Decrease %X_0: NO hybride & pitch adapter

1st approach (2008-2009): (HPK/LPNHE-IN2P3)

Chip directly routed onto µstrips by bump bonding

HPK: sensor + bonding of the chip

IN2P3: chip 96 channels

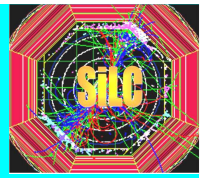
performance tests comparing

new connection wrt hybrid version

Demonstrator: 2008, production 2009

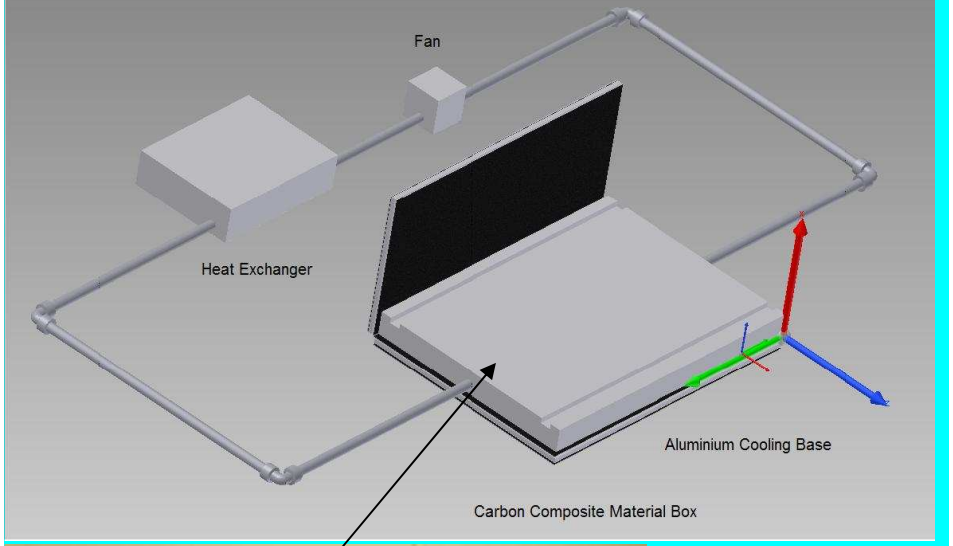
Chip bonded sensors at the price of usual sensors

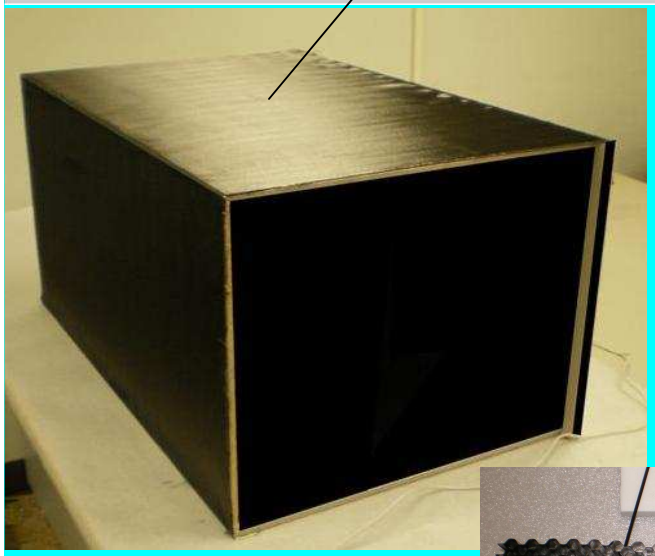
Future: 3D technology for µstrips &/or connection chip/µstrips



- R&D on sensors
- R&D on electronics
- Mechanics developments:
  - **Elementary modules, prototypes, tooling**
  - **cooling**
  - **alignment**
- Simulation
- Tests

Air dry cooling system (OSU) or just an insulating frame



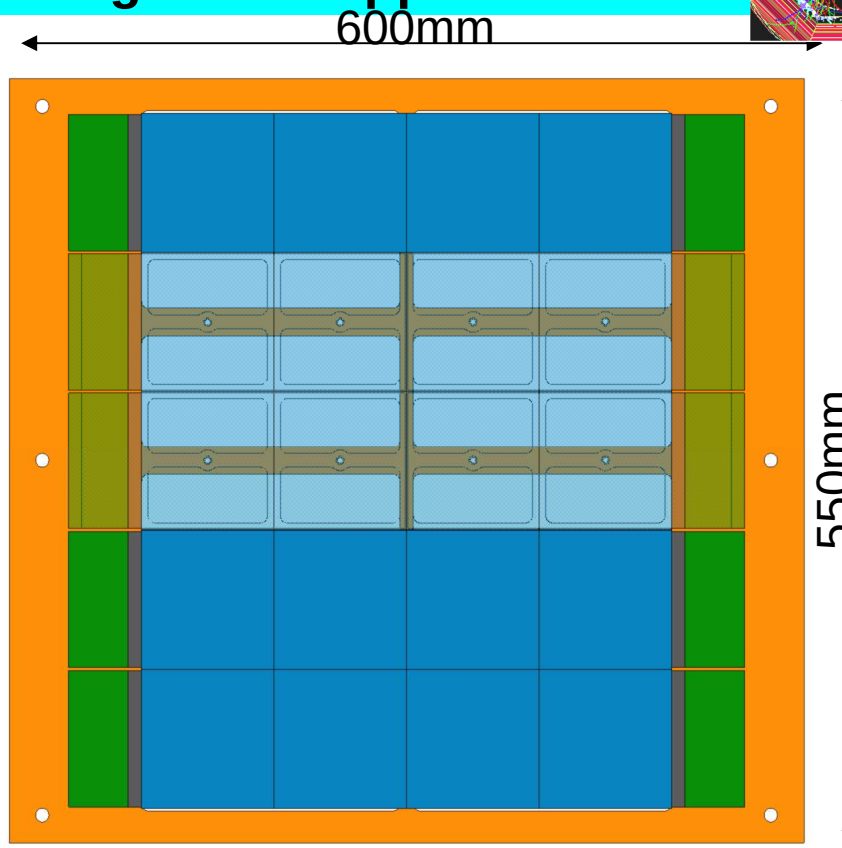


C composite material insulating box

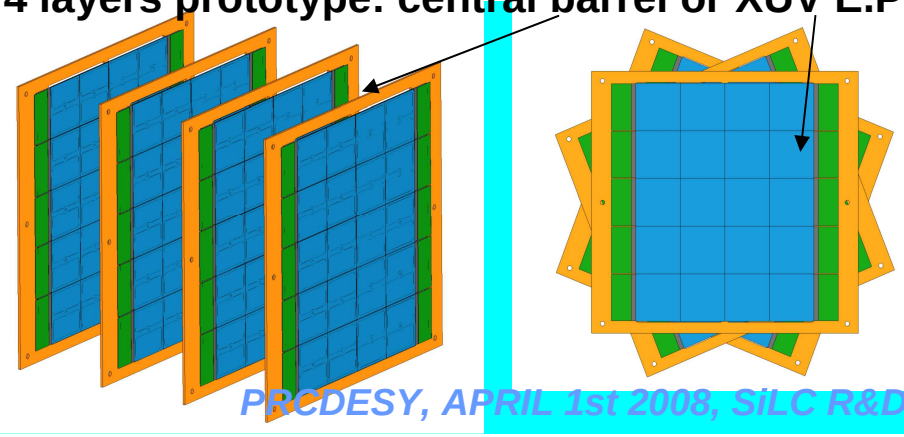
Double-sided honey-comb Carbon composite material

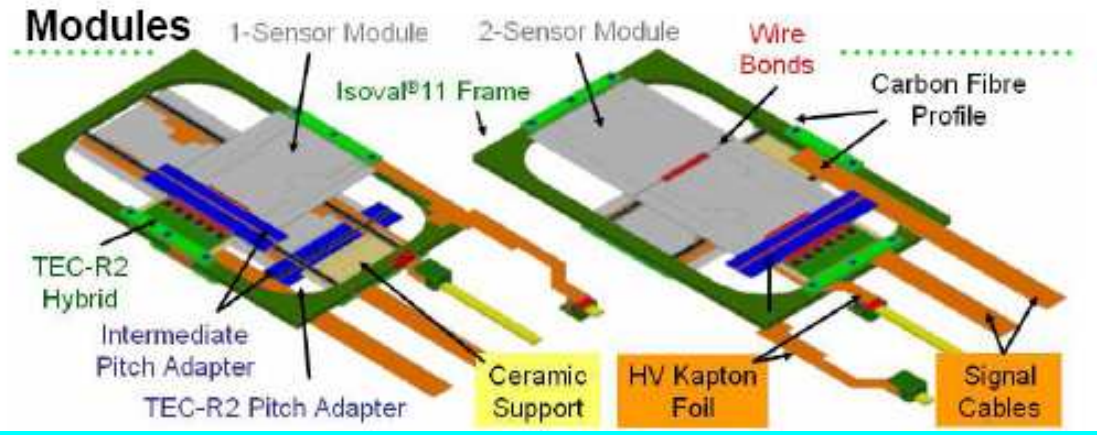
Prototypes for test beams:

- **Large size support structure**

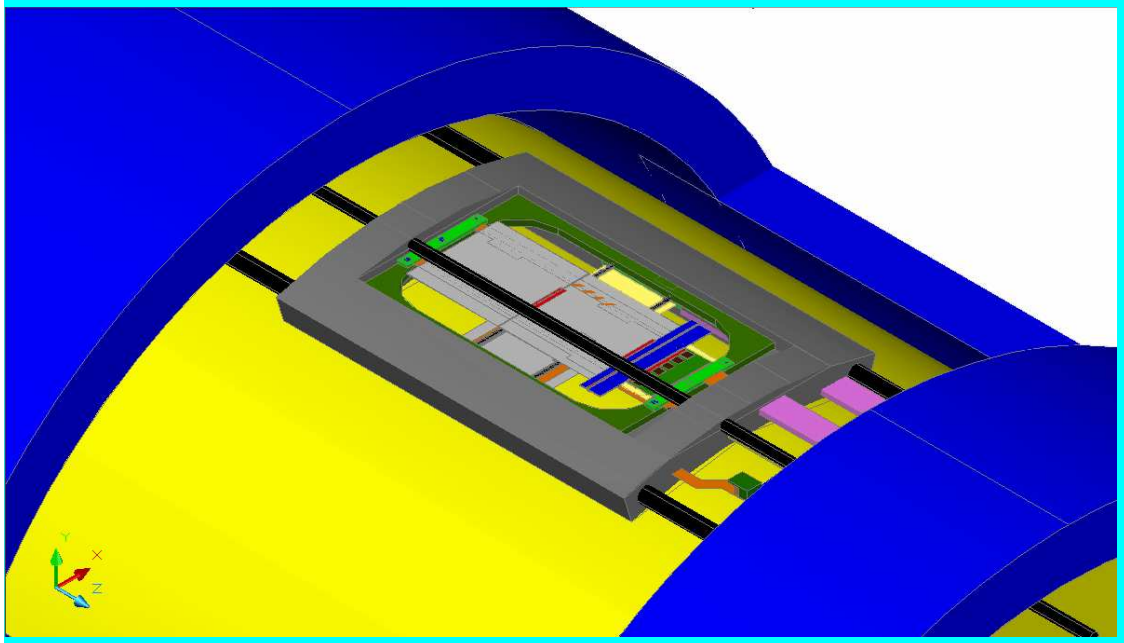


4 layers prototype: central barrel or XUV E.P.

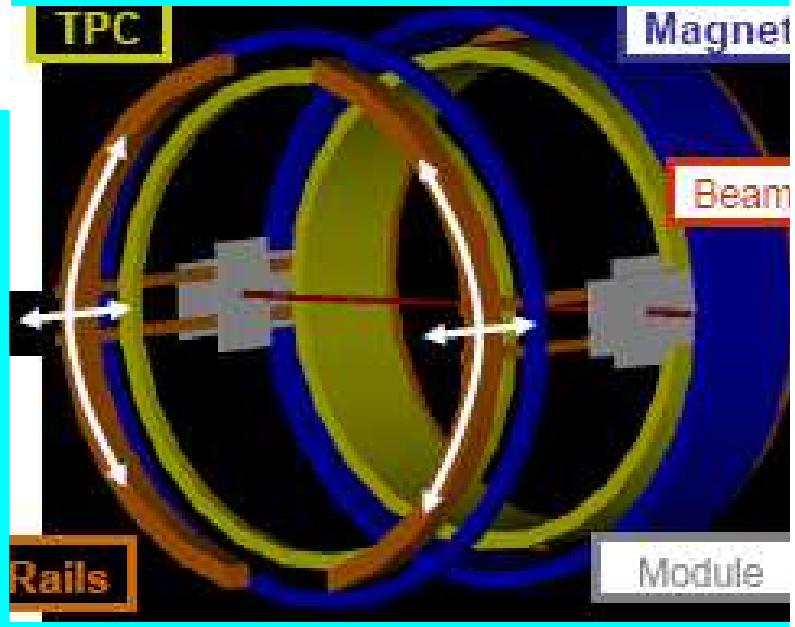




Developing tools and ''savoir-faire'' on new modules construction



Both prototypes include working on new modules starting with lighter module structure at first .



Test with of the Silicon Envelope with LCTPC in 2008 at DESY: Modules(HEPHY), structures(IEKP) final electronics (LPNHE)

Alignment: 2-fold approach

and CNM/CSIC

AMS-like approach:

baseline version: Minimum set of changes for any SiLC sensors

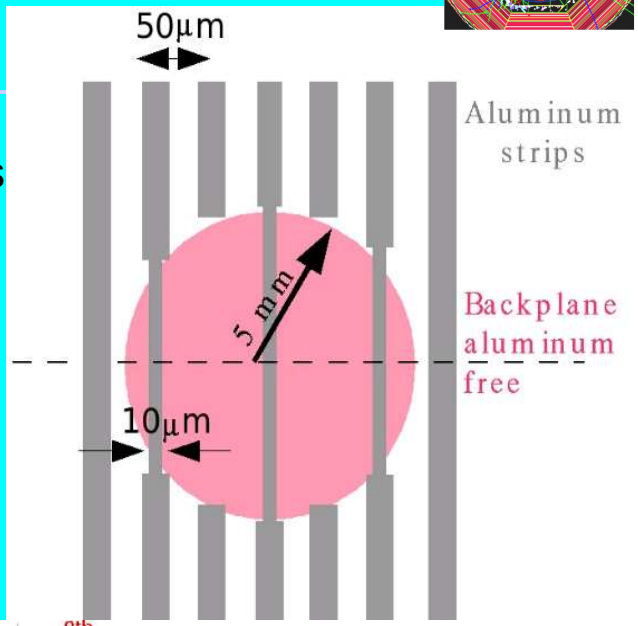
For instance, for the new HPK sensors

Implemented:

- ∅~10 mm window where Al back-metalization has been removed

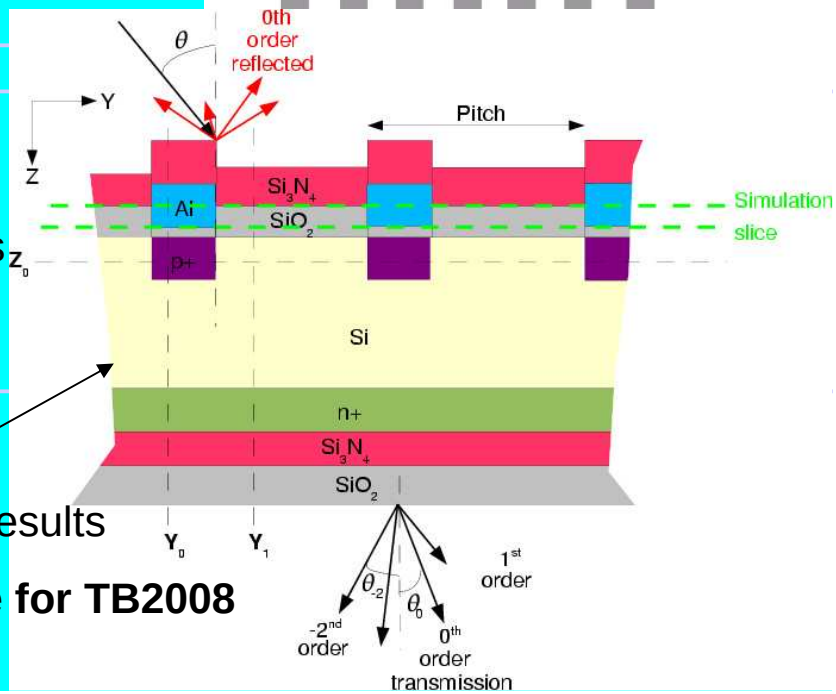
Suggested (not cost effective for small batches):

- Strip width reduction (in alignment window)
- Alternate strip removal (in alignment window)



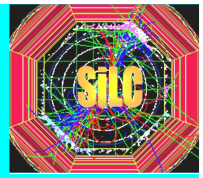
R&D on transparent Silicon µstrip sensors:

- Together with IMB-CNM (Barcelona) design, build and test new IR-transparent Silicon microstrip sensors
- Consider option of aluminum electrodes or transparent electrodes



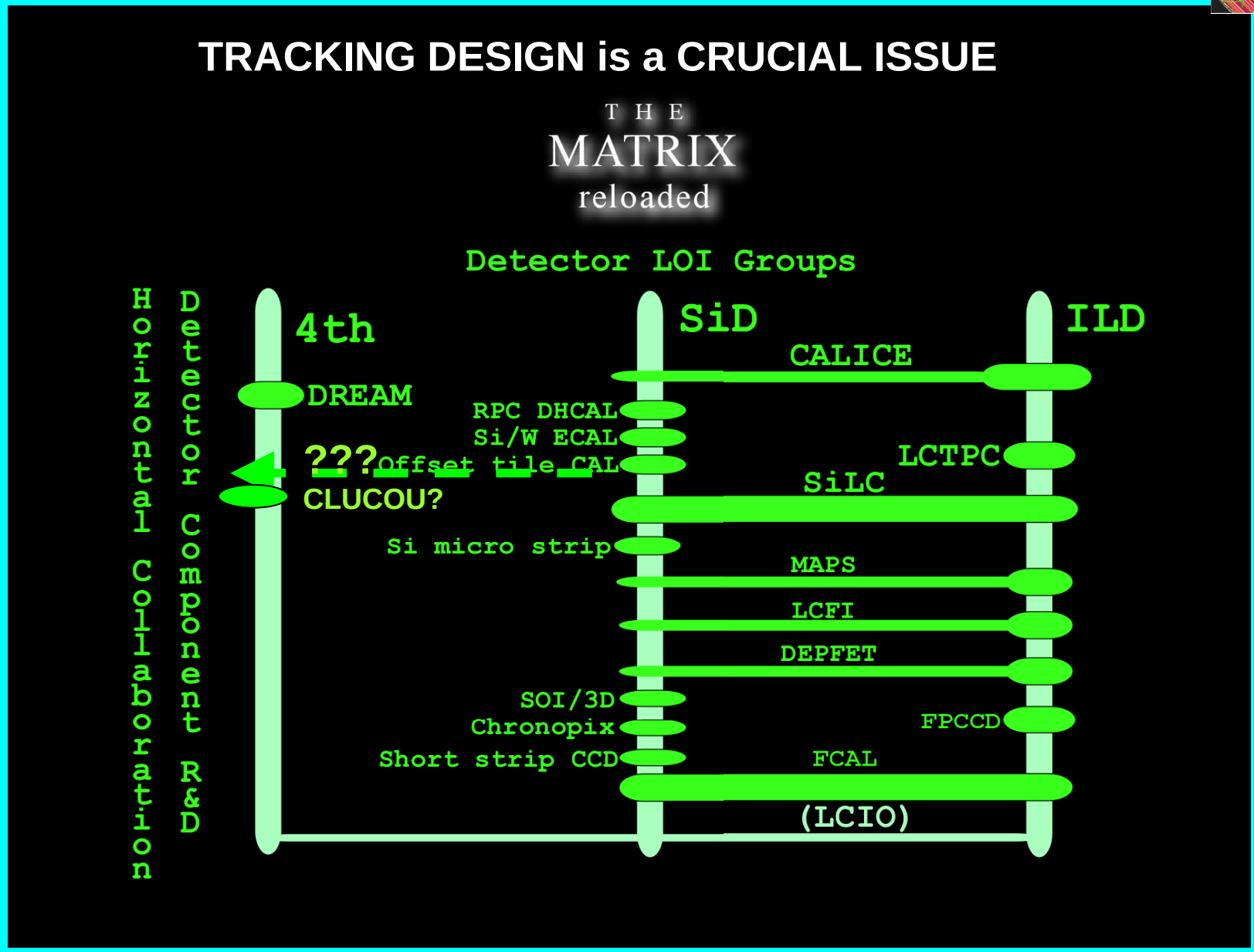
Realistic sensor simulations: very interesting studies/results

Test bench in development and alignment prototype for TB2008



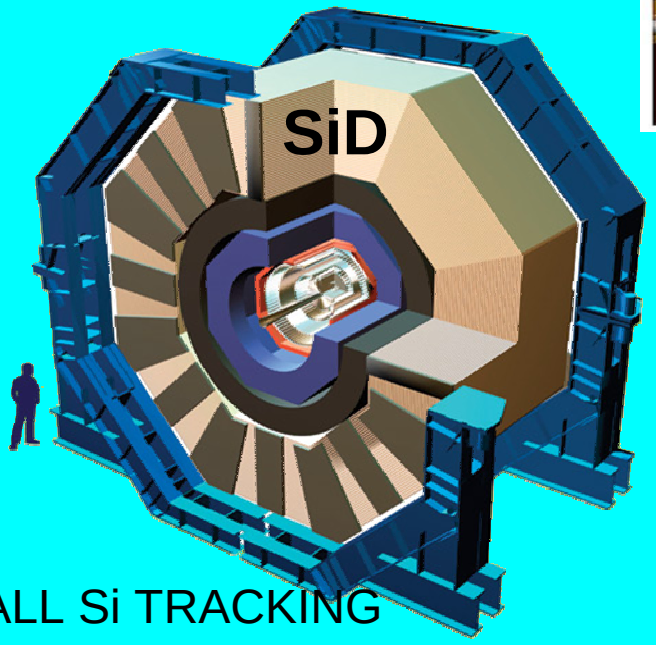
- R&D on sensors
- R&D on electronics
- Mechanics developments
- Simulation
  - ***Task force*** on simulation in SiLC collaboration since 2007:
    CU Prague, IFIC-Valencia, HEPHY-Vienna, OSU-DESY,
    LPNHE-Paris, IFCA, UCSC-Santa Cruz
  - ***Collaboration*** with MOKKA/Marlin Reco +
    Optimization ILD group (M. Thomson) + ILCROOT (starts)
  - ***Progress on:*** full simulation (superdrivers), digitization,
    FWD studies and main issue = detector optimization
- Test beams

INTEGRATION & OPTIMIZATION:

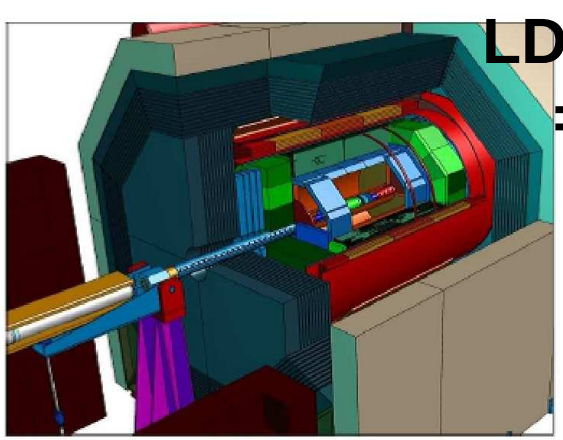


By courtesy Yasuhiro Sujimoto

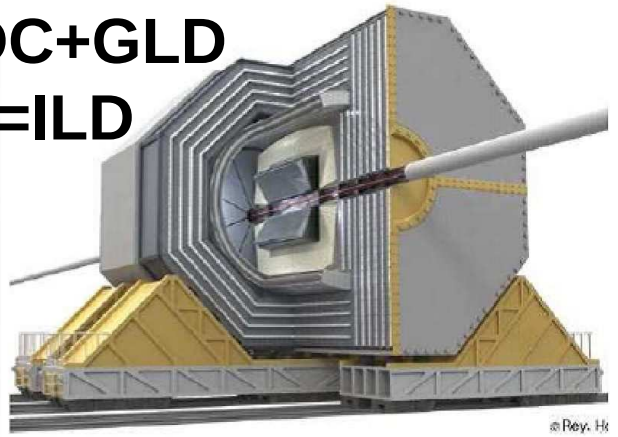
ALL (MOST) DETECTOR CONCEPTS INCLUDE SILICON TRACKING



ALL Si TRACKING

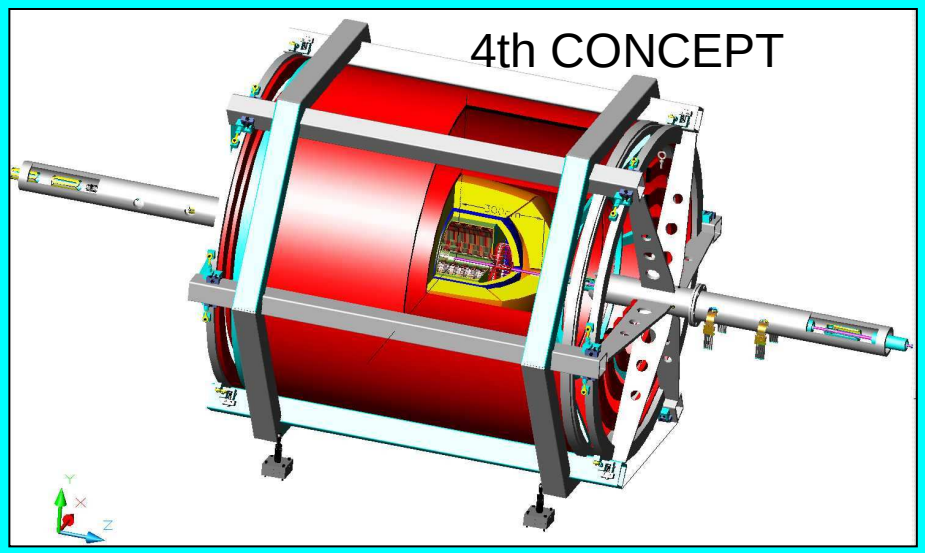


LDC+GLD =ILD



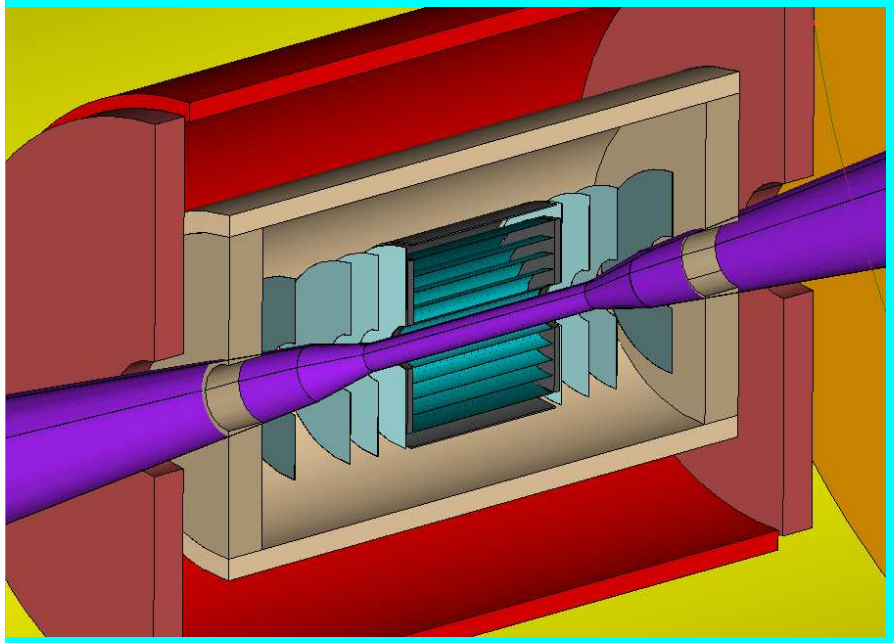
TPC+ Si TRACKING

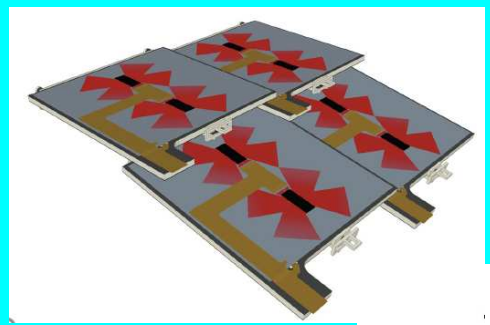
Main goals:
Best performances and Lowest %X0 everywhere (or quasi everywhere)



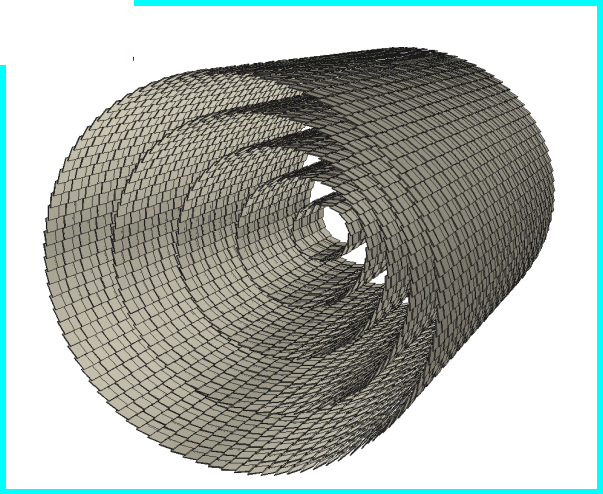
GASEOUS CENTRAL TRACKER?
(+ Si tracking? What Si tracking)
ALL SILICON TRACKING ?

Q1: all silicon versus hybride gaseous + Silicon

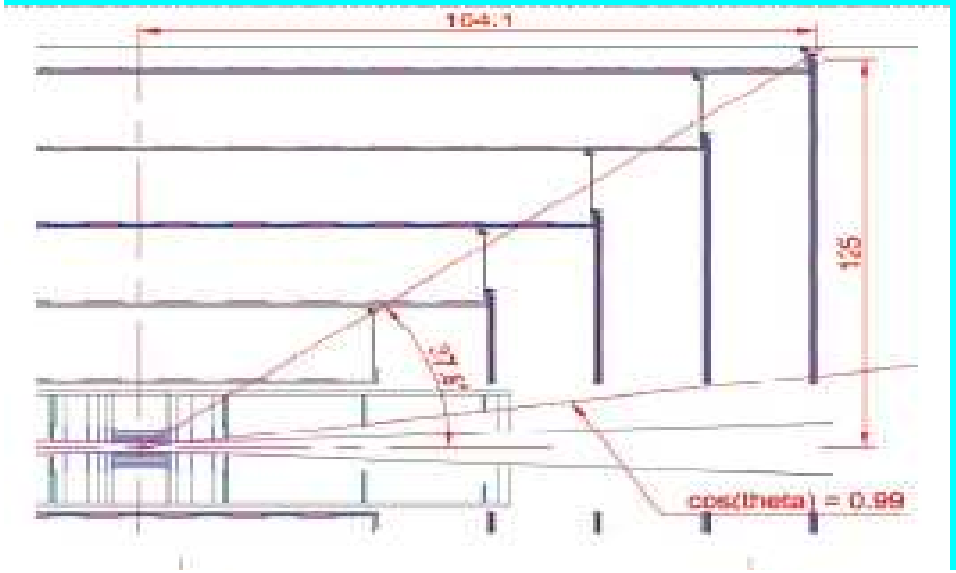




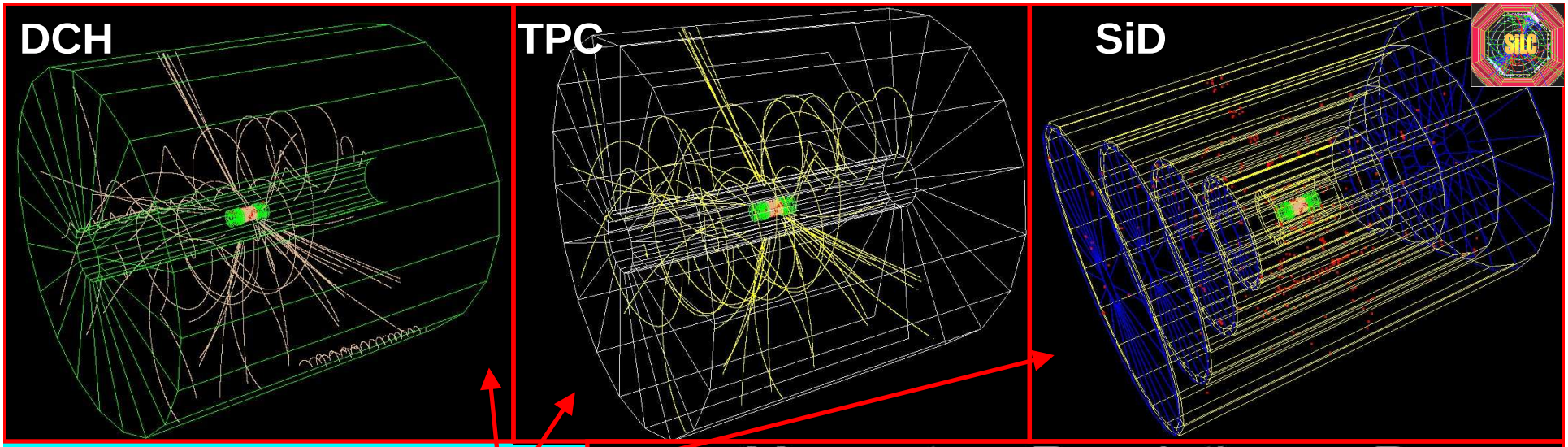
From microstrips tiles
to the all-pixel variante



The SiD tracking integrated concept



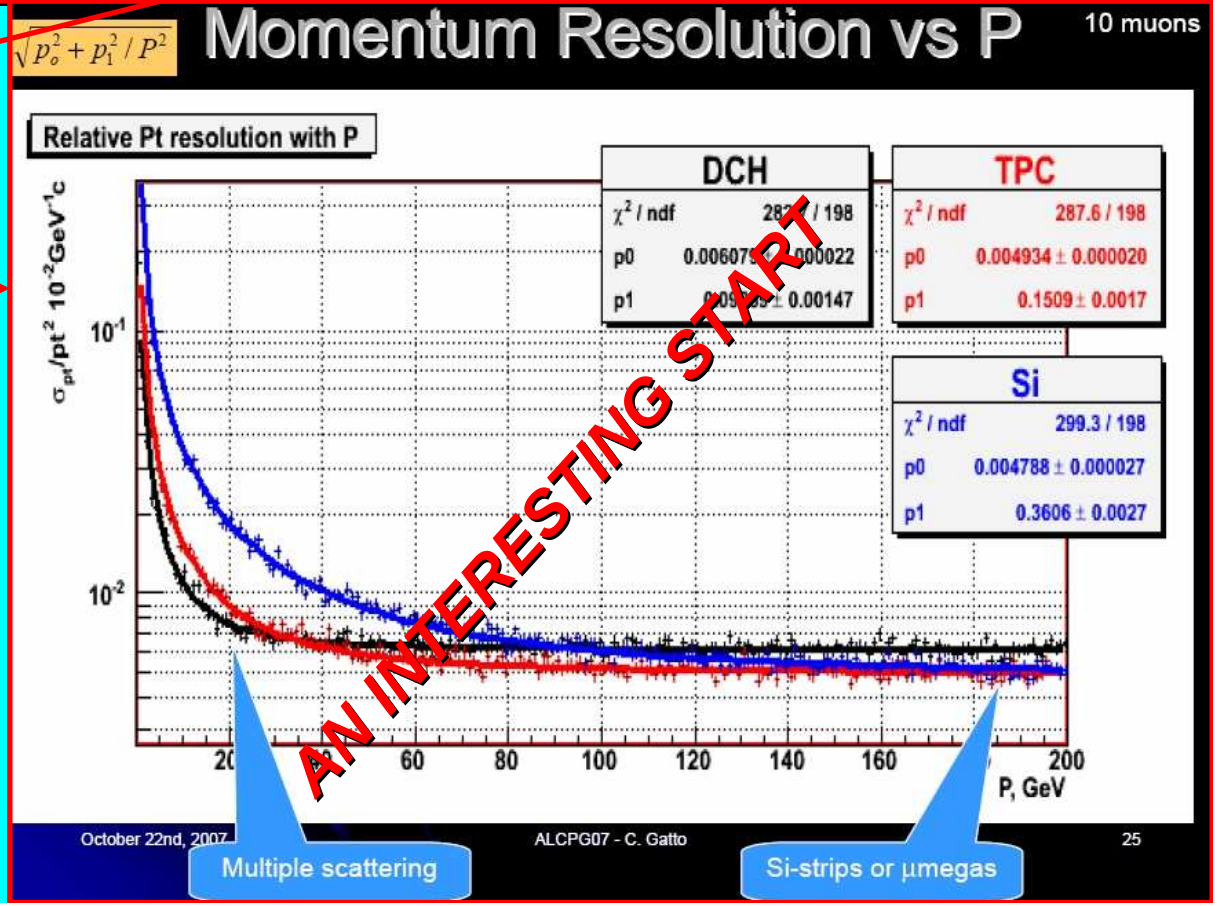
How they compare in the various tracking
Regions, especially:
Who wins at large angles?
Pros and cons of each one and how to
Improve them.
What technogical choices?



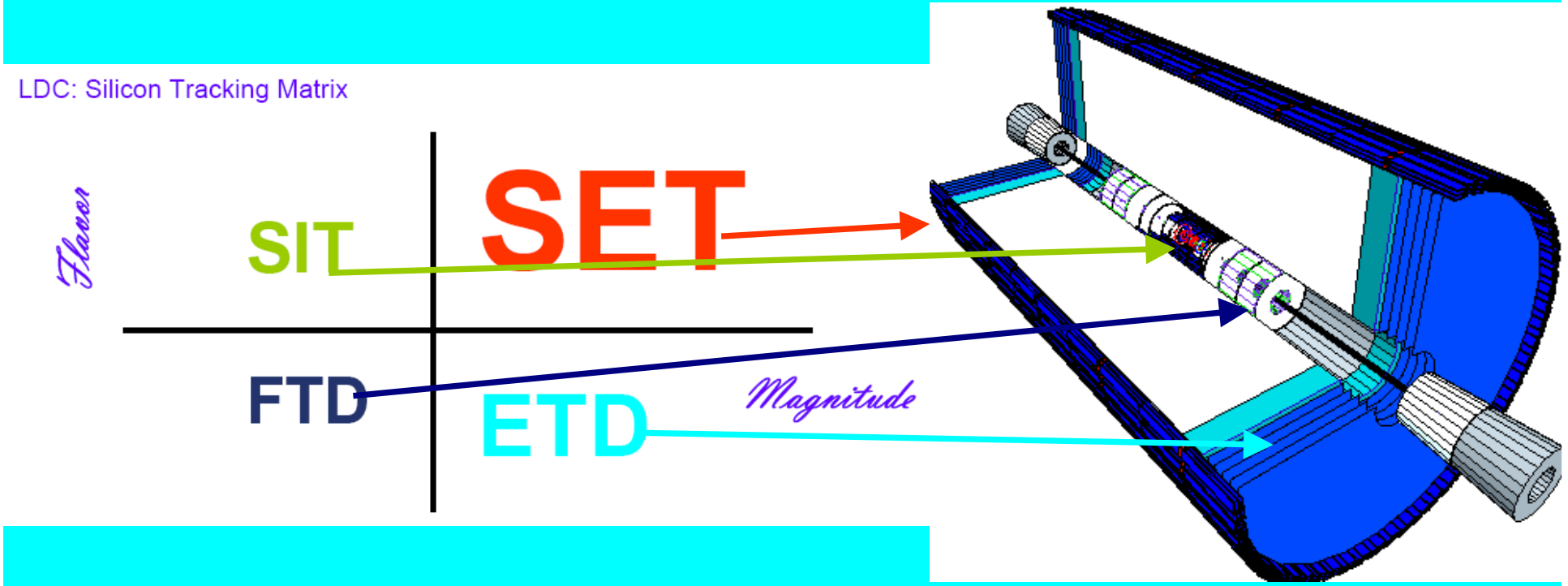
The comparison of tracking performances between gaseous & Silicon tracking has started (see results from C.Gatto & al with ILCROOT)

Joint effort with 3 detector projects with full simulation of main possible scenarios:
-> DCH + Si track. components
-> TPC + Si track. Components
-> All Silicon with various cases and:
various technological scenarios.

PRCDESY, APRIL 1st 2008, SiLC R&D

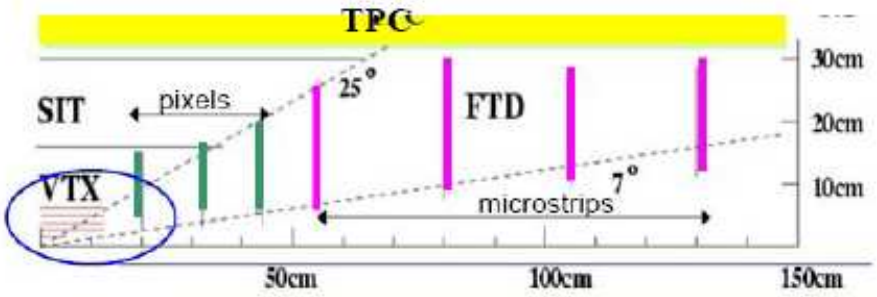


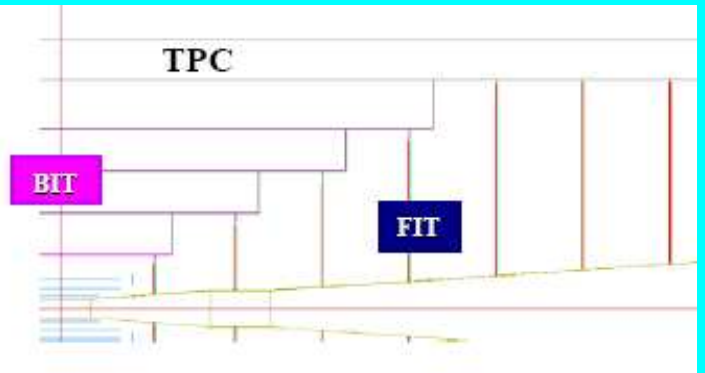
Q2: Roles of Si components in the hybride tracking case

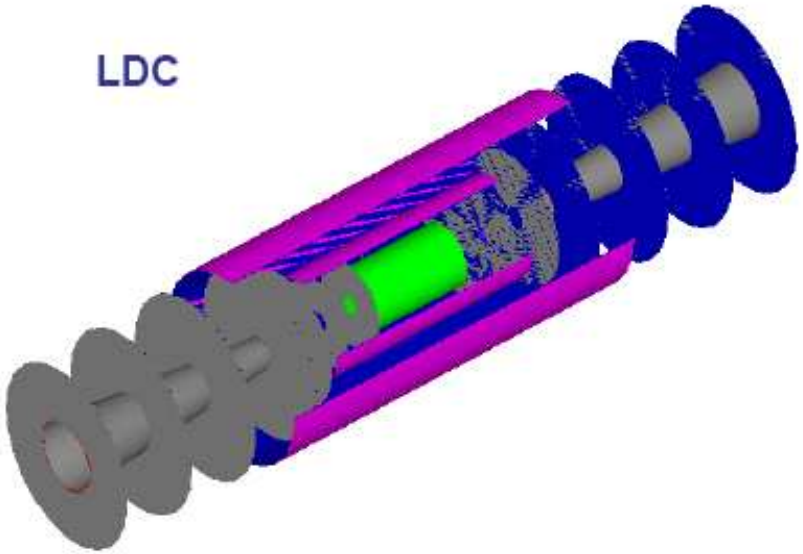


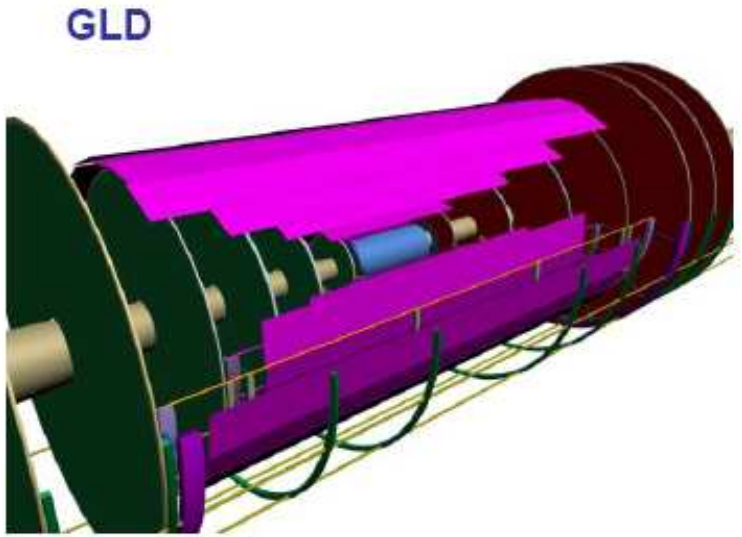
Discussed several times and a lot of simulations studies already done;
(see SiLC proposal to the ILCSC R&D Tracking panel in BILC07
http://lpnhe-lc.in2p3.fr/DOCS/beijing.pdf)
Presentation of V. Saveliev at 1st ILD Meeting in Zeuthen Jan. 08 and latest presentations by M. Vos and W. Mitaroff, at TILC08

Q4: The internal region in the hybride gaseous+ Silicon case, *how many layers, resolutions, technology…*

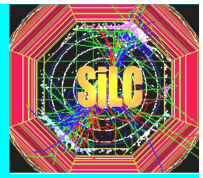








Superdrivers for the each Silicon tracking components (SIT, FTD, ETD and SET) defined and included in MOKKA framework. They will thus be part of the 1st simu round.



- R&D on sensors
- R&D on electronics
- Mechanics developments
- Simulation
- Tests: ***facilities and results***

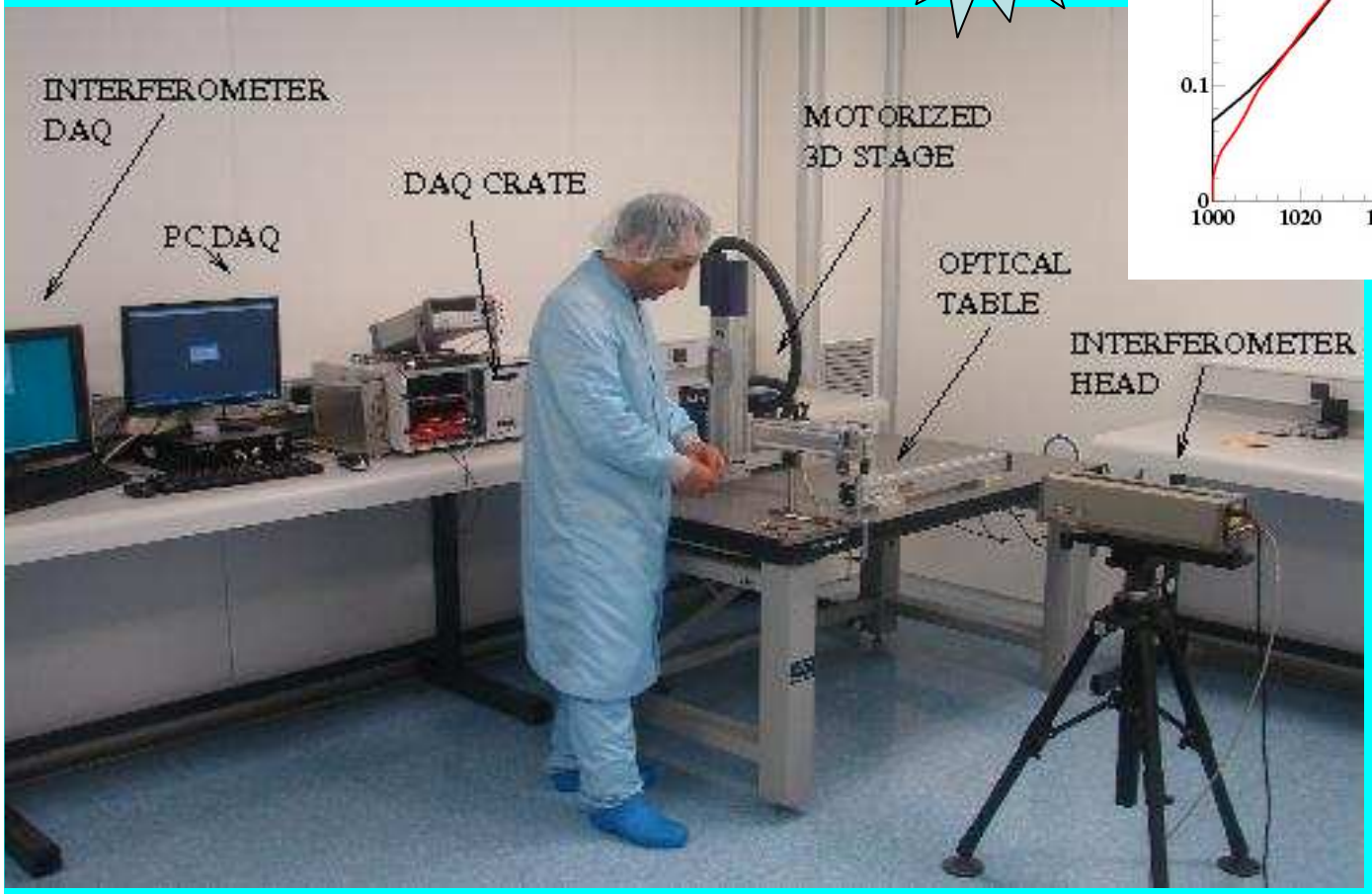
❖ ***Test benches***: QTC sensors, multipurpose, alignment (ex.)

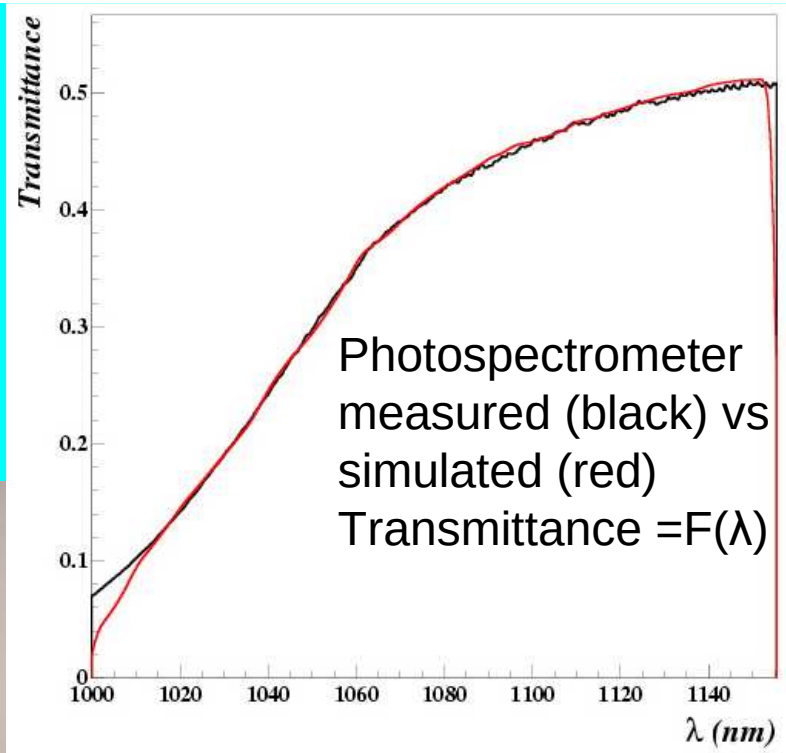
❖ ***Test beams***: DESY(06,07→), CERN(07-08→), FNAL (09→)
SiLC07 at CERN: IEKP Karlsruhe, LPNHE Paris, CU Prague,
IFCA Santander, Torino INFN & Uni,
and collaboration with MAPS-EUDET telescope: DESY & Geneva
and CERN support (Silicon Lab)

Alignment test bench

Very precise test bench and very good agreement with Optics simulation

NEW



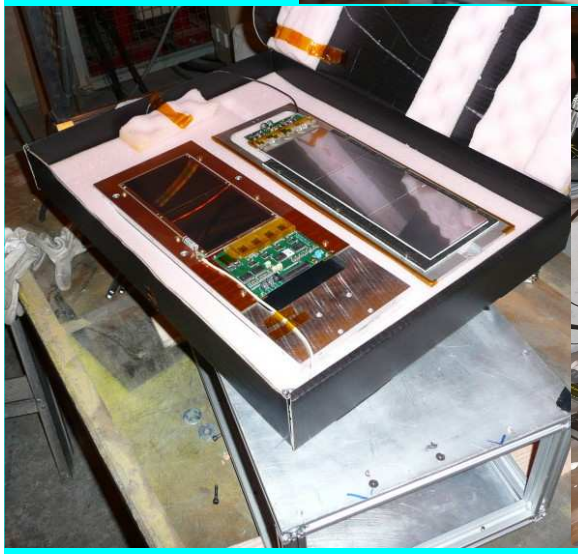


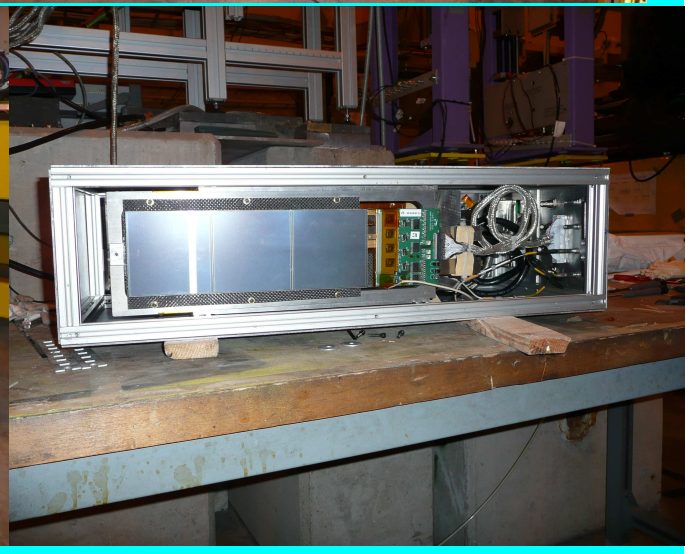
Photospectrometer measured (black) vs simulated (red) Transmittance =F(λ)

300µm thick Si wafer (no special treatment)

TEST BEAMS:

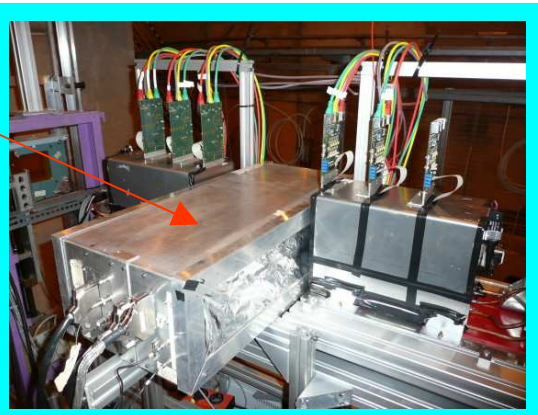
Ex: CERN-SPS West area, October 10-22, 2007

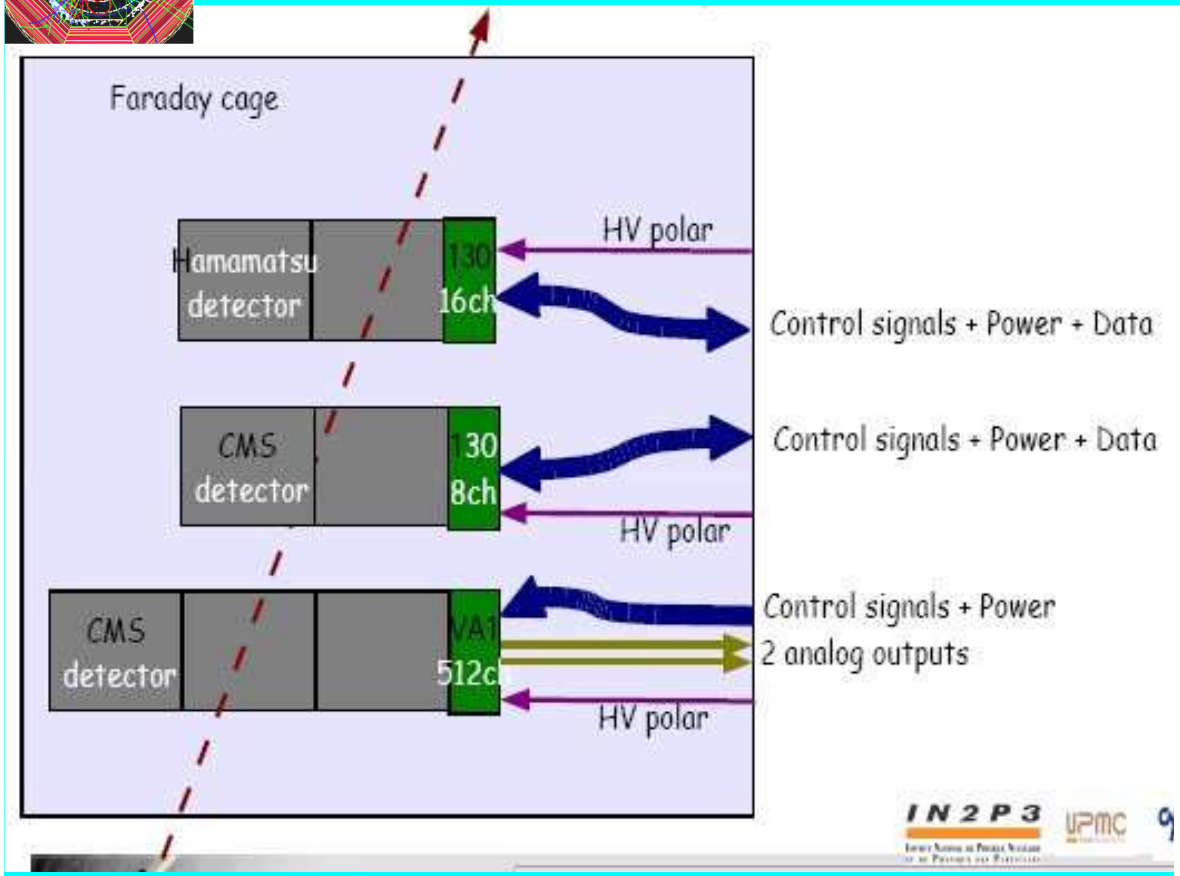




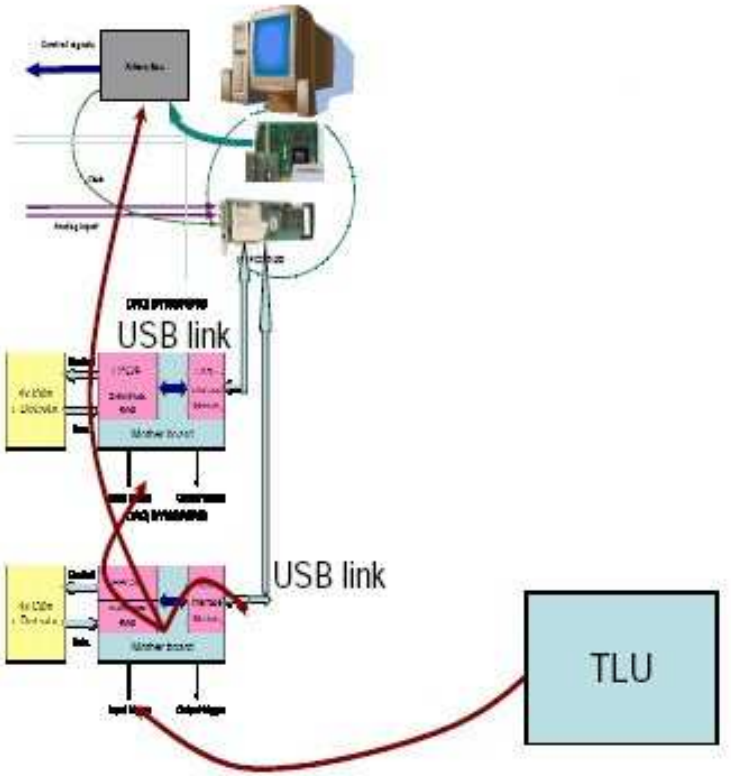
Arrival & Installation of the test set up with the MAPS EUDET telescope already in place.

Inside the Faraday cage

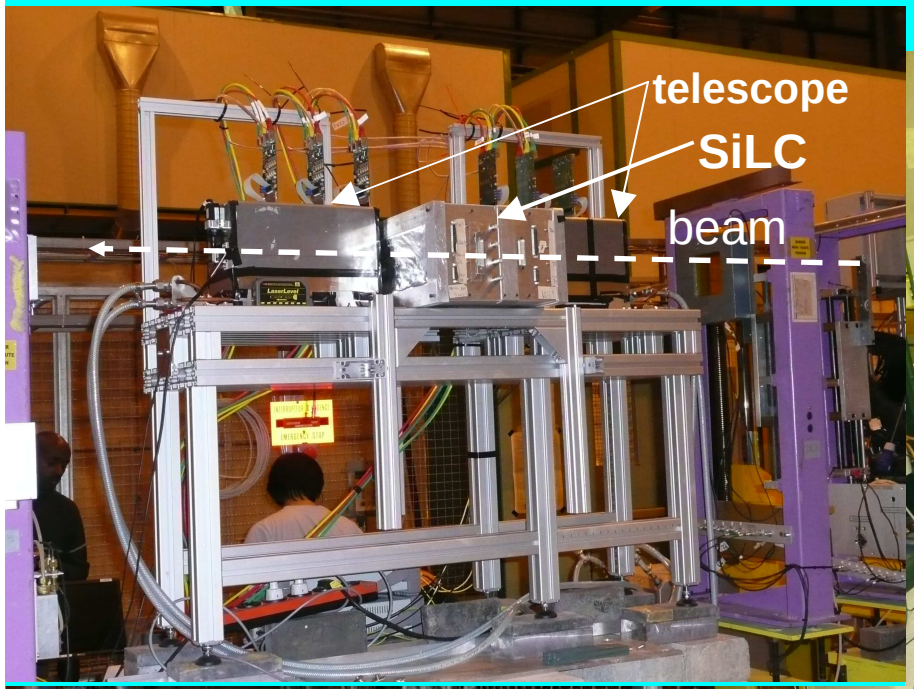


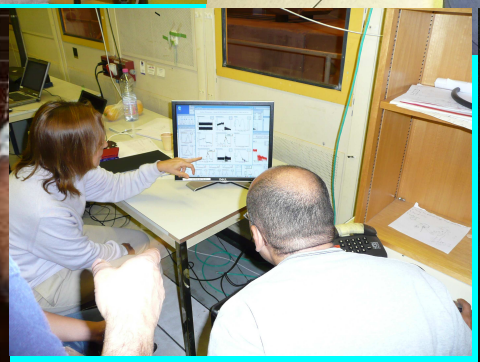


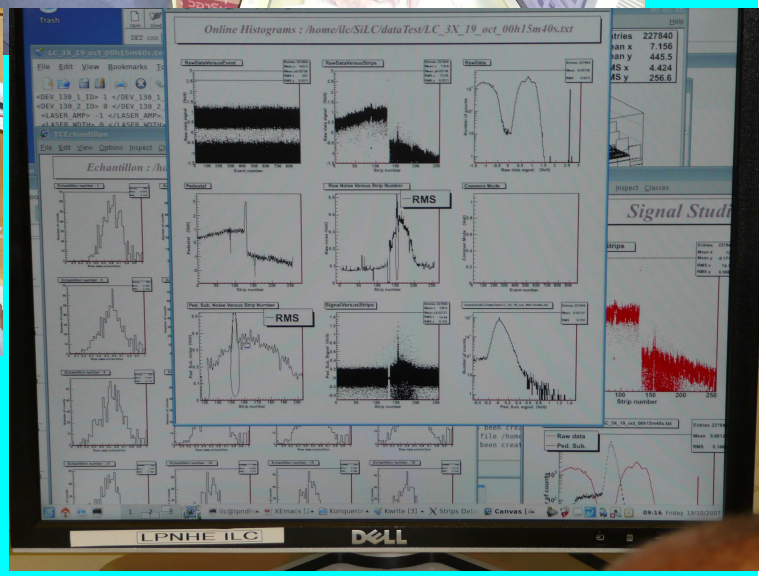
The trigger: TLU



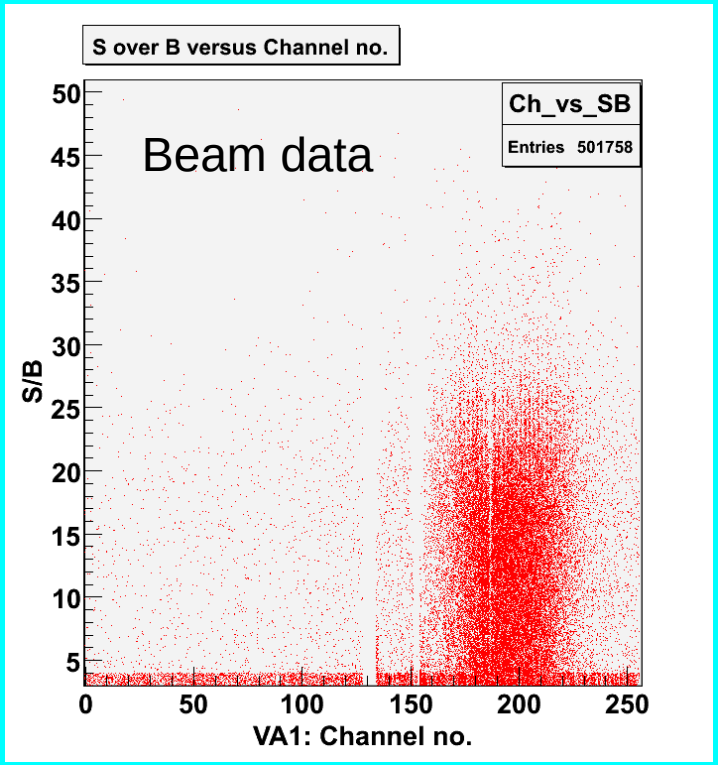
Test running and data taking

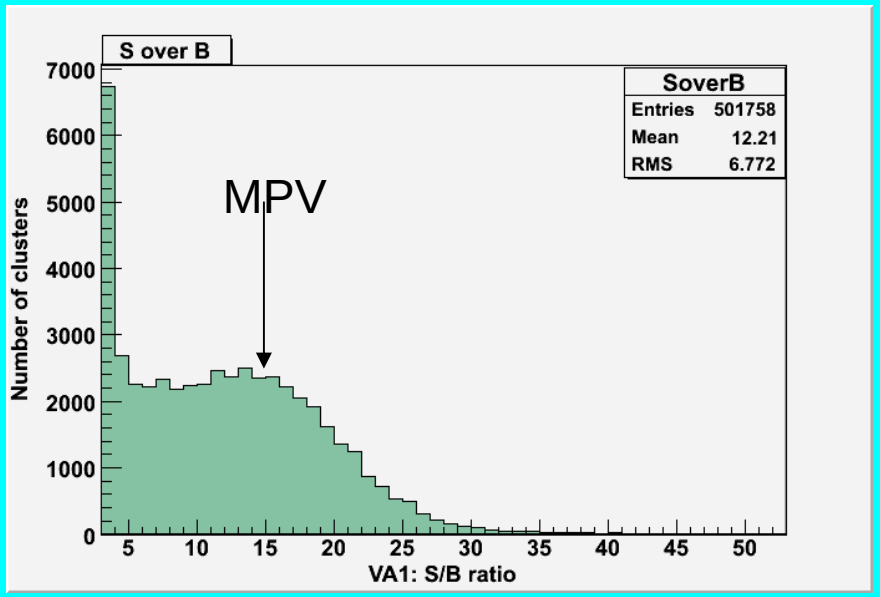






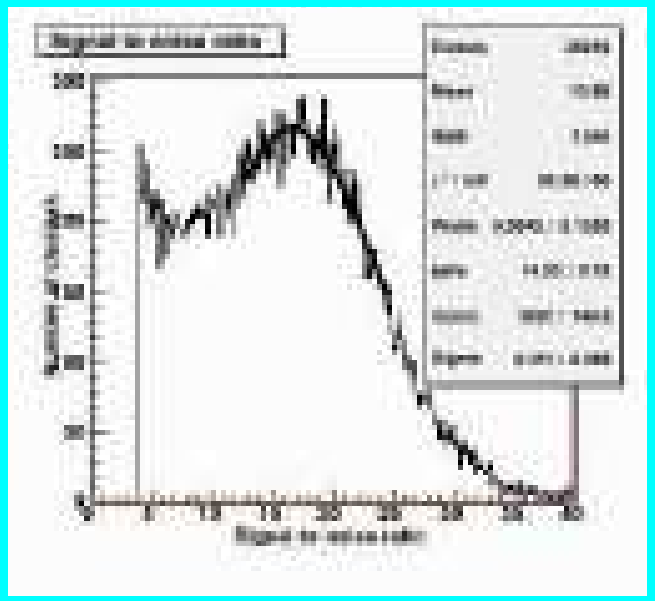
REFERENCE MODULE-VA1





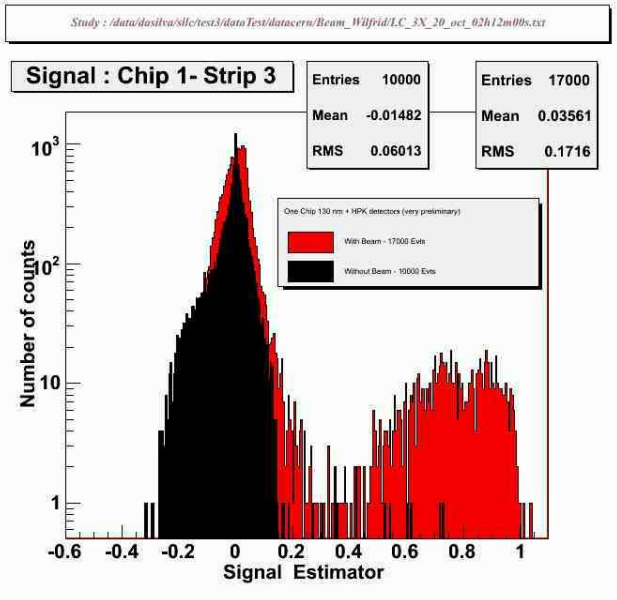
One module has its 512 strips read out by VA1' chips. It serves as reference. The strips (3 bonded ones) are about 28,5 cm long.

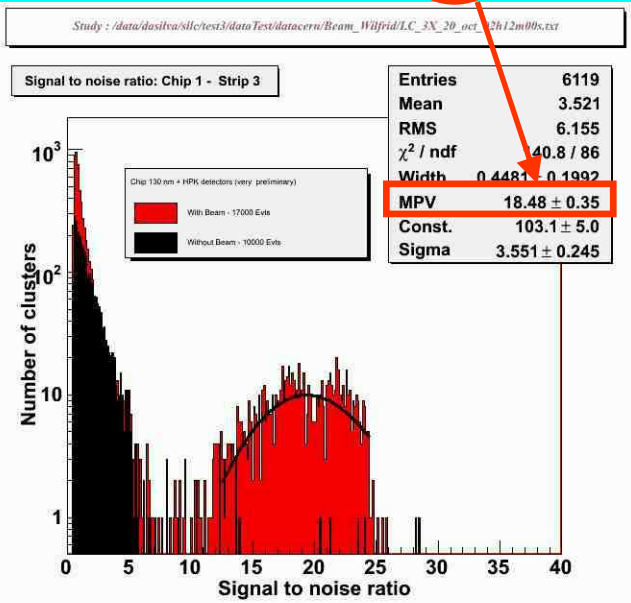
MPV(S/ N) ~ 15.

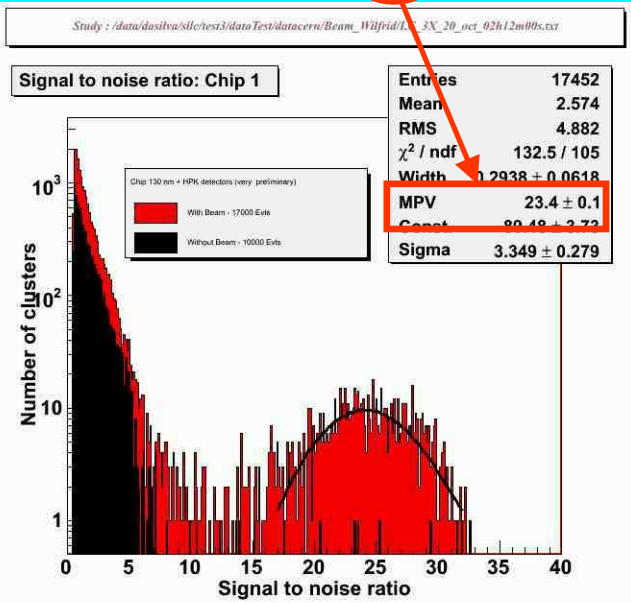


Results with the new HPK + SiTR-130

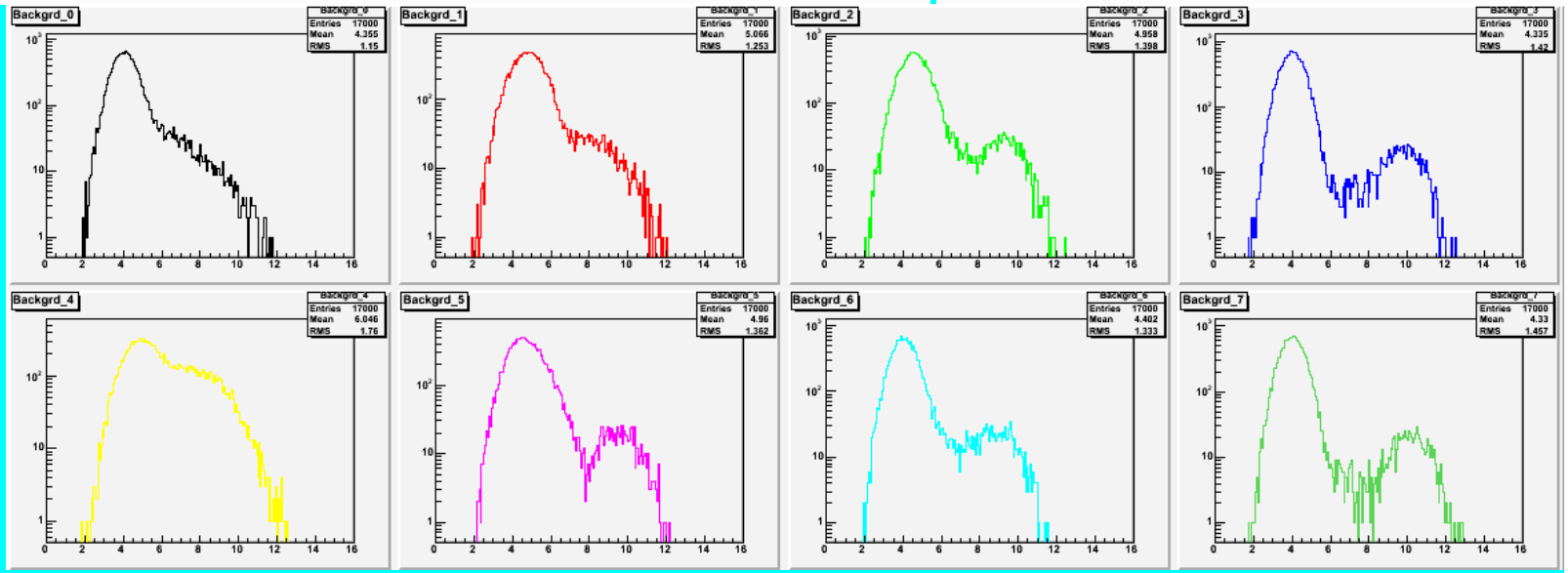
Black=beam off, red=beam on; 1 strip S/N 18 1 chip: S/N ~ 23



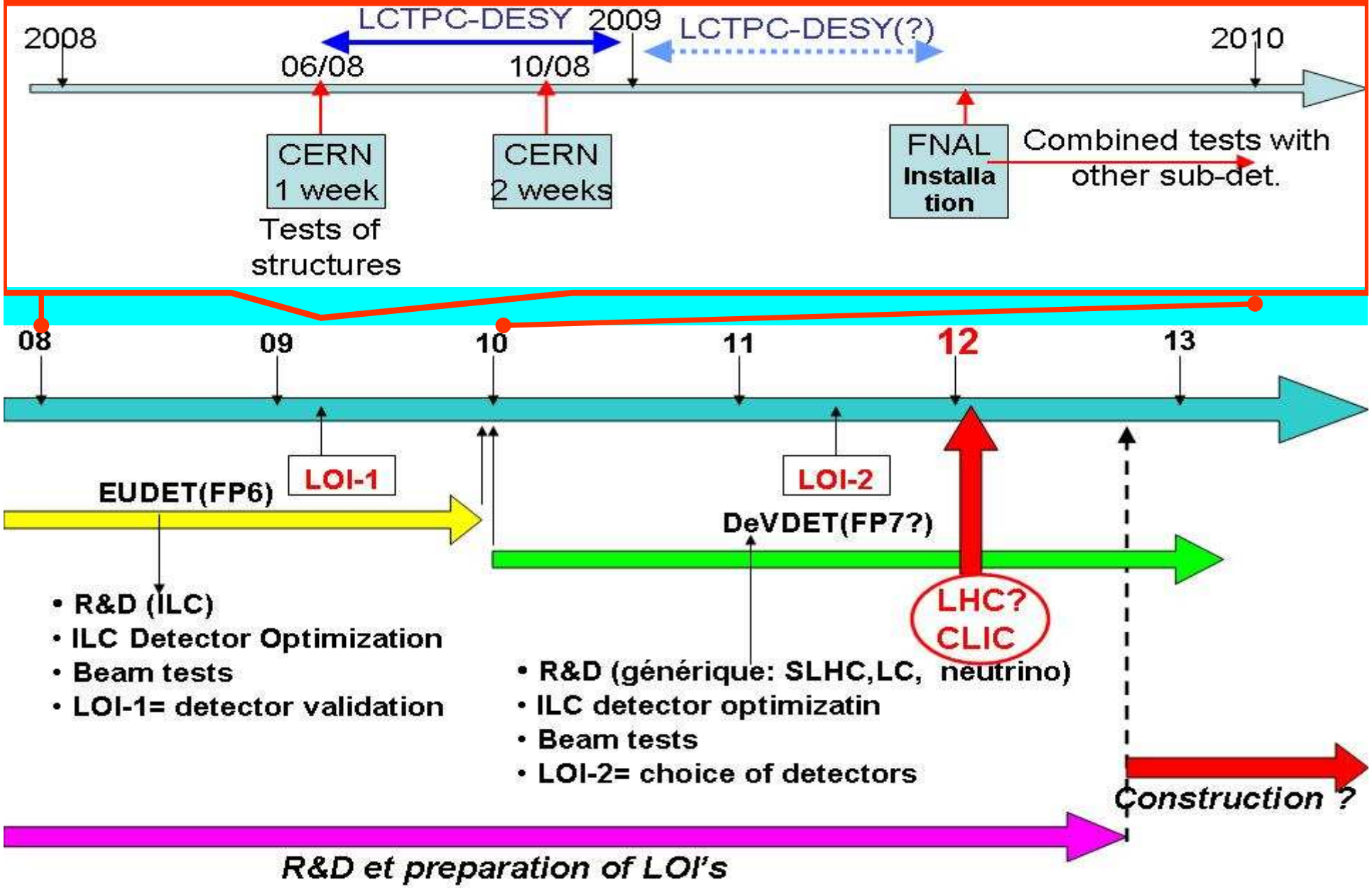




Strip length = 18,5 cm



What's next?? SiLC & ILC Roadmap



What's next: cont'd

- SiLC is a **transversal R&D activity**
- It intends to play a major role not only on the development of novel technologies needed to overcome the challenges ahead of us for constructing large area tracking systems,
- But also **to study and compare the tracking alternatives** proposed for the ILC **with a joint optimization task force**.

  At TiLC08, representatives from the 3 proposed ILC detectors decided to collaborate with a joint simulation tracking effort, sharing tools and expertise.

  It will be benefitial to help in the processus of validation, LOI's etc…in front of us.
- Same for **combined test beams** especially at FNAL in 2009.
- SiLC intends also to **further exploit synergy/collaboration with other machines and HEP domains**, especially the LHC and its upgrades.
- ***SiLC is following workplan and milestones as anticipated even on more challenging topics.***

SiLC R&D Collaboration

U.S.A

Michigan U.
SCIPP-UCSC

Connections with:
- FNAL (DOE prop 05 funded)UCSC, FNAL, LPNHE
- SLAC (DOE prop 03: funded): UCSC, SLAC Michigan U, LPNHE and meetings SiD
- CERN (collab of bonding Lab+TB infrastructures)

Europe

IMB-CNM/CSIC, Barcelone (SP) *(eudet ass.)*
U.Barcelona (SP)
Helsinki U.(Fi) *(eudet)*
VTT-Finland (Fi)
IEKP, Karlsuhe U. (D)
Liverpool U.
Moscow St. U. , Moscou(Ru) *(eudet ass.)*
Obninsk St. U., Obninsk (Ru) *(eudet ass.)*
LPNHE, Paris (Fr) *(eudet)*
Charles U. , Prague (CZ) *(eudet)*
IFCA/CSIC, Santander(Sp) *(eudet)*
Torino U. & INFN-Torino (It)
IFIC-CSIC Valencia (Sp) *(eudet ass.)*
HEPHY, Academy Sci., Vienna (Au)

Asia

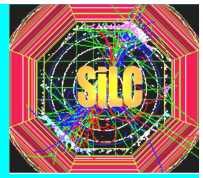
Kyungpook U. Taegu, Ko
Yonsei U., Seoul, Ko
Korea U. Seoul, Ko
Seoul Nat. U., Seoul, Ko
SungKyunKwan U. Seoul
HAMAMATSU (Japan

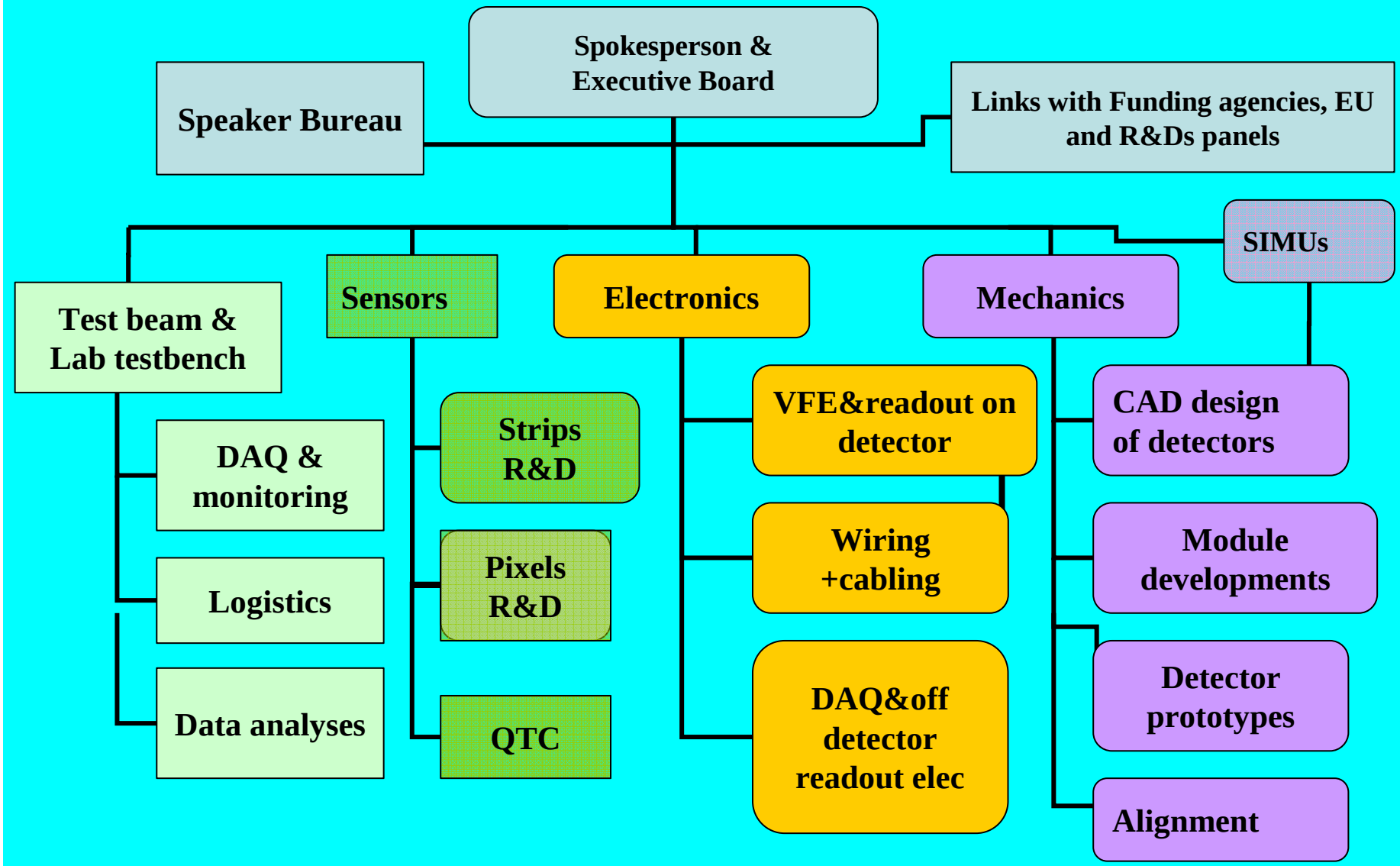
First idea Cracow ECFA-LC Nov 01, Launched 1st ALCPG Chicago Jan. 02, Proposal to PRC May 03, PRC St. R. May 05, Proposal ILCSC R&D Panel at BILCW07 Feb 07, St. R. PRC Ap 08

This brief review tempts to summarize all the SiLC collaborators hard work results: Many thanks to all of them!

Backup slides

List of tasks: flow diagram





SiLC: Current sharing of responsabilities

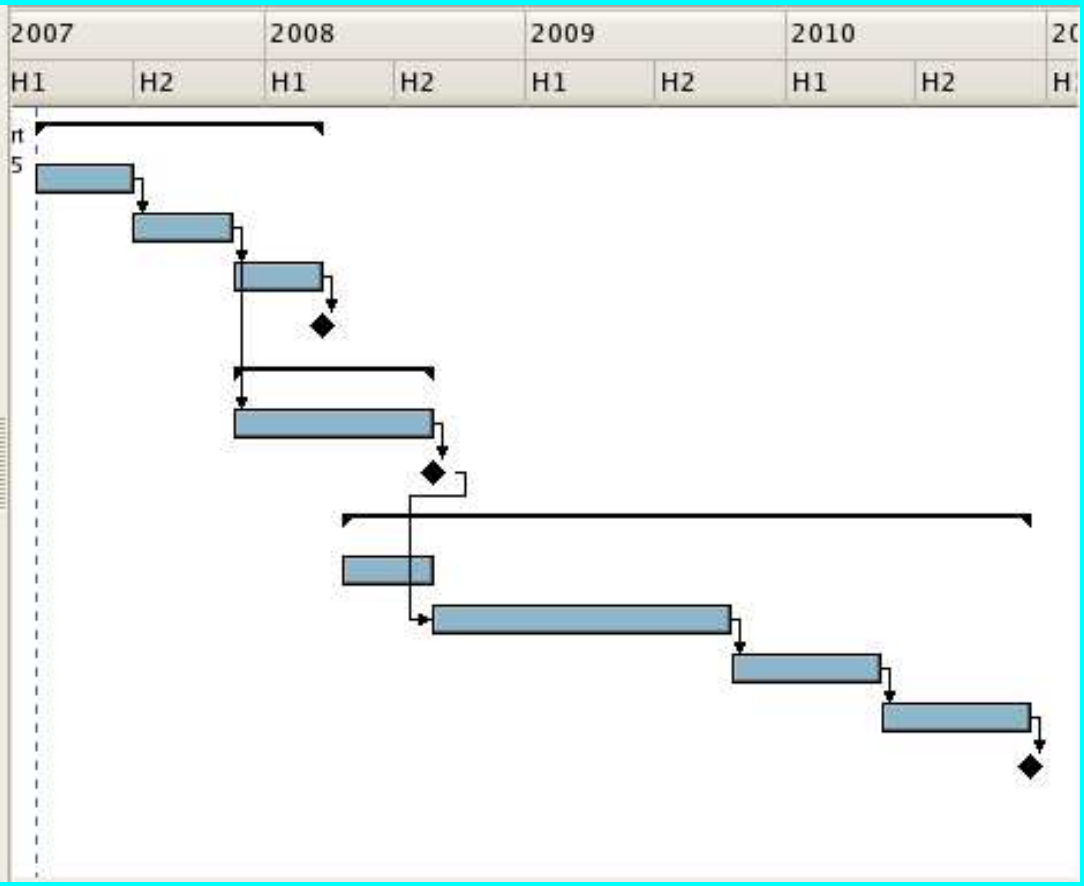
Main topic	*Specific items*	*Coordinator*	*Participating Institutes*
Sensors	**Microstrips**	**HEPHY**	**VTT-HIP, LPNHE, IFCA, Korean group, Liverpool U., HPK-Photonics**
	Pixels-DEPFET	**IFIC**	**CU-Prague,**
	Other	**tba**	**tba**
Electronics	**FE readout**	**LPNHE**	**BU Barcelona, LAPP, SCIPP-UCSC**
	DAQ (DUT)	**LPNHE**	**HEPHY (APV25), LPNHE,**
	DAQ (general)	**IFCA**	**Barcelona U, CU Prague**
Mechanics	**Modules**	**IEKP**	**IFIC, Korean group, Liverpool Uni., LPNHE**
	Prototypes	**tba**	**IEKP, LPNHE, Liverpool U., IFIC, Torino U.,**
	Alignment	**IFCA**	**Michigan U.**
	Cooling	**OSU**	**LPNHE, Torino U., IFIC**
Simulation		**IFIC(M Vos) OSU(Saveliev)**	**CU Prague, HEPHY, IFCA, Korean Group, LPNHE, UCSC**
Test beams	**DESY**	**Z. Dolezal**	**See Table 1 and 2**
	CERN	**A.Savoy-Nav. M. Fernandez**	**See Table 1 and 2**
	FNAL	**tbd**	**Table 1 and 2 + non E.U partners**
	DAQ software	**IFCA+LPNHE**	**tbd + other colabrators (EUDET et al.)**
	Analysis/monitoring tasks	**tbd**	**CUPrague, LPNHE, IFCA**

items	2007	2008	2009
Electronics (FEE)	SiTR_130-1 characterization (*including test beam*)		
	SiTR_130+128ch+pw-cy	Tests Prod. SiTR_130 for	equipping detector protos
		Explore 90nm techno	
		design ≥ 512 best DSM	tests & launch production
	LSTFE_2 full characterization	Pursue Developments on LSFTE + tests	Tests of the LSFTE
Sensors			
µstrips + thining	investigate 8" ssd wafers	Mini series equip proto	Production for prototypes
	investigate µseries/ test		
Pixels	MC Studies define	specs see details	In Gant diagram (next)
Chip-on-µstrip detector	Bump bonding preparation and feasibility tests	1st proto tests	small quantity production
Mechanics			
Elementary module	Construction proto following	evolution and success in ap	plying related technologies
Prototype construction	1st proto	test beam proto & keep	evolving the techno
Alignment	feasibility studies	test beam proto & keep	evolving the techno
Cooling	feasibility studies	test beam proto & keep	evolving the techno
Test beam (EUDET)	Modules + 1st larger proto	Large proto & combined t.b.	Combined t.b, cont'd
Simulation deviopments	Pattern recognition & full Reconstruction by end 07	Continue simulation developm	ents & performance studies

List of priorities, milestones and schedule as given to the ILCSC Tracking panel 07

Detailed workplan, milestones and schedule for the pixel R&D from proposal to te ILCSC Tracking panel in 07

WBS	Name	Work
1	**Study of specifications**	**287d**
1.1	Study of machine BG	97d
1.2	Determine cell size	100d
1.3	Optimize Layout	90d
1.4	Define specifications	N/A
2	**Technology**	**200d**
2.1	Study of diferent solutions	200d
2.2	Choose baseline technology	N/A
3	**Prototype**	**690d**
3.1	System studies	90d
3.2	Module design, component id.	300d
3.3	Construction of simple modules	150d
3.4	Multimodule operation	150d
3.5	System test demonstrator	N/A



SiLC R&D collaboration meetings

SiLC collaboration started with regular collaboration meetings at ECFA ILC Workshop, Vienna Nov'05. Quite fruitful so far.

Next ones in 2008:

- Moscow, end of May
- Santander, Mid December