

Low Power RF (LLRF) Part III

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Lecture Schedule (March 2008)

- LLRF Part I (Requirements and Design)
 - March 6, 13:30
- LLRF Part 2 (Maschine Studies at FLASH)
 - March 7: 10:00
- **LLRF Part 3 (LLRF for the XFEL)**
 - **March 11 at 13:30**
- Timing and Sync. Part I (Concepts)
 - March 14 at 10:00
- Timing and Sync. Part II (Design)
 - March 17 at 10:00
- European XFEL (Project Overview)
 - March 26 at 13:30

Outline LLRF Part III

- LLRF Requirements for the XFEL
- Comparison of Crate Standards
- Architecture of LLRF System
- Hardware
 - ATCA Carrier
 - AMC Mezzanine Cards
 - Communication links
 - IPMI, diagnostics
 - Piezo driver and piezo control
 - Downconverter
 - MO and Distribution

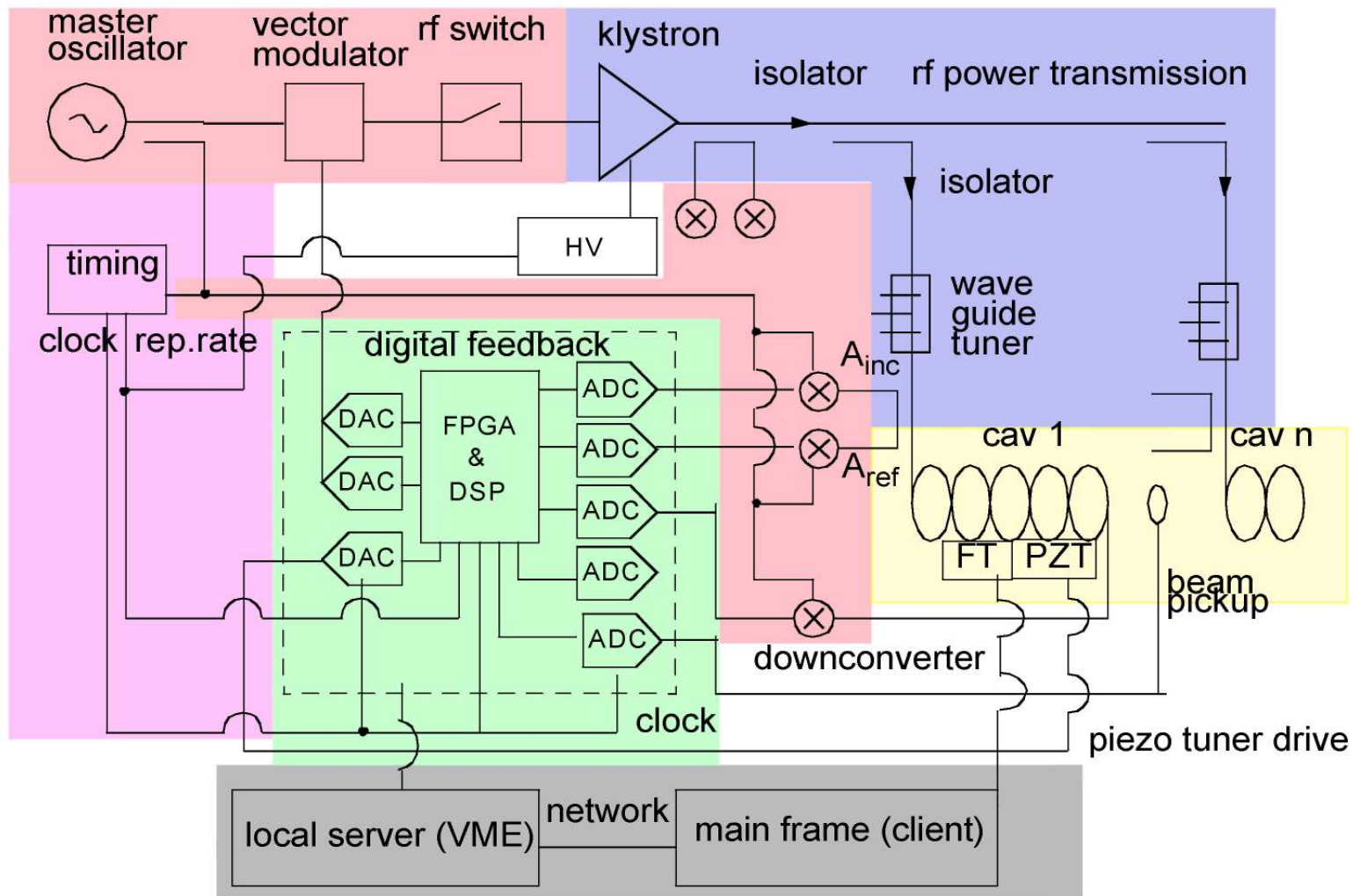
Outline LLRF Part III (C'tnd)

- Software Architecture
- Software
 - Controller (Warsaw)
 - Controller (Lodz)
 - Controller (DESY)
 - Low Level Applications
 - High Level Applications
 - Automation
 - LLRF Servers
- **Summary of LLRF Review**

LLRF Requirements for the XFEL



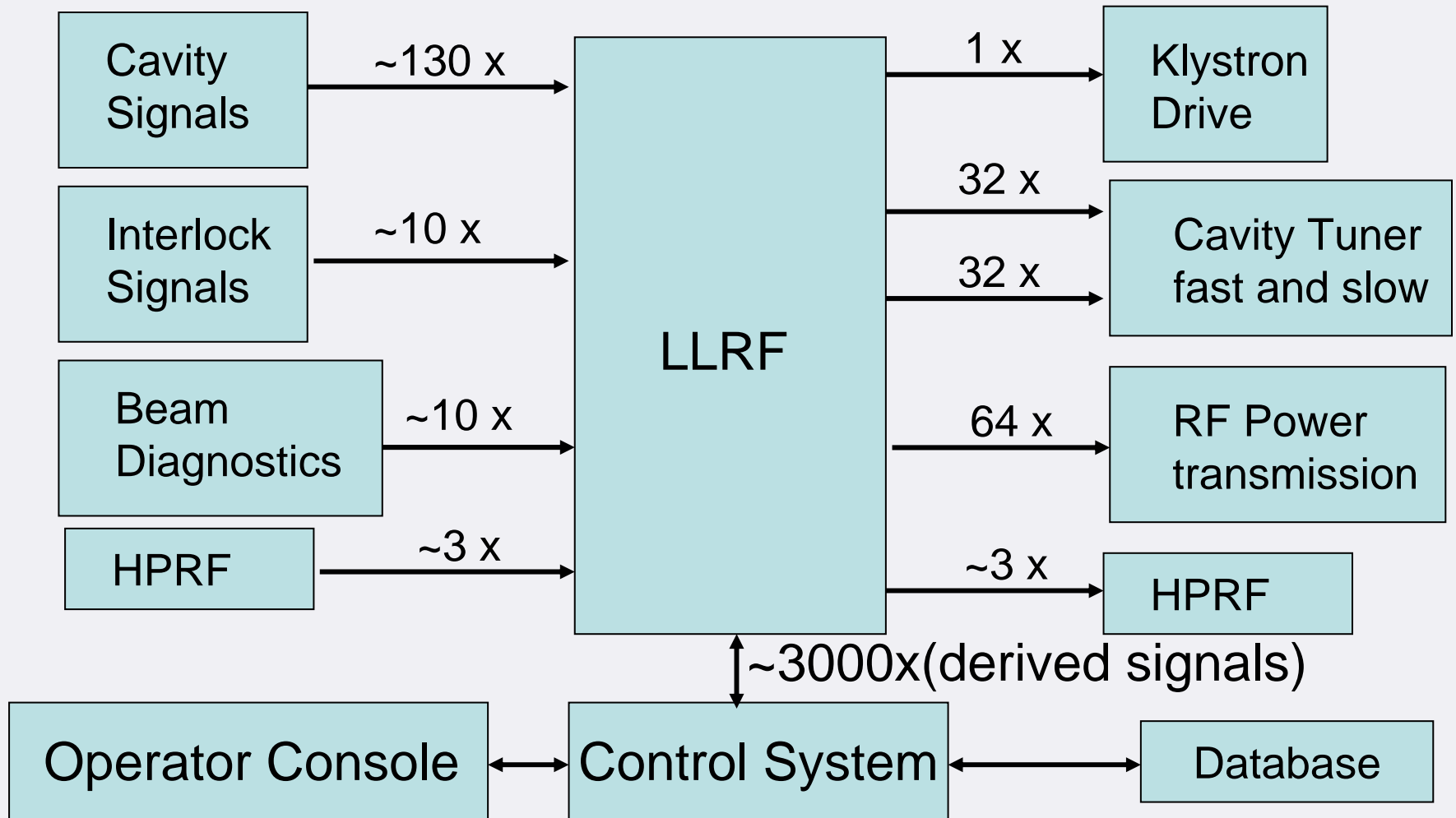
System Architecture Details



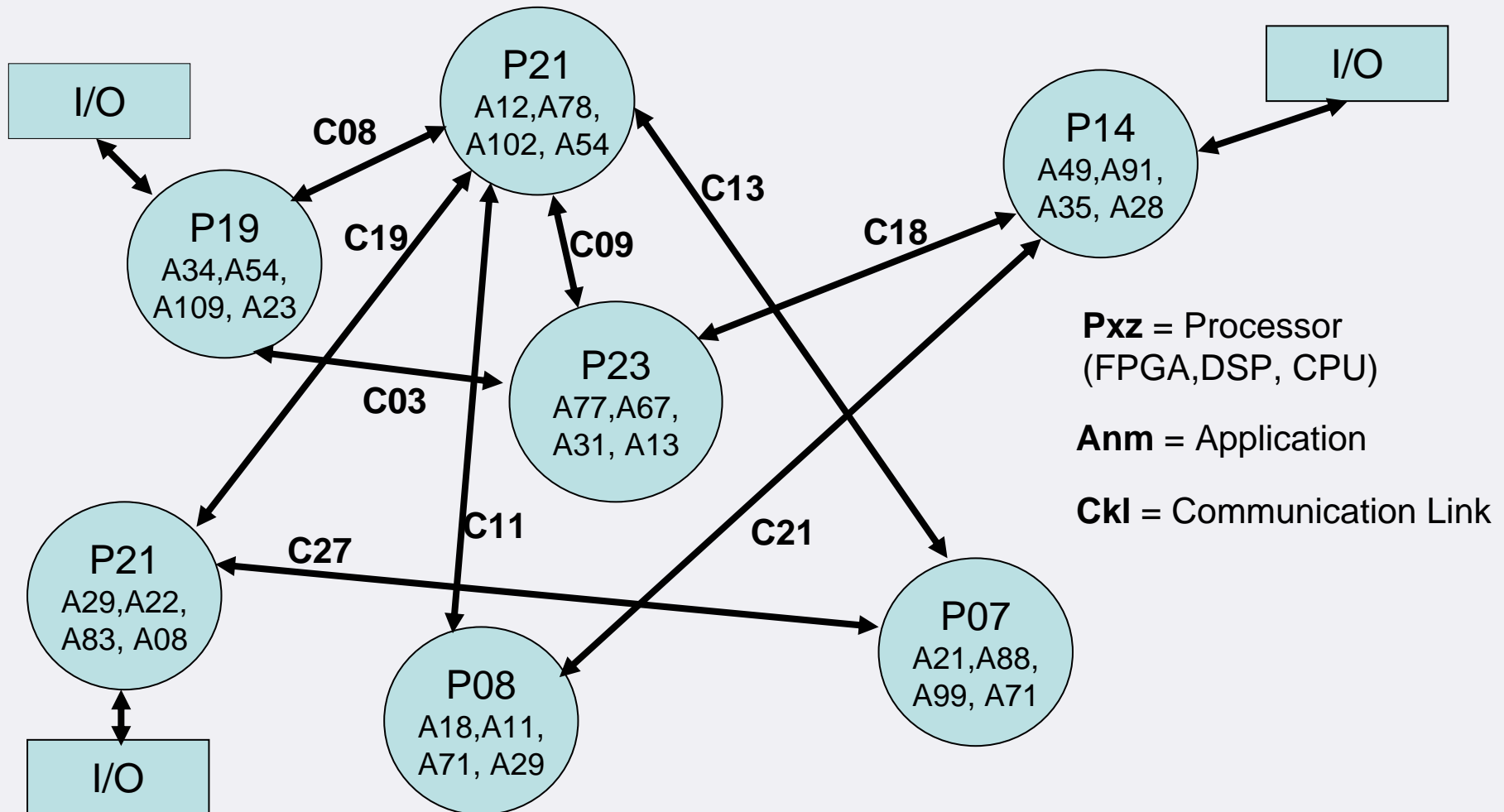
Subsystems

- | | |
|--|---|
| <ul style="list-style-type: none"> o RF phase reference <ul style="list-style-type: none"> - from main driveline - LO for downconverter o Timing System o Vector modulator o Downconverter o Digital Control (Fdbck + FF) <ul style="list-style-type: none"> - ADC, DSP, DAC - includes exception handling - Redundant simple feedforward - Redundant monitoring system o Transient detection o Interfaces to other subsystems <ul style="list-style-type: none"> - includes interlocks | <ul style="list-style-type: none"> o Waveguide tuner and controls o Cavity resonance control <ul style="list-style-type: none"> - slow (motor) tuner - fast (piezo) tuner o CPU in VME crate o Network to local controls o Cabels and connectors o Power supply for electronics o Airconditioning in racks o Software <ul style="list-style-type: none"> - DSP (FPGA) code - Server programs - Client programs - LLRF Parameters - Finite State Machine |
|--|---|

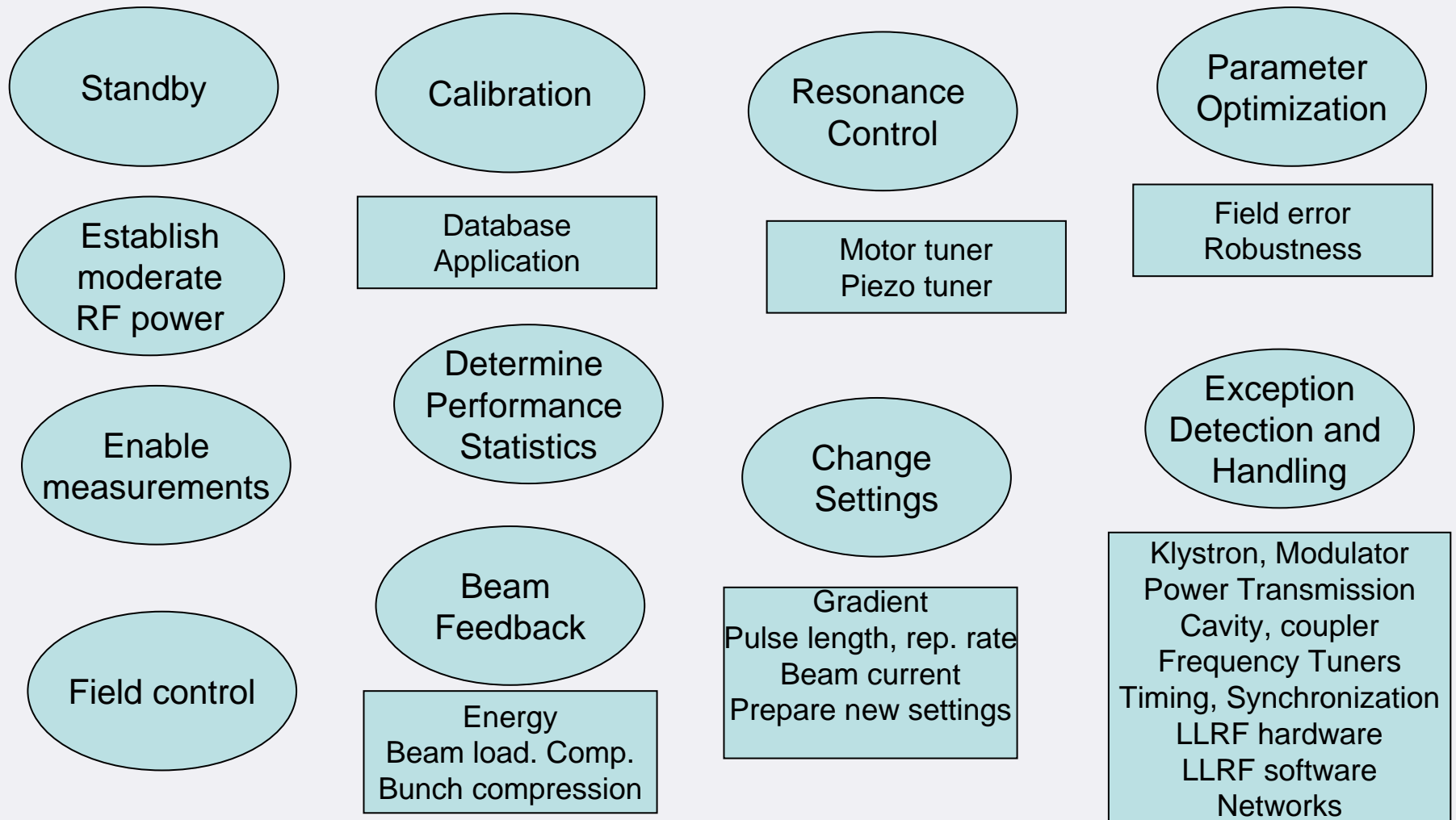
Signal diagram for RF Control (1 RF Station)



Challenge for Software Development



Use cases for LLRF System (RF Station)



RF System Requirements

- Maintain **Phase** and **Amplitude** of the accelerating field within given tolerances to **accelerate** a charged particle beam to given parameters
 - **up to 0.02% for amplitude and 0.01 deg. for phase**
- Minimize **Power** needed for control
 - RF system must be **reproducible, reliable, operable, and well understood.**
- Other performance goals
 - **build-in diagnostics** for calibration of gradient and phase, cavity detuning, etc.
 - provide **exception handling** capabilities
 - meet performance goals over wide range of operating parameters

LLRF Requirements (C'ntd)

- **Availability**
 - not more than 1 LLRF station failure / week
 - SEU tolerant
 - Redundancy of LLRF subsystems
 - ...
- **Operability**
 - “One Button” operation (Automation)
 - Application assist operators and rf experts
 - Automated calibration of vector-sum
 - ...
- **Reproducible**
 - Restore beam parameters after shutdown or interlock trip
 - Recover LLRF state after maintenance work
 - ...

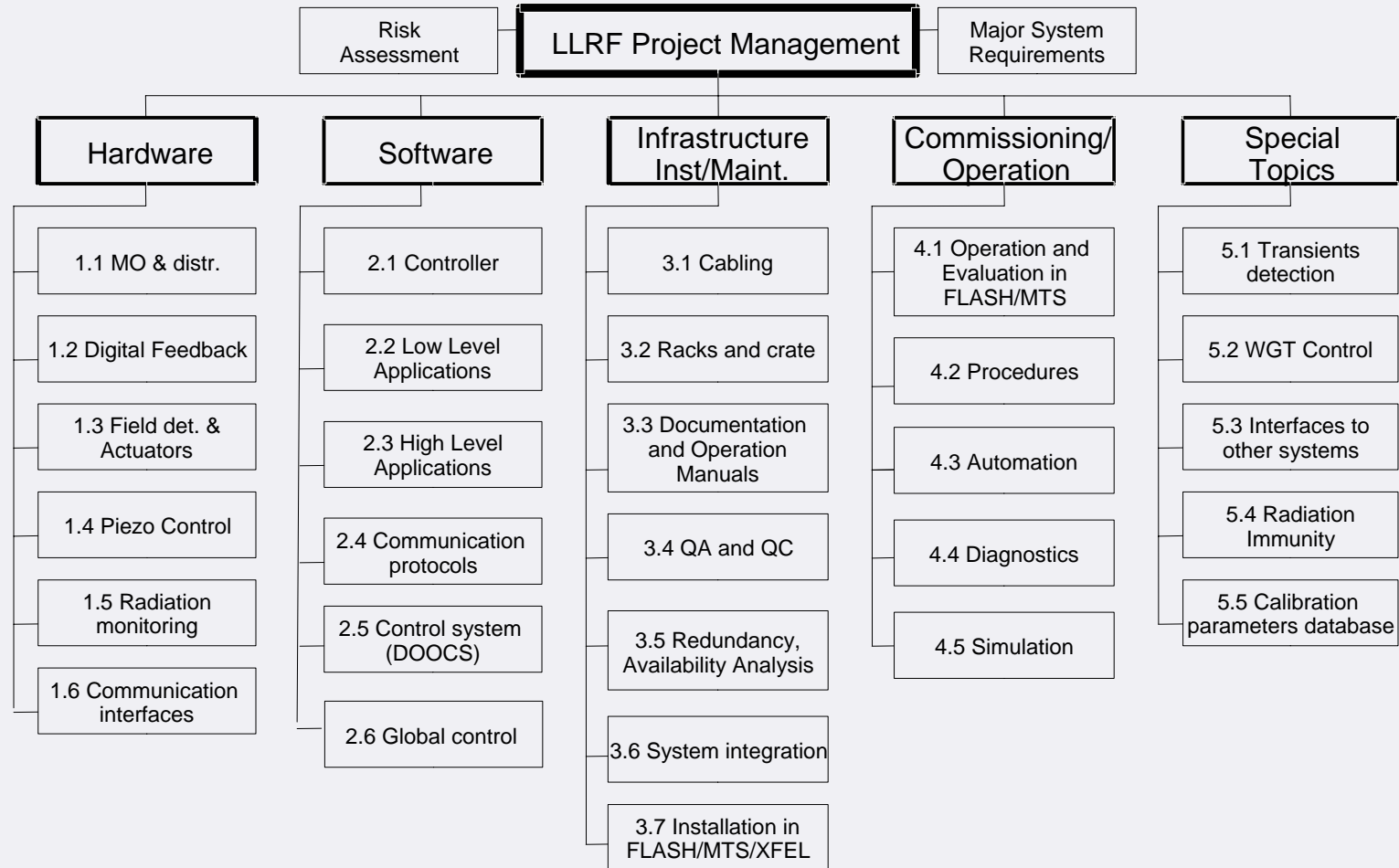
LLRF Requirements (C'ntd)

- **Maintainable**
 - Remote diagnostics of subsystem failure
 - “Hot Swap” Capability
 - Accessible Hardware
 - ...
- **Well Understood**
 - Performance limitations of LLRF fully modelled
 - No unexpected “features”
 - ...
- **Meet (technical) performance goals**
 - Maintain accelerating fields - defined as vector-sum of up to 32 cavities - within given tolerances
 - Minimize peak power requirements
 - ...

Improvement of the FLASH LLRF for the XFEL

- Field regulation :
 - Short term: Improve by factor 3 (0.03 deg. \rightarrow 0.01 deg.)
 - Phase drifts: Improve by factor 10 (2ps \rightarrow 0.2 ps)
- Need modular design with high availability (HA):
 - Upgradeability, maintenance
 - Useable by other WP, support collaborative efforts
- Automation
- Diagnostics
- Documentation (initially: good requirements are needed, then concepts, design, acceptance tests)

New WBS for LLRF for the XFEL



Main LLRF Requirements for the XFEL

1. Provide settability of voltage and phase to the desired values in all 4 quadrants up to a klystron peak power output level of $0.9 \cdot P_{\text{sat}}$.
2. Maintain stability of voltage and phase of the calibrated and high precision vector-sum of individual rf stations within given tolerances for the range of useable operating parameters.
3. Provide highly stable rf references at specified frequencies at selected locations. Includes calibration reference signals.
4. Provide adequate interfaces to other accelerator subsystems.
5. Diagnose faulty or missing hardware and software and localize areas of functional and technical performance degradation including severeness of degradation. For use by operators and experts.

Main Requirements for the XFEL (Cnt'd)

6. Optimize and/or limit operational and system internal parameters such that the performance function based on rms field stability, accelerator availability, and component lifetime is maximized.
7. Provide a simulation mode, where the klystron-cavity system is replaced by a simulator and which provides performance predictions for planned parameter changes.
8. Provide a high degree of automation of operation to assist the operator and system experts.
9. Provide calibration functions for selected signals.
10. Provide low and high level applications supporting automation.
11. Provide exception detection and handling.
12. Provide operating modes for rf system conditioning (ex. coupler and cavity).
13. Support rf system and accelerator commissioning procedures.

Basic and Advanced Use Cases for RF Station

Basic Use Cases

- Establish moderate RF power and cavity gradients
- Enable and perform measurements of all LLRF relevant signals
- Stabilize fields for beam operation

Advanced Use Cases

- Optimize parameters for best beam stability
- Set parameters to maximize availability during beam operation
- Tune or detune cavity from/to completely detuned state
- Assess performance and performance limitations of rf station
- Diagnose problems and identify the source (hardware/software)
- Detect and handle exceptions

Examples for Scenarios

1. Coarse tuning of cavity resonance with motor tuner
2. Compensate Lorenz force detuning
3. By-pass/un-bypass cavities (to/from completely detuned state)
4. Adjust klystron HV for sufficient power margin
5. Set correct timing
 - .. rf gate, rf pulse, klystron HV, flat-top with respect to beam
6. Limit field emission in cavities
7. Apply adaptive feedforward
8. (Re)-start missing or faulty llrf servers
9. (Re)-calibrate rf station
10. Calibrate vector-sum at full beam loading
11. Calibrate downconverter

Non-Functional Requirements

- **Field control** (up to 0.02% for amplitude, 0.01 deg. for phase)
 - for vector-sum of each rf stations
 - intra-pulse and pulse to pulse (0.03 deg. for several minutes)
 - Long term drifts are corrected by beam based feedback
 - Vector-sum calibration to 1 deg. in phase and 1% in amplitude
 - Adjust incident phase to ± 3 deg.
 - Adjust loaded Q to $\pm 2\%$
- **Resonance control**
 - Coarse tuning (motor tuner) to 0.2 BW
 - Fast tuning (Pietzotuner) to 0.1 BW (LF detuning)
- **Calibration of downconverter with reference signal**
- **Provide frequency and phase reference to llrf and other subsystems.**

Non-Functional Requirements (Cnt'd)

- **Electronics (racks, crates, boards, and cabling)**
 - Crate and board standard compatible with control system
 - Must tolerate moderate levels of radiation (n and gamma)
 - Modular design to facilitate maintenance/upgrades
 - Fulfill european standards for electrical safety
 - Crate cabling only from rear possible
 - Installation compatible with racks with no rear access
- **Interfaces to other subsystems**
 - Machine protection and personnel safety
 - Control system
 - HPRF, Cryo, vacuum, cavities, couplers

Crate standard related requirements

- Support ~100 ADC measurement and ~100 DAC control channels with significant data processing capability
 - Sampling rate up to 100 MHz at 14 bit (desired 16) resolution
 - Latency from ADC input to DAC output not to exceed 500 ns (desired < 250 ns)
 - Complex data processing
 - <250 ns for real time feedback in FPGAs
 - 1-10 us for intrapulse measurements
 - <50 ms between pulses
- Support centralized and distributed architecture
 - Requires high bandwidth/low latency communication links
- Scalable

Crate standard related requirements (Cnt'd)

- Modular design
 - Carrier boards with mezzanine cards (5-10 types)
- Maintainable
 - Build-in diagnostics (IPMI, and for all boards)
 - hot-swap
 - Long lifetime of standard and availability of boards
 - Easy access
- Upgradable
- High availability
 - Redundancy supported by hardware and software
 - Rear and front panel IO (few hundred high quality IO channels)

Functional Requirements

- Measurements
 - Signals
 - conditions
 - Components characterization
- Control actions
- Diagnostics
- Warning and fault detection
- Generate events
- Exception detection and handling
- Automation (of operational procedures)

Functional Requirements (Cnt'd)

- Measurements (Examples)
 - Cavity gradient and phase (calibrated)
 - Incident and reflected power (calibrated)
 - Detuning and loaded Q
 - Loop phase and loop gain
 - Klystron linearity characterization
 - Beam phase and beam current
 - ...

Functional Requirements (Cnt'd)

- Control actions (Examples)
 - set loop phase, calibrate loop gain
 - set loaded Q and cavity detuning
 - set klystron HV, adjust bouncer timing
 - Calibrate downconverter (every pulse)
 - rf and/or beam inhibit
 - klystron linearization
 - Adaptive feedforward
 - ...

Functional Requirements (Cnt'd)

- Exception detection and handling (Examples)
 - Quench
 - Field emission
 - Operational limit exceeded
 - Klystron saturated
 - Cavity severely detuned
 - Board temperature high
 - ...

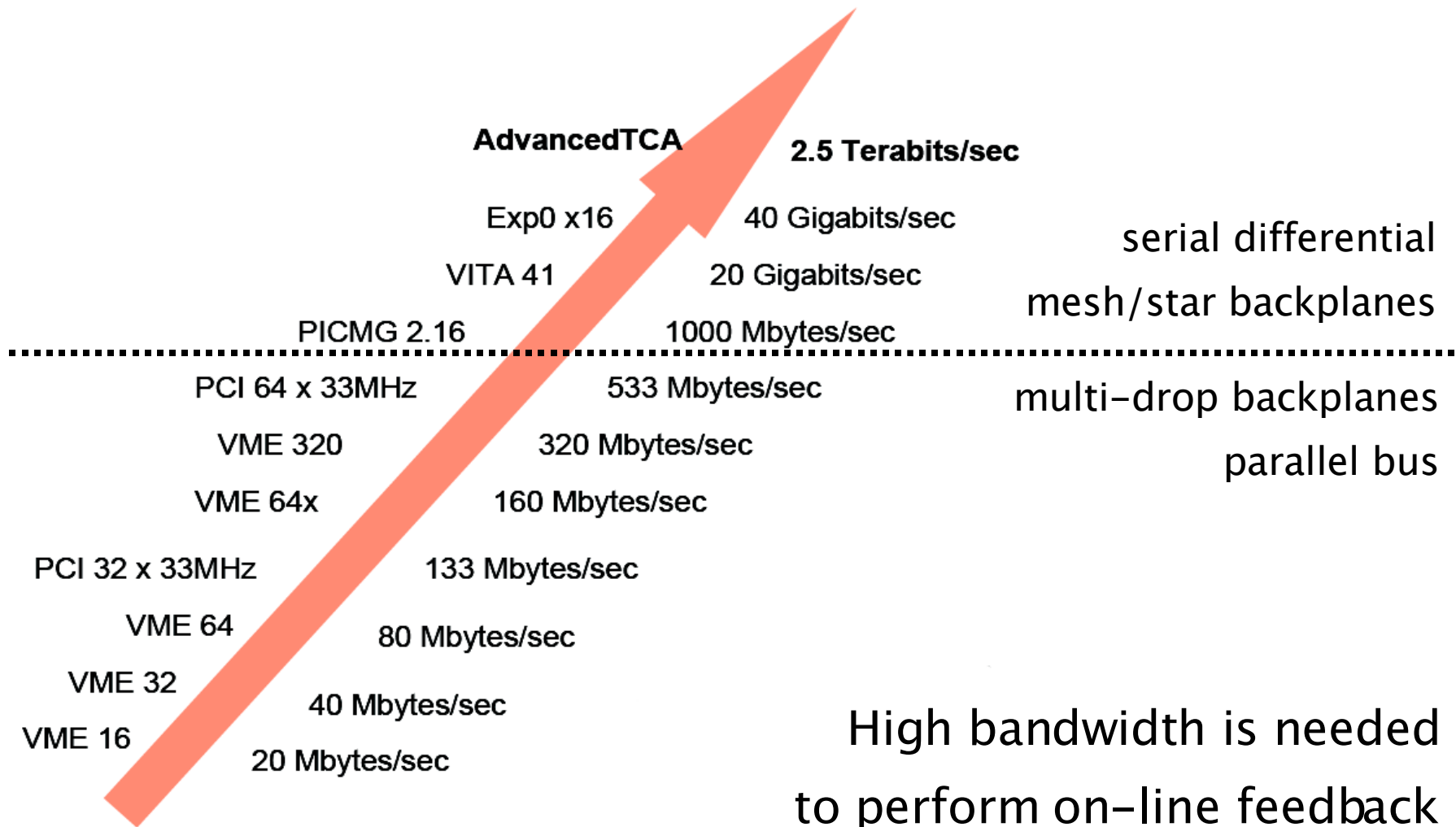
Comparison of Crate Standards



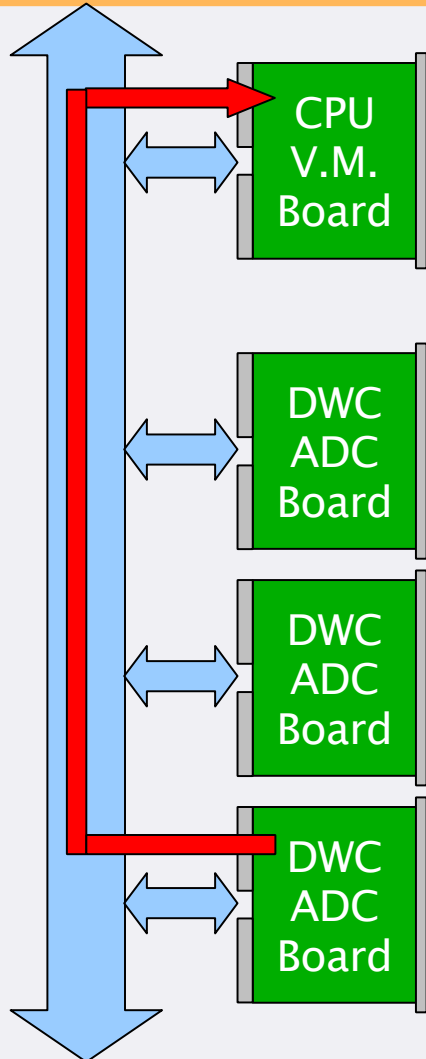
LLRF Requirements for crates

- Multi channel control require concentration of large amount of analog signals (today 14–16 bit each) in one place, due to perform vector sum calculation. There will be 96 signals per one klystron in X-FEL – it must be multi-board system (crate needed)
- To reduce number of boards in the crate, large sized PCB boards are preferred
- Since signals are distributed over several ADC boards, crate must provide fast communication on backplane to handle on-line feedback
- Crate must be a reliable platform for electronics, to achieve high availability of LLRF systems, and whole machine.

Crates evolution- bandwidth



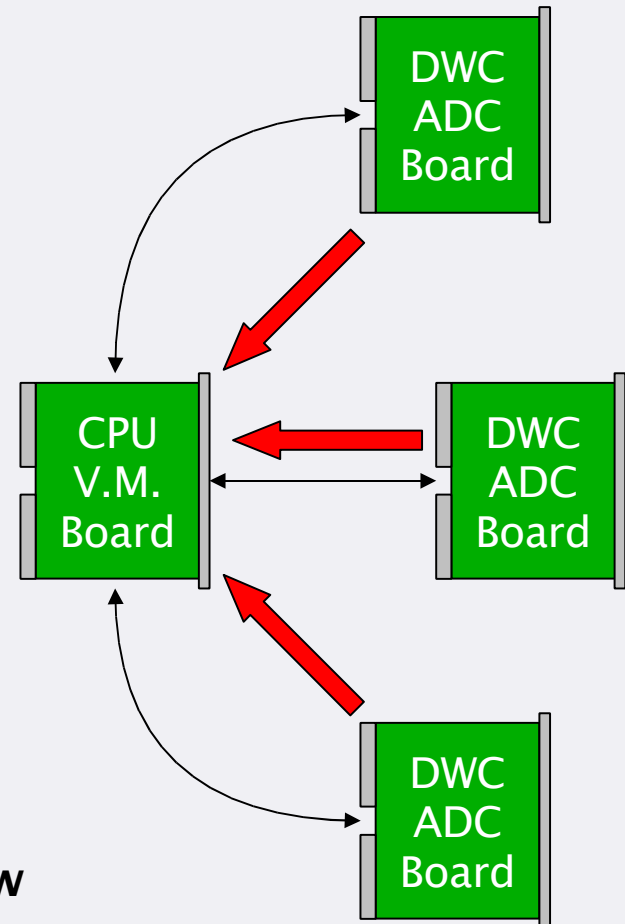
Multi-drop bus vs. Star/Mesh in LLRF



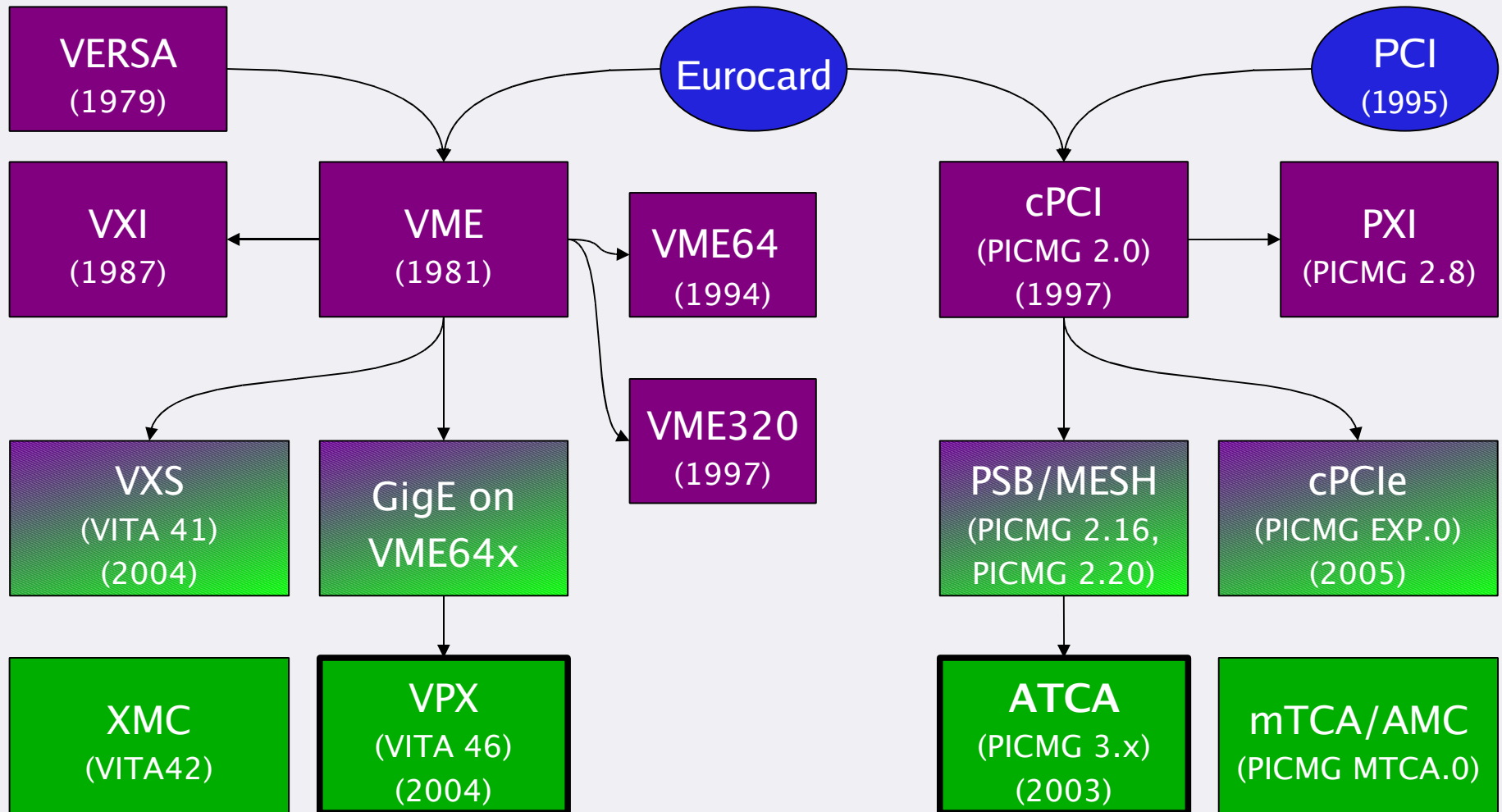
In multi-drop bus,
only one ADC board can
send data for vector sum
calculation, at same time.

In mesh or star topology
ALL ADC boards can send
data simultaneously to the
processing unit.

**This is needed to make low
latency feedback.**



Crate standards, history and overview



Architecture of LLRF System

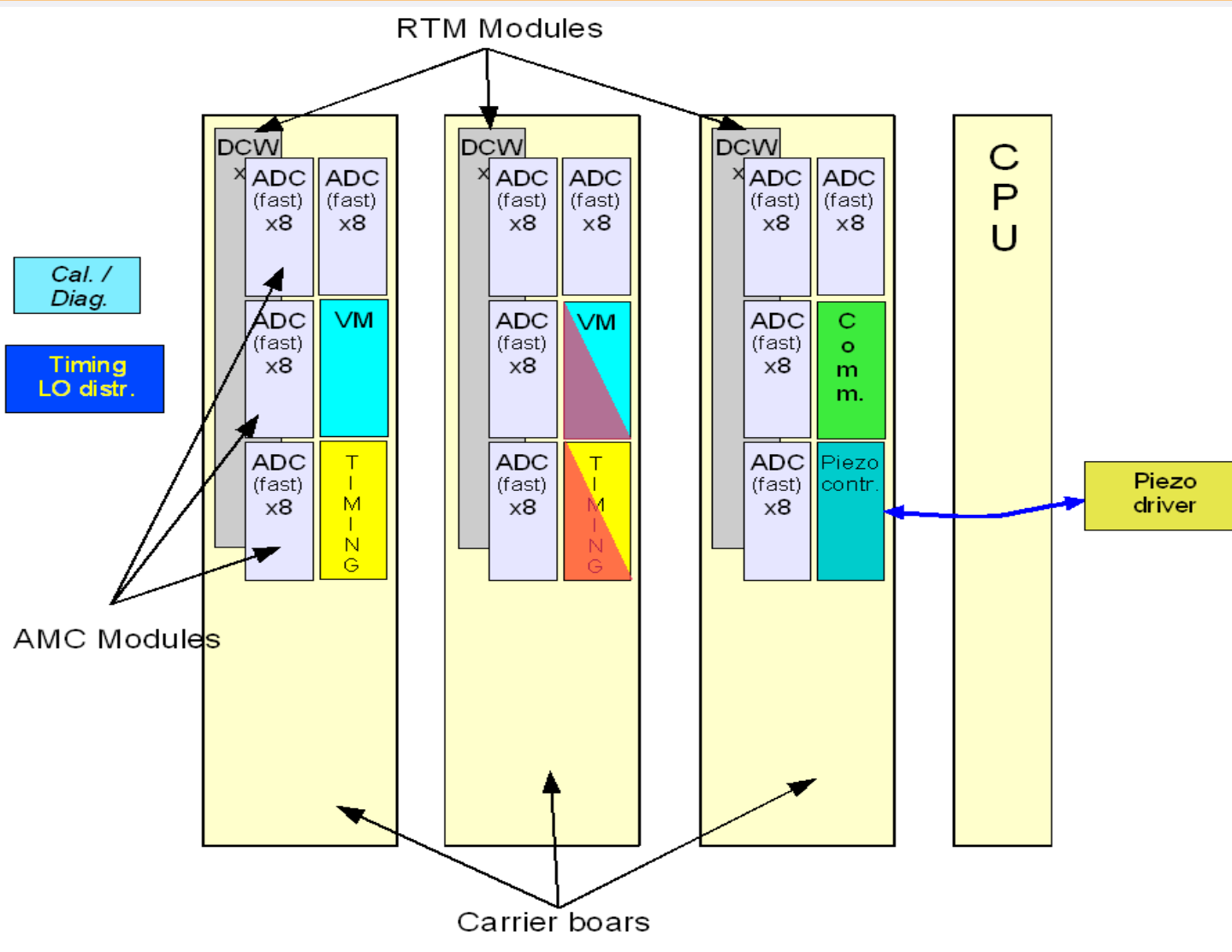


Requirements (technical)

One RF Station

- ★ 96 analog inputs 1.3 GHz, 0dBm
 - Isolation better than 50 dB
 - ADC 14 bits resolution, SF 40-100 MHz
 - Clock stability > 5 ps rms
- ★ RF drive output 1.3 GHz, 0dBm
- ★ Interface to the interlock system
- ★ System latency < 500 ns
- ★ Low latency links to other modules
- ★ 6 different clocks must be available (stability > 5ps rms)
- ★ Partial redundancy

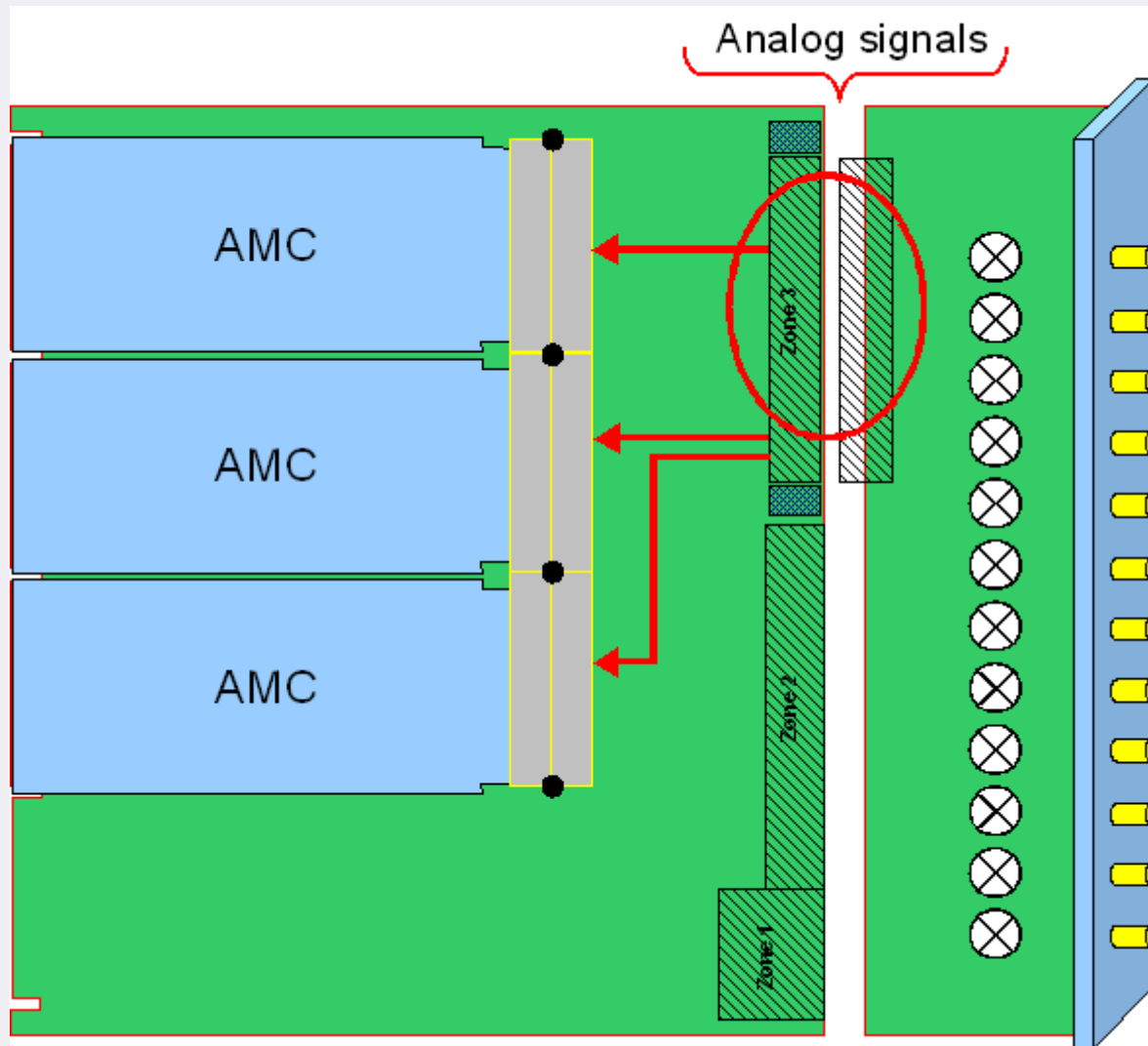
Concept – modular system based on ATCA



Problems:

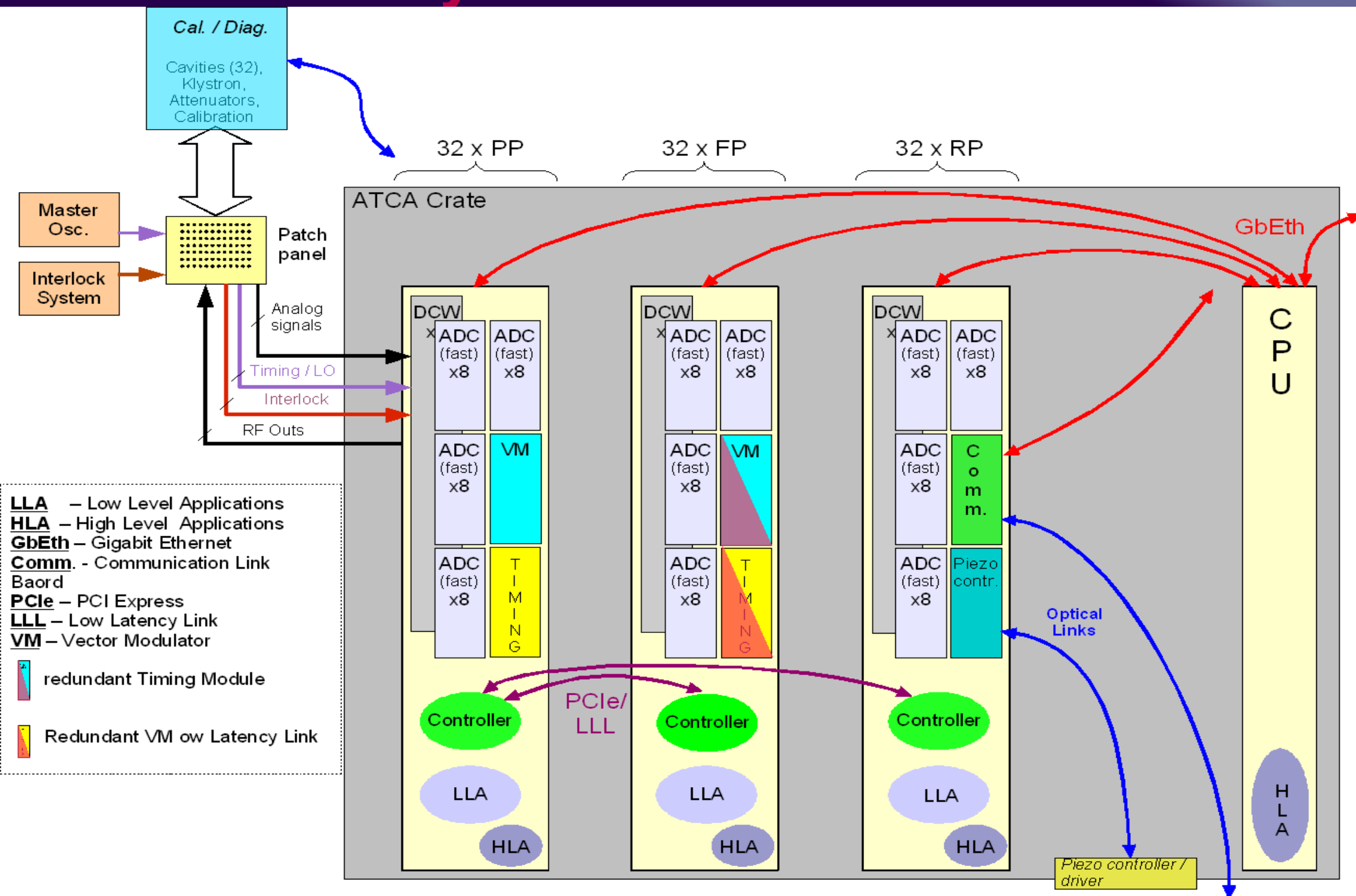
- analog signals in ATCA are not defined
- no analog I/Os connected from rear

Analog signals in ATCA



- Connections to the ATCA carrier board through RTM module
- Analog signals must be routed from Zone 3 to AMC modules

[illegible]



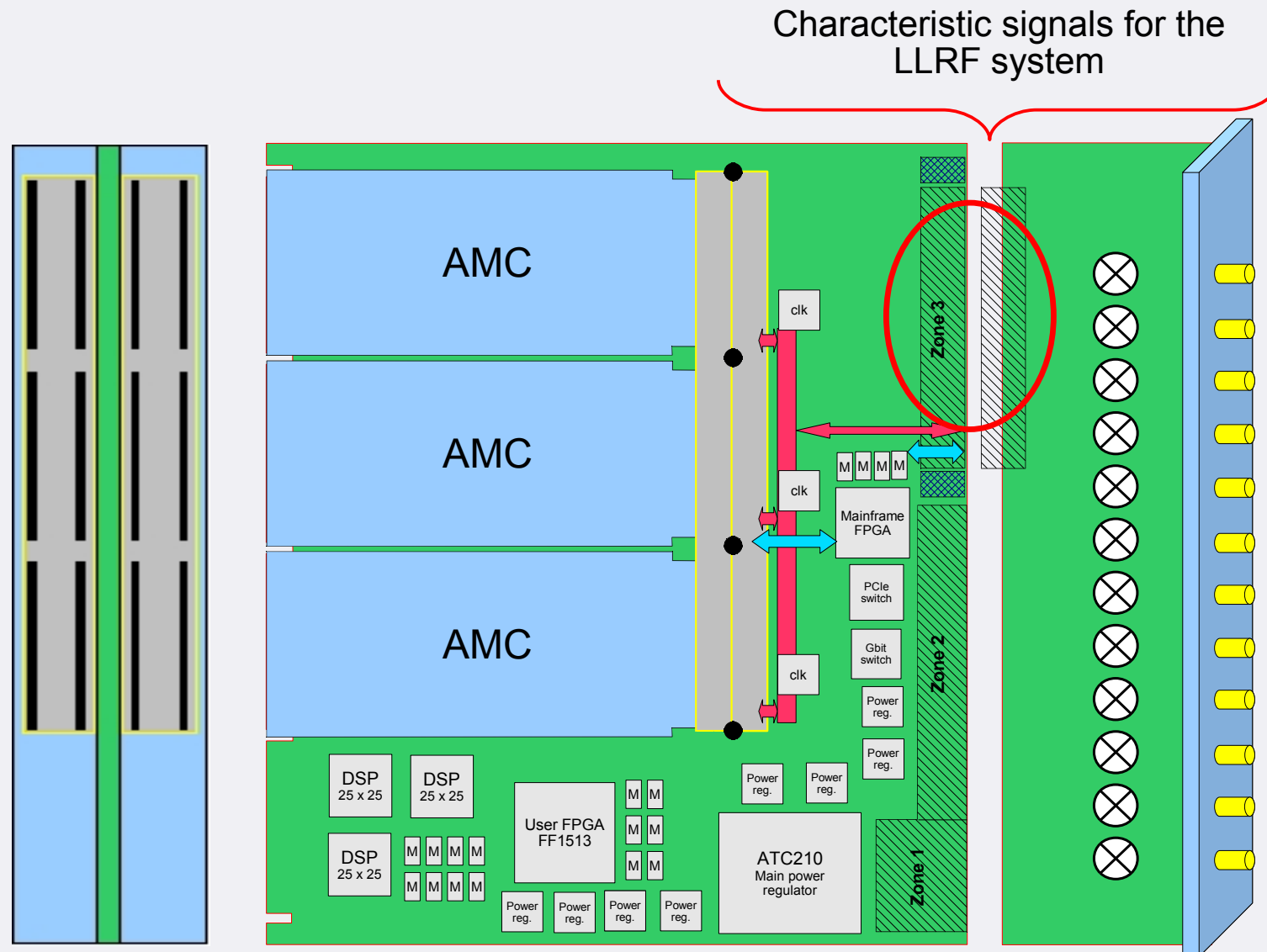
ATCA Carrier board



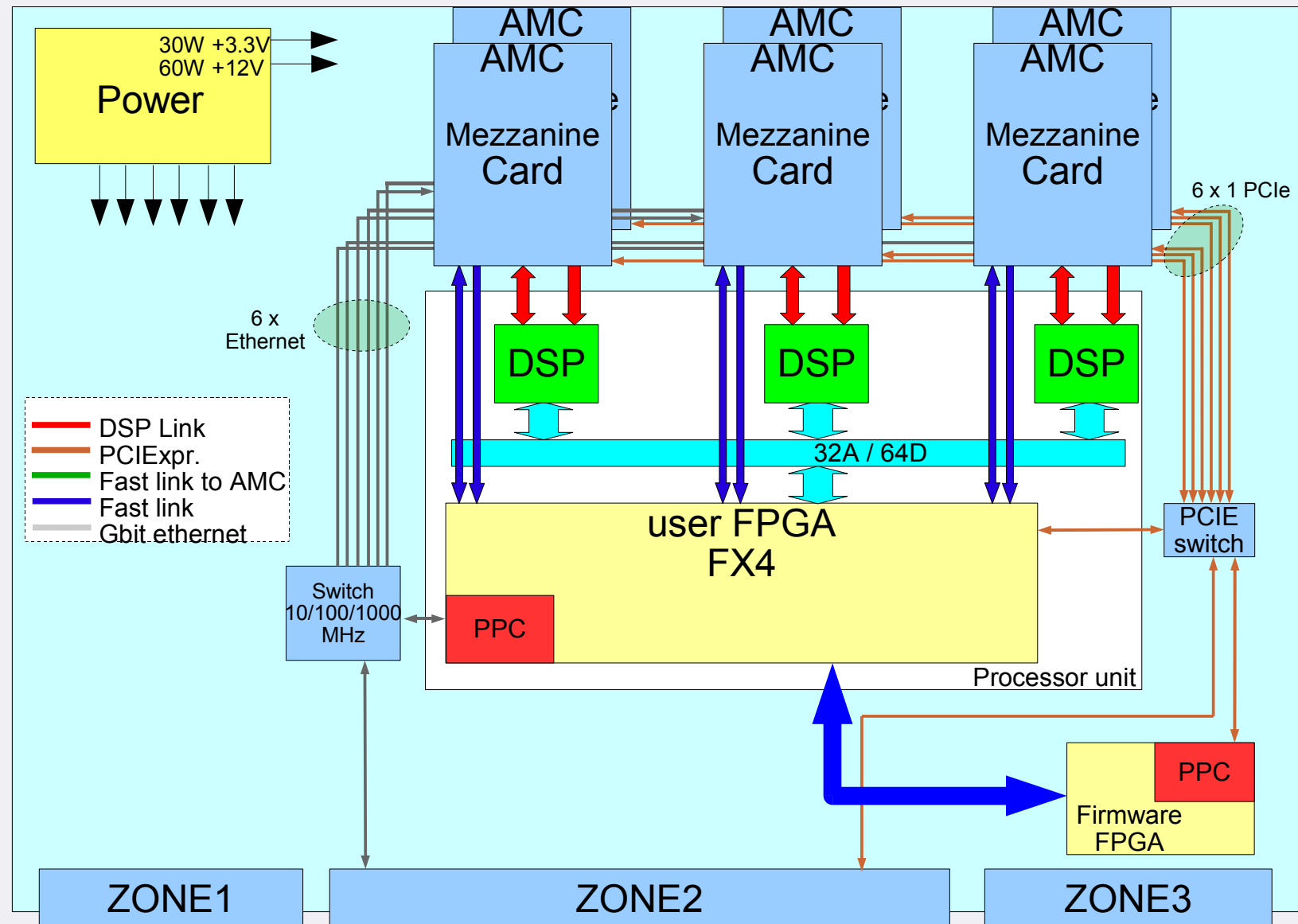
Requirements

- 6 x AMC bay compatible with AMC.1 and AMC-DESY specification
 - inputs:
 - sinusoidal signal IF (1-50 MHz) or RF 1.3 GHz, 0 dBm
 - sinusoidal signal RF 1.3 GHz, 0 dBm
 - sinusoidal signal RF 2.6 GHz, 0 dBm
 - 8 digital interlock signals
 - outputs
 - sinusoidal signal RF 1.3 GHz, 0 dBm
 - inputs/outputs:
 - 3 x clock B-LVDS (5 ps rms)
 - 3 x trigger B-LVDS (5 ps rms)
 - 10 differential lines for Low Latency Protocol (custom)
- Signals provided to AMC bays vi Zone 3 (RTM Module)
 - all signals mentioned above (for AMC bays)
- Clock signals distribution on board
- Floating Point Processor for Low Level Applications
- User FPGA for controller

Carrier board - concept



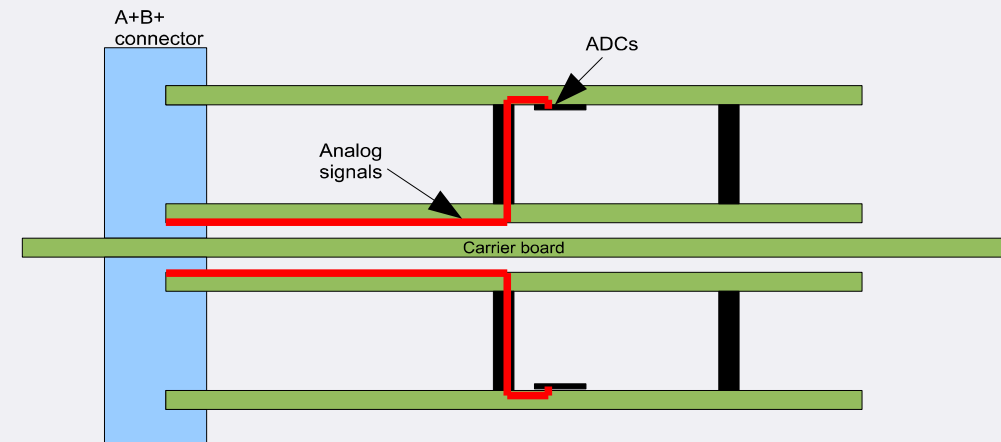
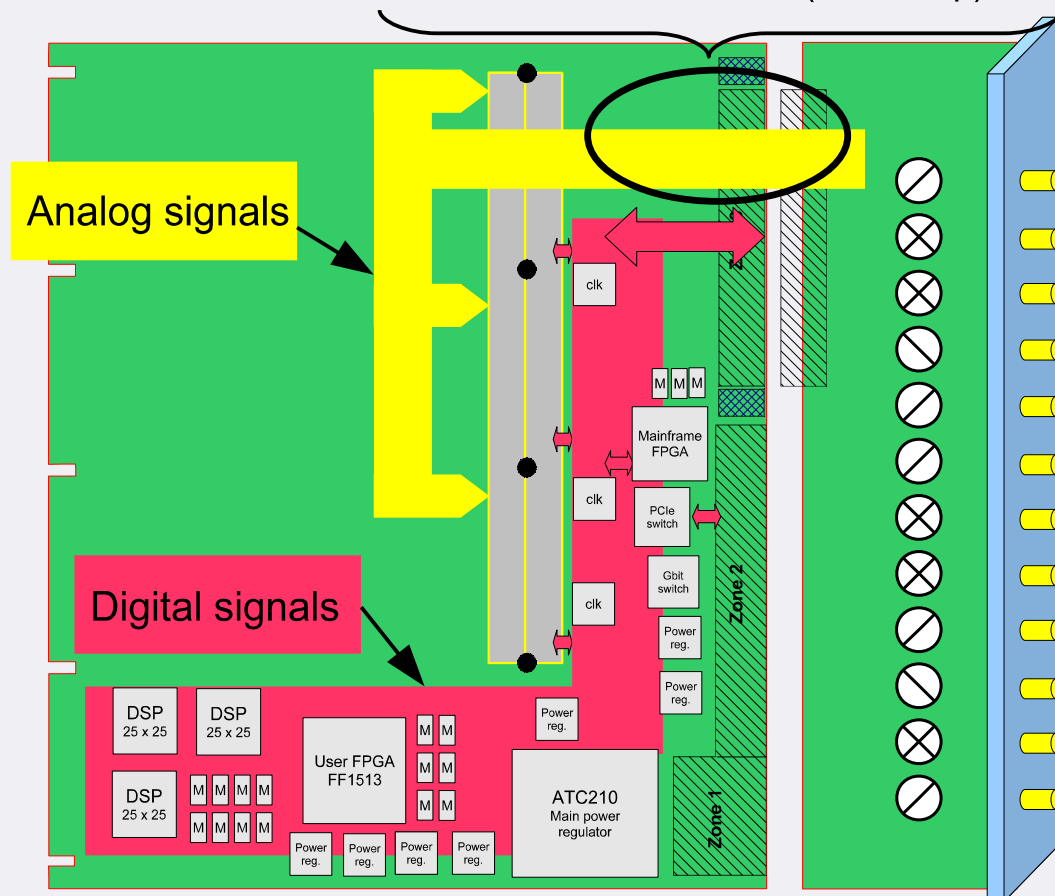
Block diagram - communication



Analog signals

- 6 x 10 differential lines for IF (p-t-p)
- 6 RF output 1.3 GHz for VM
- reference clock – 1.3 GHz (multi drop)
- coded clock – 2.6 GHz (multi drop)

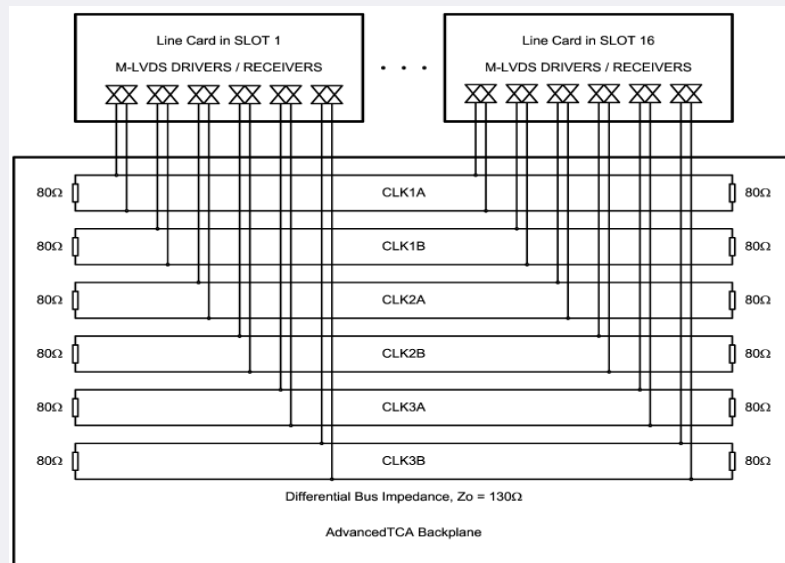
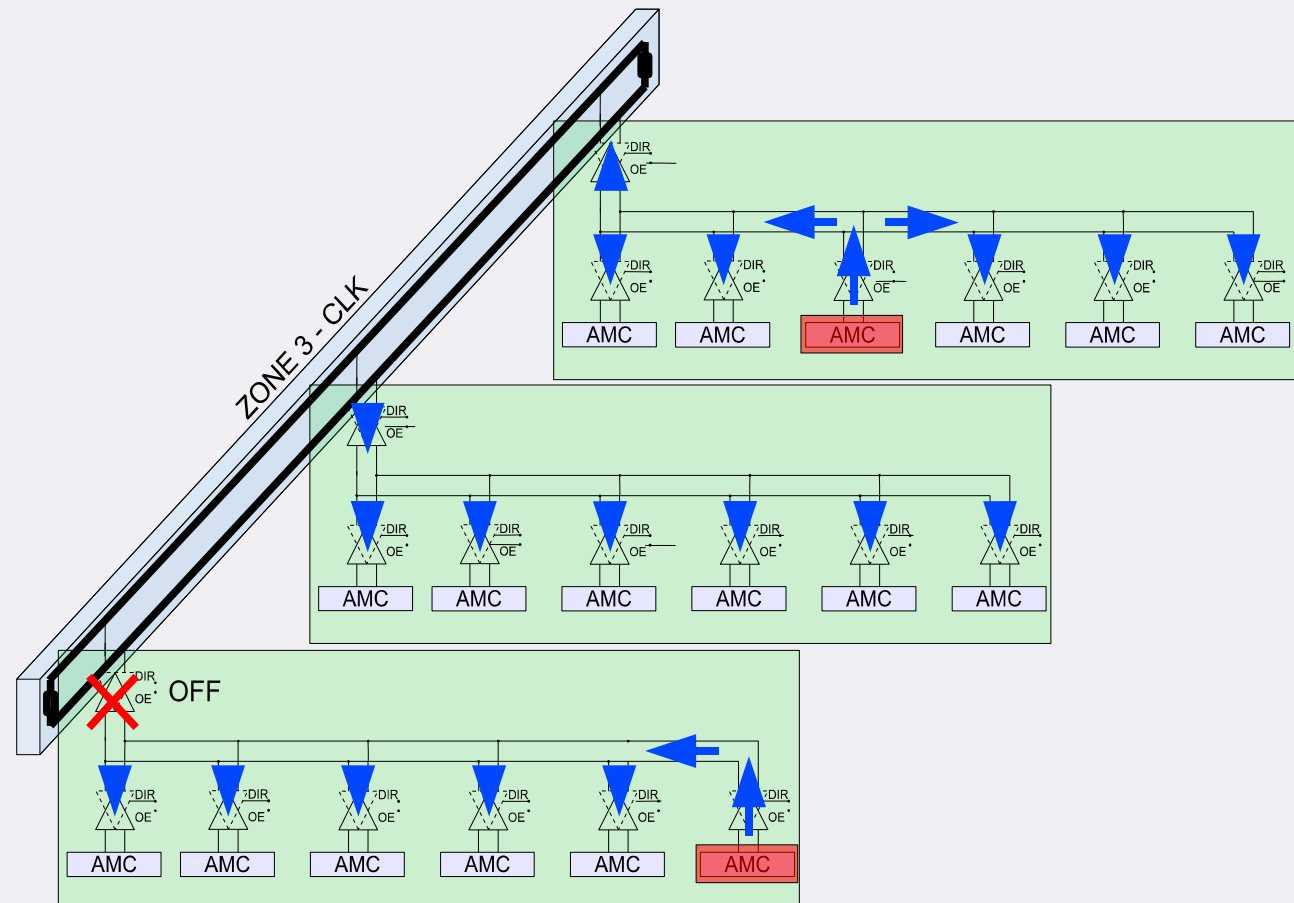
- Analog and digital lines are separated
- For analog signals and fast digital lines strip-lines are designed



Timing distribution

3 x clock & 3 x trigger signals generated at any AMC slot must be distributed to each AMC slot and others carrier boards

- LVDS bus
- ★ bidirectional buffers
- ➔ OE
- ➔ DIR



AMC Mezzanine Cards



AMC specification

Advanced Mezzanine Cards are printed circuit boards (PCBs) that follow a specification of the PCI Industrial Computers Manufacturers Group (PICMG).

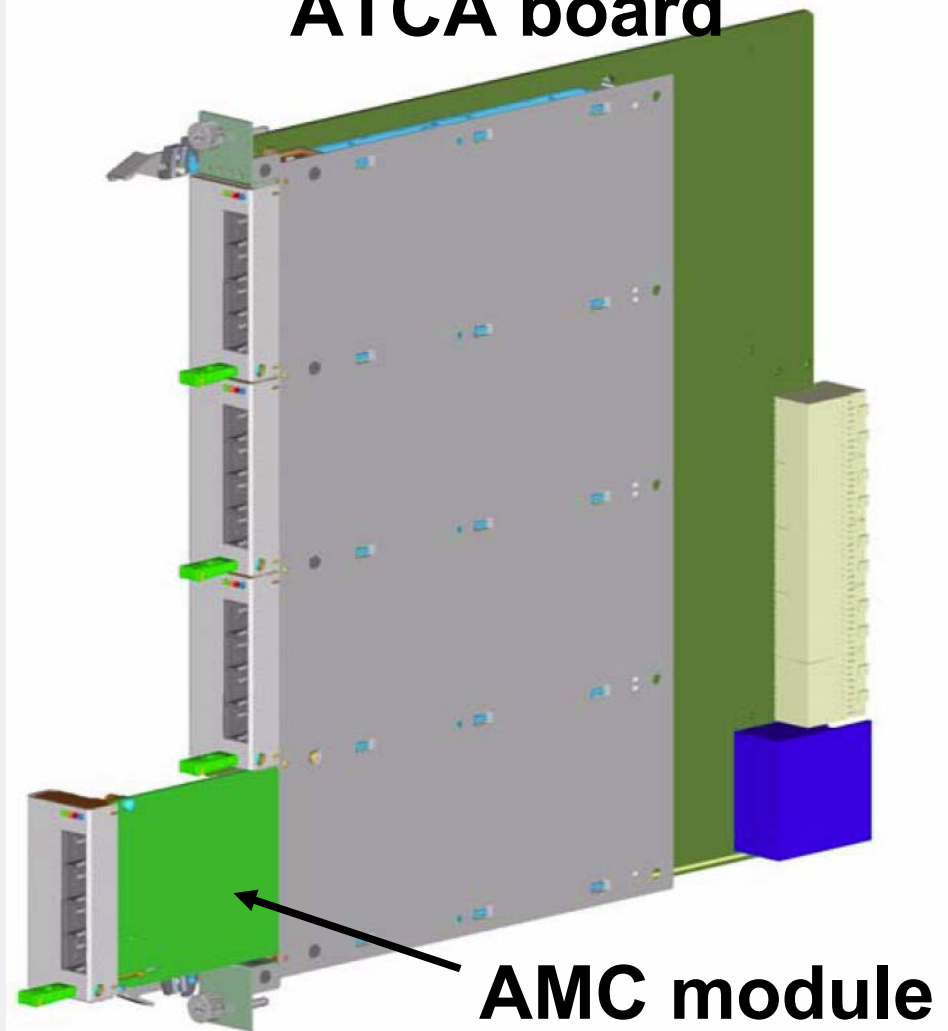
Features of AMC modules:

- ★ Edge connector (max. 340 pins),
- ★ Build-in IPMI controller,
- ★ Two power supplies +3V3/+12V,
- ★ Maximum power 60 W per module
- ★ Module dimensions:
180mm x 73mm x 28mm

Communication interfaces:

- ★ Fabric interface:
 - PCI Express (PCI Express Advanced Switching)
 - Gigabit Ethernet and XAUI
 - Serial RapidIO
- ★ System Management Interface
- ★ Synchronisation Clock interface
- ★ JTAG Test Interface
- ★ Power (+3V3, +12V)

ATCA board



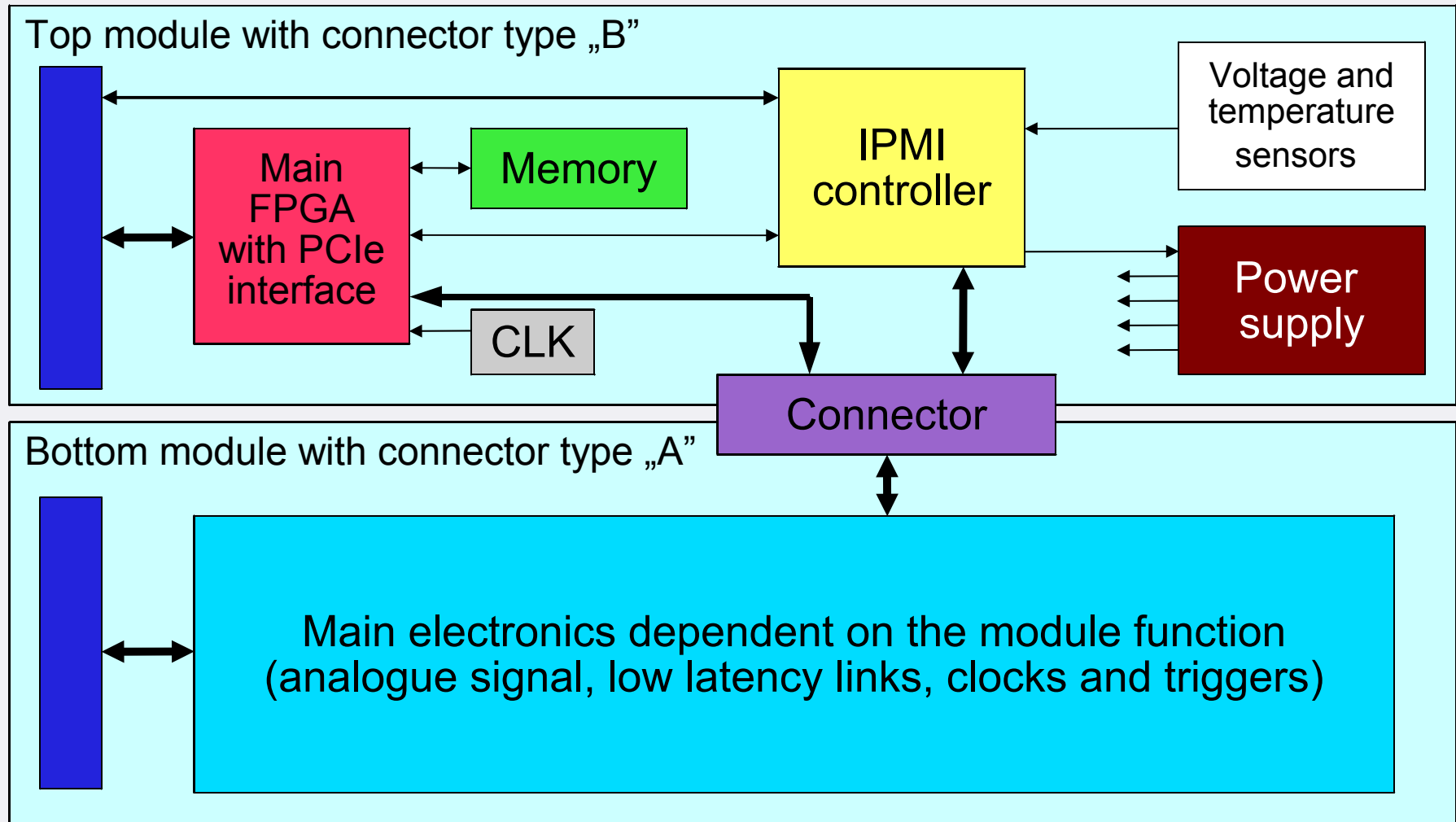
AMC module

AMC standard and Low Level RF system

Main LLRF controller will be built on ATCA carrier board, while auxiliary submodules will be build on AMC modules:

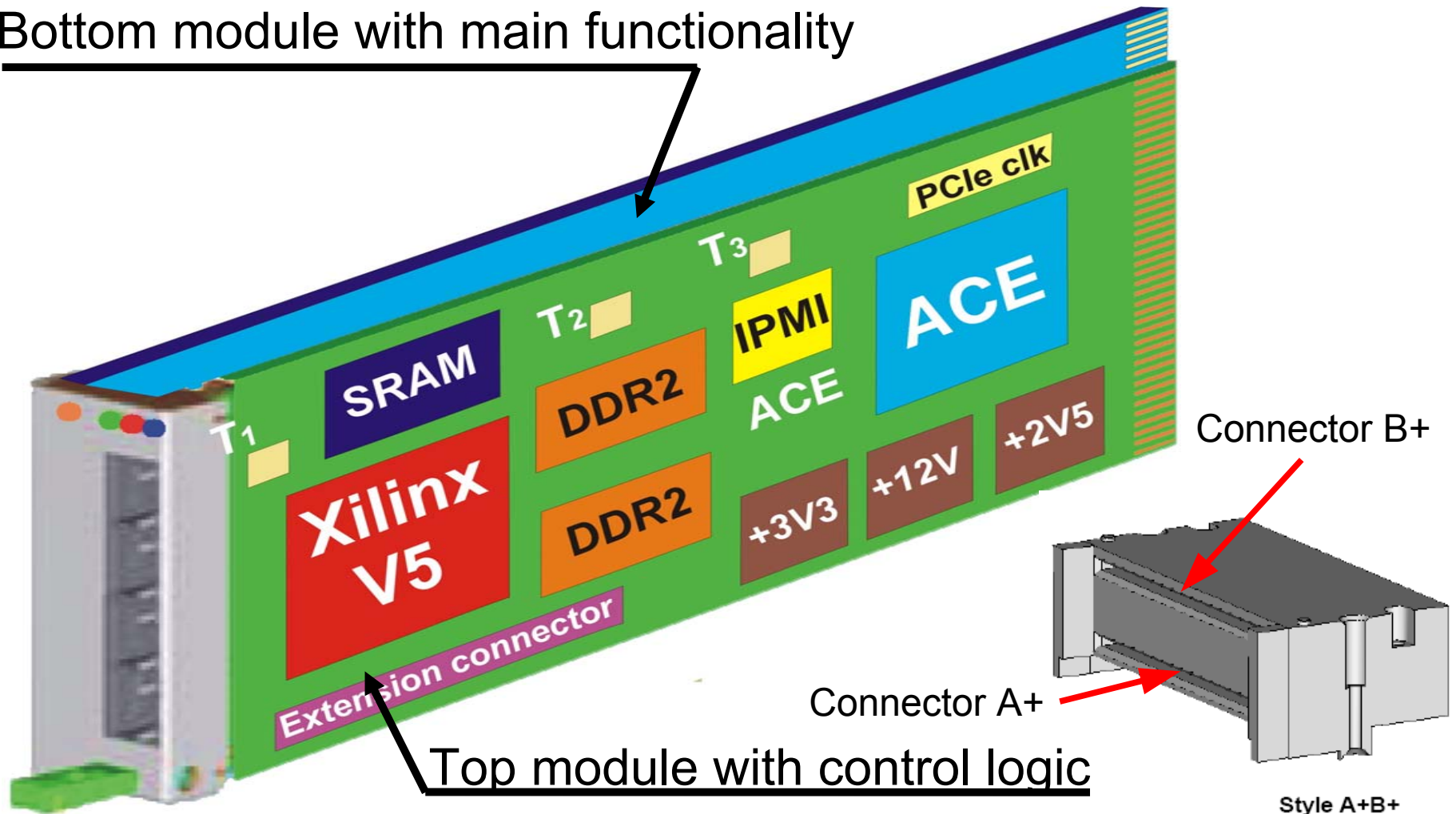
- 8 x ADC (100 MHz) + FPGA (front panel and rear connection)
 - ★ industrial module available, our design in progress,
- Vector modulator + 2 x DACs (800 MHz) + FPGA + memory,
- Transient detector, 1 x ADC (2 GHz) + fast static memory,
- Clock Synthesizer and Timing Module,
- Piezo controller,
- Radiation monitoring module (detection of neutron and gamma radiation).

Block diagram of the typical LLRF AMC module (1)



Block diagram of the typical LLRF AMC module (2)

Bottom module with main functionality



Octuple Analog-to-Digital module

Requirements:

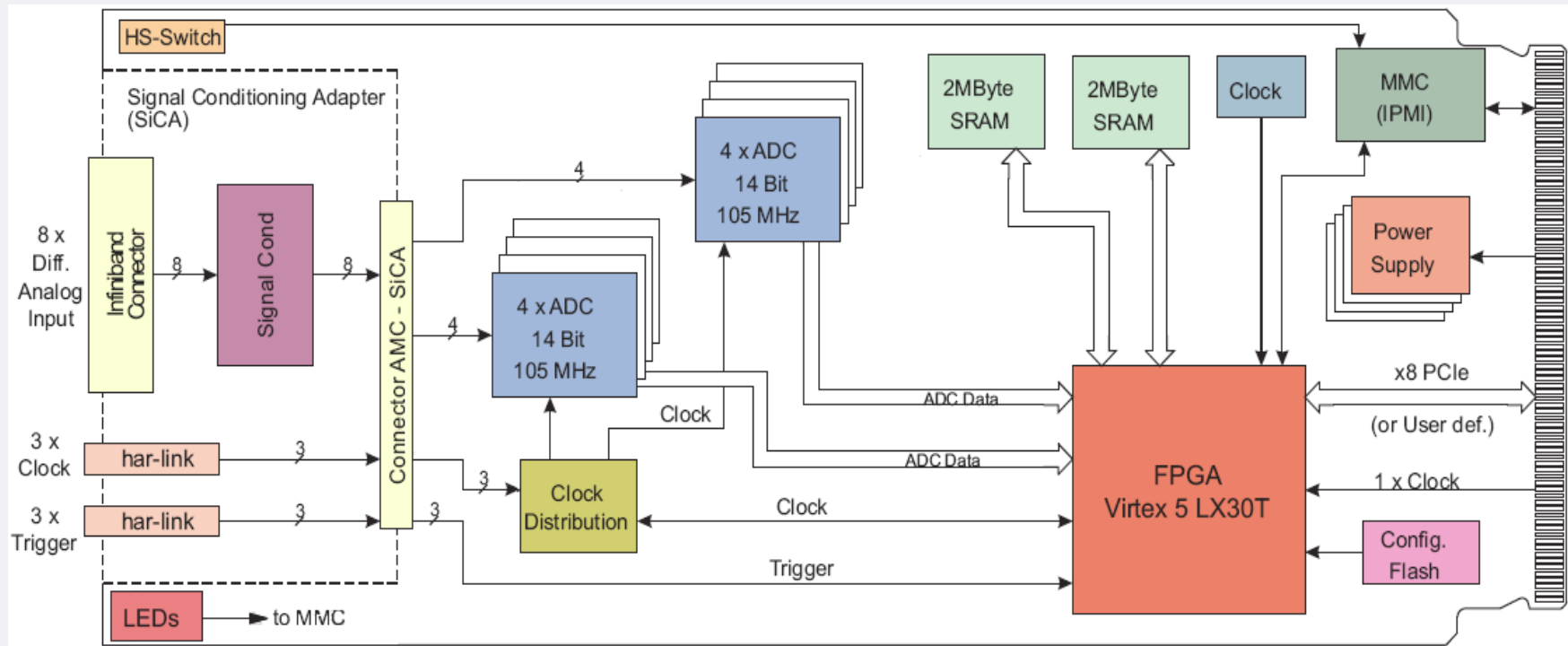
Octuple ADC: 14-16 bit, 100 MHz sample rate, conversion time up to 7 clocks
Configuration interface: AMC.1 PCI Express x1

- ◆ FPGA: Virtex 5 with external static memory (2-4 MB, 250 MHz)
- ◆ Two different configurable clocks for ADC 1-4 and ADC 5-8
- ◆ Clock distribution stability better than 5 ps
- ◆ Full support for IPMI standard

Additional signals from rear connector:

- ◆ 8 analog conditioned input signals (± 1 V, 10-100 MHz)
- ◆ 6 clock inputs up to 100 MHz (LVDS with jitter less than 5 ps)
 - 2 clocks connected to FPGA and ADC
 - 4 clocks connected to FPGA

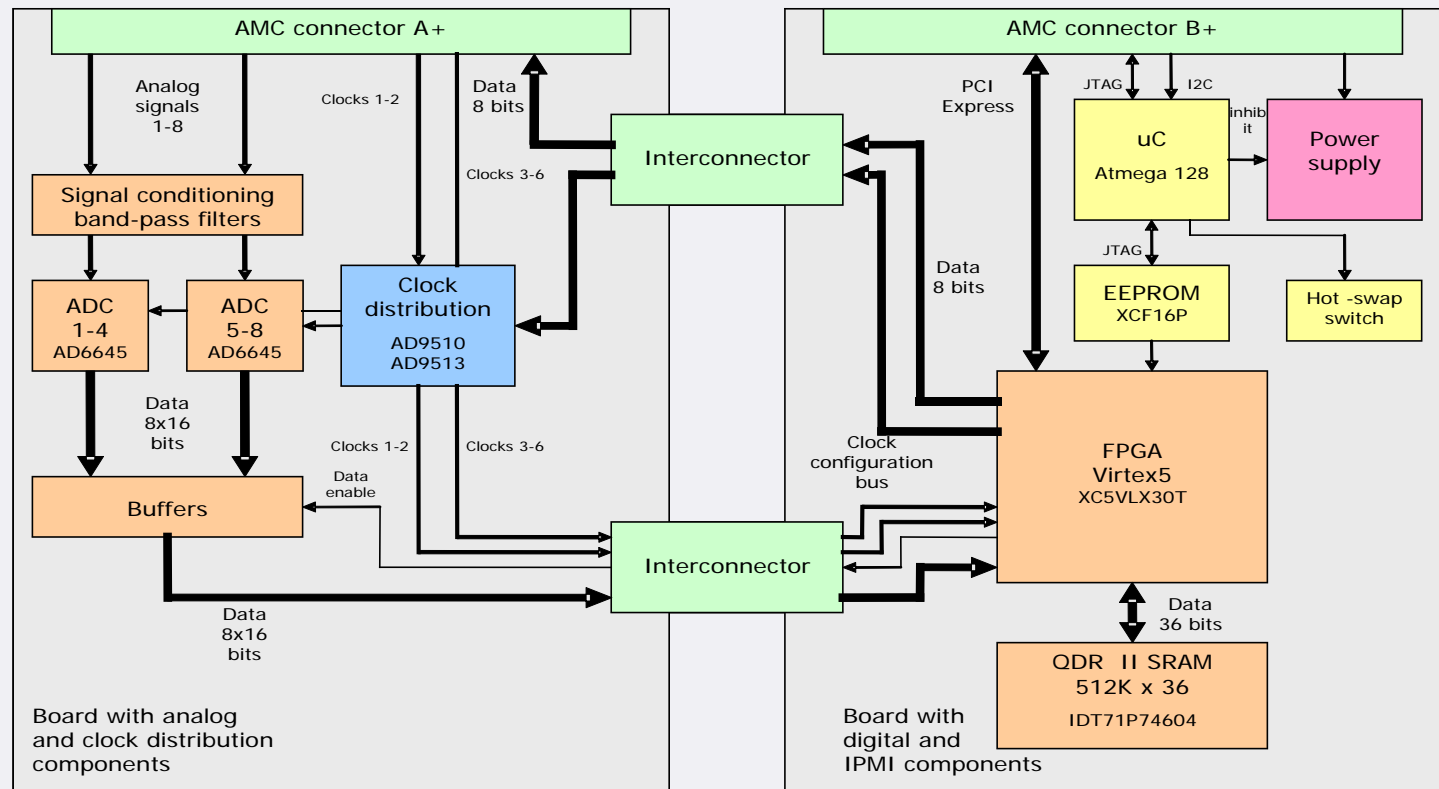
Octuple Analog-to-Digital module - TAMC900



Features:

- ★ 8 x LTC2254, 14-bit, 105 Msps ADC converter
- ★ 4 MB of QDR II memory (data buffer for maximum 2 ms)
- ★ 3 external clock and 3 trigger inputs

Octuple Analog-to-Digital module – Warsaw version



Features:

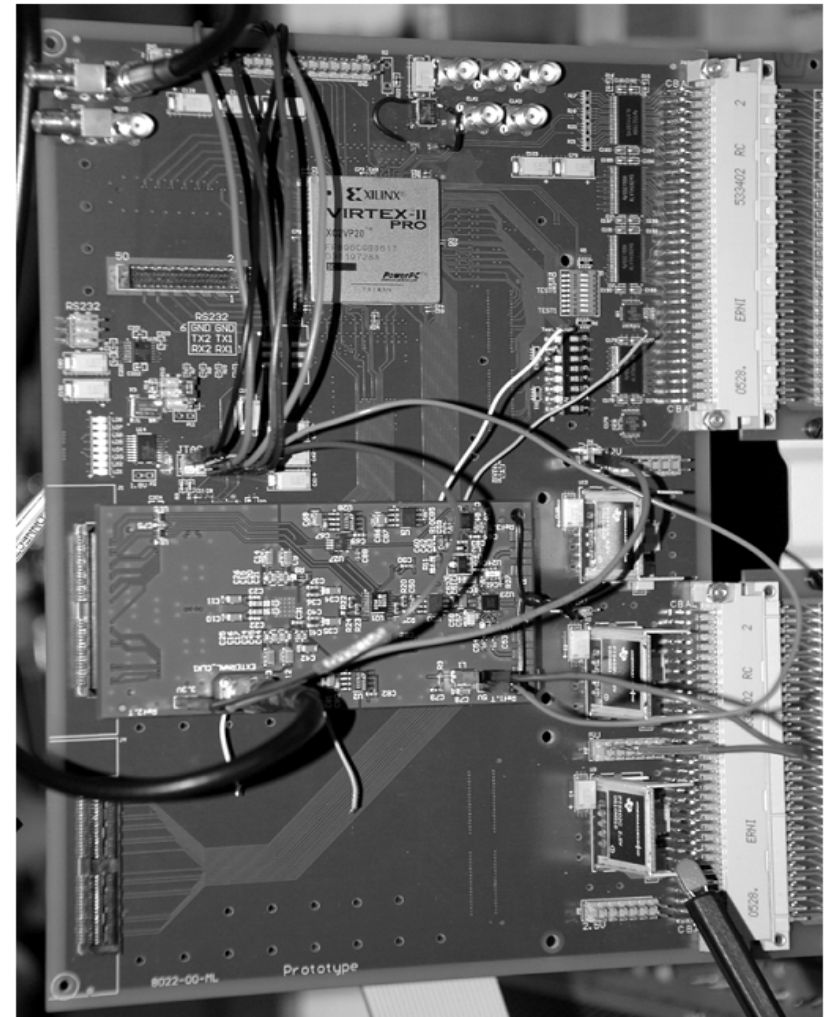
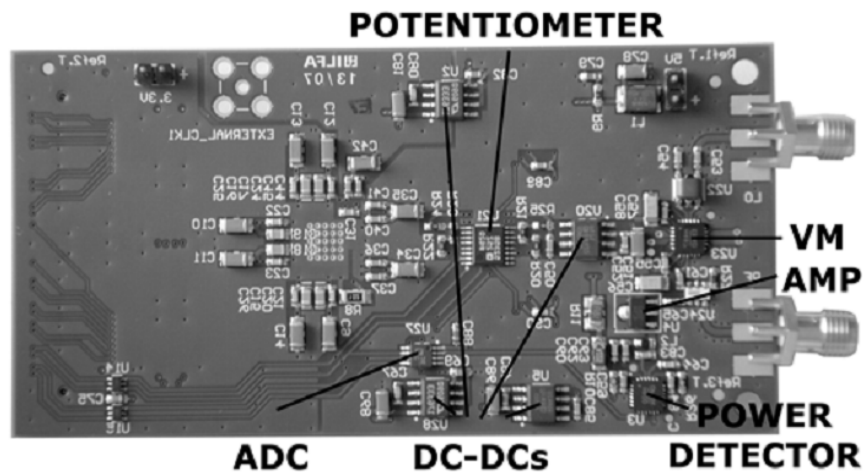
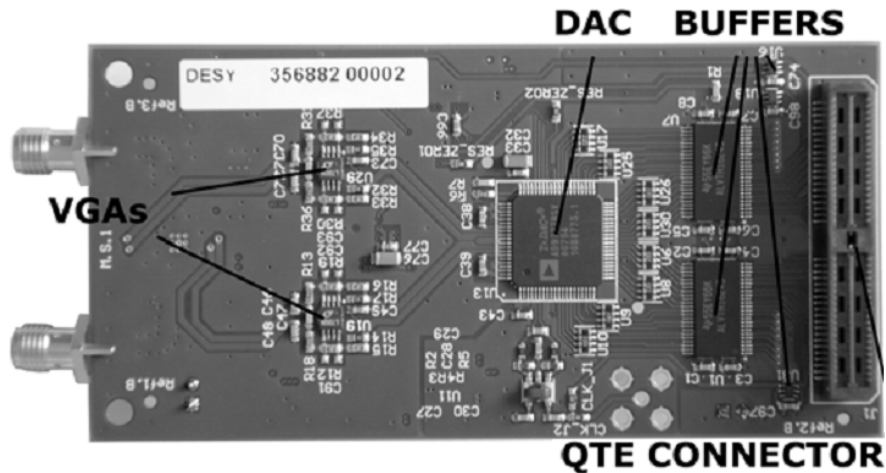
- ★ 8 x AD6645, 14-bit, 105 Mps ADC converter
- ★ 4 MB (512 kB x36) of QDR II memory
- ★ 6 external clock/trigger inputs
- ★ MMC controller

Vector modulator (1)

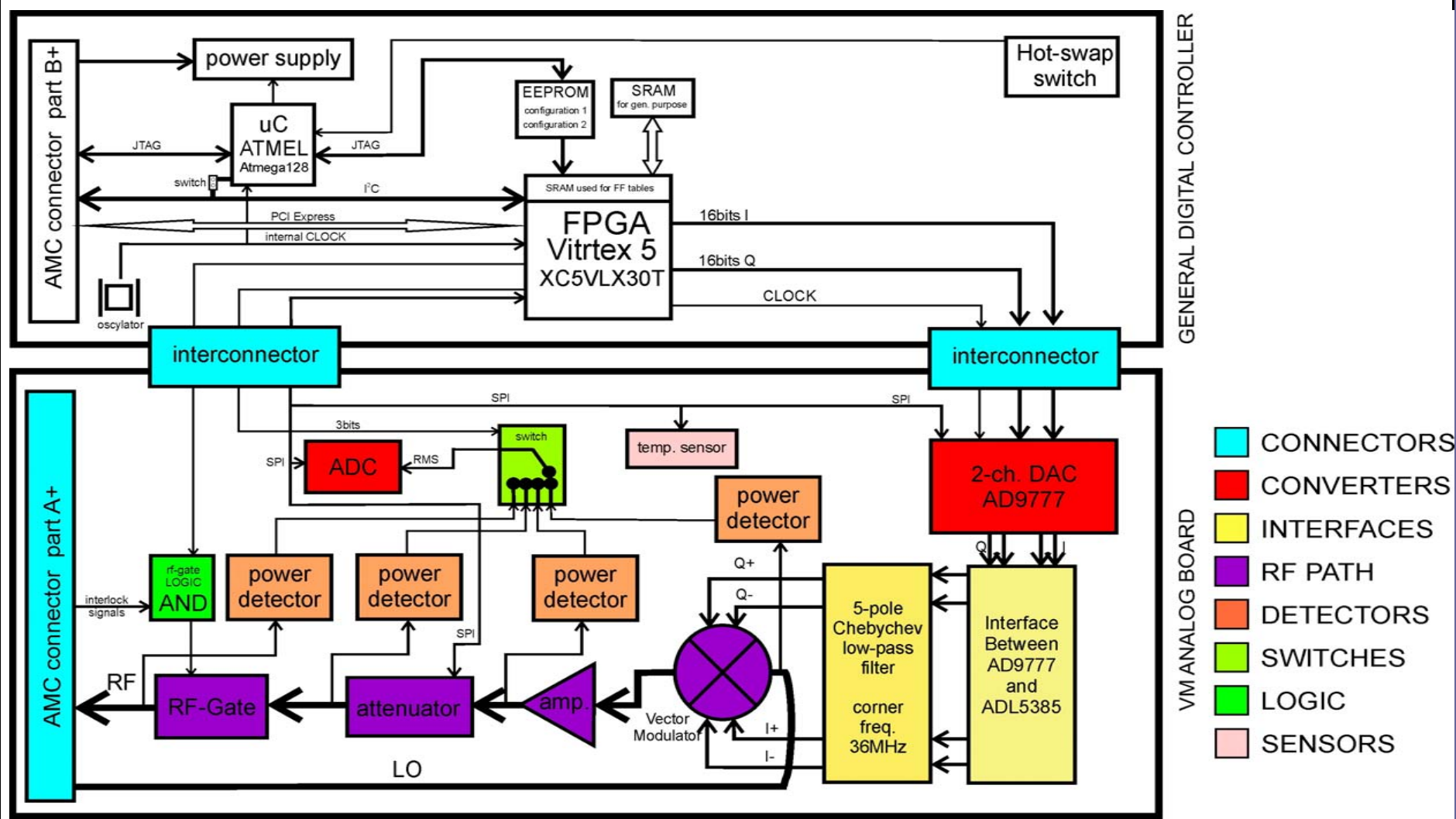
Requirements:

- ★ LO input frequency : 1.3 GHz
- ★ Nominal Input level: $\pm 1 V_{pp}$
- ★ Nominal Input power range: ± 6 dBm
- ★ Input impedance: 50 Ohm nom.
- ★ Input VSWR : max. 1.5:1
(input return loss = 14 dB for VSWR = 1.5)
- ★ Output frequency: 1.3 GHz
- ★ Output level: 0 dBm nom.
- ★ Output impedance: 50 Ohm nom.
- ★ Operating temperature range: -10 deg. C to +70 deg.C
- ★ Humidity: max. 95 % non-condensing

Prototype of vector modulator



Vector modulator (2)



Clock Synthesizer and Timing Module (1)

★ Designed by: Michał Ładno, Krzysztof Czuba

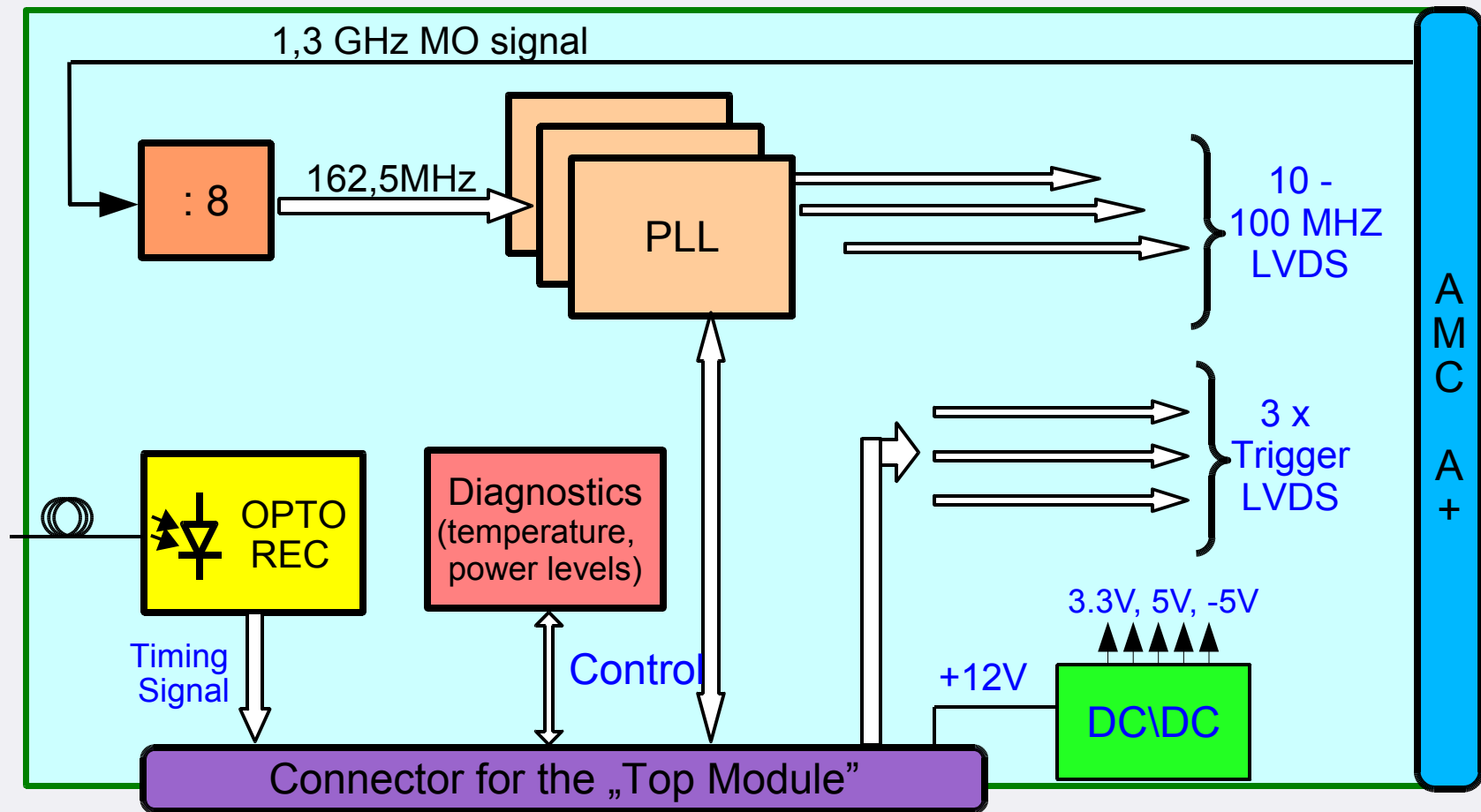
★ **Clock synthesizer requirements:**

- Synthesize clock from the MO 1.3 GHz reference signal
- Clock frequencies: 10 MHz – 100 MHz with 1 MHz step
- Clock stability better than 5 ps, (desirable < 2ps)
- 3 independent clock outputs (LVDS levels)

Timing Receiver requirements:

- Receive and decode timing signals from the existing FLASH timing
- Optical fibre input
- 3 independent trigger outputs (LVDS levels)
- Internal trigger generation mode (trigger frequency 0.1 – 33 Hz)

Clock Synthesizer and Timing Module (2)



Requirements for Radiation Monitoring (RAMC)

Requirements:

★ Detection ability:	neutron fluence, gamma dose
★ Lowest detectable level of fluence:	$10^4 - 10^5 \text{ n*cm}^{-2}$
★ Lowest detectable level gamma:	$10^{-3} - 10^{-2} \text{ Gy(Si)}$
★ Level of neutron fluence tolerance:	in range of $10^{12} \text{ n*cm}^{-2}$
★ Level of gamma rad. tolerance:	in range of 10^3 Gy(Si)
★ Dynamic range for neutron fluence:	6 orders of magnitude
★ Dynamic range for gamma:	3 orders of magnitude

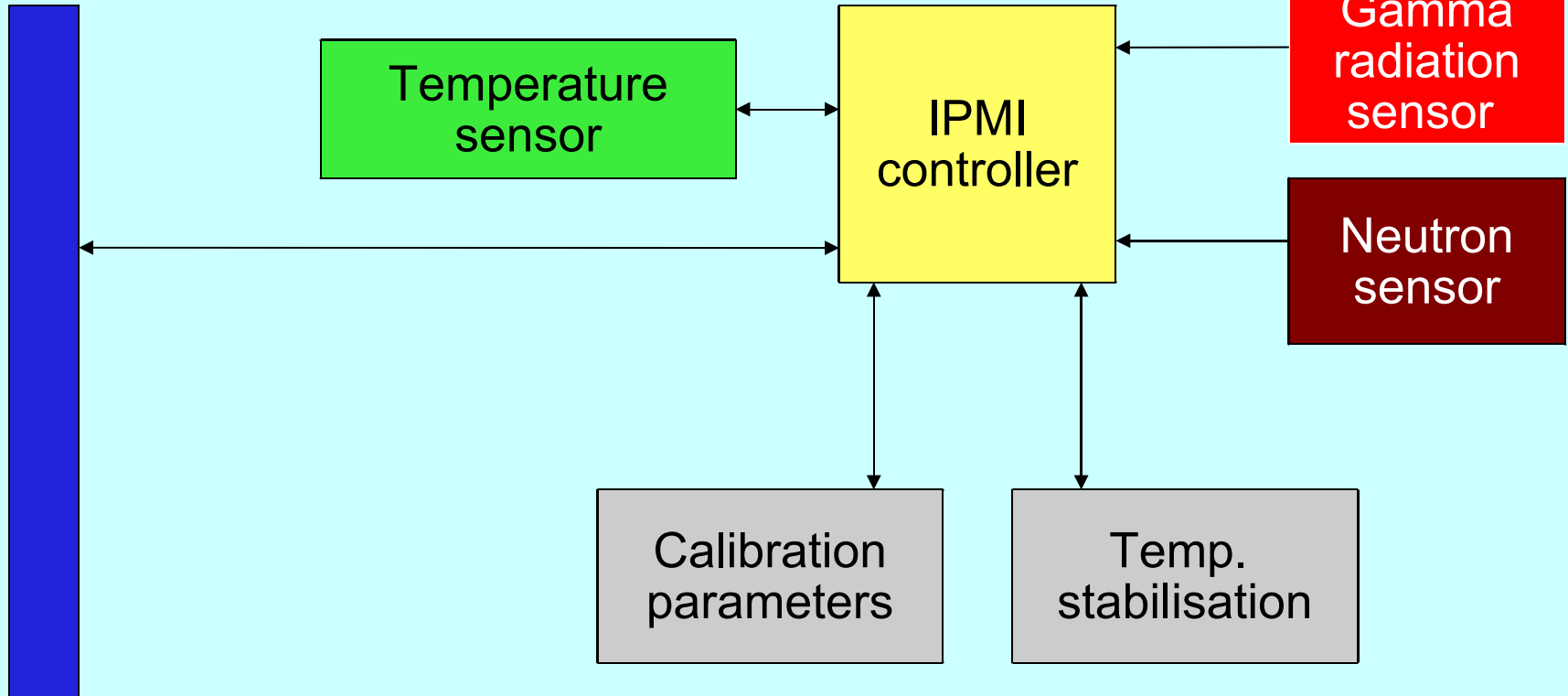
Gamma and neutron radiation should be monitoring in real-time in each ATCA crate and in various places where other electronics is installed.

When allowed dose or fluence is violated alarm should be triggered (IPMI message).

All measured data should be stored in main data base for further analysis

Radiation monitoring RAMC

Top module with connector type „B”



Communication Links



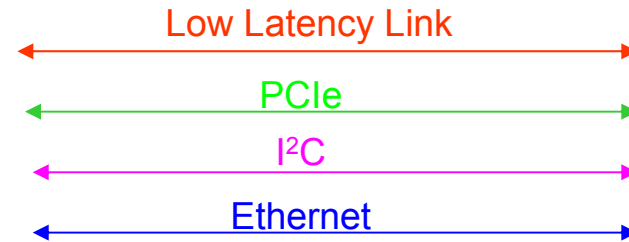
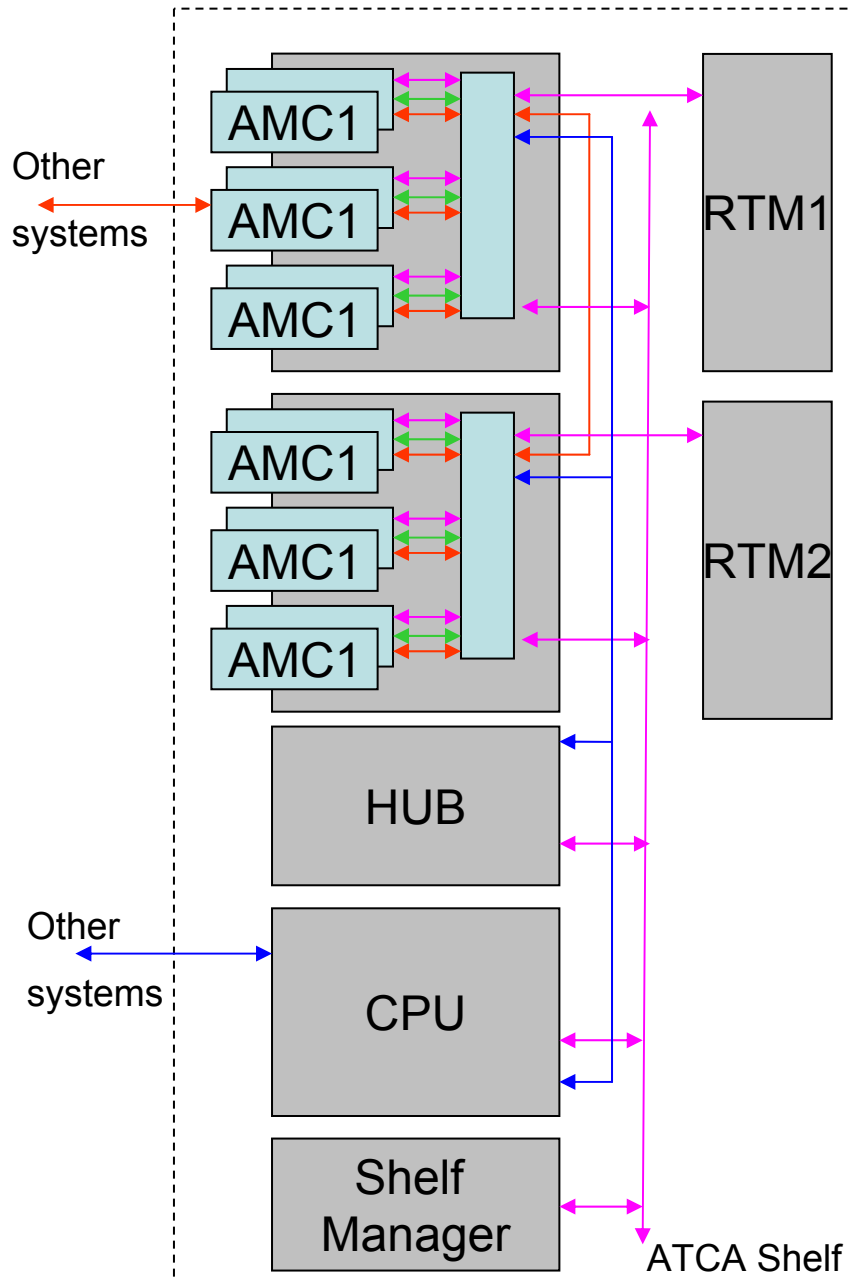
Requirements

1. **Fast, low latency links for fast feedback loop, piezo control**
2. **High throughput between pulses for DAQ systems
– sending a lot of data recorded during pulse**
3. **Boards management mechanism**
4. **Boards control in ATCA Shelf**
5. **Control of RTMs**
6. **Interfaces to other systems**

Communication interfaces offered by ATCA standard

- **PICMG3.0 – General Specification, ATCA Backplane Topology,**
- **IPMI**
- **E-Keying**
- **Subsidiary Specifications:**
 - PICMG3.1 Ethernet / Fibre Channel
 - PICMG3.2 Infiniband
 - PICMG3.3 PCI Express / Advanced Switching
 - PICMG3.4 Starfabric
 - PICMG3.5 RapidIO
 - PICMG3.6 PRS fabric

General concept

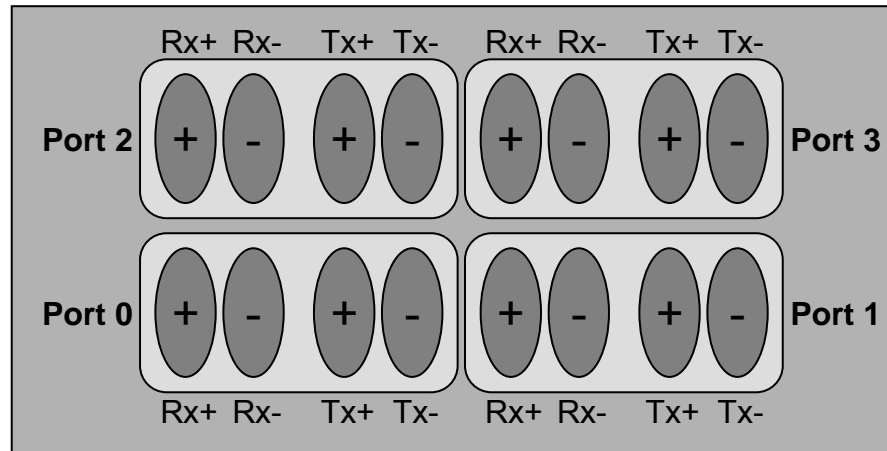


Latency in selected communication standards

- Rocket IO
 - direct peer-to-peer connections
 - latency around 300 ns (Virtex 2 Pro) and 100 ns (Virtex 5)
- PCI Express
 - connections via switch
 - minimum latency 500-700 ns depending on payload size
 - up to 10 μ s with higher switch load
- Gigabit Ethernet
 - 2.5 μ s
- 10 Gigabit Ethernet
 - 250-600 ns

ATCA-LLRF Channel Definition for Shelf Backplane

**Fabric Channel
PICMG 3.0**



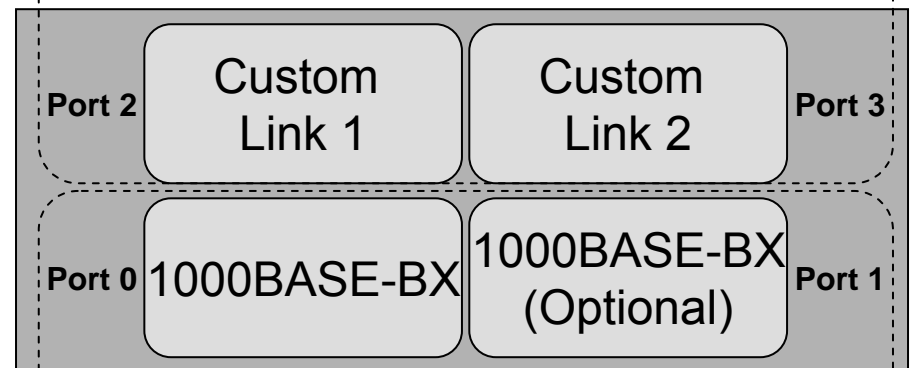
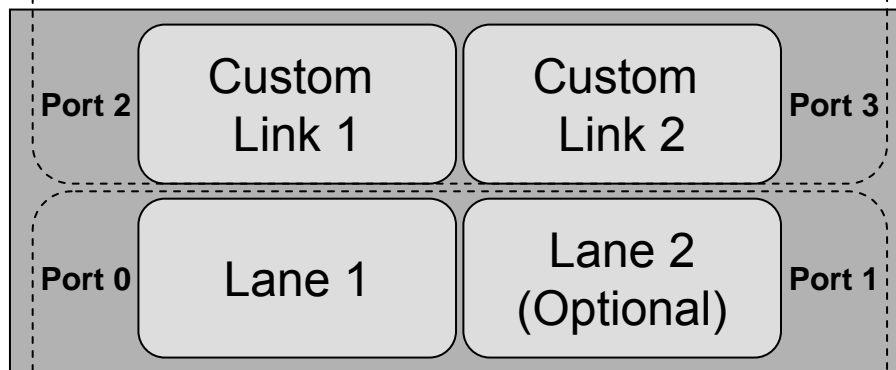
Option 1

ATCA-LLRF Channel

Option 2

Custom Link

Custom Link



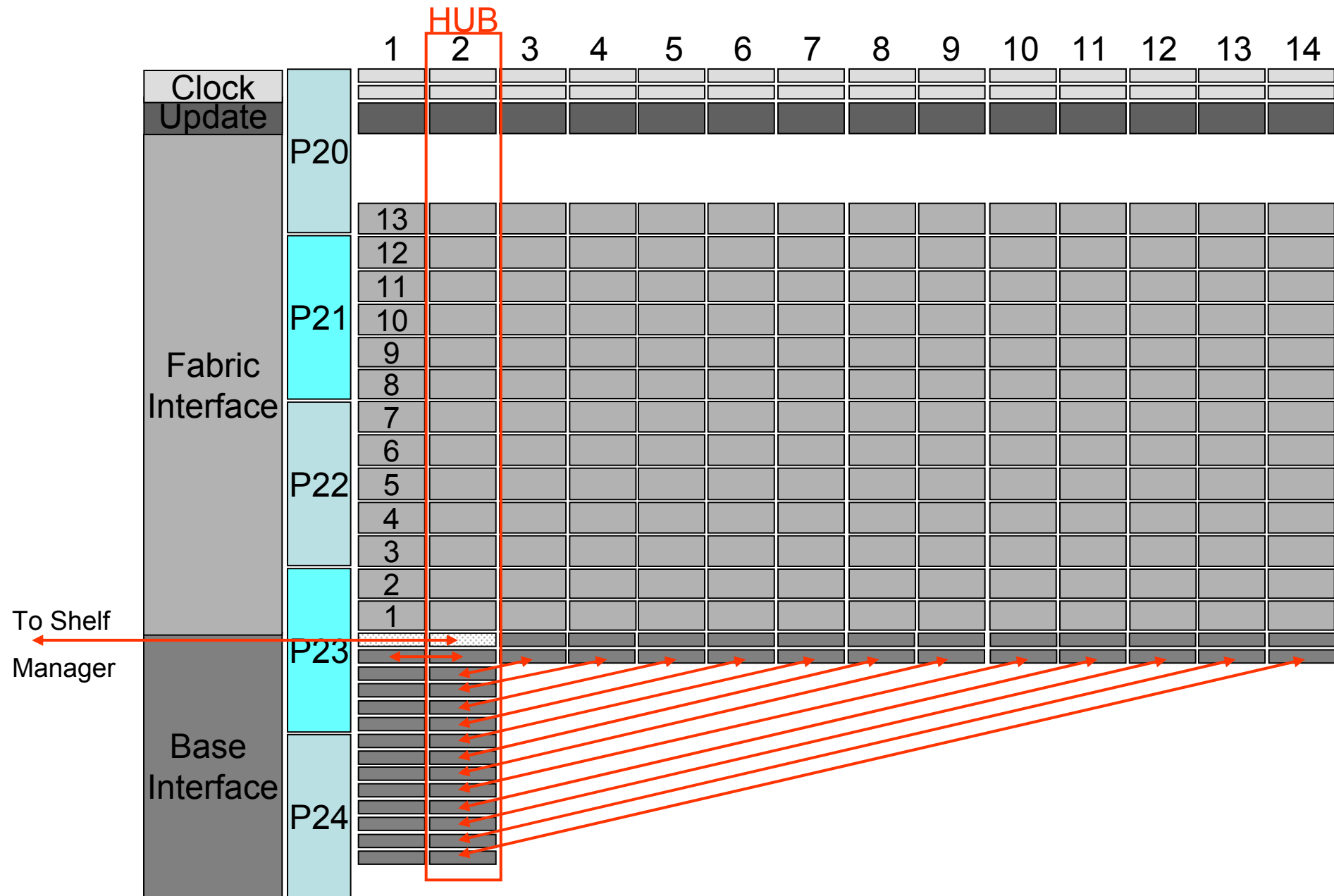
How many slots we need in one ATCA shelf?

- 5 x Carrier Boards (2 slots each) – 10 slots
 - 4 cards for 4 cryo-modules
 - 1 card as a main controller
- 1 HUB (or 2 for redundancy) – 1 or 2 slots
- CPU – 0,1 or 2 slots
 - 1 CPU without redundancy
 - 2 CPUs with redundancy
 - 0 CPU in case of distributed control system (AMC-CPU cards)

TOTAL: 12-14 slots ATCA shelf

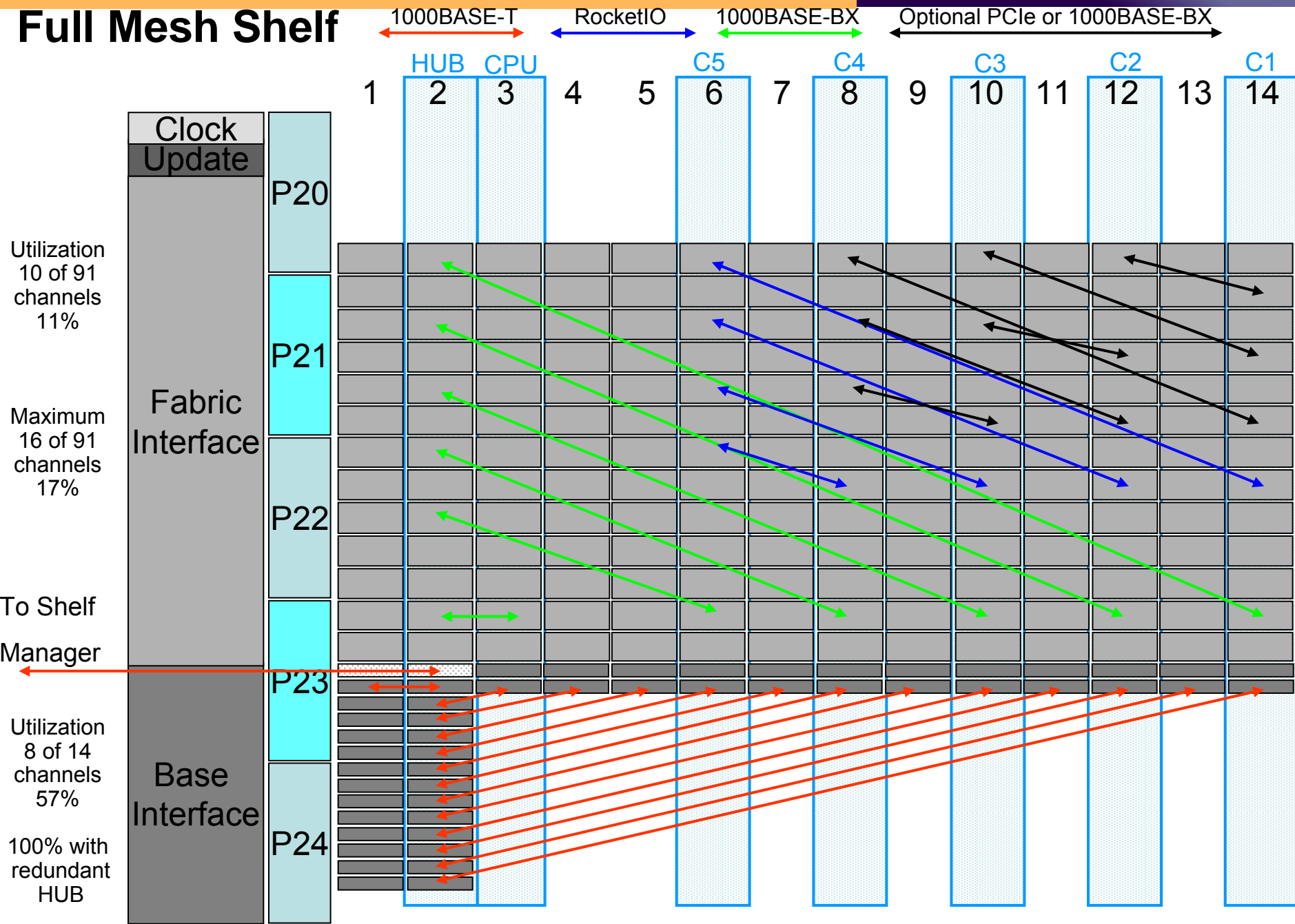
The European
X-Ray Laser Project

XFEL
X-Ray Free-Electron Laser



Backplane Links in the 14 Slots

Full Mesh Shelf



IPMI, Diagnostics



Intelligent Platform Management

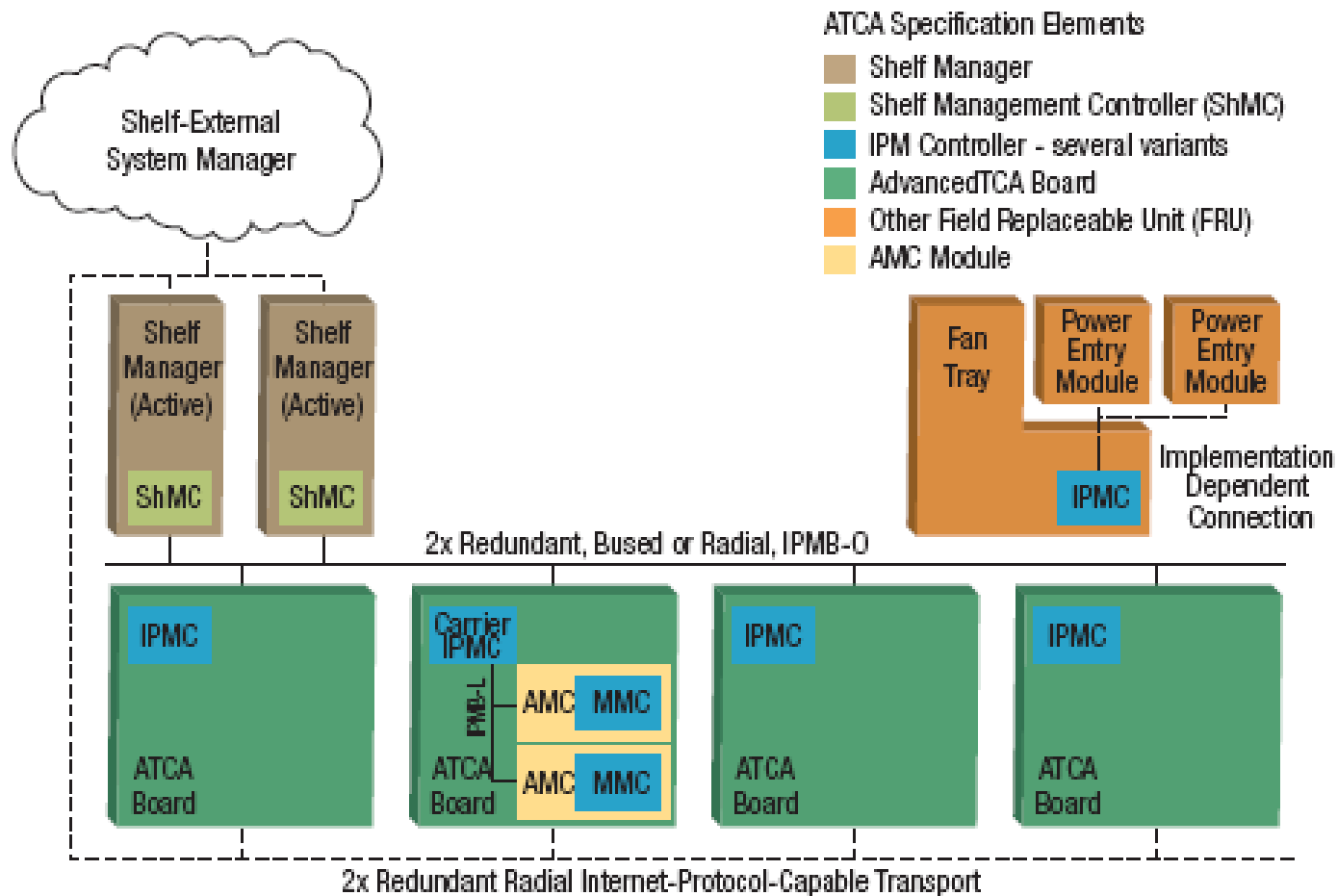


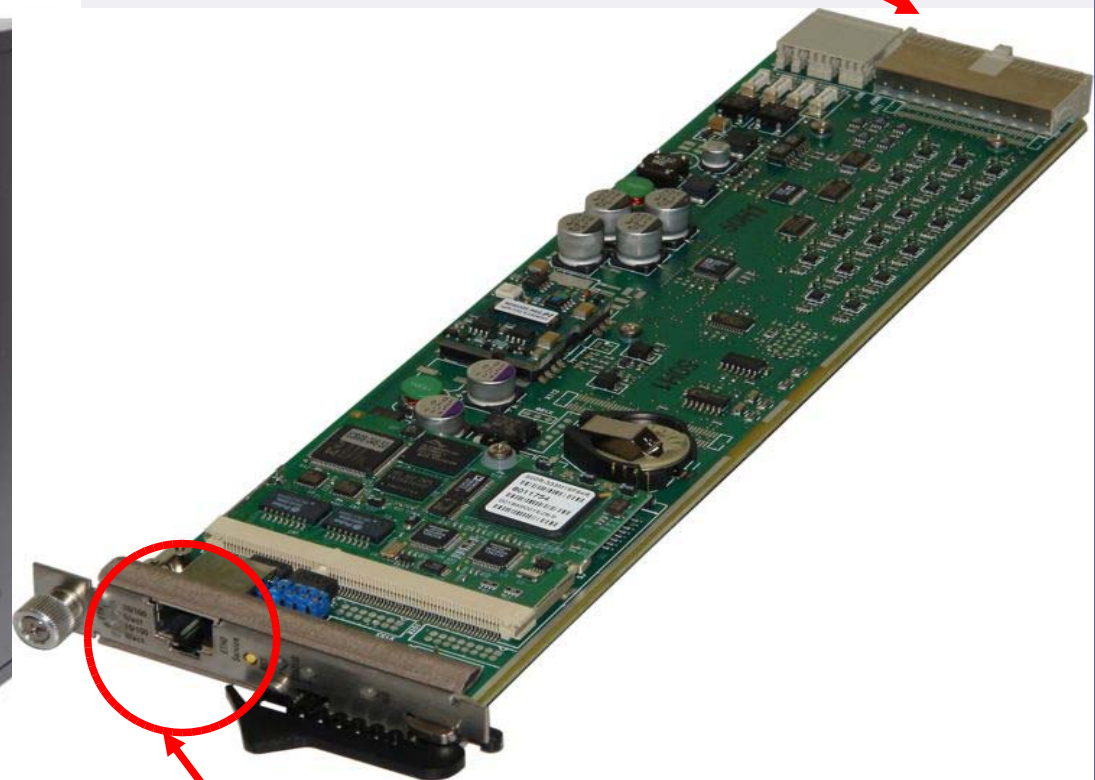
Figure 1 All types of management controllers in an ATCA/AMC-based shelf are building block candidates.

ATCA crate and ShelfManager



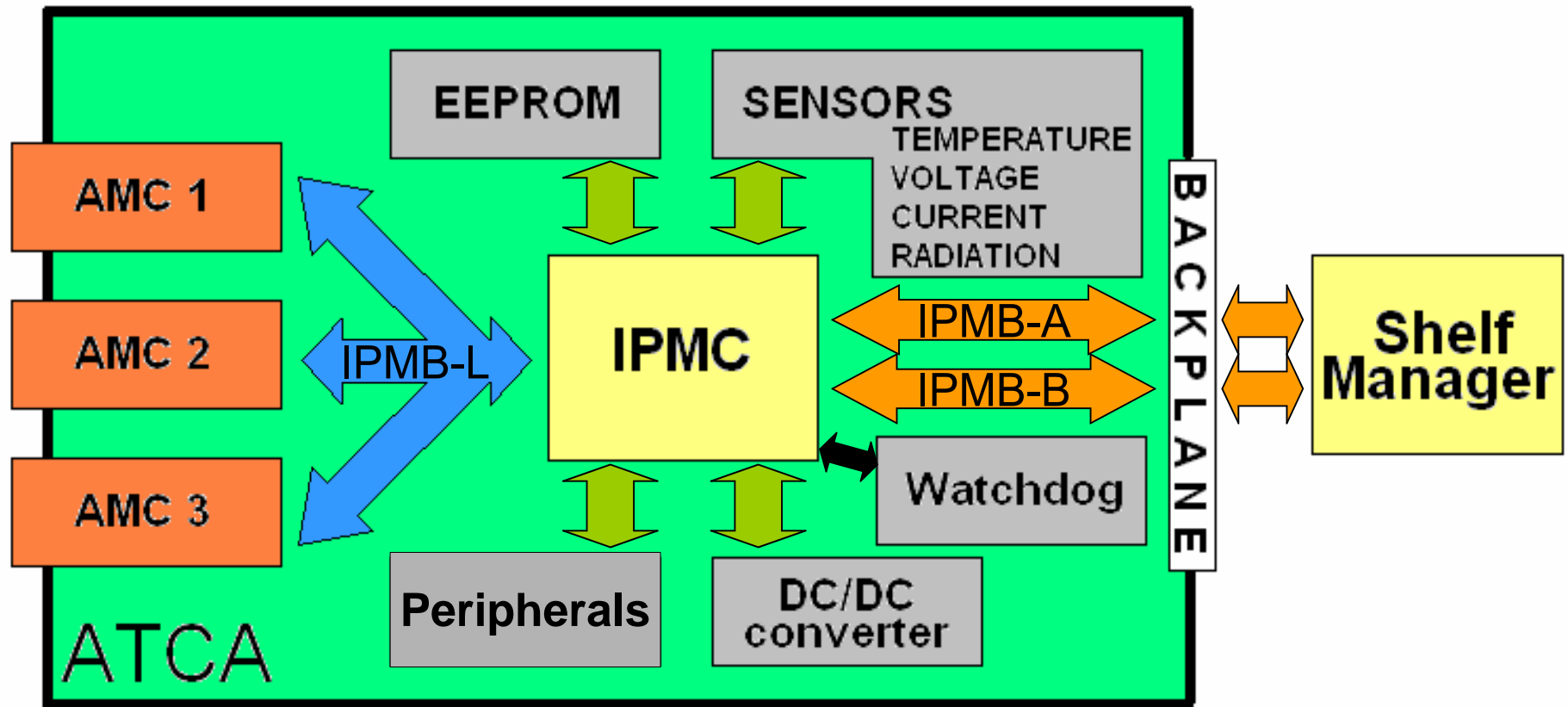
Redundant ShelfManager

IPMI interface I²C



Ethernet 10/100 Mbit

ATCA carrier board with IPMC

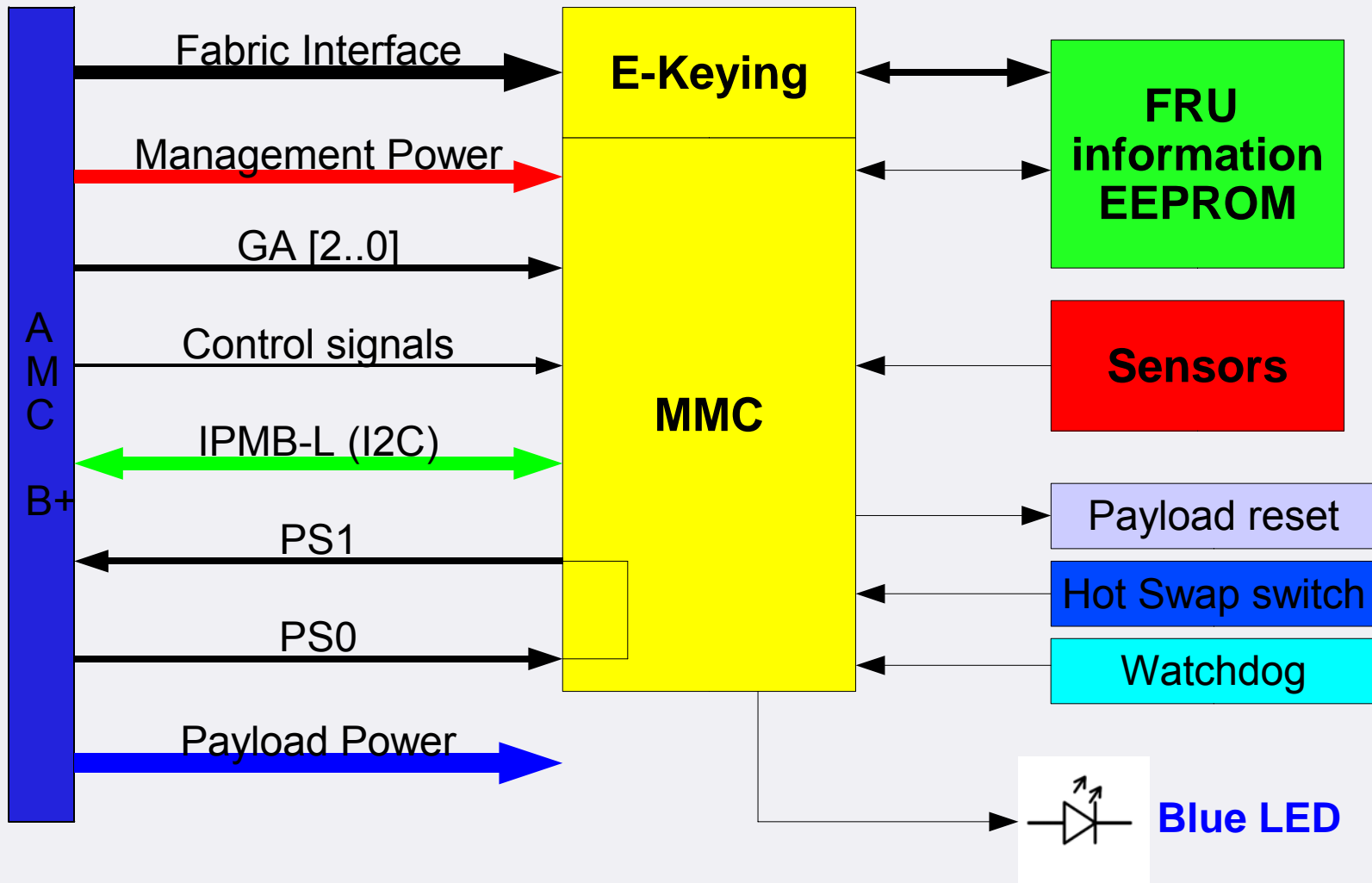


Blue arrow: IPMB-L AMC - I2C Bus

Green arrow: Peripheral I2C Bus

Orange arrow: Redundant I2C IPM-Buses that aggregate into IPMB-0

Module Management Controller



Power Distribution Management Architecture

SM

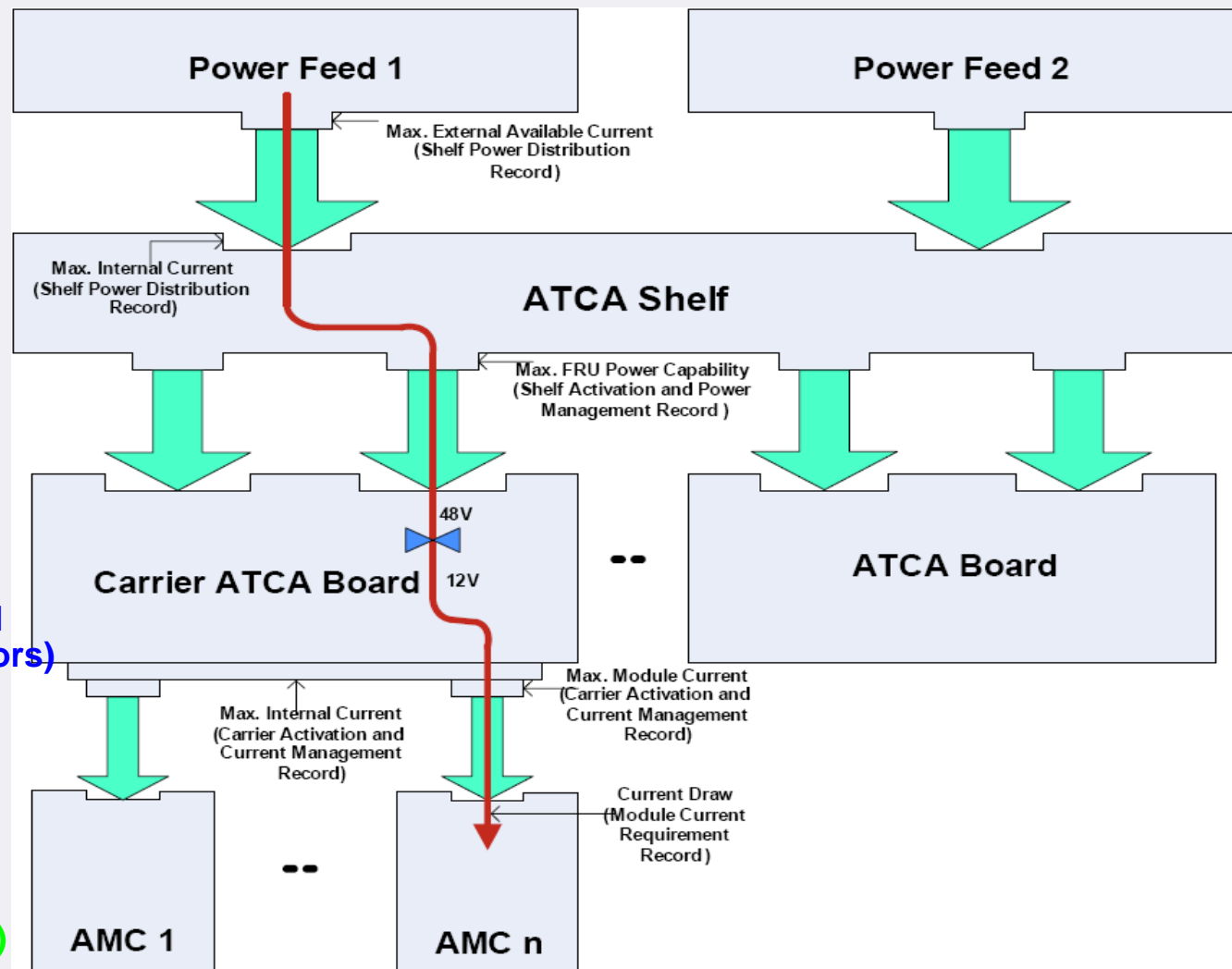
(Power budget)

IPMC

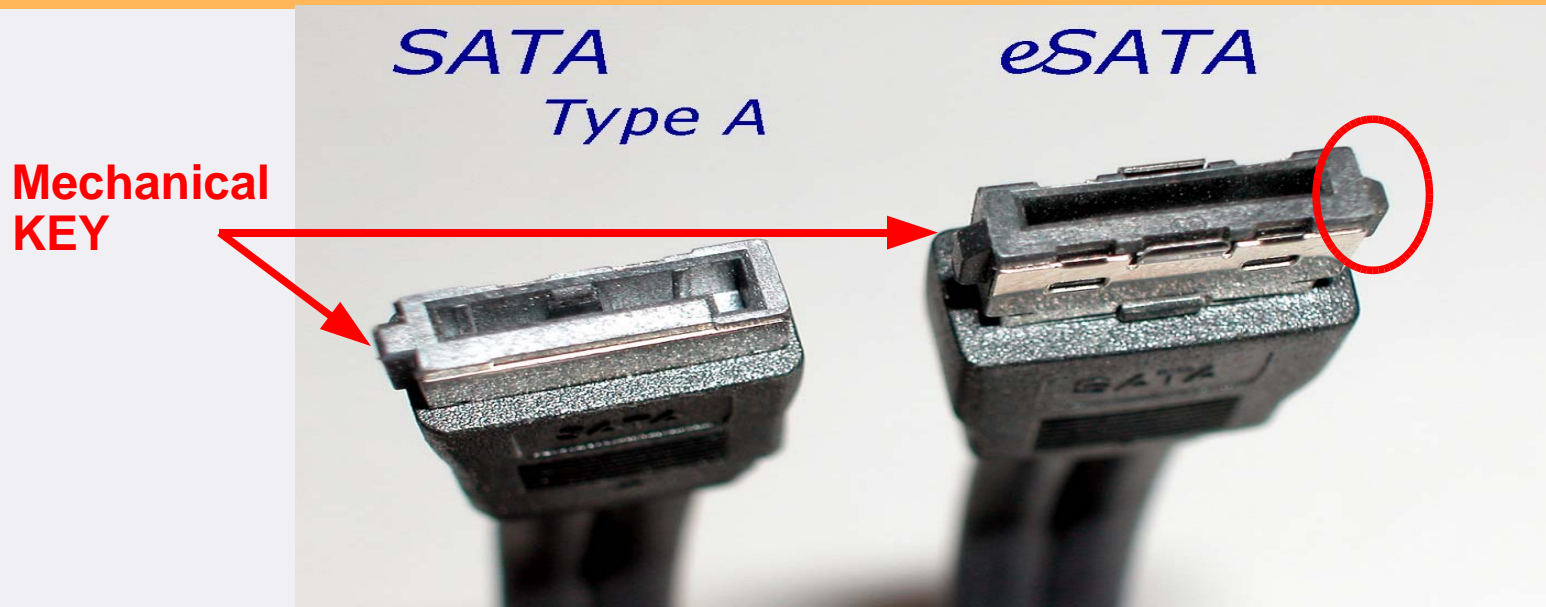
(Carrier current and
AMC bays descriptors)

MMC

(Current descriptor)



Electronic-keying



Electronic Keying is the mechanism used to dynamically satisfy the needs that had traditionally been satisfied by various mechanical connector keying solutions:

- ★ Prevent mis-operation
- ★ Verify fabric compatibility
- ★ E-Keying between the Modules and switch(es)
- ★ Point-to-point E-Keying for AMC modules

Diagnostics of ATCA-based systems

Useful diagnostics offered by ATCA standard:

1. Thermal violation – IPMC controls temperature of ATCA and AMC components
2. Monitoring of supply voltages
3. Monitoring of supply currents
4. Monitoring of main power converter (-48V to +3V3/+12V)
5. Payload control (read of device state, reset and other user-dependent diagnostics)
6. External watch-dog for IPMC (with external oscillator independent from IPMC oscillator)
7. SM periodically tests state of IPMC on ATCA boards
8. Electronic Keying (E-Keying)

Additional diagnostics:

1. Monitoring of gamma and neutron radiation in ATCA crates and other important spots in accelerator tunnel
2. Reference clocks detectors

Piezodriver and Fast Tuning Control



The main aim of Piezo Control system

Drive the piezoelements assembled in fast tuners frames to minimize the Lorentz force and microphonics effects

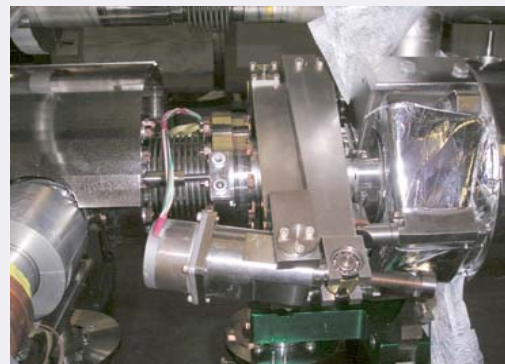
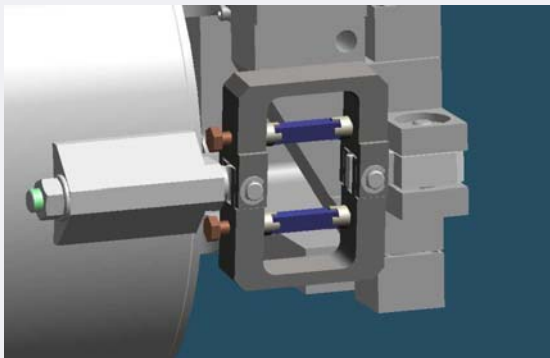
On-line frequency detuning calculation

Microphonics measurement
(i.e. diagnostics of cryogenic system)

Dimensions: **10x10x30mm**
Manufacturer: **NOLIAC**



Dimensions: **10x10x36mm**
Manufacturer: **PI**



General requirements of PiezoControl system

Lorentz force detuning (LFD) during flat-top $\Delta\omega_{\text{flat top}} < 10$ Hz for field up to 30 MV/m
(compensation up to 600 Hz – possible resonance compensation up to 1kHz)

Commercial available piezoelements (PI and NOLIAC)

$C_{2K} = 3 \div 5 \mu\text{F}$, $V_{\text{max}} = 100 \text{ V}$, oper. freq. for LFD/microphonics up to 1 kHz (full voltage scale),
 $\rightarrow I_{\text{load}} \sim 300\text{mA}$

Maximal repetition rate of RF (LFD compensation) pulse under 10 Hz
(20 Hz optional if better klystron available – driver need to be verified)

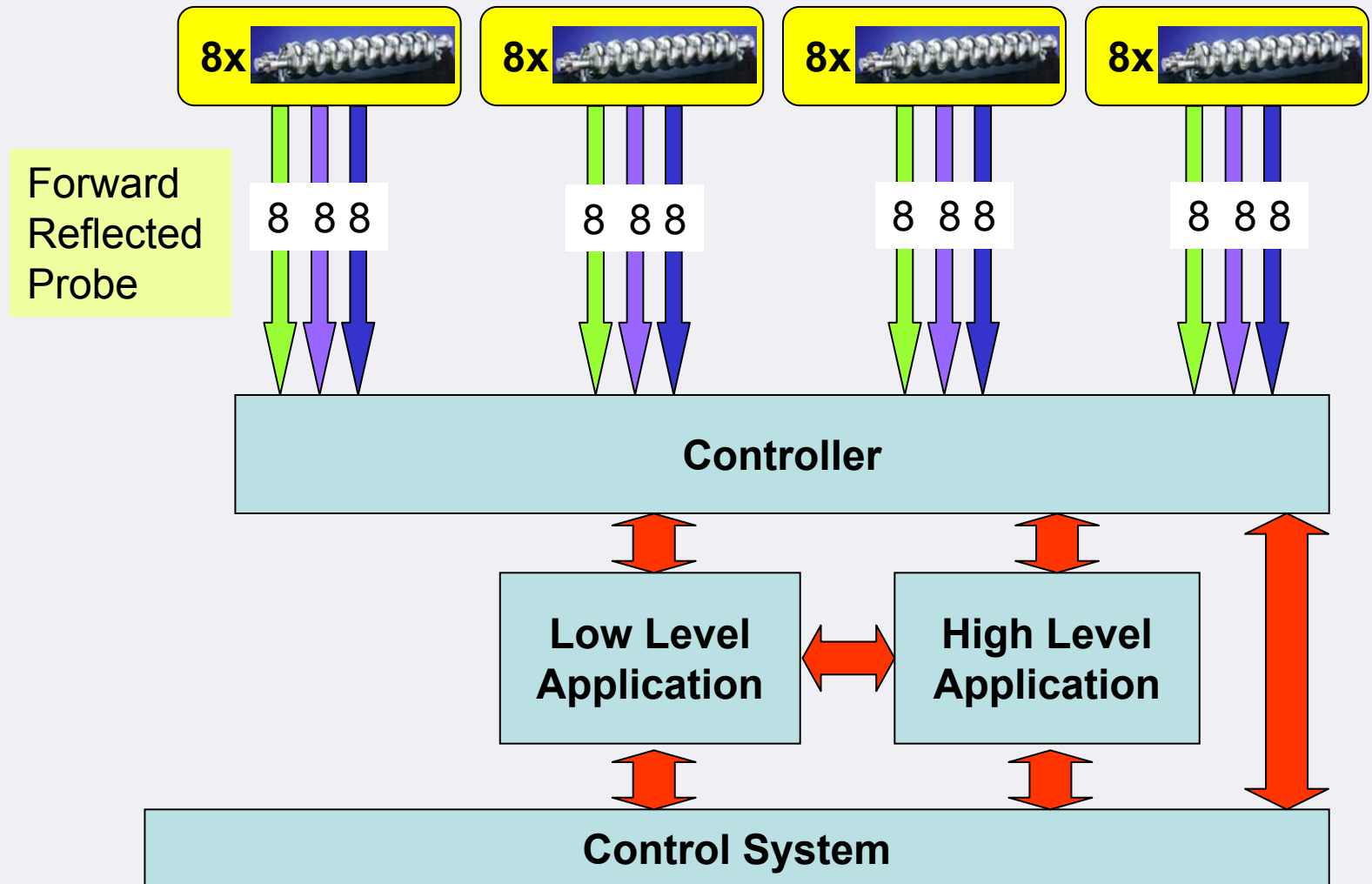
Scalable system: 101 modules, 808 cavities, 1616 Piezos

Piezo must be protected and monitored – 2 piezo for each cavity (higher reliability)
(piezo is fragile to over current and over voltage ($>150 \div 200$), piezo lifetime must be over 10^{10} pulses, resonance in the cables, piezo might fall out when stepper motor is wrongly tuned)

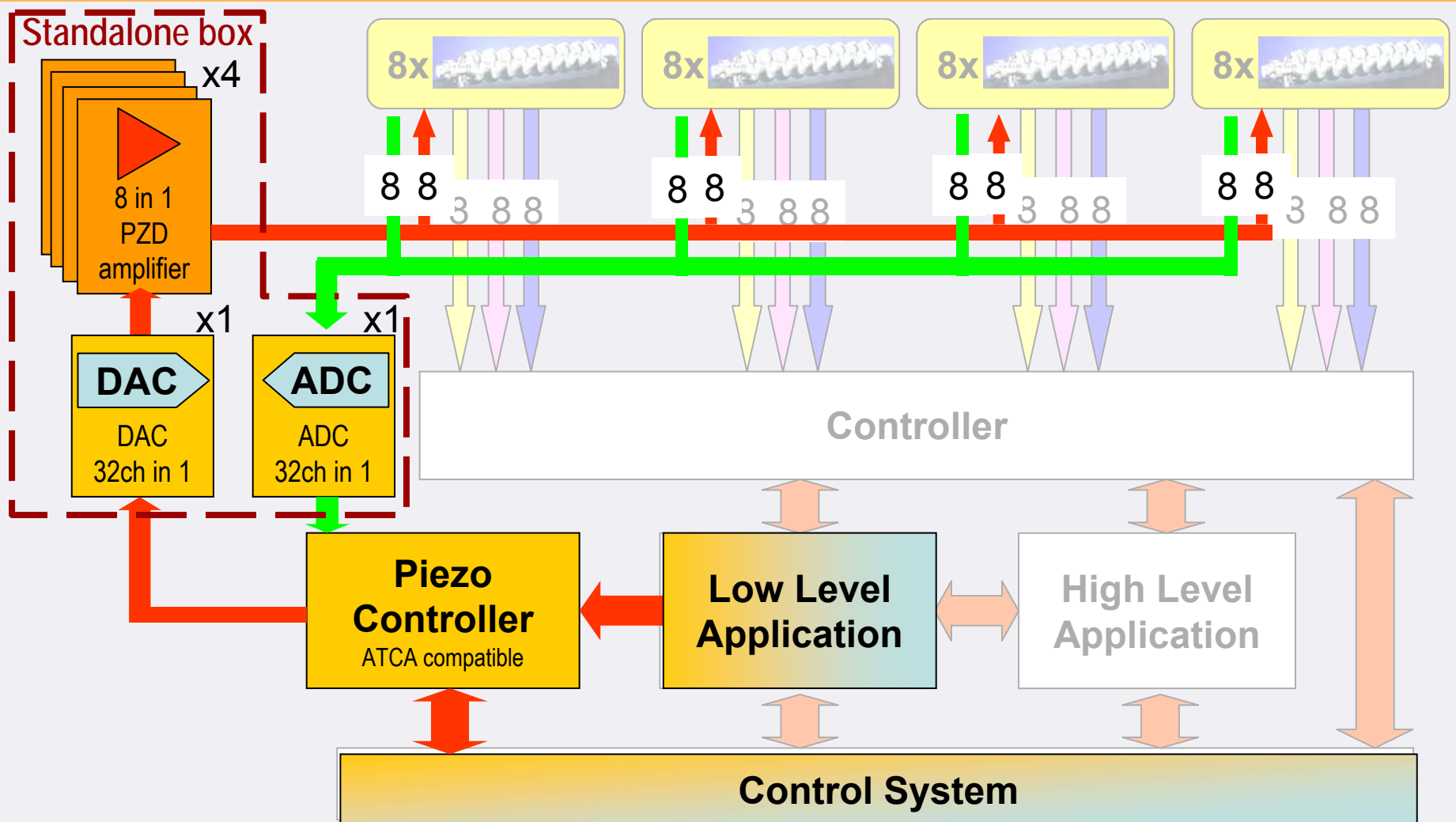
System must adjust pulse generated to piezo in regards to RF pulse
(different accelerating field gradient, flat-top and rising time duration demands different settings – feed-forward tables)

Possible microphonics compensation between the RF pulses (sensor/actuator mode)
(microphonics has smaller impact than LFD, constant offset of $\Delta\omega$ during flat top, feedback loop)

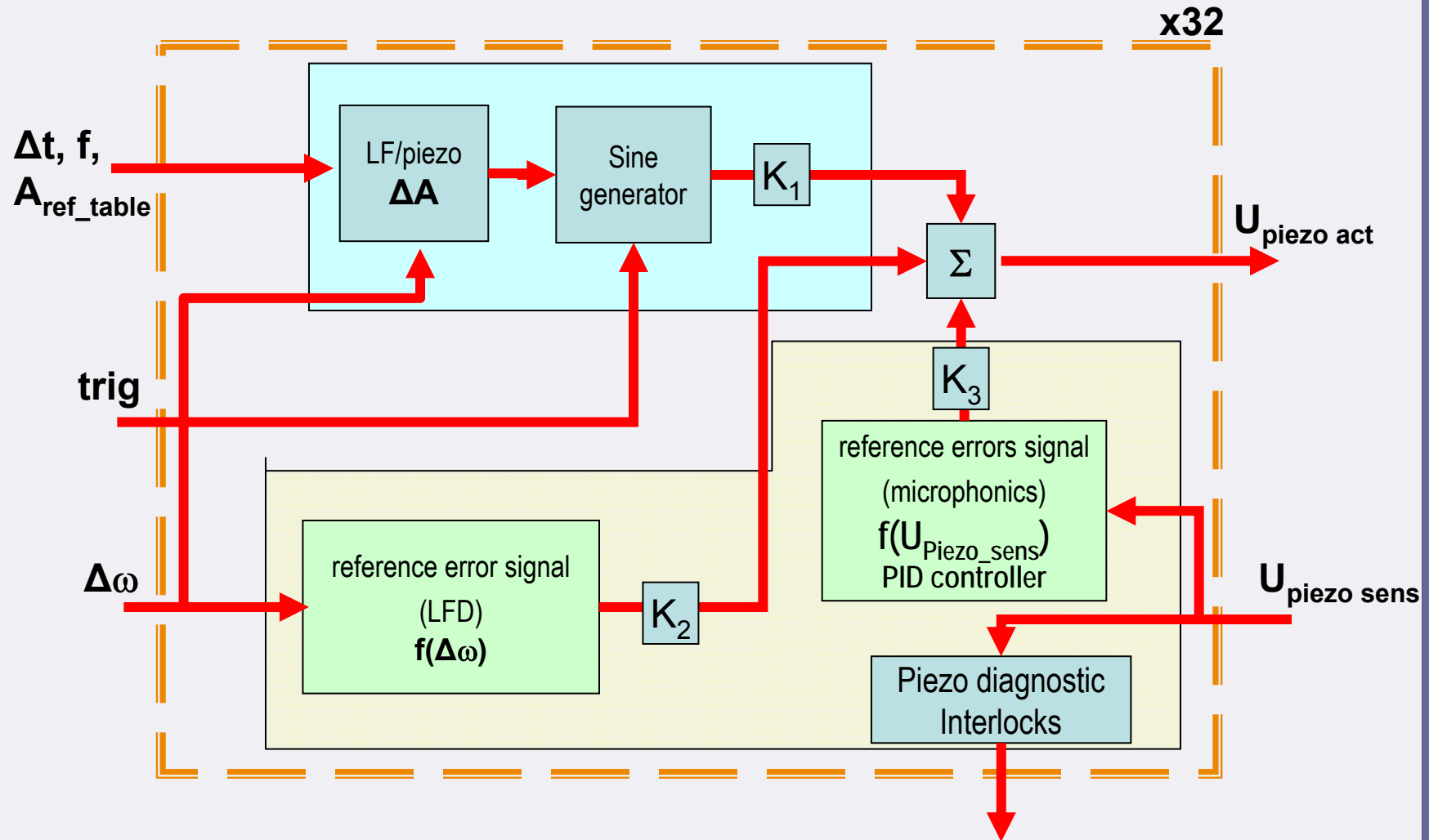
Overview of the piezocontrol system



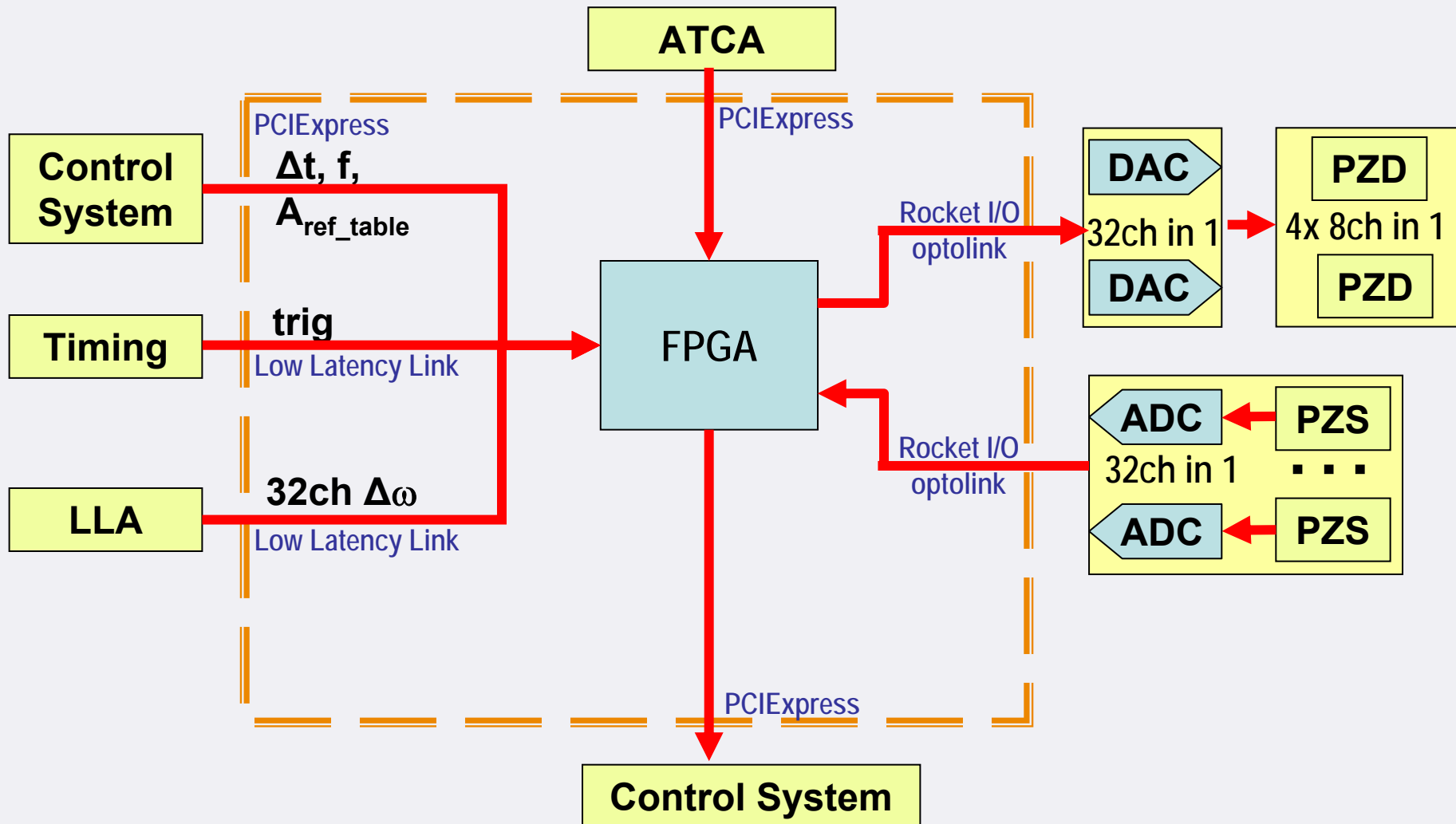
Overview of the piezocontrol system



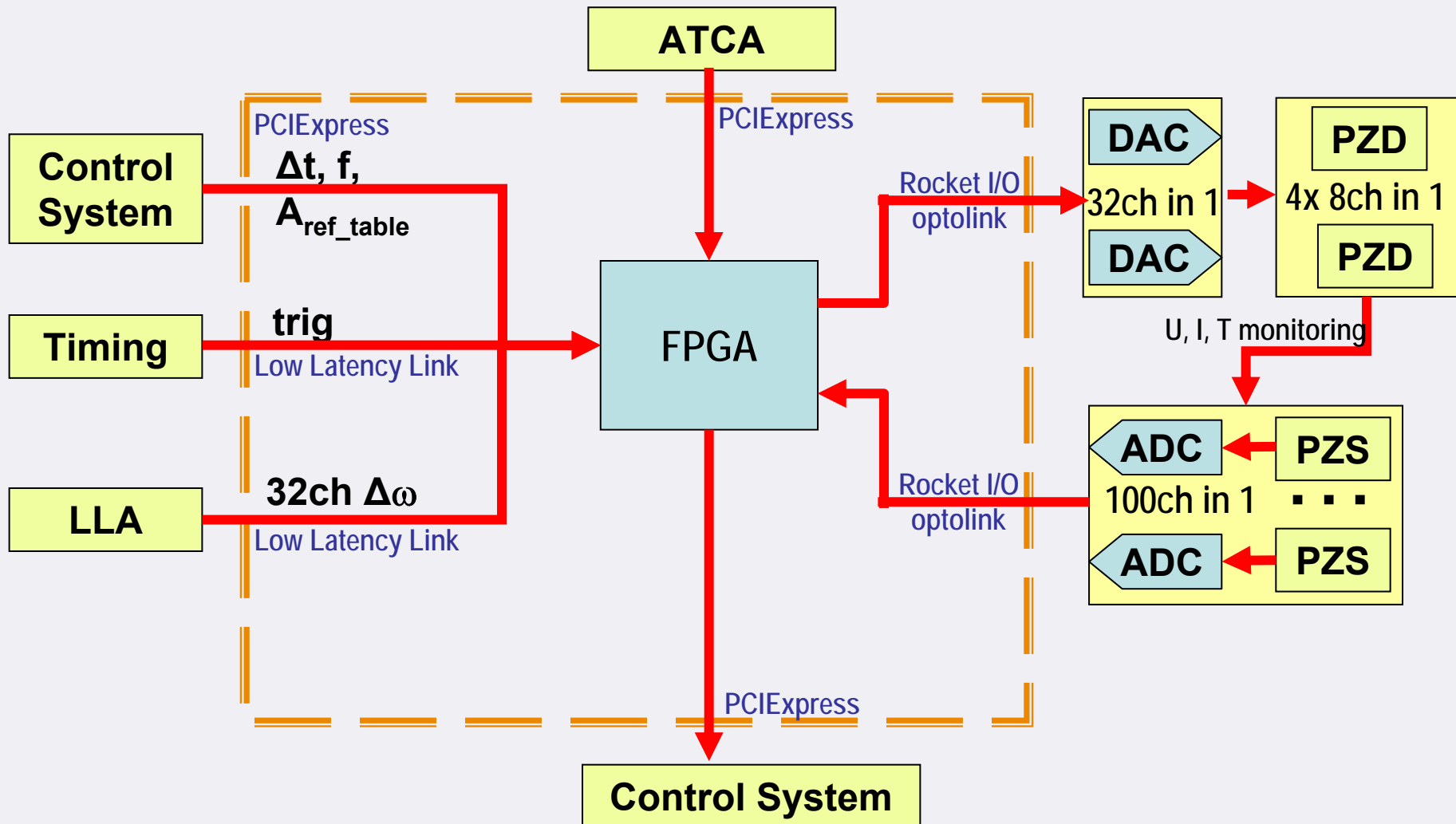
Piezocontroller - FPGA



Piezocontroller architecture for 32 cavities



Piezocontroller architecture for 32 cavities



Piezo Read-out (ADC card)

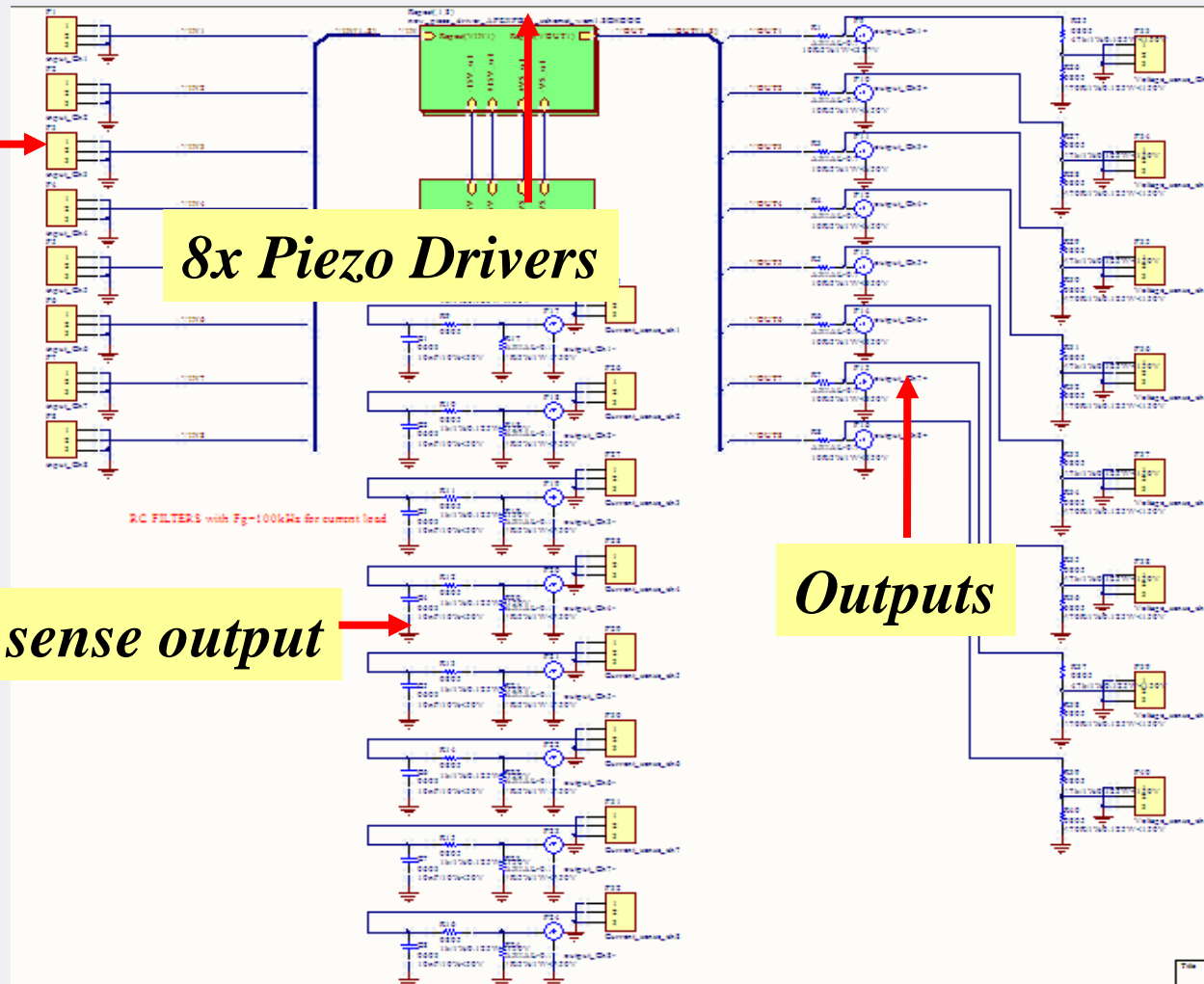
Main objective:

- read and adjust the impedance of piezoelements, which work as sensors in fast tuners,
- convert to digital representation

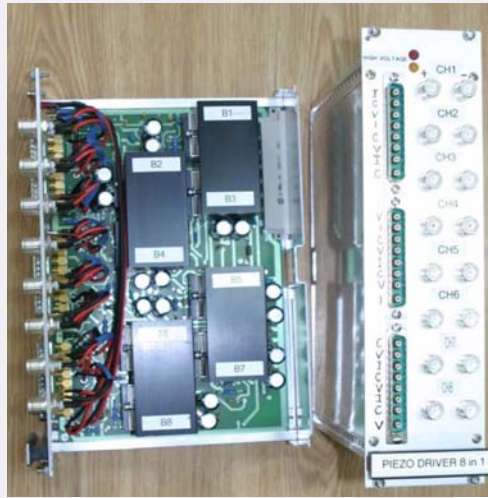
General overview:

- Standalone box (no ATCA, EuroCrate),
- close to PZD for exchanging piezostack functionality
- 32 analog input channels (for 4 cryomodules),
- 32 channel ADC (sampling higher than 10 kHz/channel)
- Optical Link to PiezoController for data exchange and board monitoring
- Piezo diagnostic (i.e. capacitance measurement)

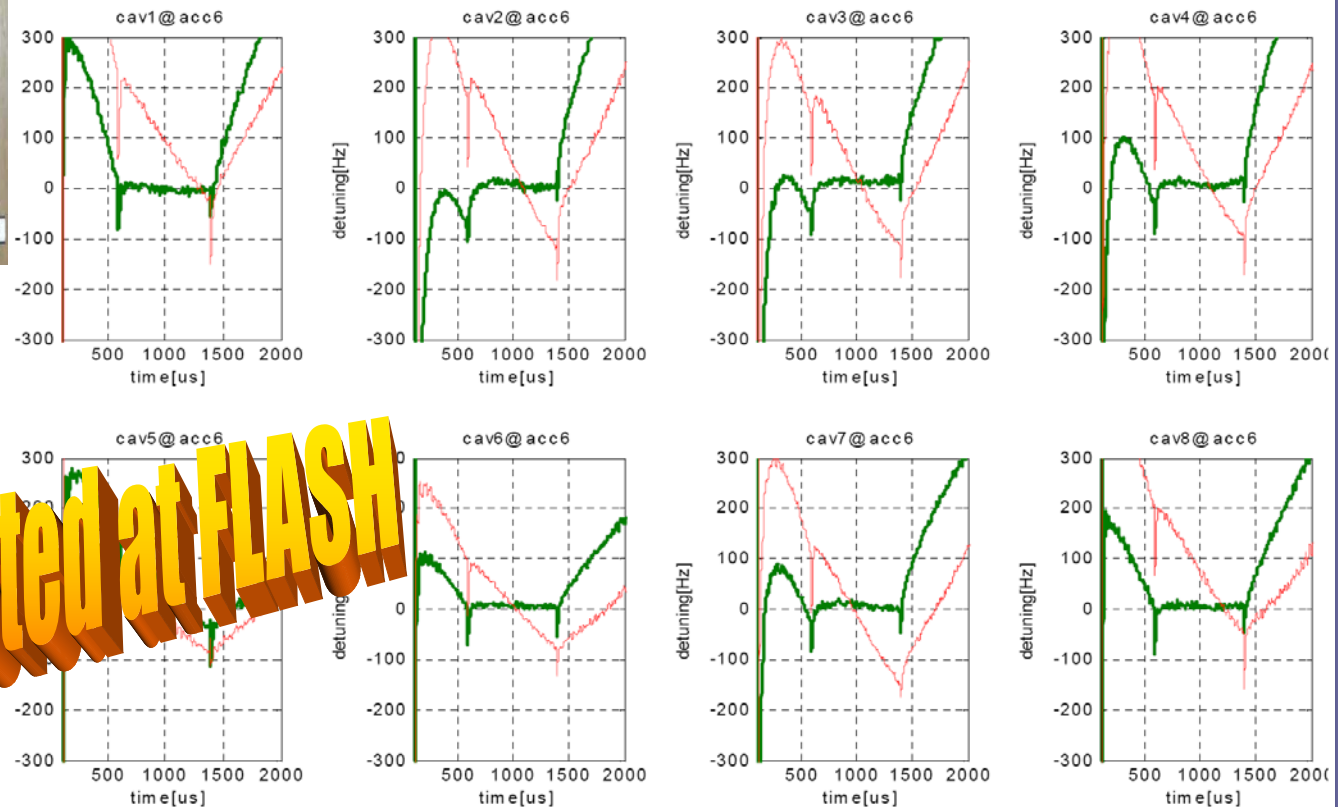
Piezodriver scheme



Results



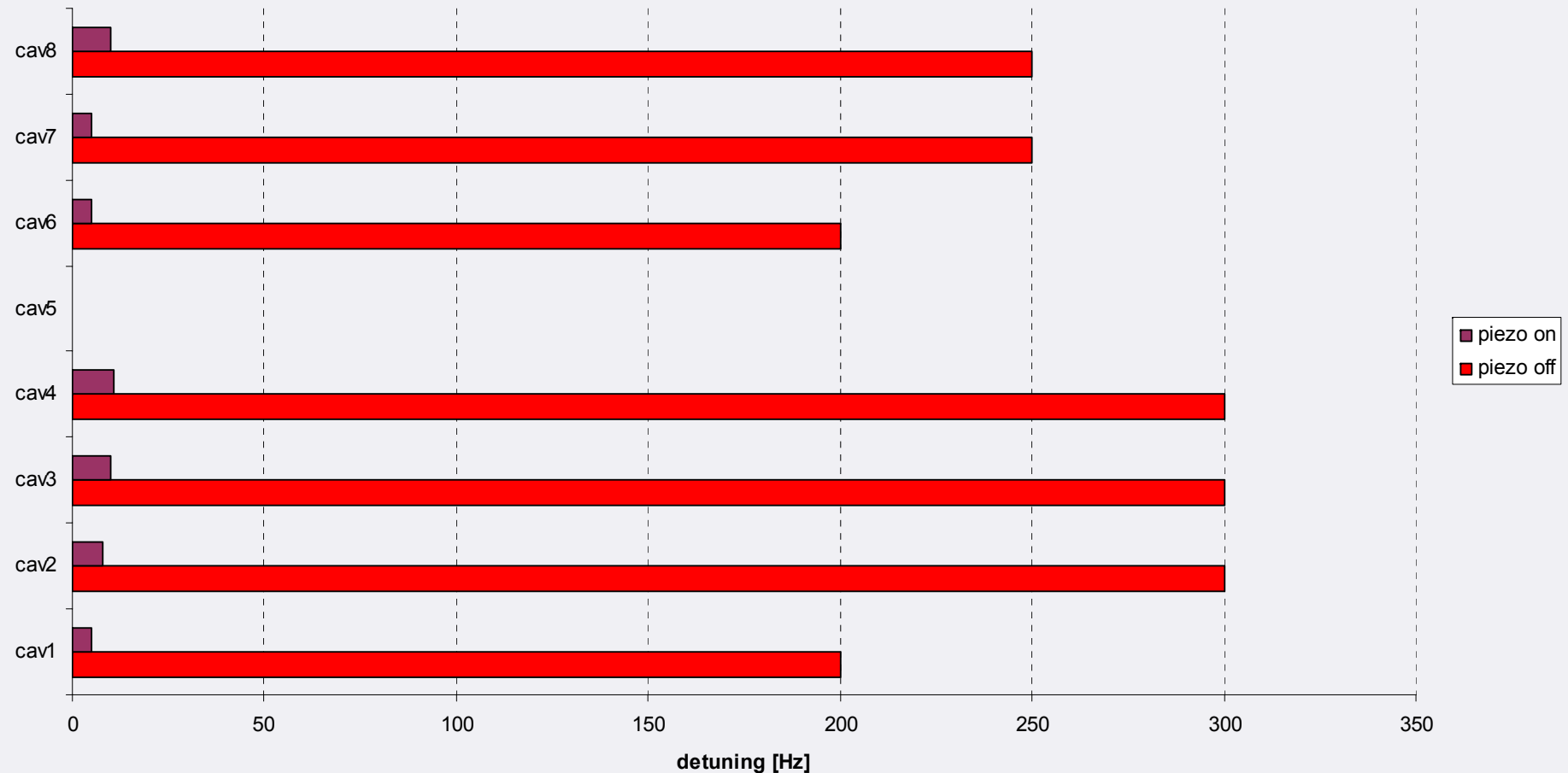
FLASH, ACC6 Acc. Grad = 22MV/m, Rep. Rate=5Hz

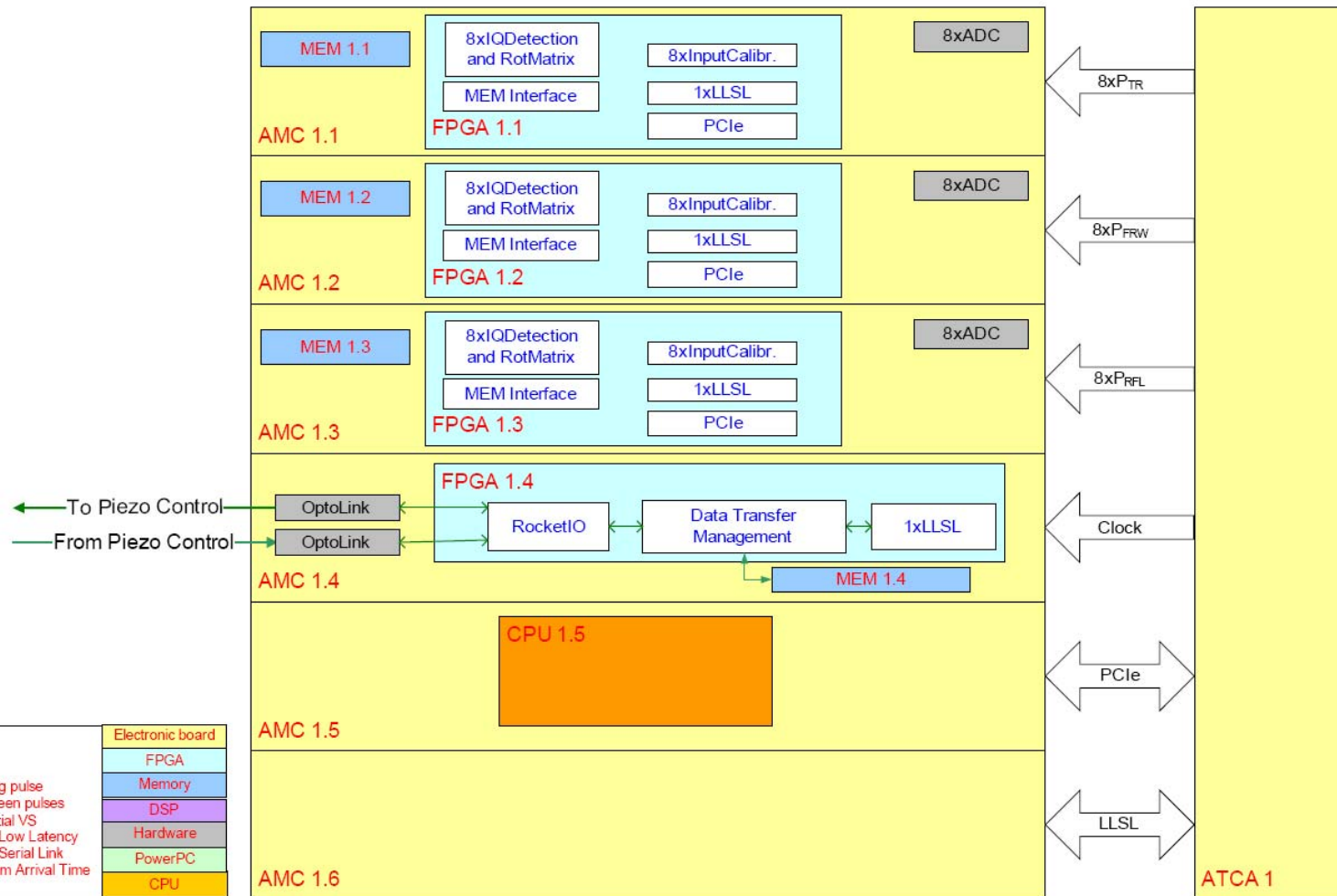


Successfully tested at FLASH

Results from ACC6

LFD compensation ACC6





PiezoController architecture

The feedback loop's latencies (including calculation) < 0.5 ms

The piezo-to-piezo feedback loop based on PID controller
(vibration cancellation between the pulses – BESSY experiments)

The detuning-to-piezo loop based on adaptive feed-forward
(short RF pulse in comparison to mechanical action of cavity)
BESSY experiments

OptoLink to DAC board and ADC cards

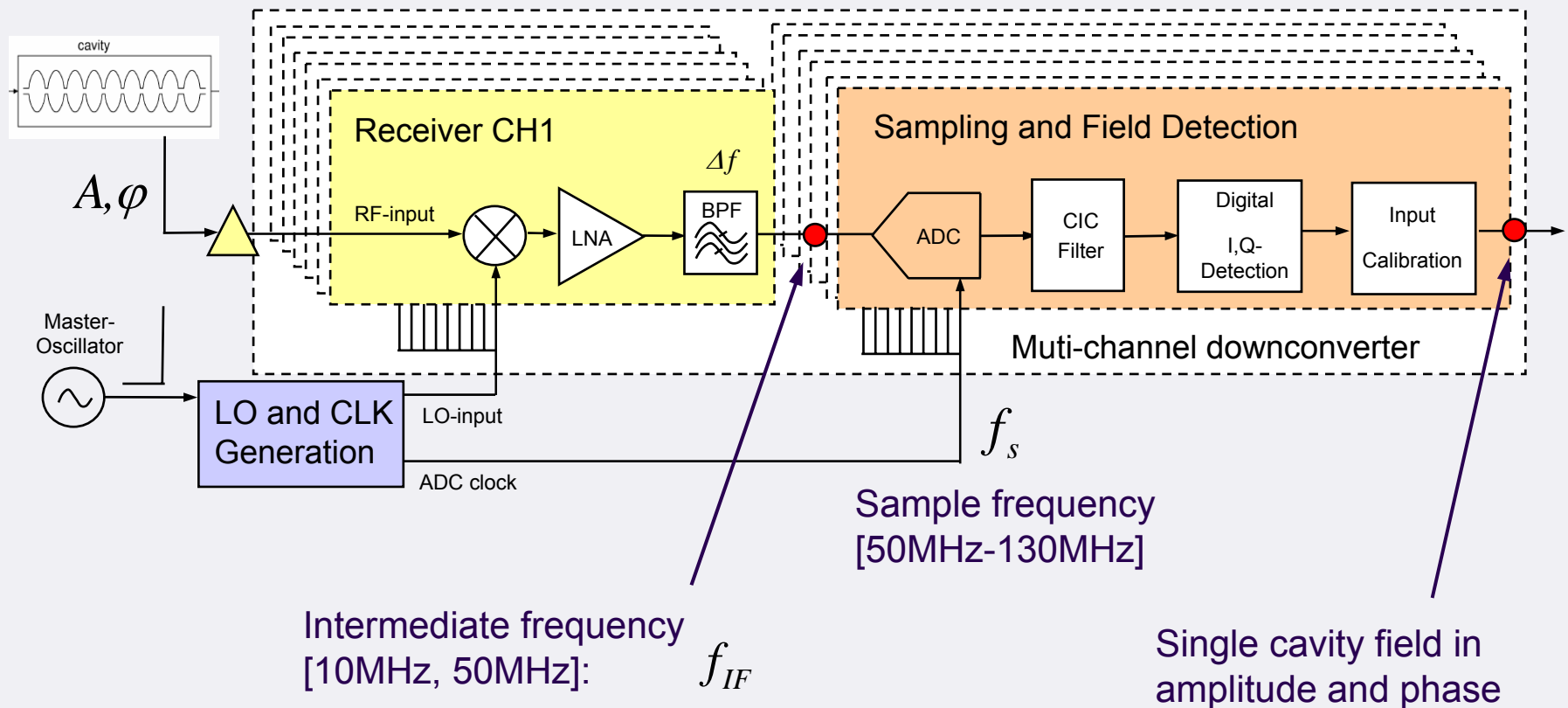
Piezo diagnostic (i.e. capacitance measurement)

Interlocks (i.e. protection (cut-off) when module is warm)

Downconverter



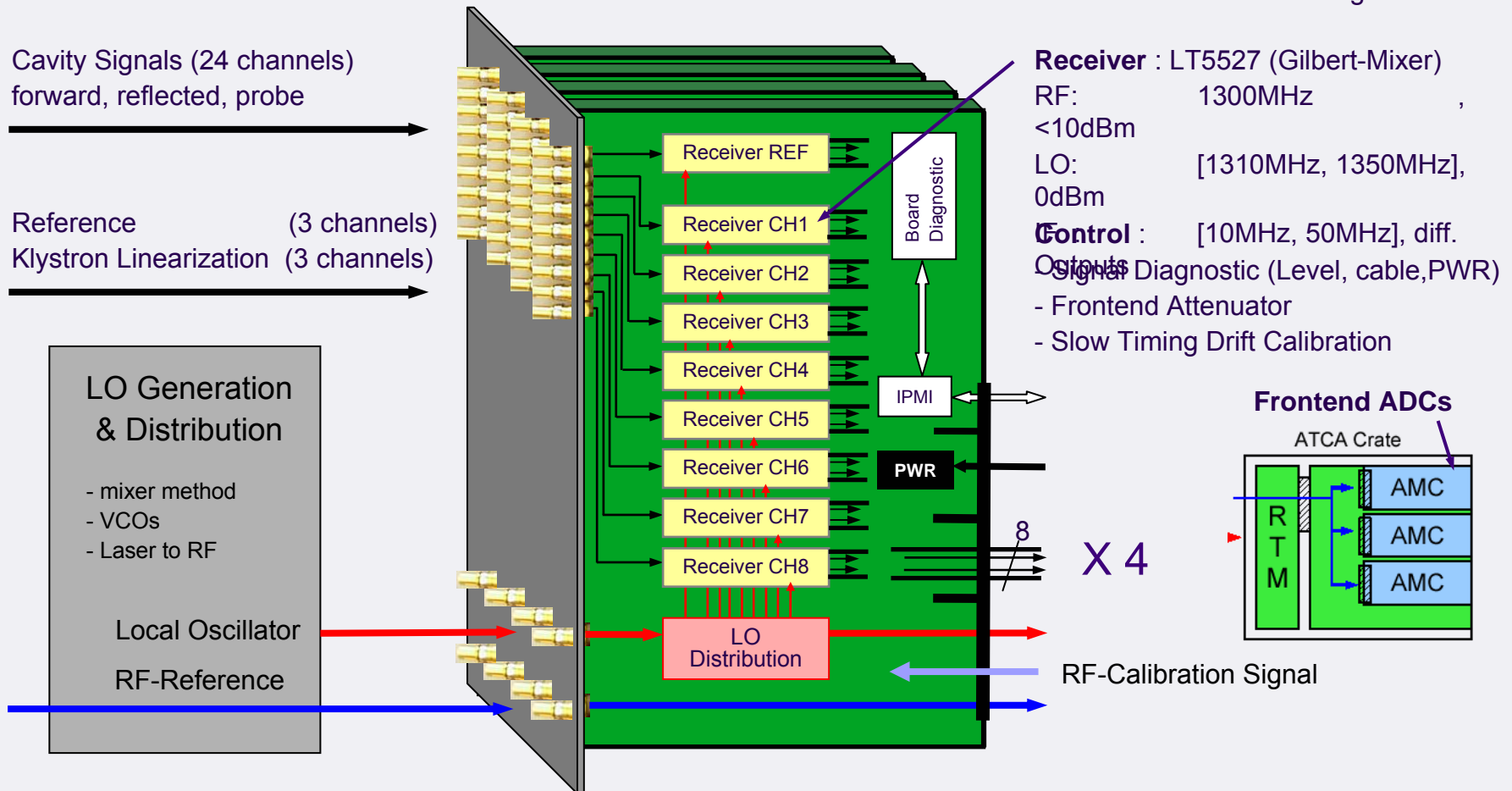
Downconverter for LLRF



Main and Booster Section Downconverter

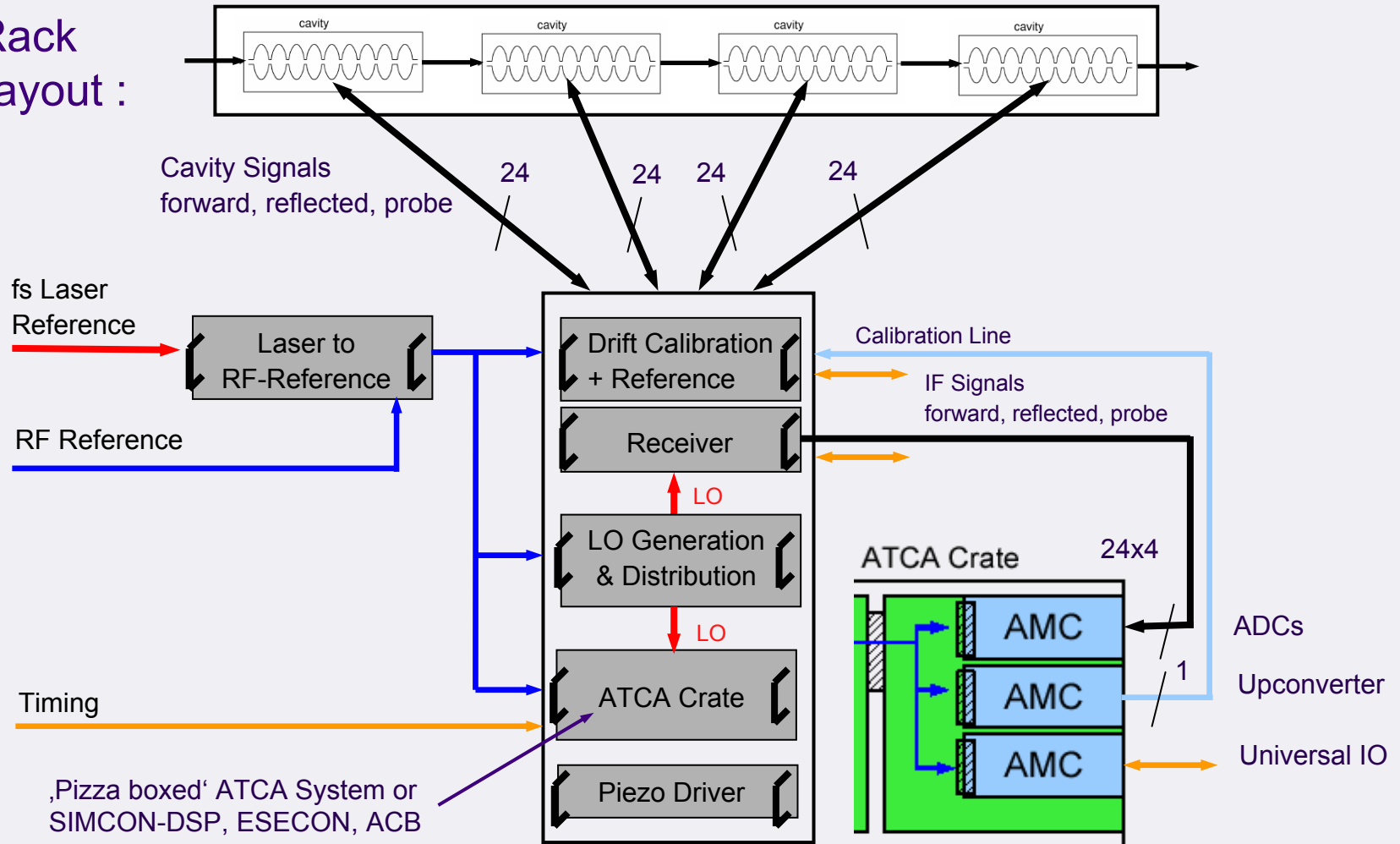
• Rear Transition Module (RTM)

Number of Receivers : 4x8, 4x12 or 4x16 depending on receiver cell size and PCB routing



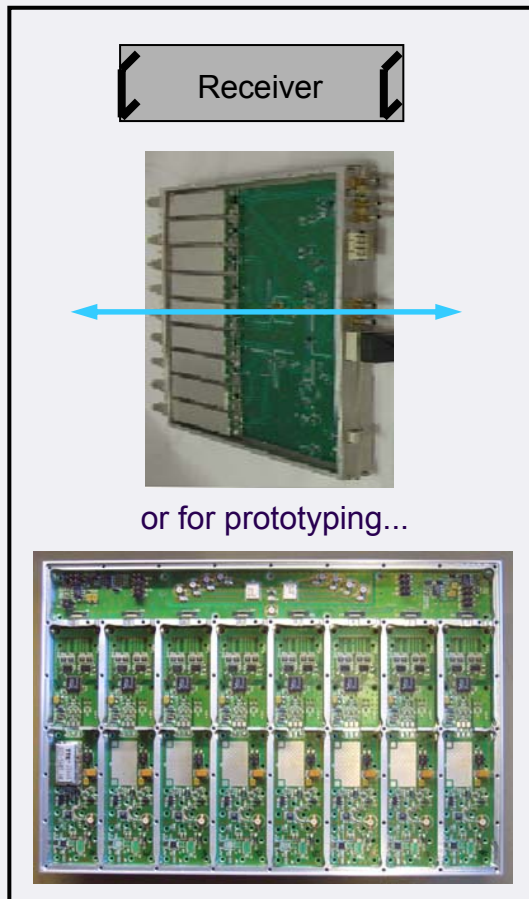
Injector and 3rd Harmonic Section Downconverter

● Rack Layout :



Injector and 3rd Harmonic Section Downconverter

• High Level Downconverter



1.3GHz Injector Receiver :

Passive high level mixer

RF: 1300MHz , 20dBm

LO: 1313MHz, 20dBm

IF : 13MHz (propose), single ended

3.9GHz Injector Receiver :

Passive high level mixer

RF: 3900MHz , 20dBm

LO: 3939MHz, 20dBm

IF : 39MHz (propose), single ended

Features :

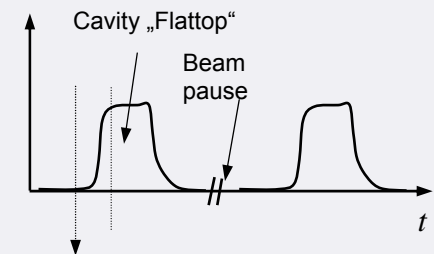
- Needs more than +20dBm LO Power
- Required space more than VME sized (Stripline design, directional coupler...)
- Amplitude/Phase noise <0.01%, <0.01 deg
- Easy servicing and investigation of LO and IF
- Individual Power Supplies

Automated Drift Calibration

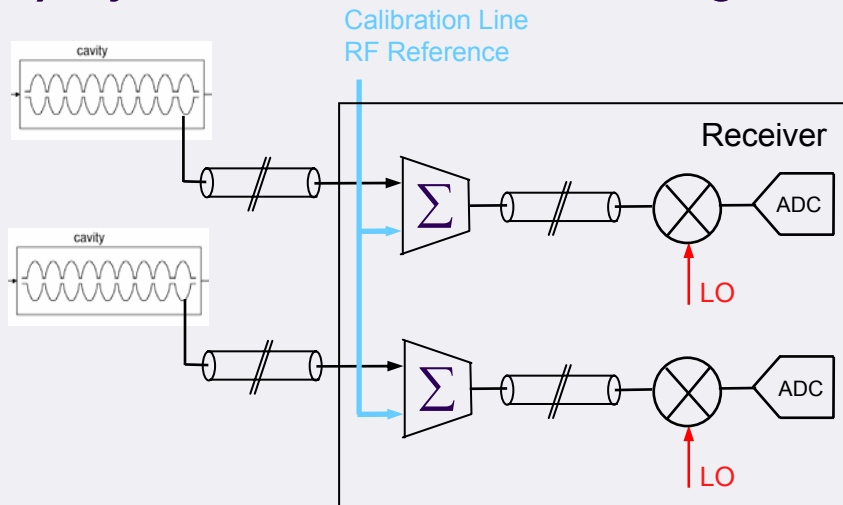
A drift compensation is needed to compensate drifts from

- Cavity pickup cables (4 module) $5 \text{ fs m}^{-1} \text{ K}^{-1}, \pm 125 \text{ fs K}^{-1} (\pm 25 \text{ m}), \Delta T \approx 1 \text{ K}$
- Downconverter (mixer) $\theta_A = 2 \text{ e-3}^\circ \text{ C}, \theta_P = 0.2^\circ \text{ C}$
- LO generation (dividers, amplifiers, filters) (Injector)
- ADC CLK generation (timing system, less critical)

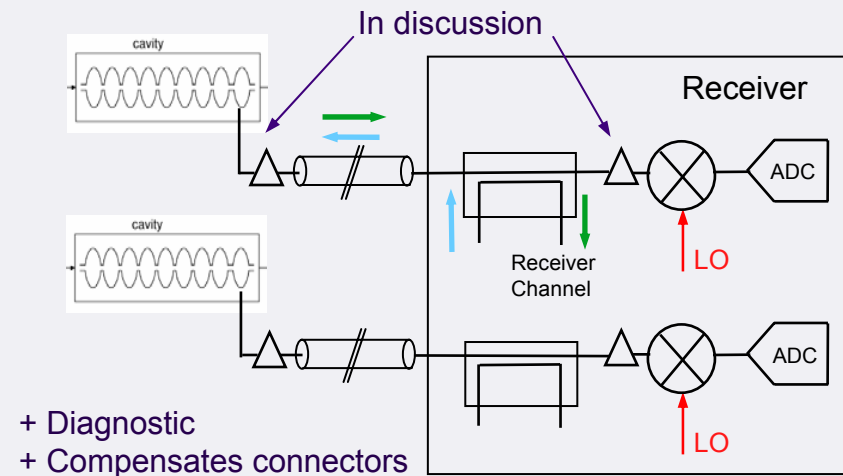
to have a robust machine operation.



1) Injection of the reference signal :

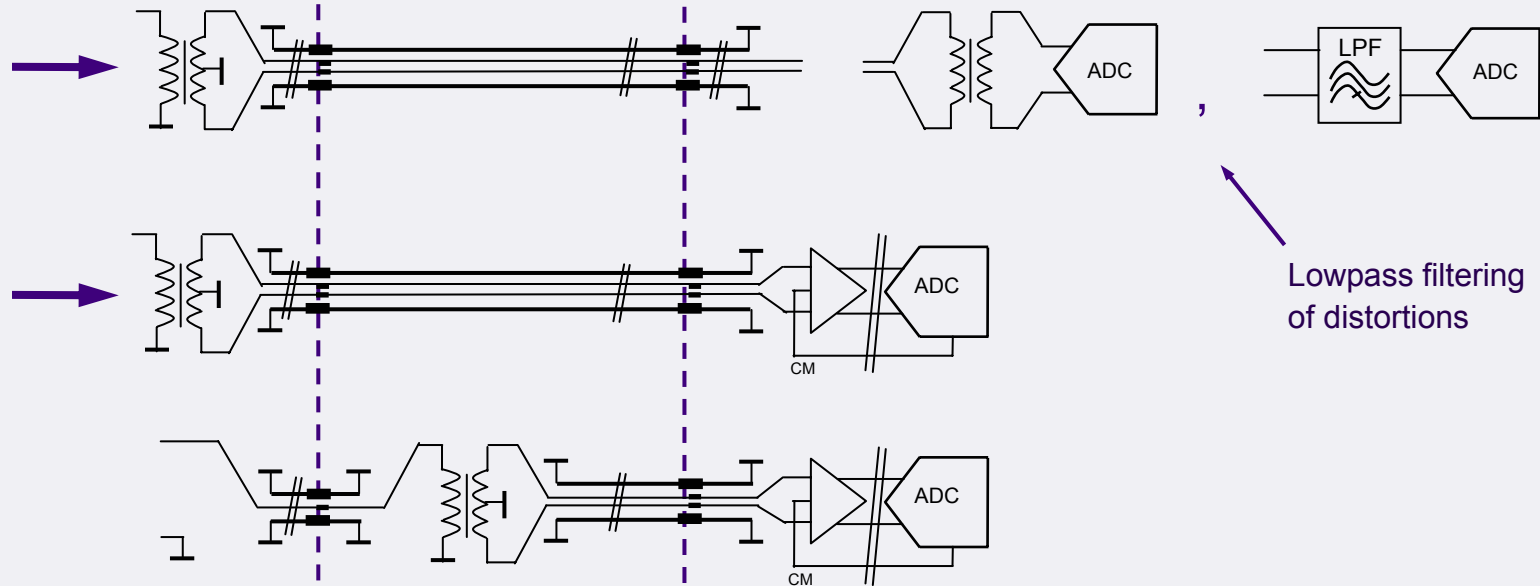


2) Reflection at the cavity :



Problems to be solved

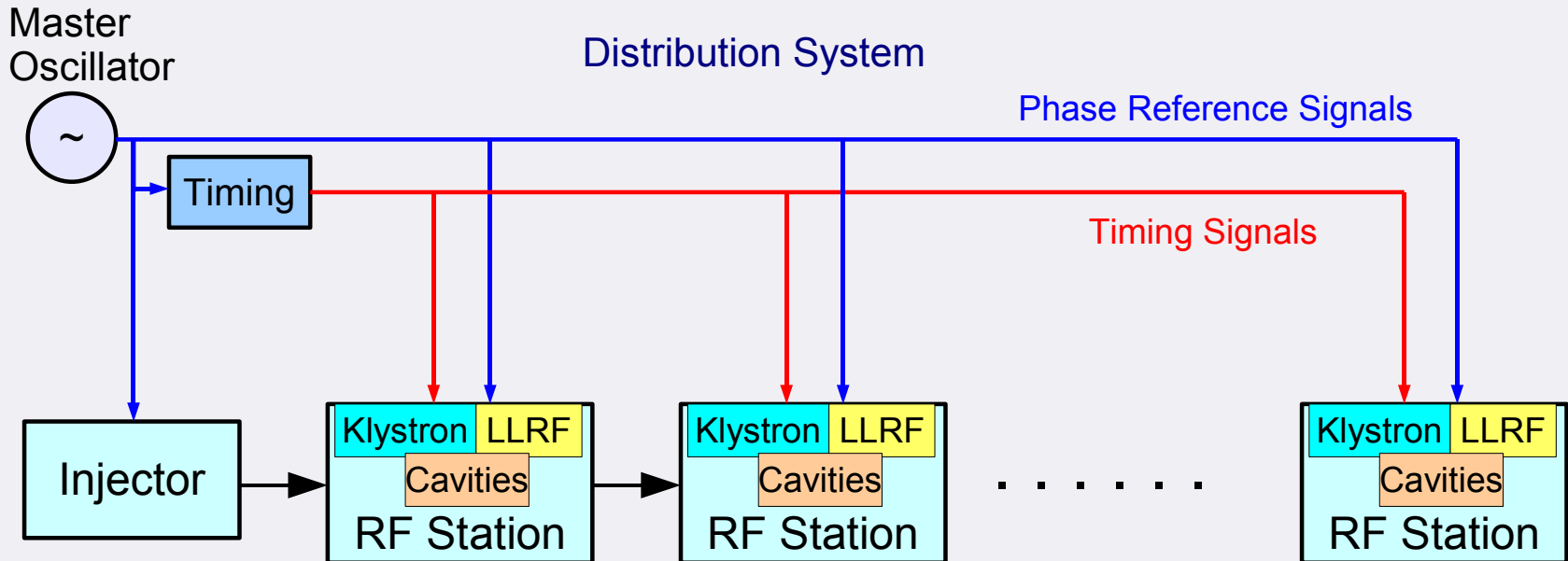
- Distribution within crates :
 - Interference from high-speed digital circuits
 - RTM | ATCA | AMC diff. / single ended interfacing ?



MO and Distribution

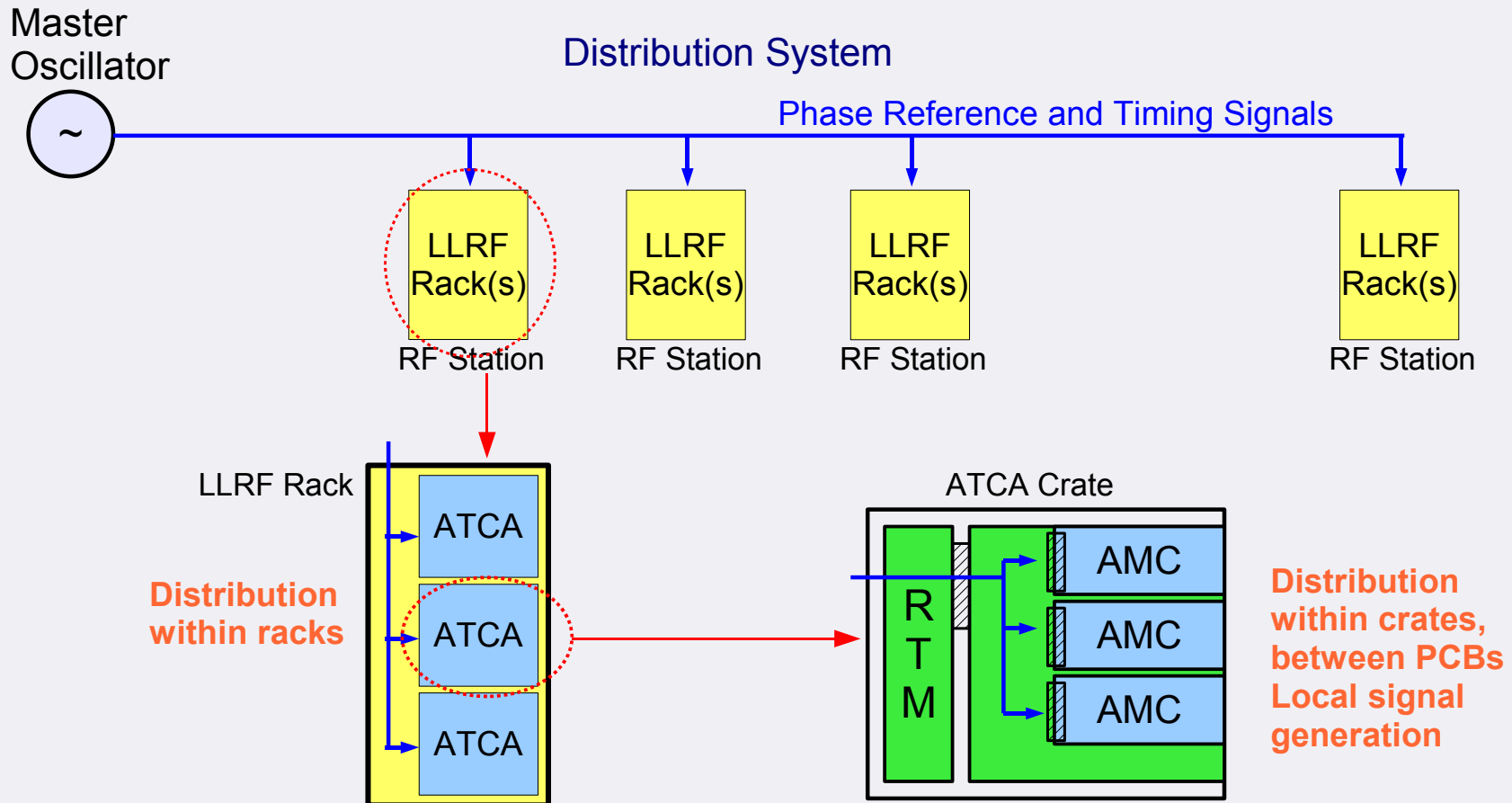


Need for Precise Synchronization



- Electronic devices should be synchronized with high accuracy
- Required jitter for phase reference signals:
 - 0.1 ps short term (10 fs at some locations in XFEL)
 - 1 ps long term

Global and Local Distribution



Problems

- Global: choice of distribution frequency
- Distribution within racks: choice of cables and connectors
- Distribution within crates:
 - Stable distribution in multilayer PCBs and dense connectors
 - Distribution between PCBs, problems with terminations when PCB removed
 - Interference from high-speed digital circuits
- Local signal generation
 - Building a circuit generating required signals from the distribution frequency with satisfying accuracy

AMC Clock Synthesizer and Timing Module

Objectives:

- Synthesize ADC clock signals from the MO signal
- Receive signals from the FLASH timing system and provide trigger signals for FPGAs

Module will consist of two PCBs:

- “Analogue” part (bottom): receiver and synthesizer. Designed by M. Ladno and K. Czuba
- Digital part: control and interface for the analog part. Universal module (top) with FPGA designed by D. Makowski

Requirements for the AMC Timing Module

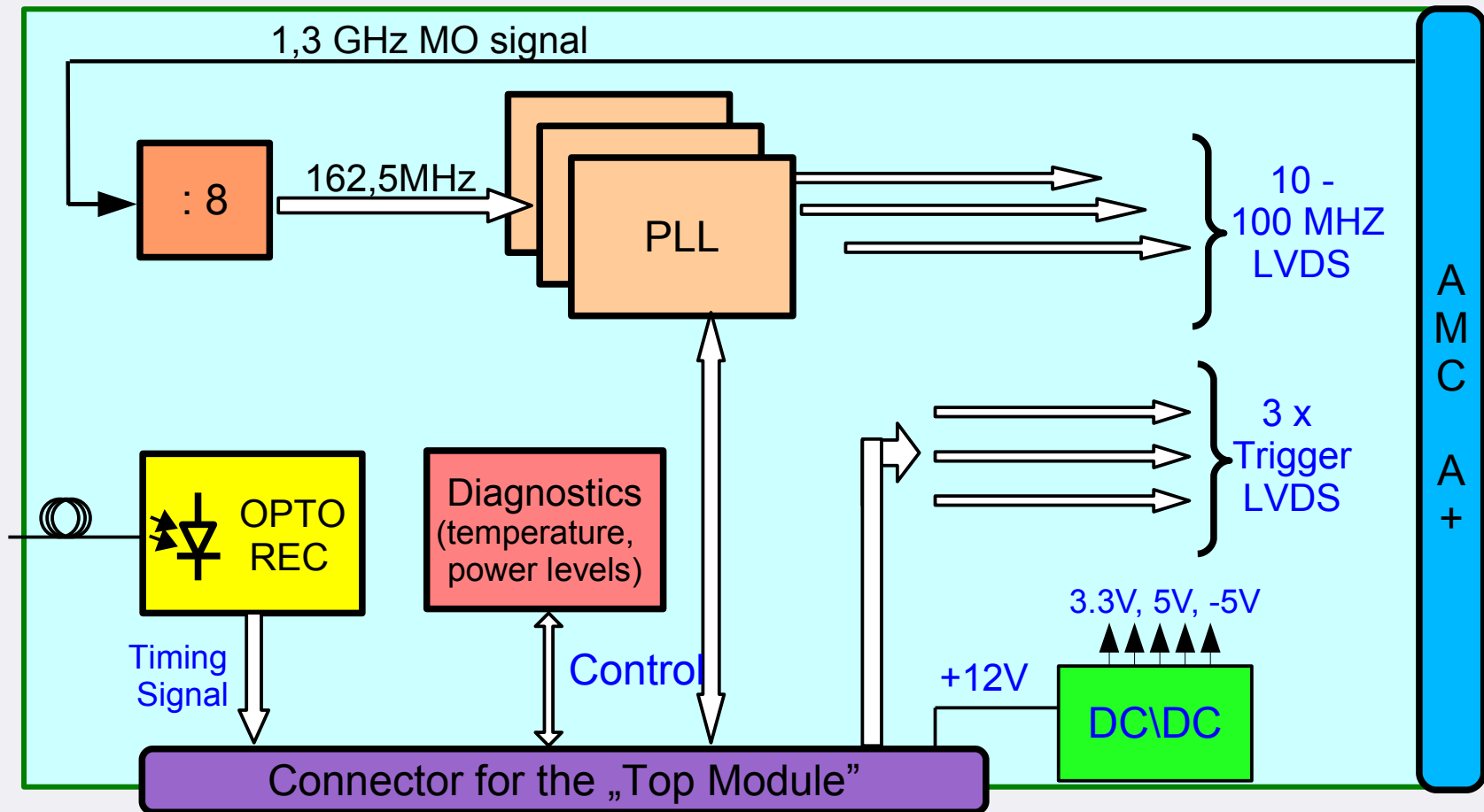
Clock synthesizer requirements:

- Input signal: 1.3 GHz from MO
- Output clock frequencies: 10 MHz – 100 MHz, 0.1MHz step
- Clock stability <5 ps, (desirable < 2ps)
- 3 independent clock outputs (LVDS bus)

Timing Receiver requirements:

- Receive and decode timing signals from the existing FLASH timing
- Optical input (at front panel)
- 3 independent trigger outputs (LVDS)
- Mode with self trigger generation (trig freq. 0.1 – 33 Hz)

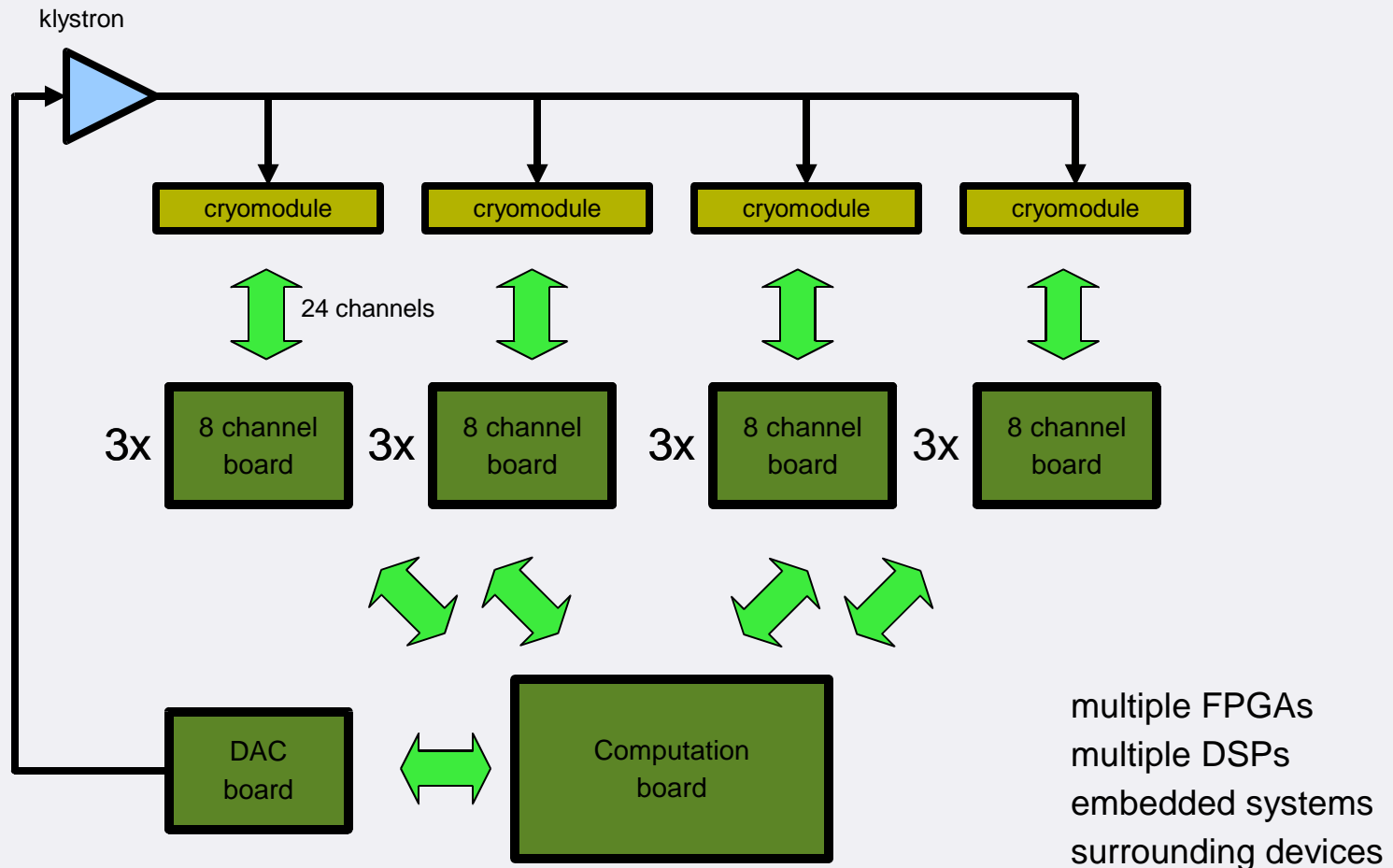
Block Diagram



Software Architecture



Overview of the distributed system

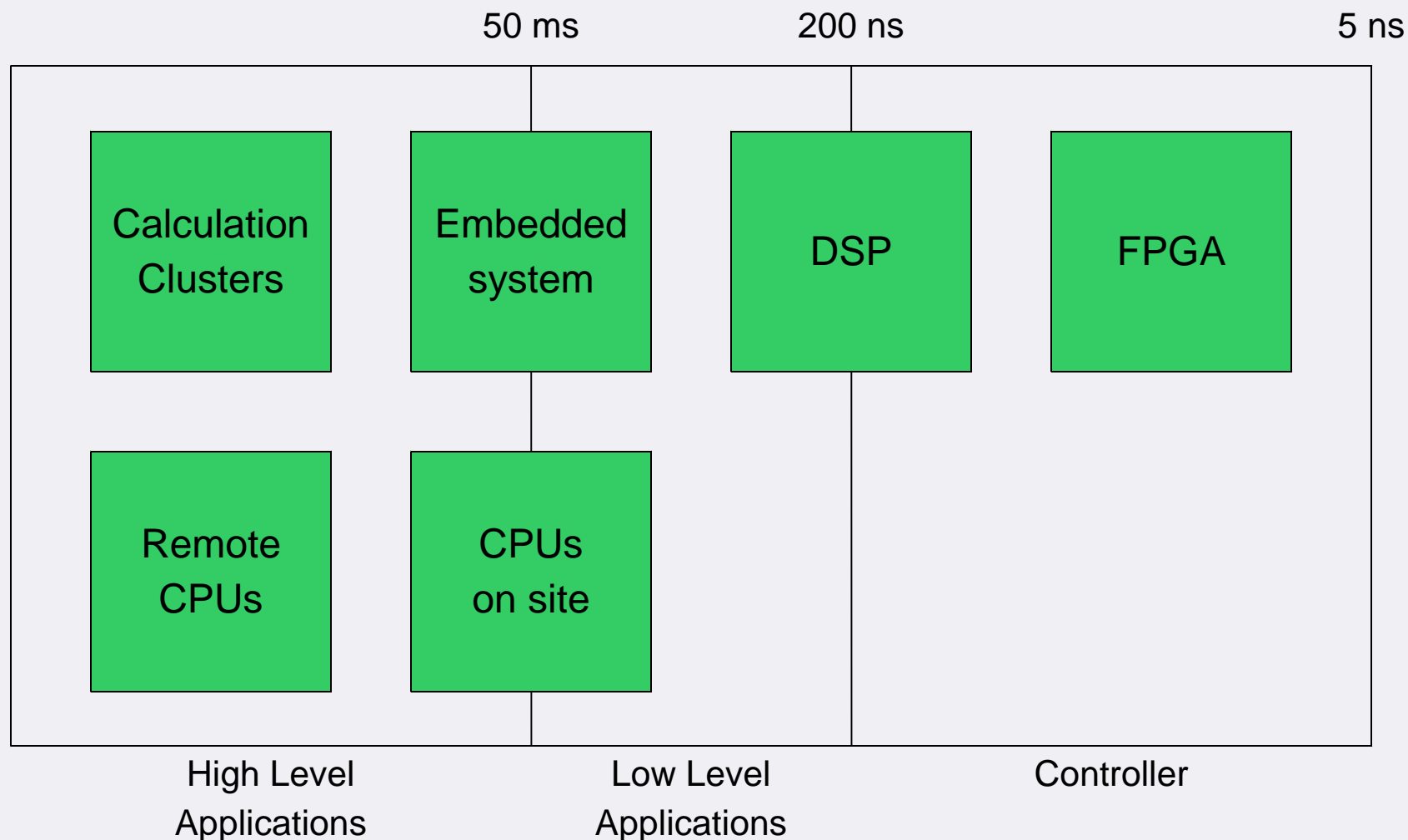


Requirements

The software architecture must fit to the distributed and redundant hardware platform.

The scheme must integrate and interact with all possible applications to allow them to fulfill their requirements.

Possible algorithm locations



Definitions of different software groups

Controller

The controller is the element of the system which has direct influence on the RF station. The main task of this application is to provide RF power to the cavities in a controlled way. During normal operation it controls vector sum of the cavities with a given precision. To achieve that, its reaction time must be as short as possible. Moreover, it provides interfaces for other software components giving them possibility to change the RF field parameters.

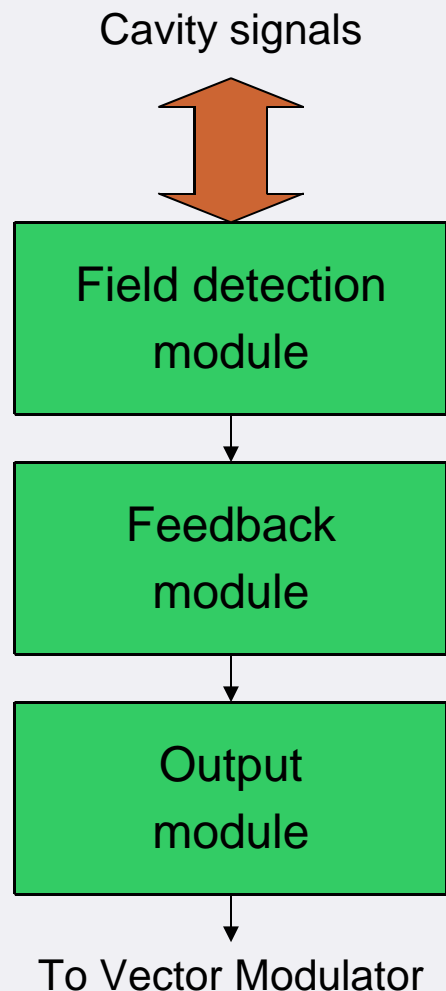
Low Level Applications

This is a set of applications designed mostly to execute algorithms and measurements between pulses. Parameters calculated during that time can be uploaded to the controller and used in the next pulse. These applications may also function as support to the controller during on-line operation. In this case, only DSP processor can be considered – other elements of the system cannot meet timing constraints.

High Level Applications

This is a set of applications designed mostly to run in the background of working system in long execution intervals. Parameters calculated by these algorithms are uploaded to the controller every few pulses. The main execution platforms for these applications are control servers and computation cluster.

Controller



Computation Pipe of the controller

- detection of the components of the field
 - I-Q
 - Amplitude, Phase
- parametrized control function
 - P-I-D
 - MIMO
- output corrections
 - klystron chain linearization
 - beam load compensation
 - etc.

Piezo Control

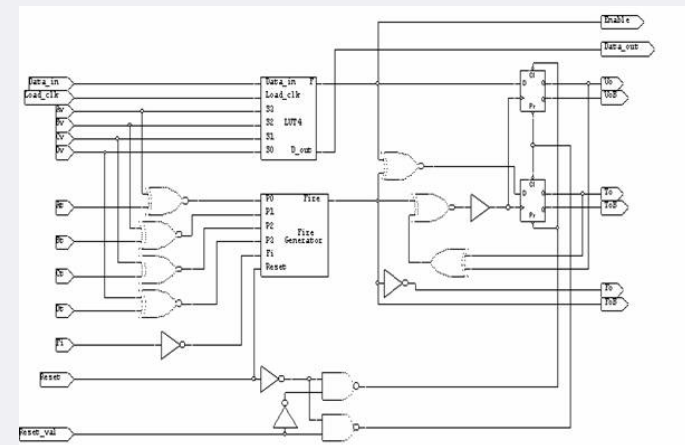
The **controller** is used for interaction with RF part of the RF station. The piezo sensors and actuators are handled by **piezo controller**. It executes algorithms and measurements related to the detuning and microphonics compensation.

The **piezo controller** implemented on the separate hardware platform with high analogue channel count interacts with the **controller, low and high level applications**, using dedicated interfaces.

Low Level Applications

This includes:

- Adaptive Feed-Forward
- System Identification
- Loop gain and loop phase calculation
- detuning and loaded Q calculation
- Vector sum calibration
- Beam Diagnostic
- Exception Detection and Handling

[illegible]

High Level Applications

This includes:

- Adaptive Feed-Forward
- Vector sum calibration
- Beam Diagnostic
- Automated frequency tuning
- Exception Detection and Handling
- RF-Gun control



Applications summary

The functionality of the low and high level applications overlaps.

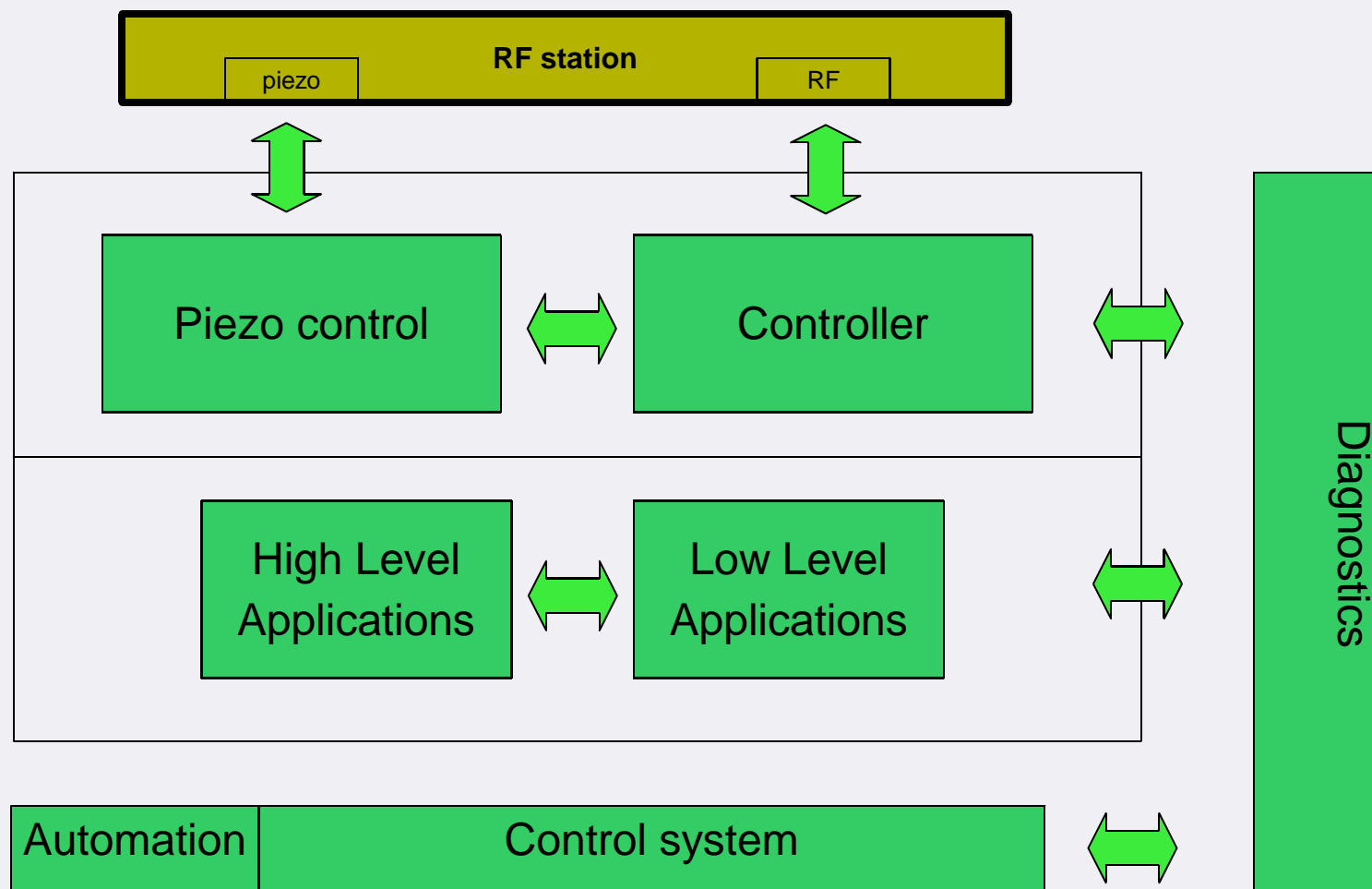
So how can we know where to put given algorithm ?

It depends on our timing constraints:

if we want to execute given algorithm **as fast as possible** (during a pulse or just between) it should be implemented as low level

if we want to execute given algorithm **with extended precision and functionality** we implement it as high level

Software layout

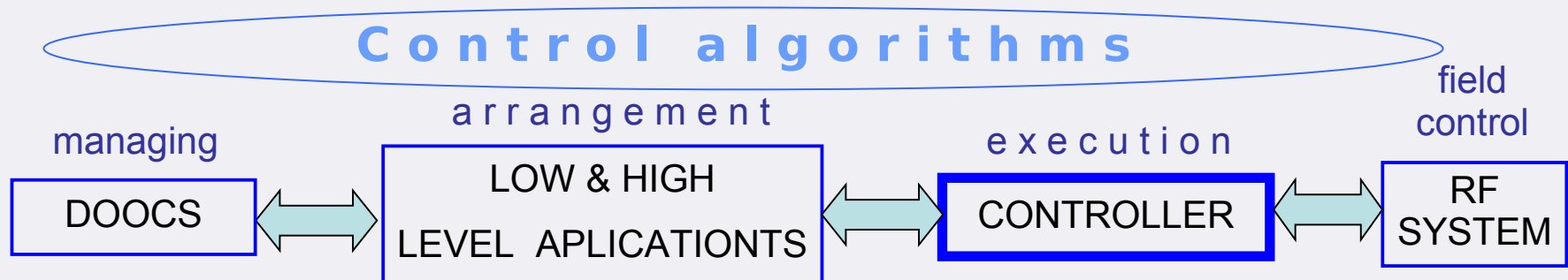


Controller I (Warsaw)



Controller definition

Simple & low latency automat stabilizing the amplitude & phase of electrical field during the single pulse



TASKS:

- Execution of control algorithm basing on Control Data provided by Low Level Applications and on results of measurement of the Input signals.
- Providing of processed measurement data to the Low Level Applications layer
- Monitoring and Exception Handling for safety requirements

Requirements for the controller

- Basic technical requirements
 - Multiple input channels
 - Low latency (as low latency as possible, however it depends on IF and technological limits)
- Modular, parametrized and reconfigurable structure
 - Modularity - It should be possible to distribute the design between a few AMC boards, and even between a few ATCA carrier boards (however it will impose some additional latency)
 - Parametrized – the number of memory blocks, of DSPs used, of input channels serviced may be changed without significant redesign
 - Reconfigurable – the general structure of the controller will be stable, even if some blocks are moved from FPGA to DSP.
- Design methodology related requirements
 - Controller is supposed to be a complex system, to assure high maintainability e.g. to avoid human errors the automatic implementation methods (DSP on FPGA, DOOCS integration) must be developed
 - Full testability is needed (in simulation, with real hardware, with hardware-software cosimulation)

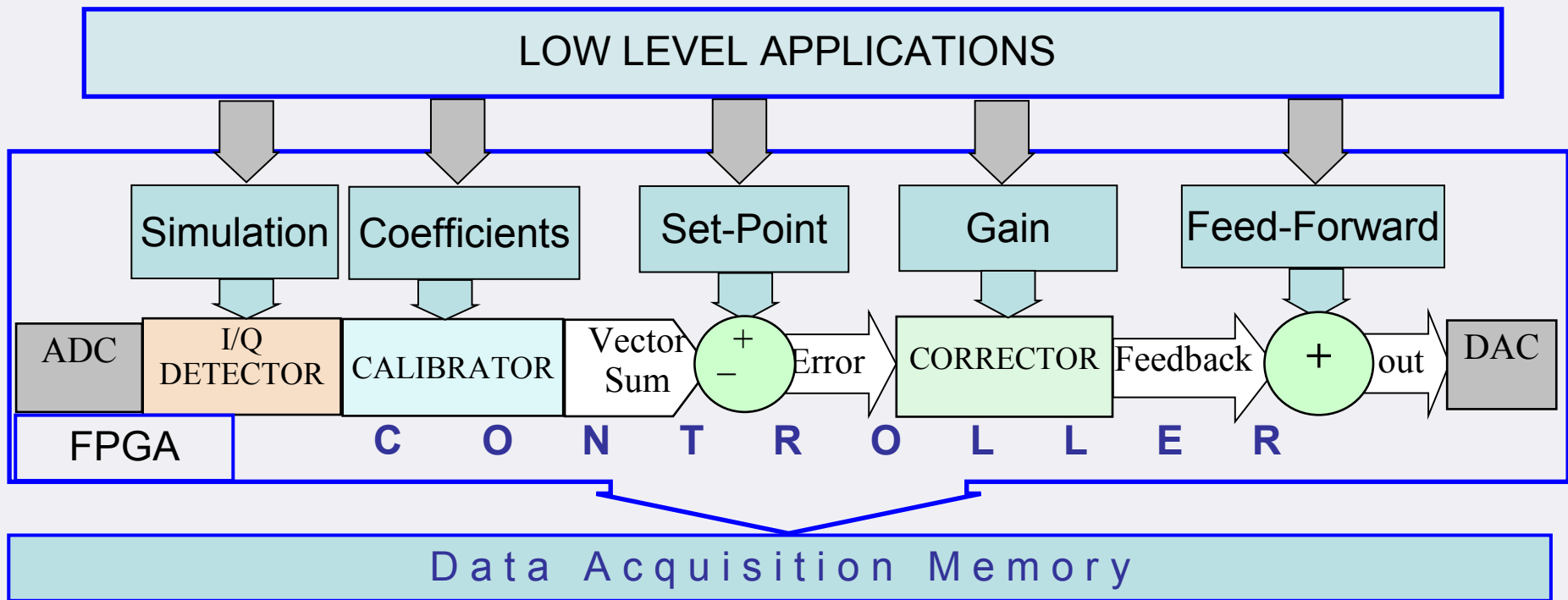
Reliability requirements of the XFEL controller

- Required: Continuous operation, one maintenance day per month
- ATCA provided functions for increased availability:
 - Redundant power supply
 - Full mesh topology – no global bus for boards' interconnection, which could be blocked by a damaged board
- Controller design features contributing to increased availability
 - Algorithm able to operate even when some analog inputs are failed
 - Use of redundancy in the analog input signals
 - Use of feed-forward alone as the „last resort solution”
 - Possible redundant implementation of the controller
 - Cavity gradient monitoring with exception handling

Functional requirements for the controller

- Channel calibration
- Rotation matrix
- Vector sum
- Error calculation
- Feed forward
- Generation of output signals with klystron linearization
- Provision of measured data for:
 - Low Level Applications layer for updating of Control Data for the Controller
 - For monitoring (DOOCS) and diagnostics (Exception Handling)

Functional Concept of Controller

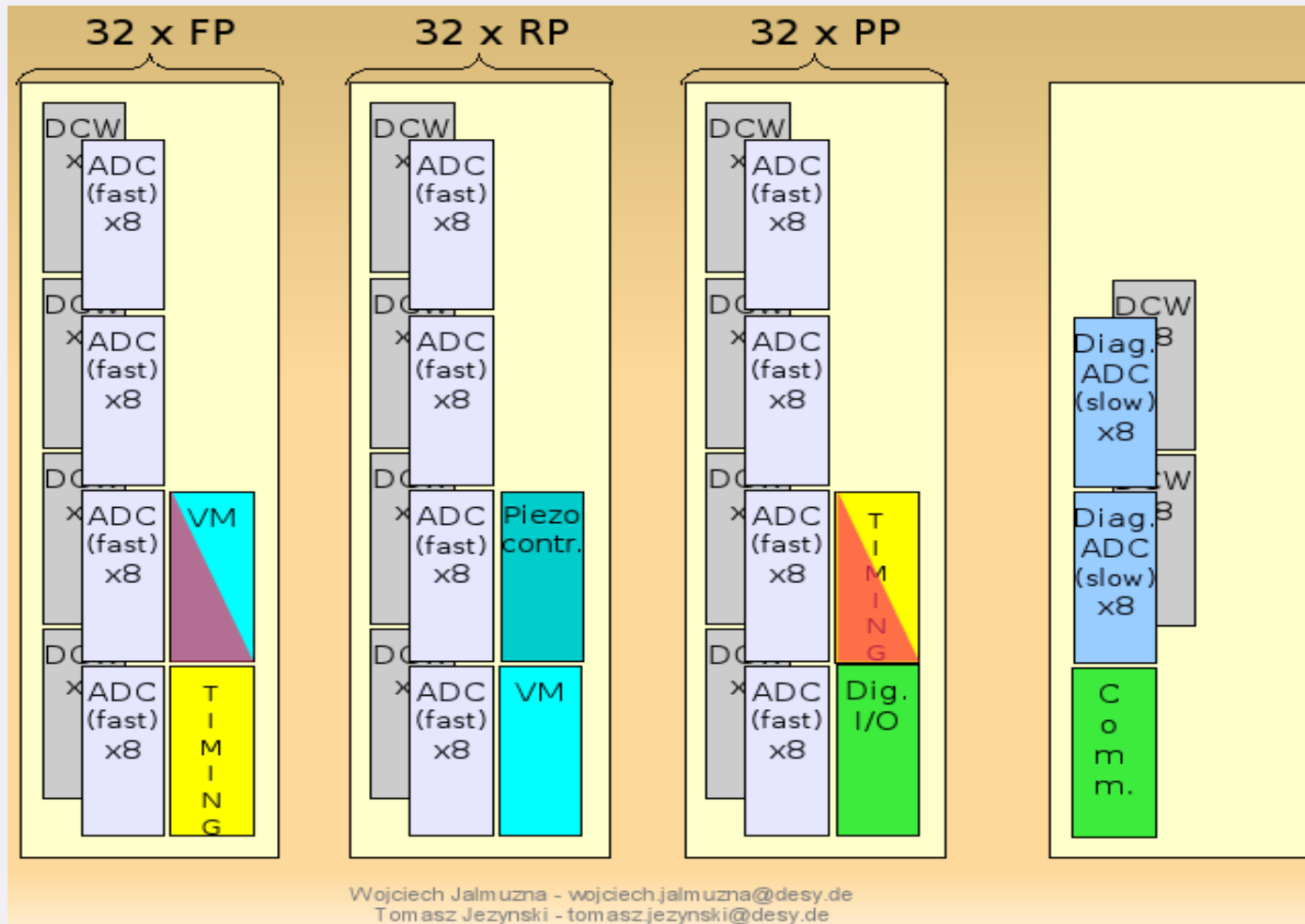


Multiboard implementation of the controller

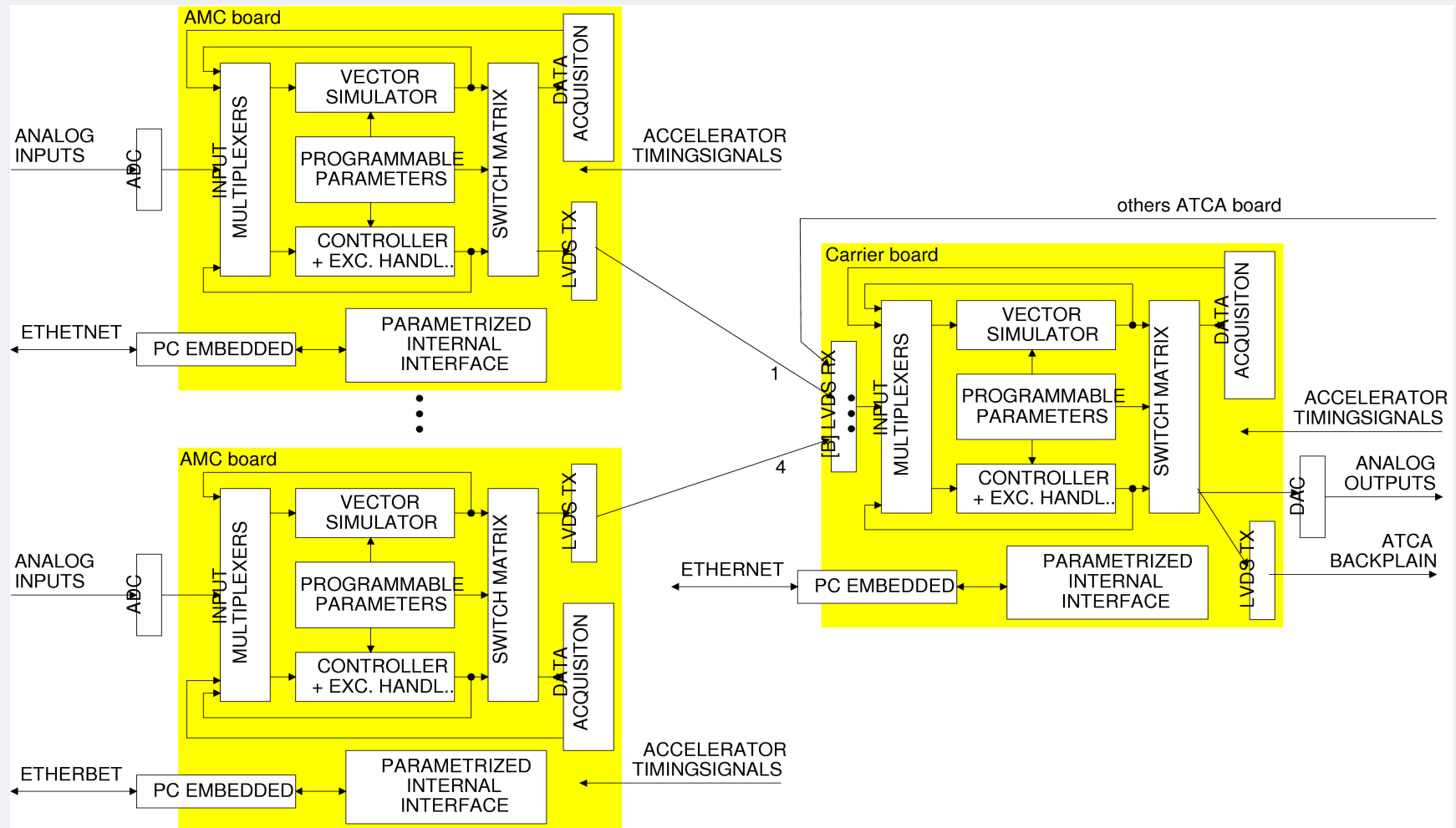
- Single board implementation impossible:
 - Main problem – multiple A/D converters (96 channels needed)
 - reasonable limit: 8 or 12 channels/board
- It is necessary to transmit the converted signals between the boards
- If possible, it will be preferable to split the algorithm between the boards

Proposal of distribution of the LLRF system

(LLRF Team, presented by T.Jezynski and W.Jalmuzna)



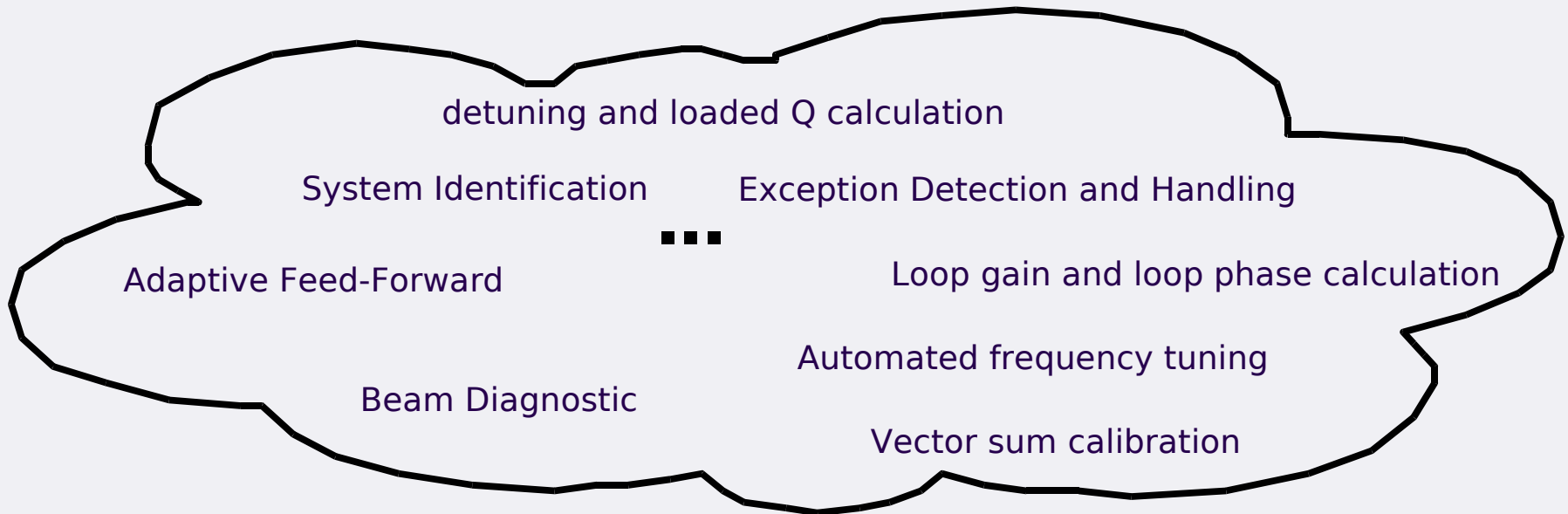
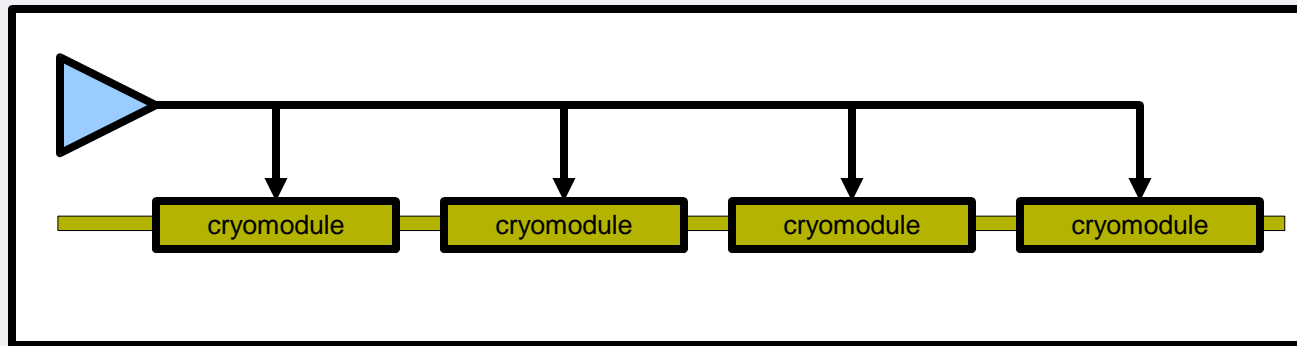
Structure of the ATCA LLRF controler



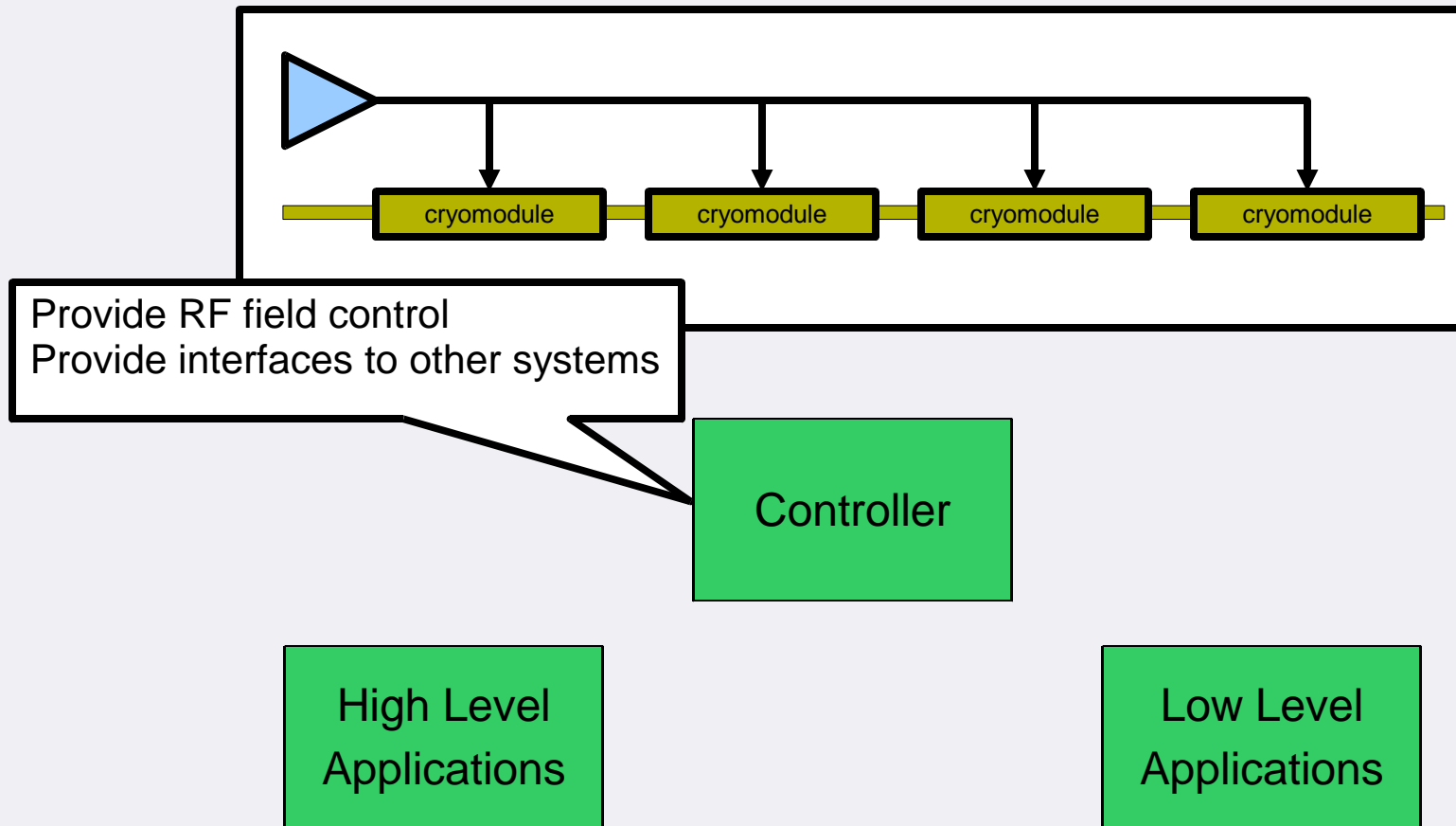
Controller II (Lodz)



Introduction



Introduction



Basic Requirements

The controller must provide RF power for RF station in the controlled way, using different operation modes.

The supported operation modes are:

- **Control mode** used for control of the RF field with a given precision
- **Diagnostic mode** used for measurement of basic parameters of a single cavity.

Control Mode

When using **control mode** additional requirements must be fulfilled:

The controller must work with open loop.

*The controller must work with closed loop using
different transfer functions.*

Diagnostic Mode

When using **diagnostic mode** additional requirements must be fulfilled:

The controller must work in SEL mode
with amplitude and phase lock.*

The controller must work in Frequency Sweep mode.

*) SEL – Self Excited Loop

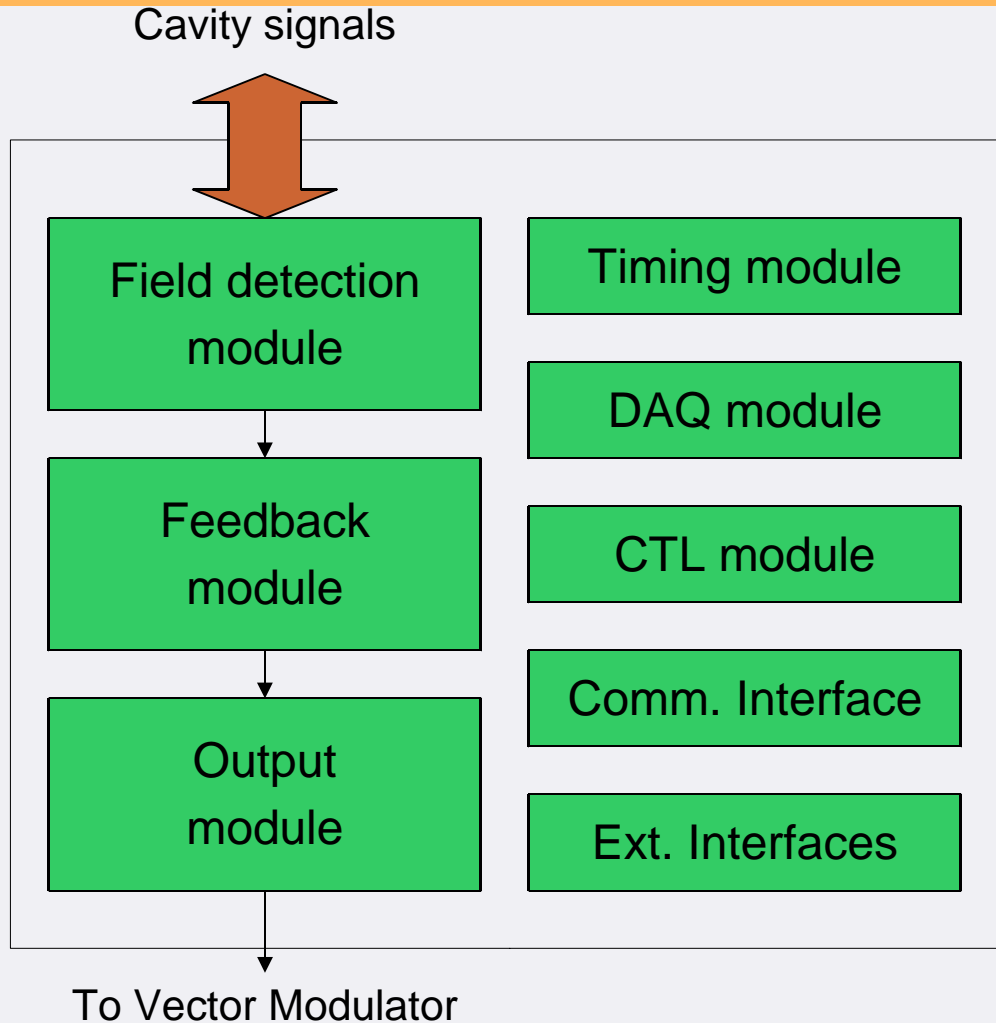
Basic Requirements

The controller must provide interfaces for algorithms and applications implemented as part of other Work Packages.

These include:

- **Low Level Applications**
- **High Level Applications**
- **Piezo control**
- **Control system**
- **Diagnostics**

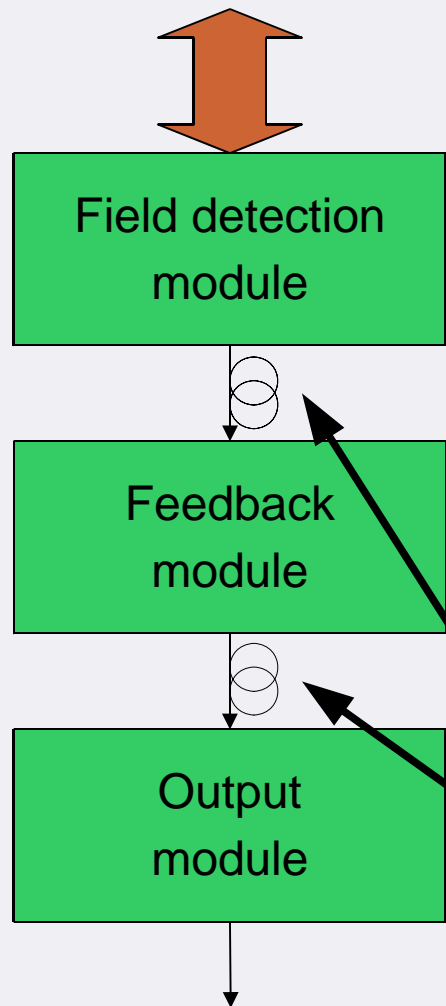
Structure of the Controller



The **computation pipe** of the controller was divided into 3 subcomponents

Additional components provide means of communication with the external environment.

Structure of the Controller



Each part of the controller can be implemented on the separate board (or separate FPGA chip). The field detection module can be duplicated to increase input channel count.

The remaining peripheral controller modules are duplicated as necessary for each location used for implementation.

communication links implemented using **low latency** communication protocols

Functional features

Field detection module includes:

- Field measurement
- Support for different IFs
- Input linearization
- Field calibration
- Field I component detection
- Field Q component detection
- Components conversion to field amplitude
- Components conversion to field phase
- Measurement filtering

The features can be used both in control and diagnostic mode.

Diagnostic mode provides such functionality as SEL or Frequency Sweep mode etc.

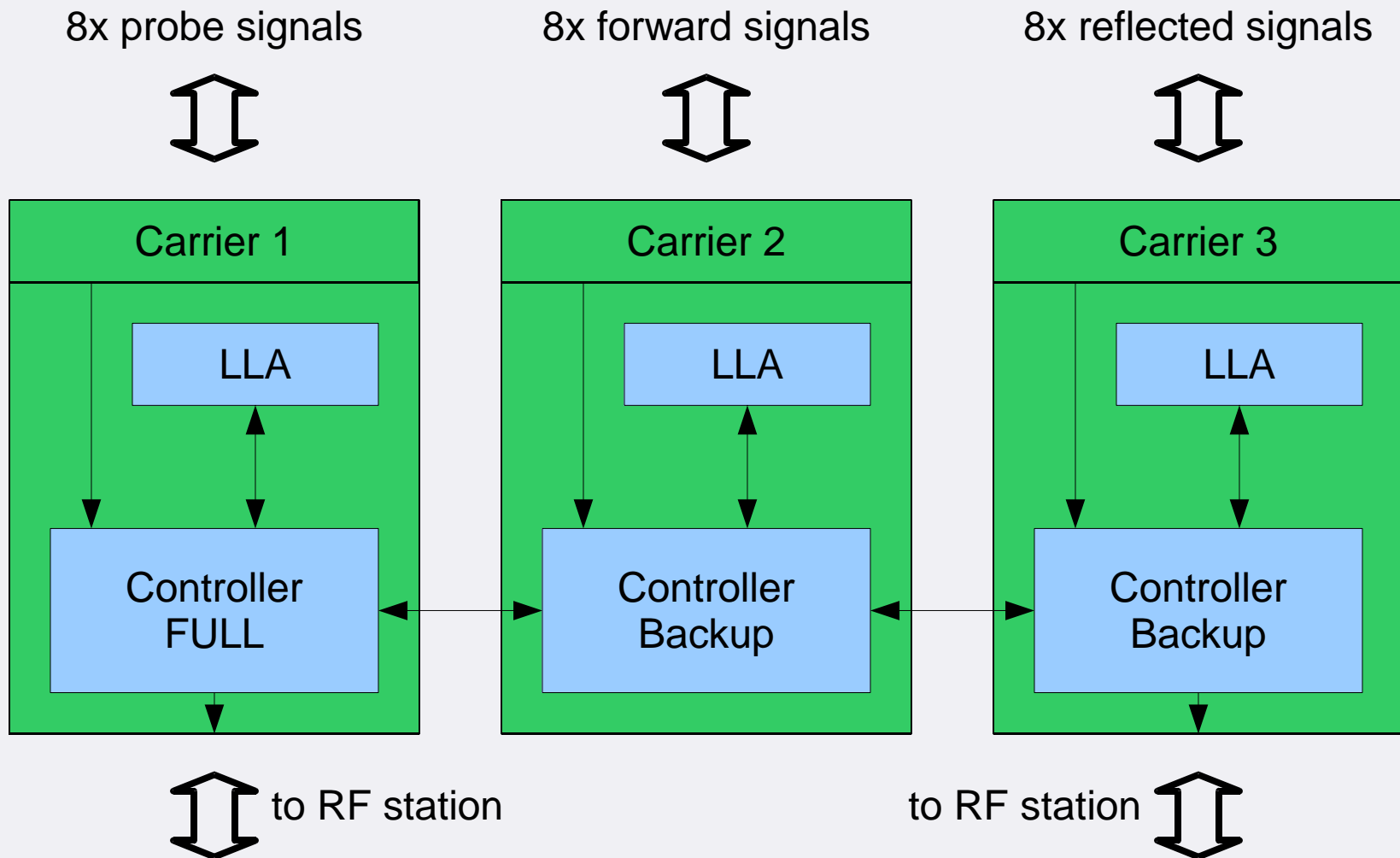
Feedback module includes:

- Field error calculation
- PID transfer function
- MIMO controller

Output module includes:

- Output linearization
- Correction tables
- Offset compensation
- Control signal adjustments
- Control signal limiters
- Loop phase adjustment
- Loop gain adjustment
- Output delay

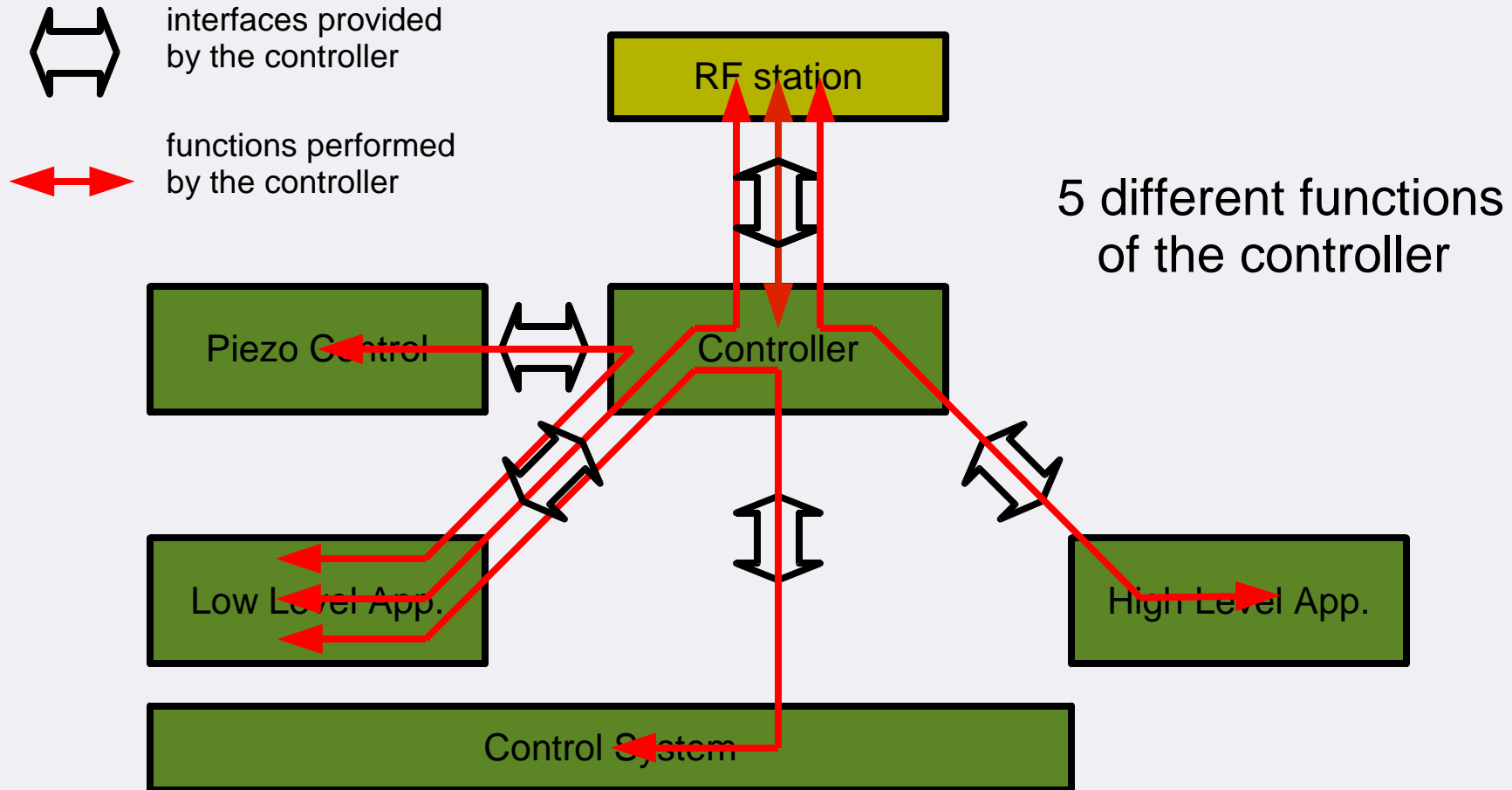
Controller in ATCA system



Advantages of the ATCA system

- distributed system provides multiple locations for algorithms – it increases the number of available resources
- individual projects are much simpler than one big project– easier debugging and control over the application
- high availability of the hardware platform (redundancy) decreases down time of the machine
- fast communication amongst the boards provided by the standard – no such possibility on VME – better integration of the algorithms

Against the background of the whole system



Controller III (DESY)



Estimation and tuning of the first Multivariable RF Controller for the Free Electron Laser FLASH

Christian Schmidt

Deutsches Elektronen Synchrotron
Technische Universität Hamburg Harburg

2nd ICE Workshop

26. Feb 2008

Outline

- The XFEL Project at DESY
- Low Level Radio Frequency Control System (LLRF)
- System Identification
 - disturbance sources
 - black box modeling
 - model validation
- Fixed order controller design
 - MIMO controller structure
 - H_∞ design with shaping filters
 - Iterative learning control
- Outlook

Physical modeling

starting with the differential equation for the resonant circuit

$$\ddot{U} + 2\omega_{12}\dot{U} + \omega_0^2 U = 2 R_L \omega_{12} I$$

- with the Ansatz

$$U = \hat{U} e^{-i\omega t}$$

$$\omega_{12} = \frac{1}{2R_L C} = \frac{\omega_0}{2 Q_L} \approx 2\pi \cdot 216 \text{ Hz}$$

$$Q_L = 3 \times 10^6$$

$$\Delta\omega = \omega_0 - \omega$$

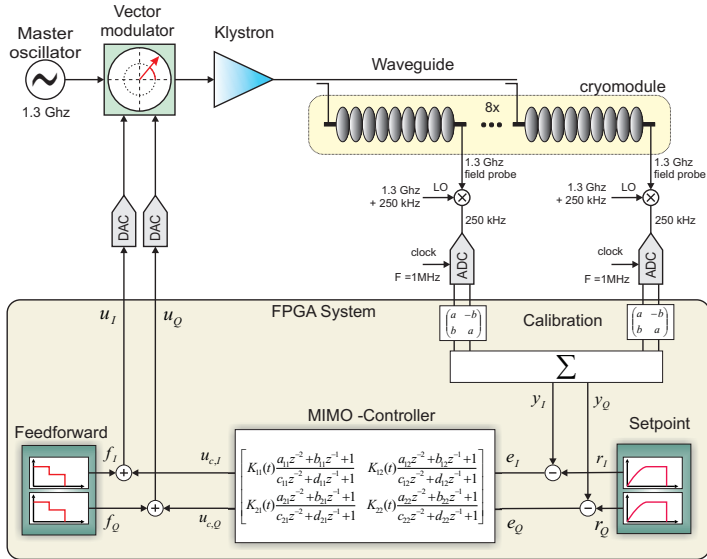
$$R_L = \left(\frac{r}{Q}\right) Q_L \approx 3.07 \times 10^9 \Omega$$

The cavity can be described as a first order lowpass, where the envelope of the electric field is given by the real and imaginary part

$$\begin{pmatrix} \dot{y}_r \\ \dot{y}_i \end{pmatrix} = \begin{pmatrix} -\omega_{12} & -\Delta\omega(t) \\ \Delta\omega(t) & -\omega_{12} \end{pmatrix} \begin{pmatrix} y_r \\ y_i \end{pmatrix} + R_L \omega_{1/2} \begin{pmatrix} u_r \\ u_i \end{pmatrix}$$

u and y denote the input and output respectively

Schematic View of the LLRF Control System



Disturbances

- Lorentz Force Detuning

- constant of $-1\text{Hz}/(\text{MV}/\text{m})^2$ results in steady state detuning of -625 Hz at $25\text{ MV}/\text{m}$
- mechanical dynamics decrease the frequency change to $400\text{ Hz} \rightarrow (\pm 45^\circ)$
- correlated perturbation

- Microphonics

- microphonic noise level measured in FLASH are about $\pm 10\text{ Hz}(\pm 2^\circ)$
- has to be compared to the cavity bandwidth (HWHM) of 216 Hz
- microphonics are uncorrelated along the linac

- Beam Loading

- single bunch ($5 \times 10^{-10} e^-$) induces a transient of 1.4×10^{-3}
- 10% rms bunch-to-bunch charge fluctuation will results in an energy spread contribution of 1.4×10^{-4}
- correlated

Estimation of a black box model

The physical model describes the ideal system, but:

- for controller design it might be not sufficient enough
- disturbances and noise effects are hidden
- therefore black box modeling is used

general state space system

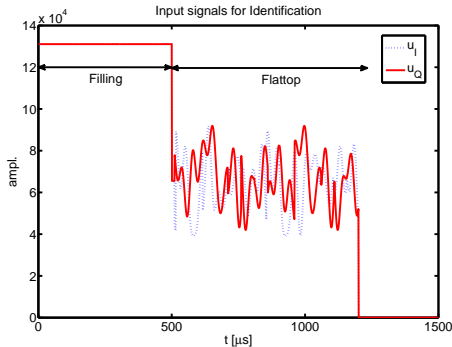
$$\begin{aligned}\dot{x}(t) &= Ax(t) + Bu(t) \\ y(t) &= Cx(t) + Du(t)\end{aligned}$$

estimating system parameters A, B, C, D with subspace algorithm
"n4sid", provided by Matlabs System Identification Toolbox¹

¹The Mathworks, *System Identification Toolbox User's Guide*, The Mathworks, Inc., Natick, 2004

Identification procedure

For Identification the system dynamics special chosen input disturbances need to excite the system

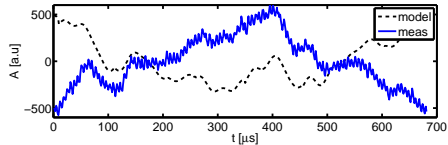
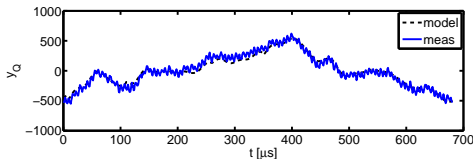
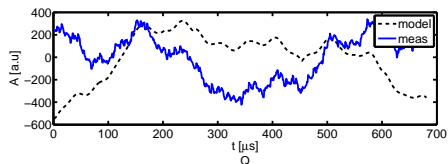
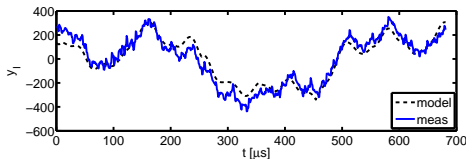


- wide bandwidth (rich enough)
- limited flattop time (max. 800μ s)
- good signal to noise ratio
- excite close to operation point

Sufficient model must be found to describe all "real" system dynamics and neglect artificial disturbances

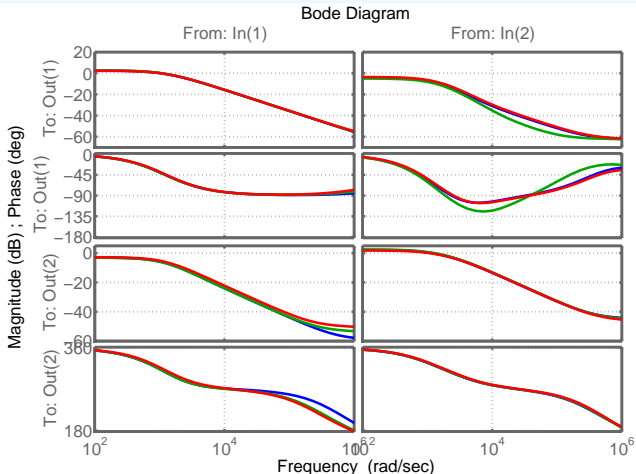
Model validation

Focus on prediction or stability?



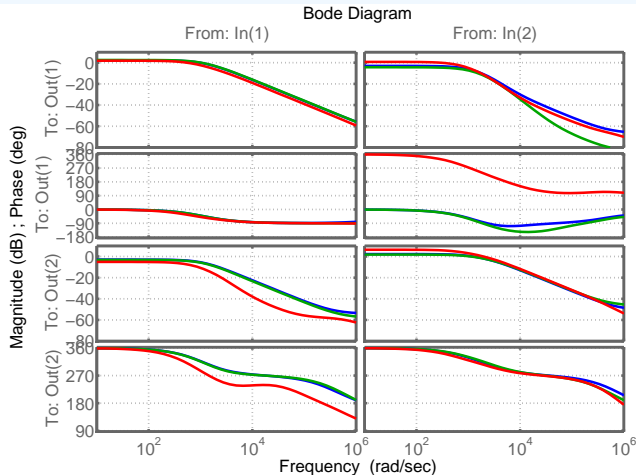
- medium dynamic range can be modeled (cross validation)
- focus on prediction leads to unstable models (detuning?)
- system is known as stable (open loop measurement)

Models Pulse to Pulse



- small variations in the frequency range of interest
- diagonal dominant system

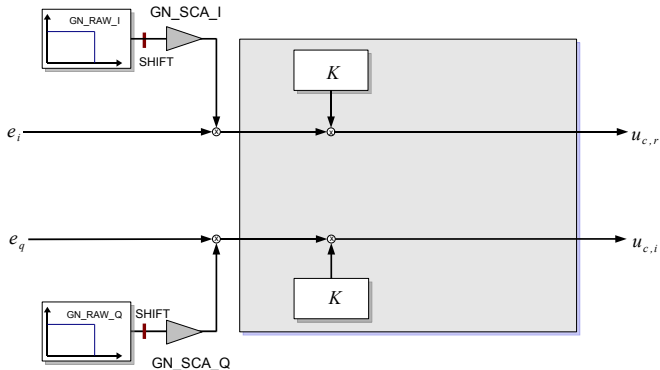
Models Long time measurements



- variation bigger but still sufficient for different input signals and Machine drifts
- instead of I,Q, use A,p for identification (but nonlinear)

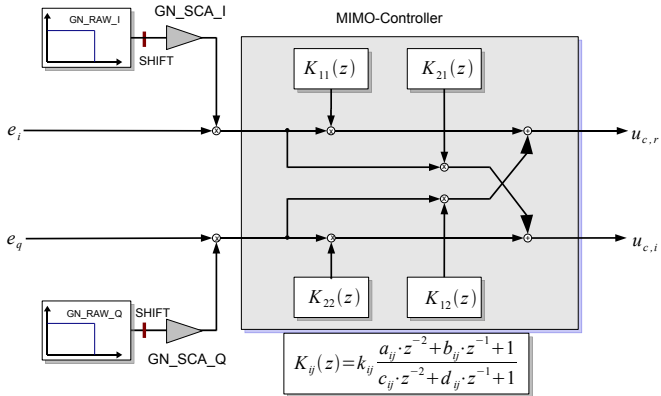
Controller Structure

- so far a decentralized P Controller is used



Controller Structure

- so far a decentralized P Controller is used
- new FPGA implemented controller is given by:



- tuning 20 parameters manually is not possible for users

Design Objectives

RF field flatness during the flattop is the desired goal

- perfect tracking (reference = output)
 - only possible for low frequencies due to system physics
 - high loop gain amplifies also disturbances
 - complementary sensitivity $T(s)$

Design Objectives

RF field flatness during the flattop is the desired goal

- perfect tracking (reference = output)
 - only possible for low frequencies due to system physics
 - high loop gain amplifies also disturbances
 - complementary sensitivity $T(s)$
- disturbance rejection
 - high frequency noise is filtered by lowpass characteristics
 - good suppression demands small feedback gain
 - sensitivity $S(s)$

but...

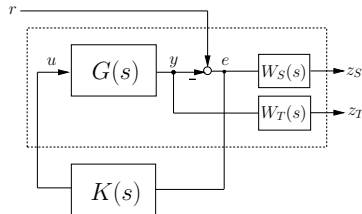
$$S(s) + T(s) = I$$

↪ therefore weighting filters are introduced to shape the closed loop behavior

Generalized Plant with weighting Filters

- using shaping filters to restrict closed loop behavior on fictions outputs of the generalized plant

$$W_S(s) = \frac{1}{M_S} \frac{(s + \omega_{S1})(s + \omega_{S2})}{(s + \omega_{S3})(s + \omega_{S4})}$$
$$W_T(s) = \frac{1}{M_T} \frac{(s + \omega_{T1})(s + \omega_{T2})}{(s + \omega_{T3})(s + \omega_{T4})}$$



- parameter estimation can be found by solving norm-optimal H_∞ with HIFOO¹

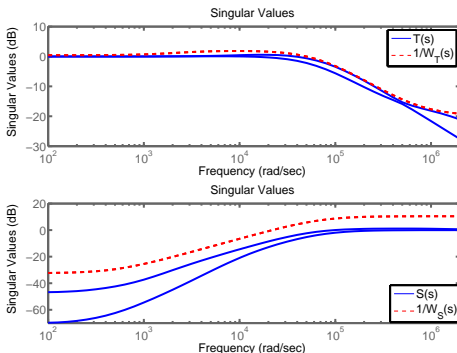
$$\| W_S(s) S(s) \|_\infty < 1$$

$$\| W_T(s) T(s) \|_\infty < 1$$

¹J. V. Burke, D. Henrion, A. S. Lewis, M. L. Overton, *HIFOO - A matlab package for fixed-order controller design and H_∞ optimization*, Proceedings of 5th IFAC, 2006

Tuning shaping filters

Shape closed loop system to desired performance

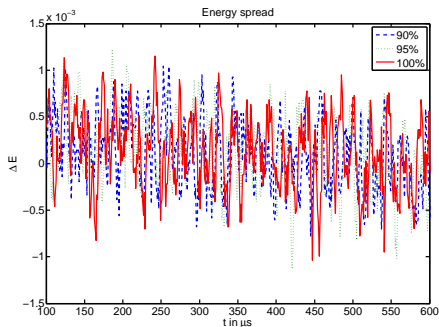
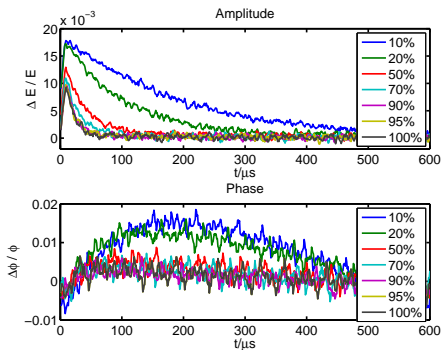


- pulse duration $700\mu s \sim 1kHz$ \triangleright lower limit
- intermediate frequency $250kHz$ \triangleright upper limit
- restrictions on controller output are not shaped so far

First implemented controllers

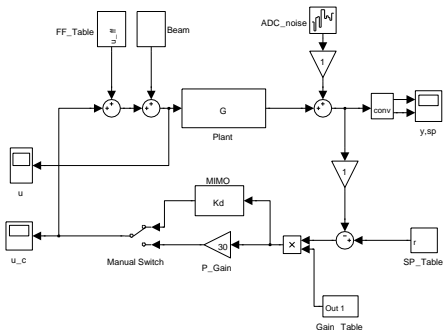
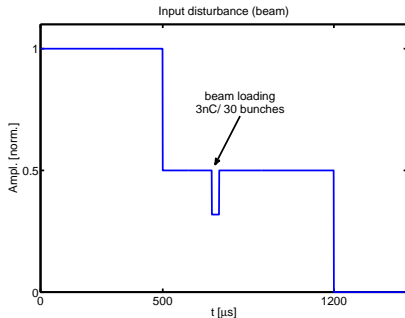
slow approach (C) to estimated controller gain

$$K(z) = C \cdot \begin{pmatrix} K_{11}(z) & K_{21}(z) \\ K_{12}(z) & K_{22}(z) \end{pmatrix}$$



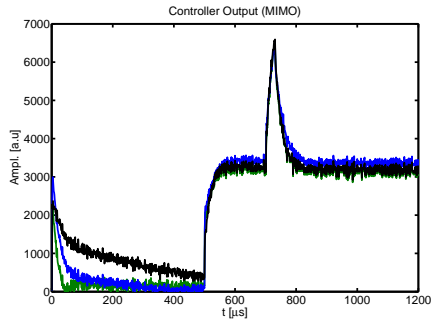
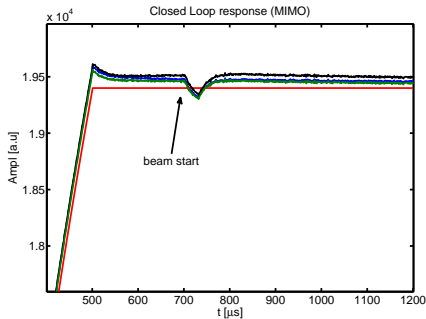
- highest performance reached so far (P)
- instability problems with full order controller parameters
- limited measurement time restricts online tests

Closed Loop Simulation



- simple simulink structure for closed loop simulation
- modeling beam disturbance with estimated controller parameters
- added output disturbance (measurement noise)

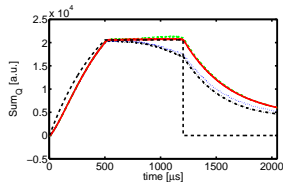
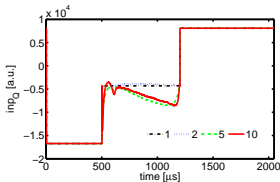
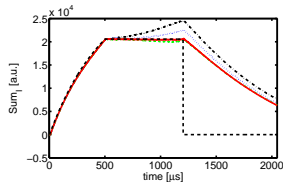
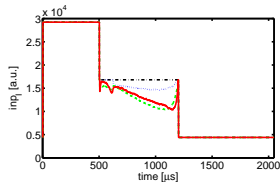
Closed Loop response to input disturbance



- disturbance suppression for high frequency oscillations
- short beam pulses can not be regulated by feedback
- adaptive feedforward might be used to compensate beam energy gain

Iterative Learning Control

Adaptive feedforward using an iterative learning algorithm³



- first open loop measurements show promising results
- tests with beam must be performed in next measurements

³N. Amann, D.H. Owens and E. Rogers, *Iterative learning control for discrete-time systems with exponential rate of convergence*, IEEE Proceedings - Control Theory and Applications, 217-223, 143, 1996

Outlook

- first MIMO-Controller parameters can be estimated
- self updating identification procedure
- self adapting controller design
- automatic beam based vector sum calibration
- Iterative Learning controller
- Adaptive Feed Forward
- Automation !

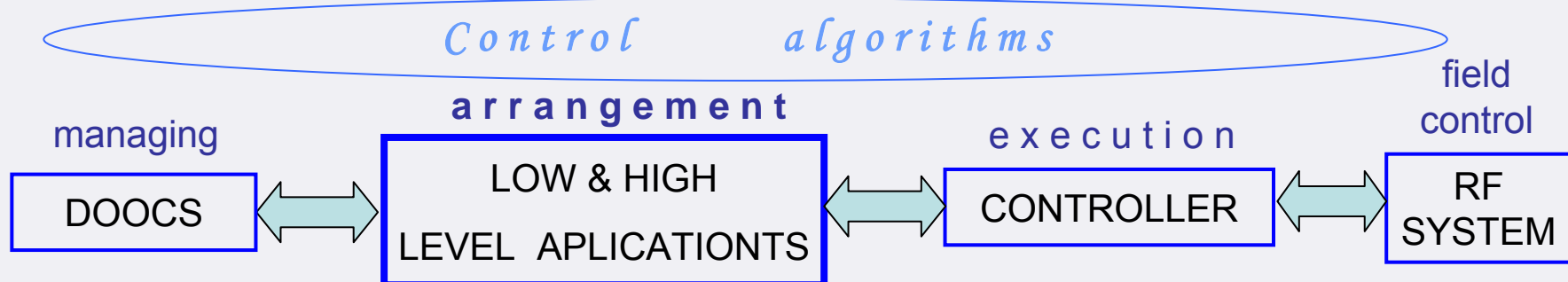
There are several tasks which need to be optimized to get a user friendly "one button machine" !

Low Level Applications



Low Level Applications introduction

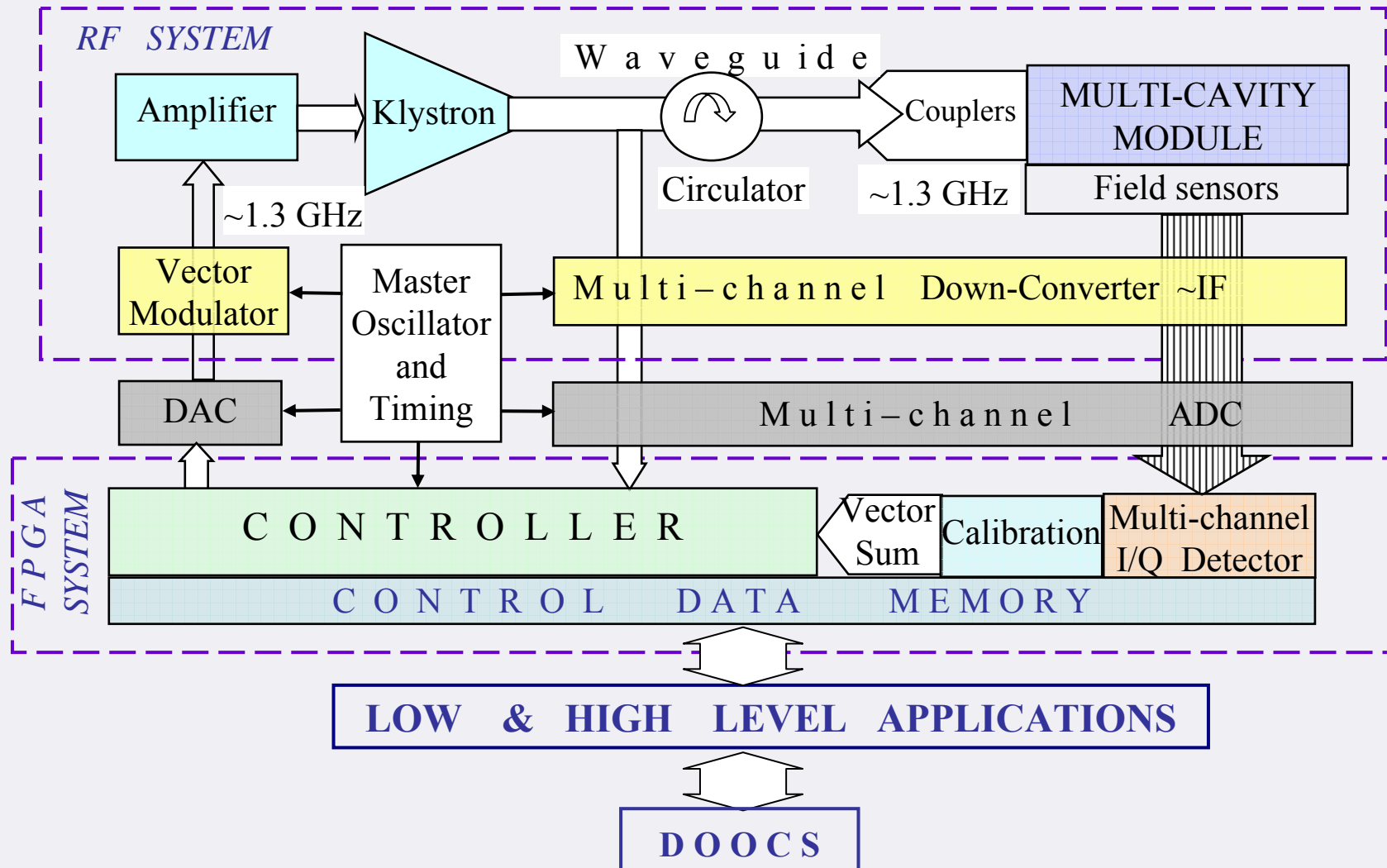
The part of Software adjacent to the Controller responsible for the arrangement of the control algorithms



TASKS:

- Implementation of the procedures and supplementary data processing to arrange Control Data for the Controller
- Monitoring and Exception Handling for safety requirements

Functional block diagram of LLRF control structure



Requirements

Functional

- Compute new Control Data pulse to pulse
- VM offset compensation – one time per day
- Vector Sum calibration – always for new operational condition

Performance

- Control Data meet requirements for cavity field control:
- efficient *filling* : energy efficiency = stored/expanded energy;
optimal target = ~74% for 0.5 ms filling
- stable *flattop*: field stability : 10^{-5} in amplitude, 0.01° in phase

Reliability

- robust algorithms

Usability

- on/off button

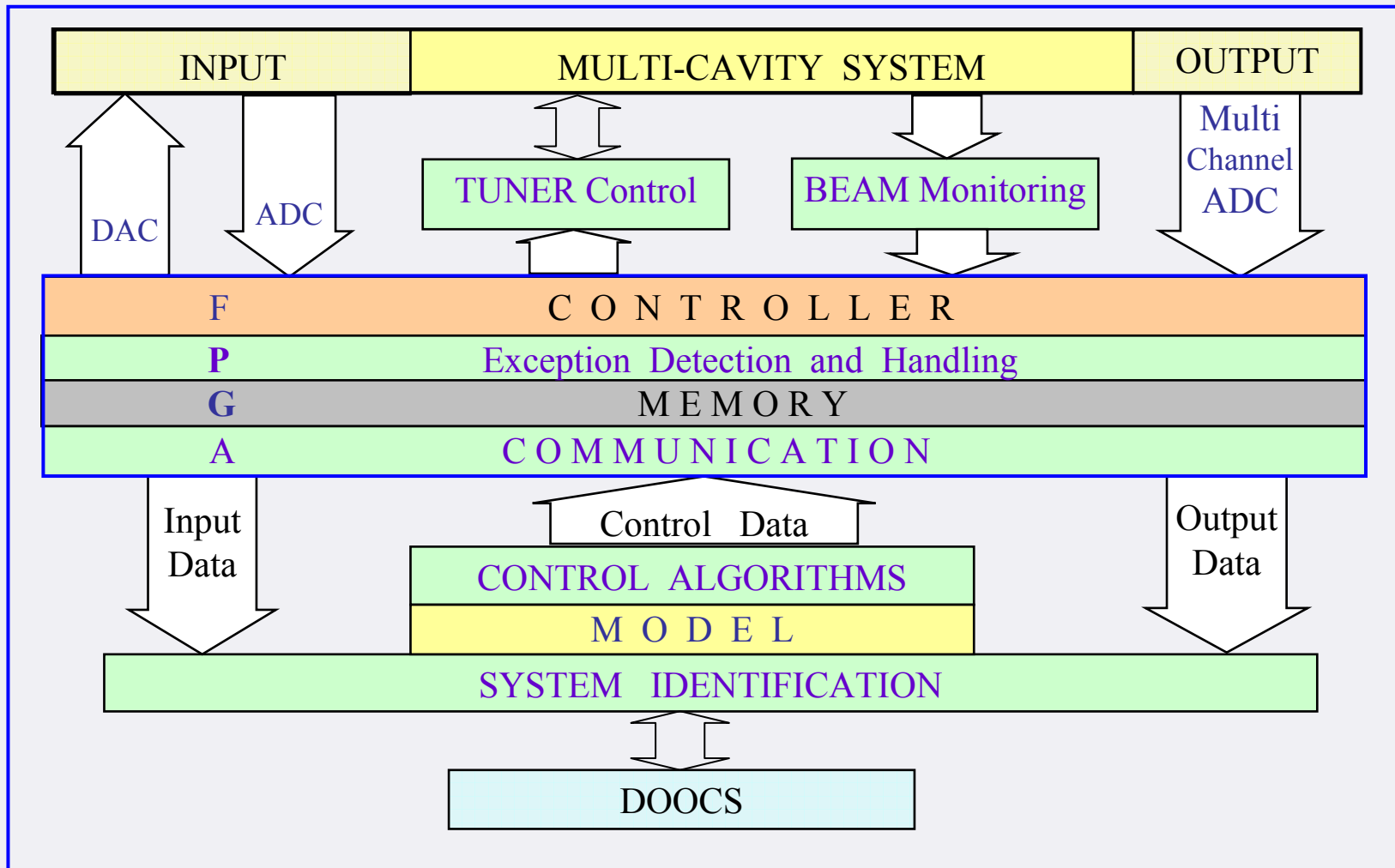
Interface

- Input/outputs to High Level Applications and Controller

Safety

- monitoring and exception handling
- gradient, quench detection, klystron power

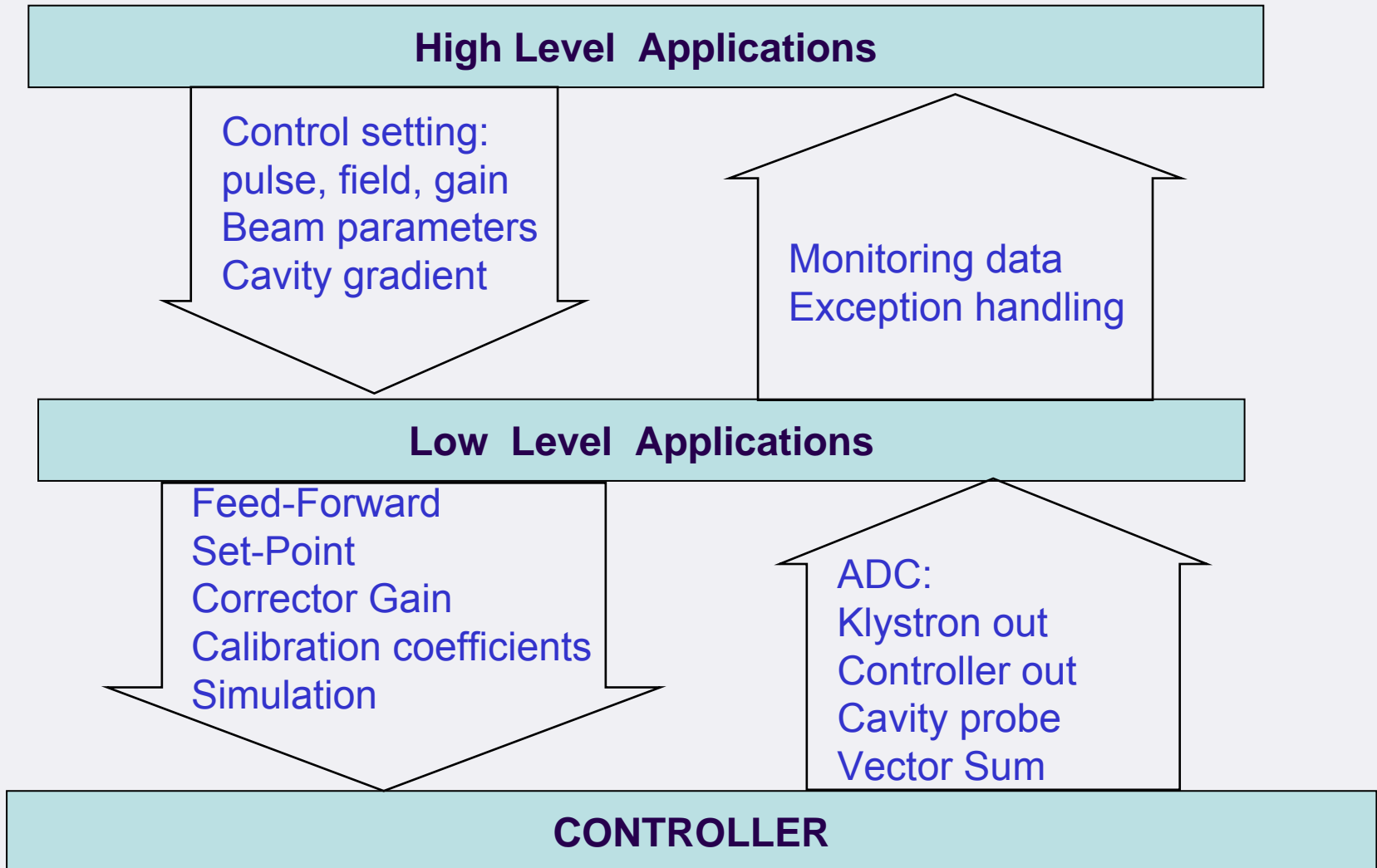
Low Level Applications functional arrangement



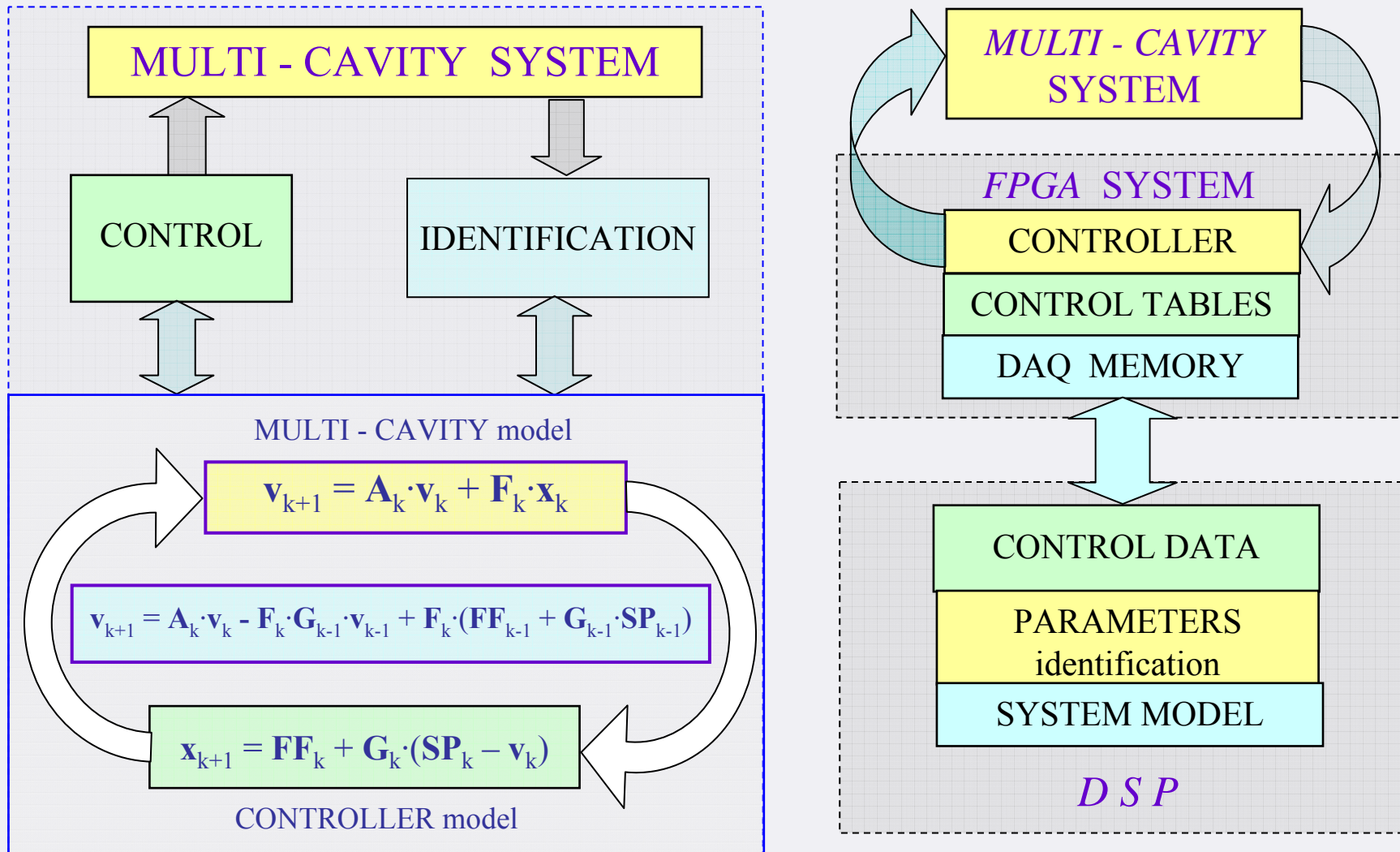
Set of Low Level Applications

SYSTEM IDENTIFICATION	CONTROL	MONITORING
VM offset Klystron characteristics Coupling factor Cavity detuning Half-bandwidth System complex gain Beam parameters	Feed-Forward Set-Point Corrector Gain Calibration coefficients	Field gradient Klystron power Loaded Q Detuning
EXCEPTION HANDLING: controller off, beam off		

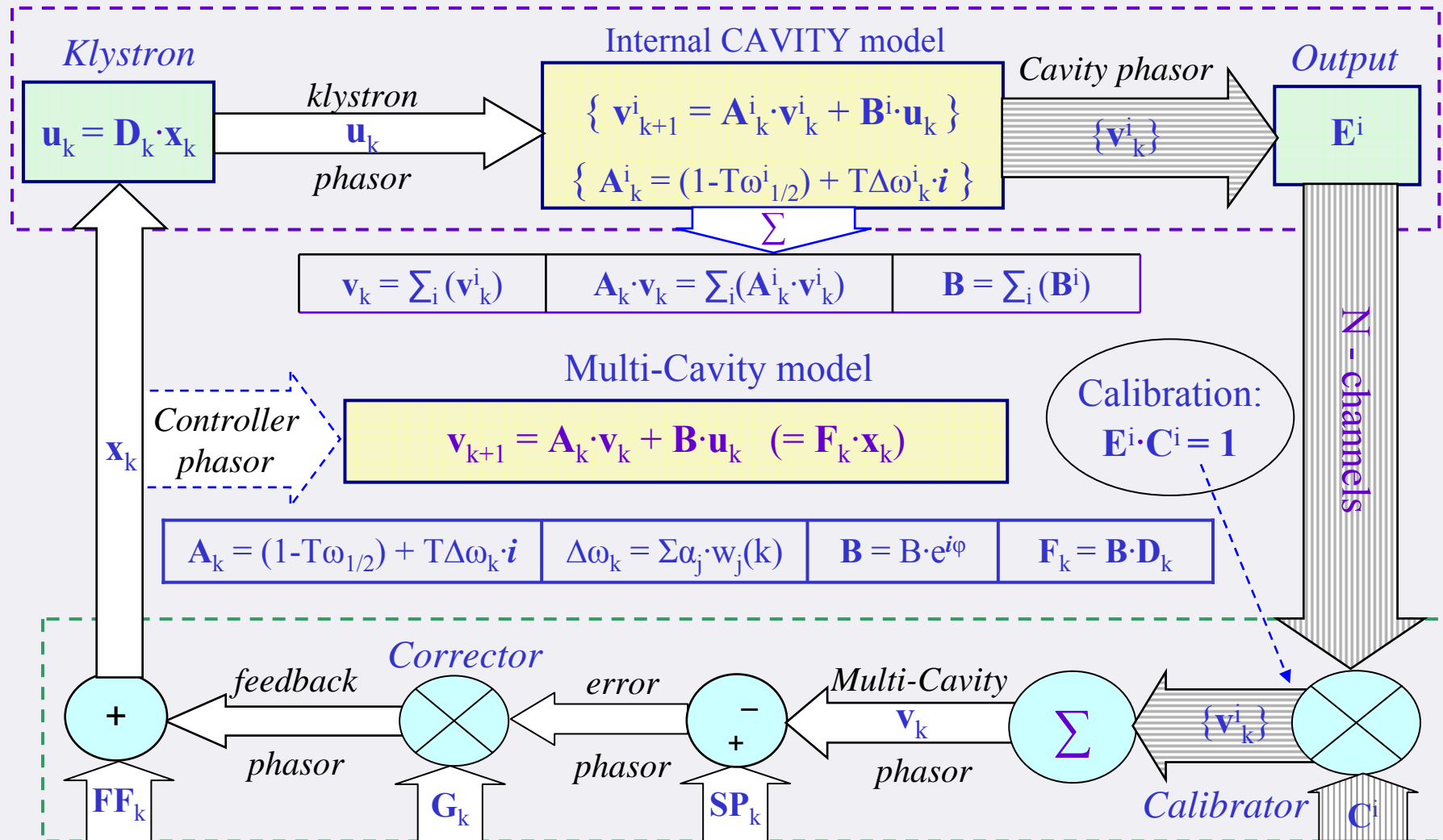
Interfaces



Adaptive Control Algorithm based on System Identification



System Model for Identification Algorithm



High Level Applications



HLA XFEL Requirements.

Main requirements:

- Provide customized control algorithms of RF system components which demands high computation power.
- Provide customize diagnostic algorithms of RF systems components which demands high computation power.
- Established with commonly used tools and environments for instance: Matlab, C, C++.
- Ready for development and modifications for the accelerator users (not demand expert knowledge in electronics, microwave electronics).
- Equipped with the interface to automation and the software control system (DOOCS servers).
- Supporting interface to the local control and diagnostic signals.
- Not restricted to the in-pulse reaction.
- Provide testing environment for future low level applications

FLASH/XFEL - High level applications background

The High level Applications was developed for use in the FLASH accelerator LLRF systems, MTS and Chechia LLRF control systems.

HLA in FLASH has been implemented as a Matlab environment based tools (V. Ayvazyan, W. Cichalewski, A. Brandt) or standalone processes – satellite DOOCS servers (A. Brandt).

HLA's used in FLASH operation:

Control applications:

- redundant adaptive feed forward,
- vector sum calibration,
- loop phase and gain estimation,
- high power amplifiers chain linearization (microwave preamps and klystron),

Diagnostic and system tuning applications:

- cavity field error calculation,
- local oscillator signal generation optimization (configuration for 250kHz)
- HPAC components characterization and diagnostics.

XFEL – High level applications list

Control applications:

1. redundant adaptive feed forward, *
2. vector sum calibration, *
3. loop phase and gain estimation, *
4. cavity gradient and phase SP calibration
5. High Power Amplifiers Chain (HPAC) linearization (microwave preamps and klystron),
6. momentum management,
7. driving signal offset calibration,
8. wave-guide tuner adjustment (phase, loaded Q),
9. beam phase measurement,
10. beam loading compensation,
11. modules operational limits estimation,
12. gradient and gain increase (ramping),
13. klystron HV modulator bounce timing adjustment.
14. cavities frequency tuning, *

Diagnostic and system tuning applications:

15. cavity field error calculation,
16. cavity overloading detection (soft quench), *
17. local oscillator signal generation optimization (configuration for IF 250kHz),
18. HPAC components characterization and diagnostics,
19. forward and reflected signals crosstalk estimations and compensation,
20. HF signals attenuation level adjustment,
21. klystron HV stability diagnostic,
22. modules operational limits estimation,
23. power margin estimation.

* - can be implemented as Low Level Application in time with time

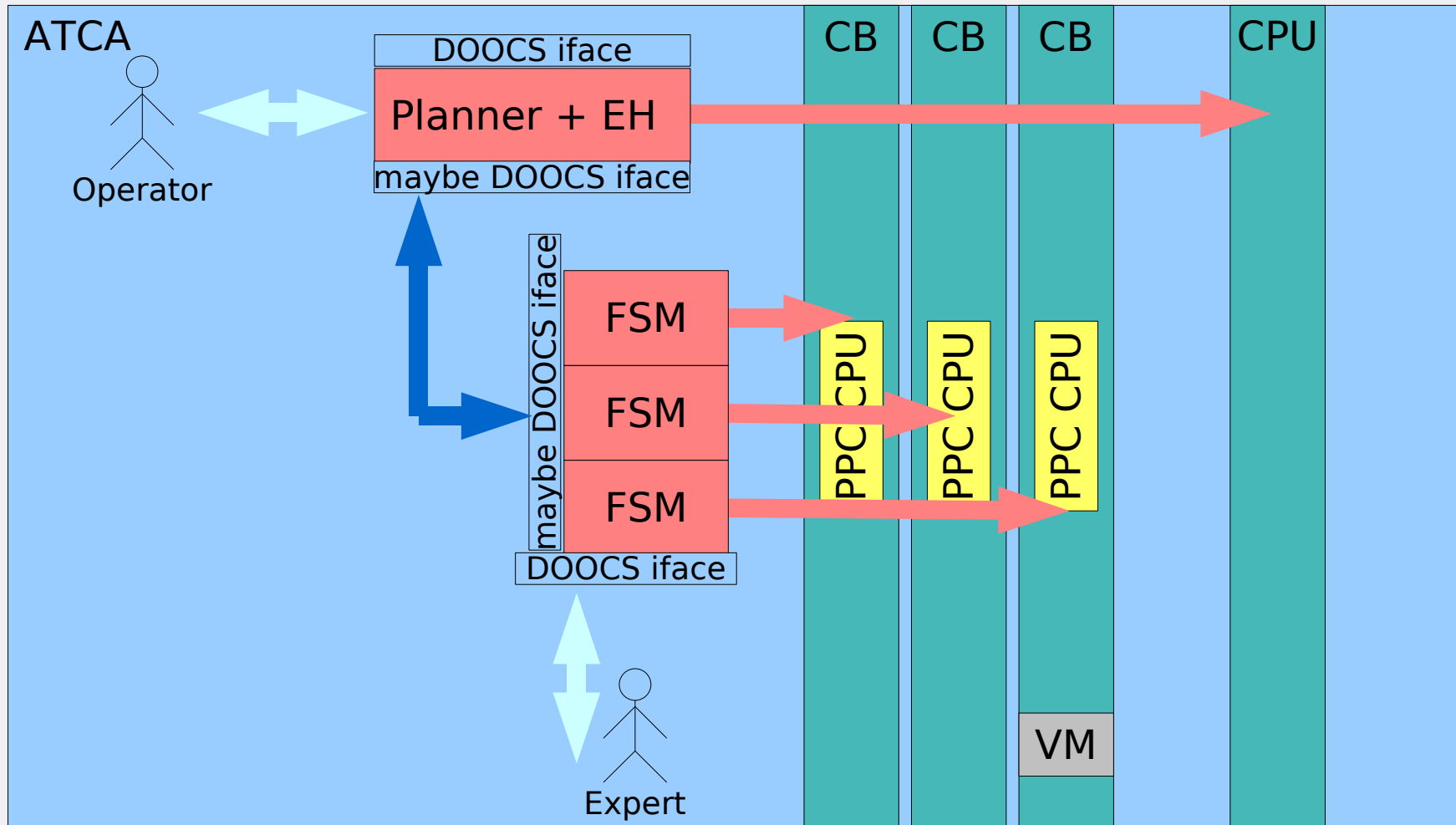
Automation



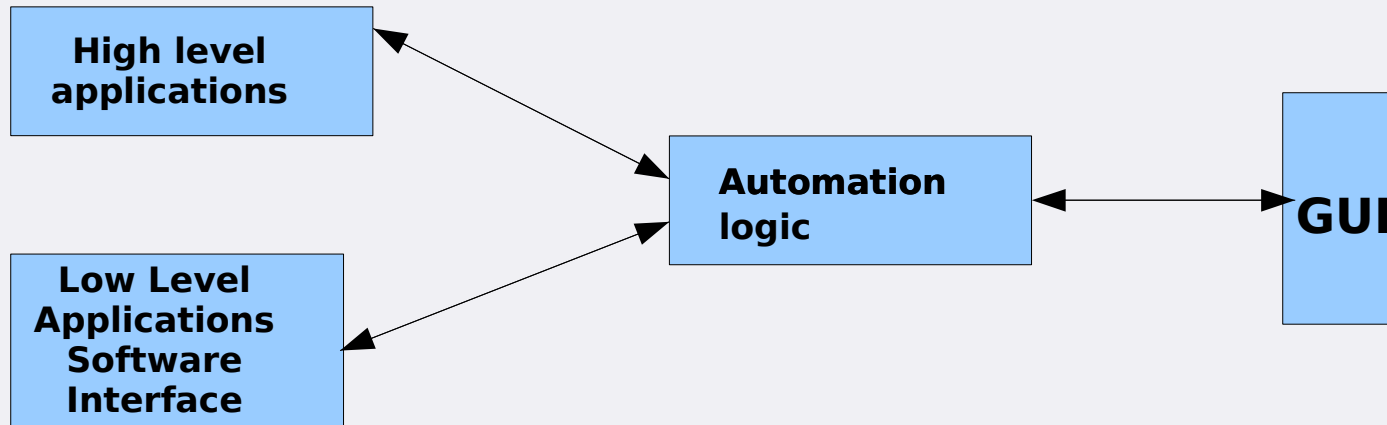
Tasks of automation

- To automate routine operators tasks
- To adapt to unpredictably changing conditions of underlying hardware
- To recover the subsystem from known faults
- To perform above activities **safely!**

General scheme of the automation in ATCA



Automation in the ATCA - design



- Does not communicate directly with the hardware, so the design of the automation logic **has nothing in common with the ATCA architecture**.
- Situation is **different for the implementation** of the senses and hands of the FSM (high/low) level applications and monitoring signals, the ATCA can facilitate implementation of these applications by its performance and interconnectivity.

Automation in the ATCA

Automation relies on dozens of high/low level applications and diagnostic signals so:

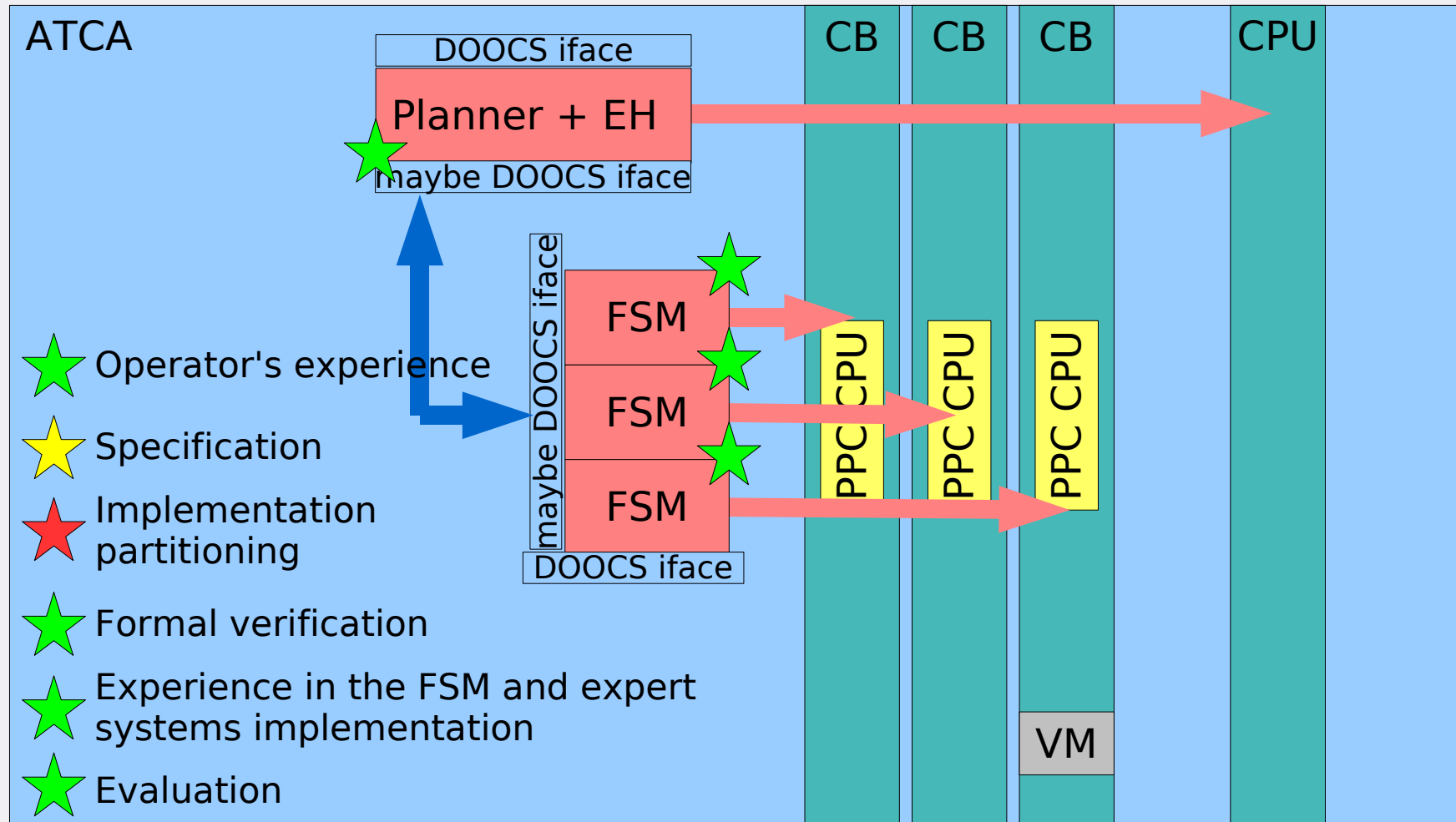
- Interconnectivity of high and low level applications will be surely better supported by the ATCA than by the VME
- Better performance of the ATCA crate will better suit high network traffic generated by the automation software
- ATCA shelf manager will provide many diagnostic information used by the fault recovery automation module

Automation in the ATCA - design/spec

Specification – the rhapsody way:

- Use cases
- Activity charts
- Tests of the charts within the confines of operation procedures.
- Statemachines – when necessary
- Planner specification when necessary

Experience



To do

- **Specification** of the LLRF system as a family of simple FSMs - they will limit system users to proper operation.
- **Specification** the tasks for the planner and the exceptional situations – they will implement routine operation tasks and perform fault recovery
- Remote GUI for the automation module for automating routine operator's procedures (so far. the DDD does not provide creation of dynamical GUIs)
- Optimization of the planning algorithm used by the automation.

Automation prerequisites

- Low level applications
- High level applications
- Proven operation procedures

Summary of LLRF Review



Summary of the LLRF ATCA Review

- Focused on evaluation of an ATCA based LLRF system:
 - With demonstrated technical performance with beam at FLASH
 - With demonstrated operability by machine operators
 - Which serves as development platform for XFEL LLRF software
 - Which is close to what is needed for XFEL
 - Project time line: January – December 2008
- Covering all LLRF subsystems to be installed at FLASH
 - Master Oscillator, frequency distribution and timing
 - Downconverters, vector-modulators
 - Digital feedback hardware, piezo controller
 - Controller software, low and high level applications software
 - Automation

Note: This was not a review of the XFEL LLRF system although it covered many aspects.

Individual Comments from Reviewers

- Hardware development quite advanced and detailed
- Software development less advanced and still requires significant work.
- Hardware and software development schedule very ambitious
- Some concerns with specific solutions (high signal density at AMC connector, signal integrity for routing from RTM module, placement of AMC connectors on both sides of carrier board)

Individual Comments from reviewers

- The change from R&D to production mode for the XFEL requires a change of mode of operation :
 - Senior personnel (responsible for workpackages) from collaboration partners must join the core team at DESY for a significant portion of their time (~6 months / year) and commit their participation for the duration of the project.
 - Collaboration partner must be involved in project management
 - Must commit to agreed schedule and deliverables
 - Work on LLRF cannot be sacrificed by commitments toward the universities.
 - Intellectual property must be accessible to all collaboration partners

Answers to Committee

http://ferrari10.desy.de/mediawiki/index.php/Answers_LLRF_Review

http://ferrari10.desy.de/mediawiki/index.php/LLRF_Backup_Solution