BAM Electronics

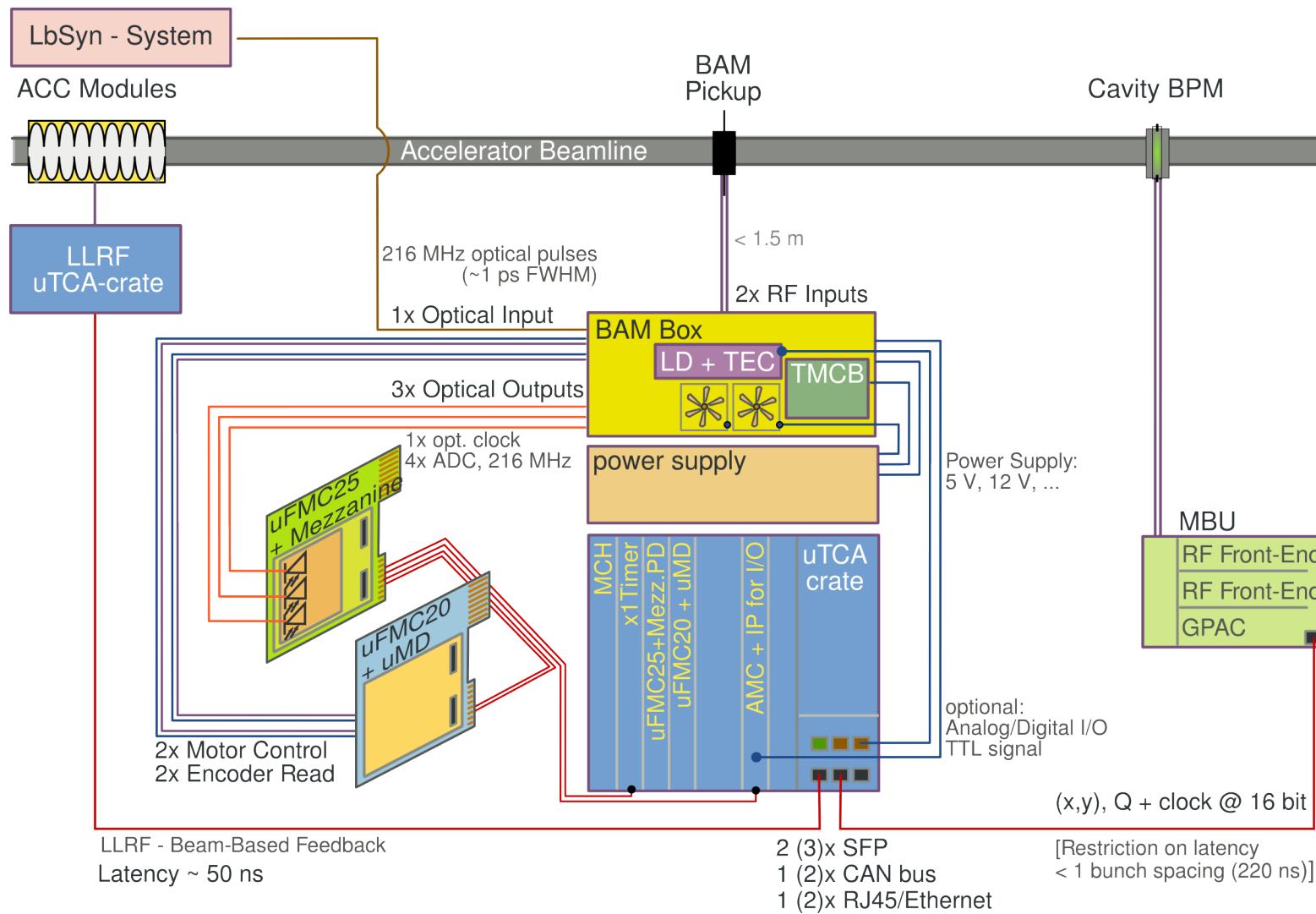## Overview & Specifications

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BAM Generation 3 – Overview on Specifications for Electronic System

2nd Follow-up Meeting on MTCA.4 Board Development

15. October 2013, DESY

DESY

Interfacing

> ## DFMC25 ↔ DFMC20+MD22

- ideally, communication via backplane

- MD22:

    > control of 2 stepper motors
    > read-out of position encoder: EnDat2.2 data format
- data rates: 10 Mbit/sec

> ## DFMC25 ↔ I/O cards

- Option: control of optical switch (e.g. via TTL signal)

- synchronised to machine trigger

uFMC25 + mezzanine & PD: open questions

> ## Challenge:

- Conversion of laser pulses (~ps FWHM) to electr. Signal (clear pulse w/ flat baseline)

- Sampling rate of 216 MHz (laser rep. Rate):

    > 2 channels
    > 2x ADCs per channel (peak & baseline)

> ## Requirements & Current Status:

- PD input:

    > PD output power level wrt optical input power
    > set diff. amplifier according to expected opt. power
    > characterisation of pulses (pronounced separation between peak & baseline):
        - first tests promising: clean shape of PD output
    > amplitude jitter at peak & baseline

- ADC performance:

    > dynamic range
    > buffer current for optimal SFDR
    > employment of time shifters
    > SNR
    > ENOB
    > max. clock jitter wrt to full BW signals
    > amplitude jitter (peak & baseline):
        - first estimation promising, but with single FMC carrier in MTCA crate

Firmware & Server

> ## Basic firmware for FMC25

> ## Data processing in FPGA:

- specialised firmware for BAM signal processing
- collecting data from other diagnostics: BPM, BCM, …
- sending data packets to LLRF for intra-train FB

> ## BAM Server for "slow" operations

- averaging, internal feedbacks, …

Rough timeline

> <mark>Original Plan (Feb. 2013):</mark> Boards ready for installation

- FLASH /FLASH II:

  > 1x needed June **2013**

  at the moment 2nd highest priority →
  » Test system for BAM.15ACC7
  → timing information for FEL users

  > at least 2 more until August/September **2013**

  now highest priority →
  » BAM.3DBC2 & 4DBC3
  → connection to LLRF for Feedback

  > 3 more by end of **2013**

  » BAM.1UBC2 and 1SFELC

  > 2 more by mid **2014**

  » 2x for FLASH2

- Europ.XFEL:

  > 1x for September **2014**

  at the moment 3rd highest priority →
  » XTIN: BAM.47.I1

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