LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

LMU München - Excellence Cluster Universe

PS & Services

Stefan Rummel

DEPFET Collaboration Meeting
Hamburg
21.1.14-24.1.14

Overview

- Preproduction status
- Test Beam preparation
  - Upgrade of Demonstrator
  - Hardware
  - Firmware development
  - Slow control integration
- PS Operation – Load regulation
- Services - Kapton development, power cable
- Outlook

Preproduction

- Goal: 10 Units, 24 Channels, full output power → Final designs specifications
- Output connectors suitable for final cables (mixed layout D-Sub)
- Final DC/DC converter cards → Full output power
- Bug fixing / optimizing
  - MCU card finalized (Interlocks)
  - Regulator cards finalized (Temperature measurement on regulators, opt. SNR of ADC's)
  - Breakout boards adapted
  - OVP substitute

Preproduction status

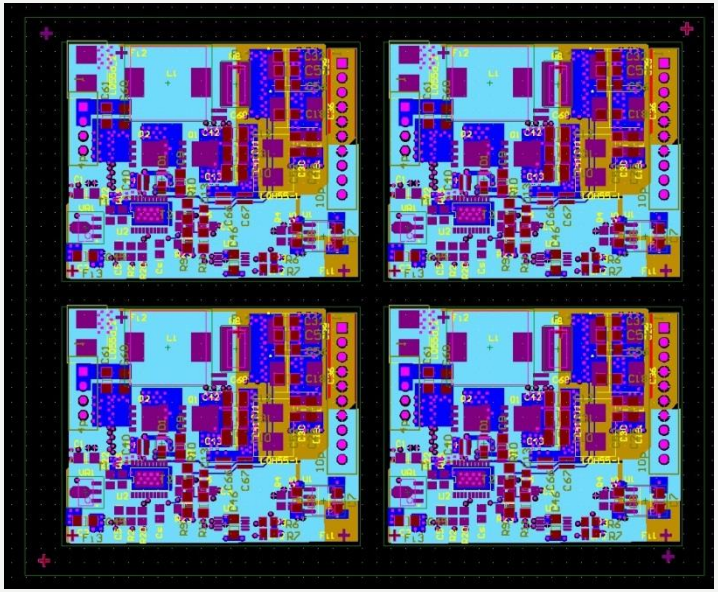
- PCB's are delivered
- Components provided by us ordered 90%

→ Production is under way – see the following slides

Preproduction status – Step Down Converter

- IC's and PCB's ordered
- Production data created (BOM, assembly plan, pick and place)

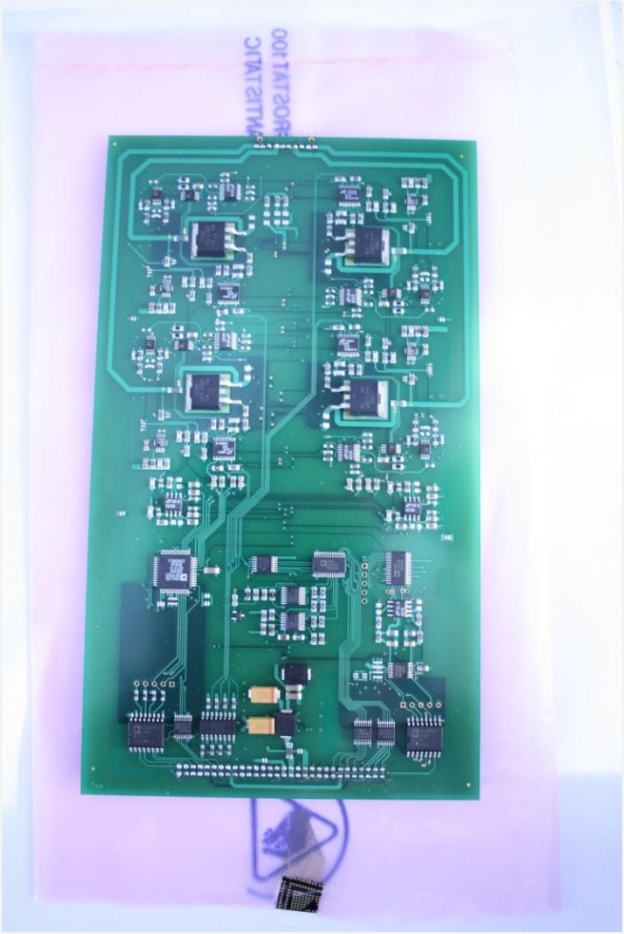
→ Delivery 2.2.14



Preproduction status – Regulator cards

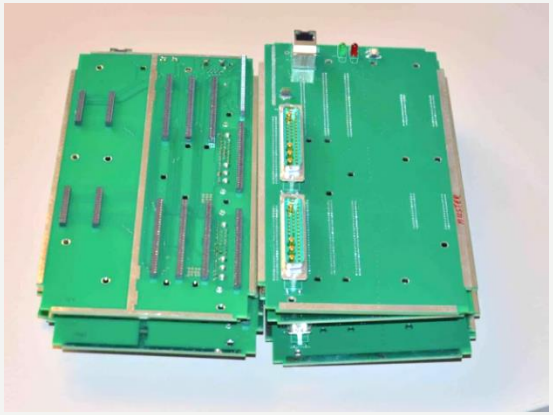
- IC's and PCB's ordered
- Production data for bipolar - regulator cards created (Bom's, assembly variants)
- 40 cards in 3 assembly variants
  - 10: With HV-Channel's to -100V
  - 10: Mixed with +28V and -20V range
  - 20: Bipolar with +10V - (-20V) range

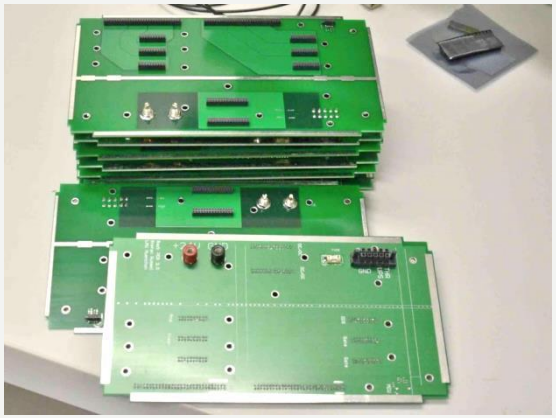
→ Delivery scheduled by EMS (CadUL) 3.2.14



Preproduction status – Summary

- Front- and Back and OPV placeholder PCB ready
- Bipolar regulator cards ordered
- Step Down converter ordered
- MCU, DC/DC Cards and Unipolar regulators are in work





PS for TB

PS for TB

- Decision on last October meeting: → PXD6 Hybrid is baseline for TB

- Demonstrator PS's not able to provide full current due to "old" DC/DC converter card

- PXD6 DEPFET need additional voltage for level shifter / buffer and polycover

→ Upgrade of Demonstrator with final converter cards required
→ Added the last available Regulator Cards to have 20 output voltages
→ Design of breakout board

- Two upgraded Demonstrator PS's are commissioned
  - Full power to operate 4 ASIC pairs
  - 20 output channels

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Firmware

- The commissioning revealed some issues on Firmware level
- Errors while accessing low level IO (I2C, SPI) are not caught and lead to a hang up of the software
  → Fixed this issue by performing hardware shutdown and introducing an Error state where PS is in OFF state
- Firmware stops execution of commands in case of high rates of commands
  → Fortiss fixed a bug the queues
- Firmware stability has been significantly improved!

Slow control integration

- EEPICS integration done by Thorsten

- Initial Power up sequence needed significant change due to new requirements form hardware operation
  - Current limits must be increased step by step to prevent damage
  - Higher granularity of hand-shakes required (previously assumed one)
  - Testing of PS state after each step

Next steps in integration / testing:

- Full manual power up using EEPICS gui - already available
- Software assisted power up (subsets are set automatically) - expected today
- Full automatic power (requires adaptions on DHH software) - soon

→ First tests this afternoon

PS Operation – Load regulation

- Last October meeting measurements from Florian showed that the DHP is sensitive to voltage changes as low as 20mV

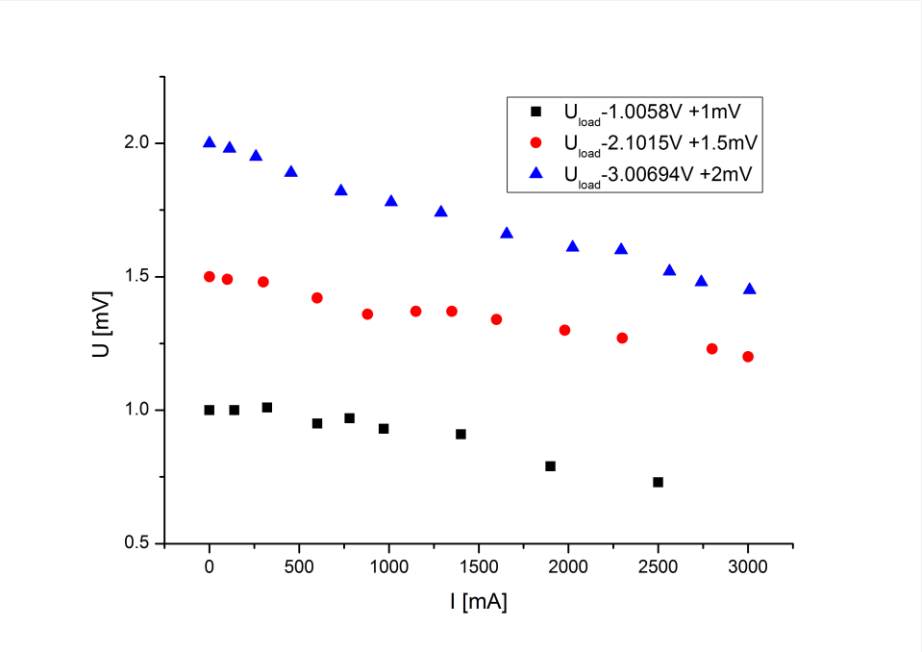
Which precision can we expect from our PS in sensed operation?

The answer is frequency depended…

PS Operation – Load regulation

- For DC and low frequencies (up to ~kHz):

→ PS load regulation is active

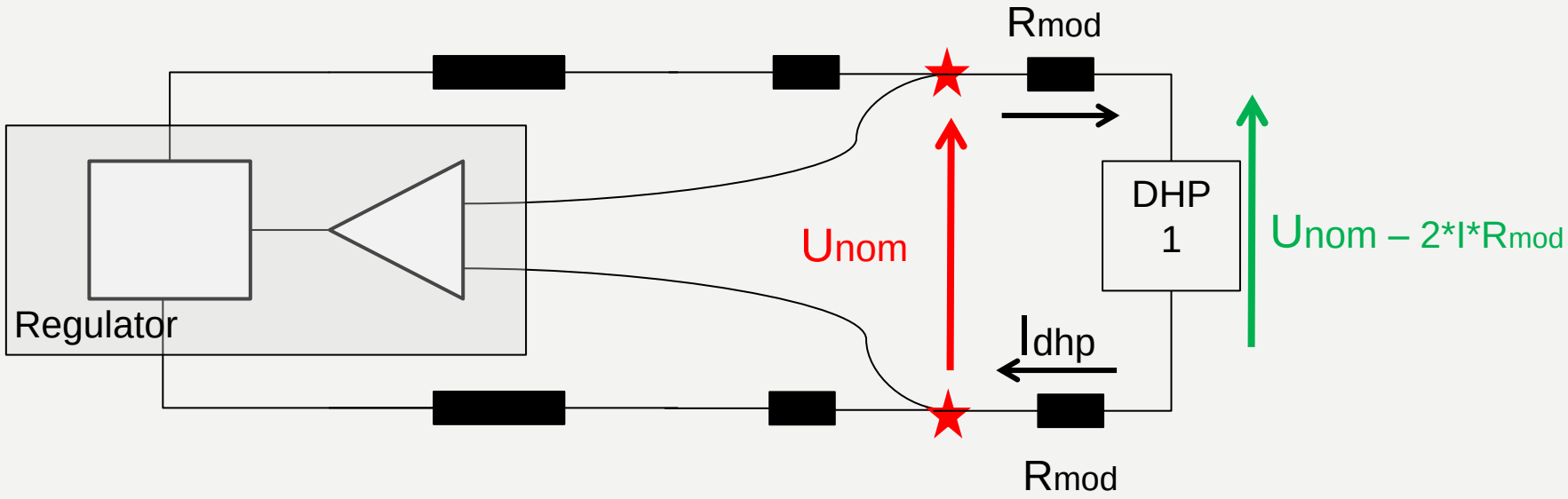


Prototype regulator
15m cables, load regulation
Voltage constant within 500µV

→DC output impedance <.2 mOhm → 0.2mV deviation at 1A load

PS Operation – Load regulation

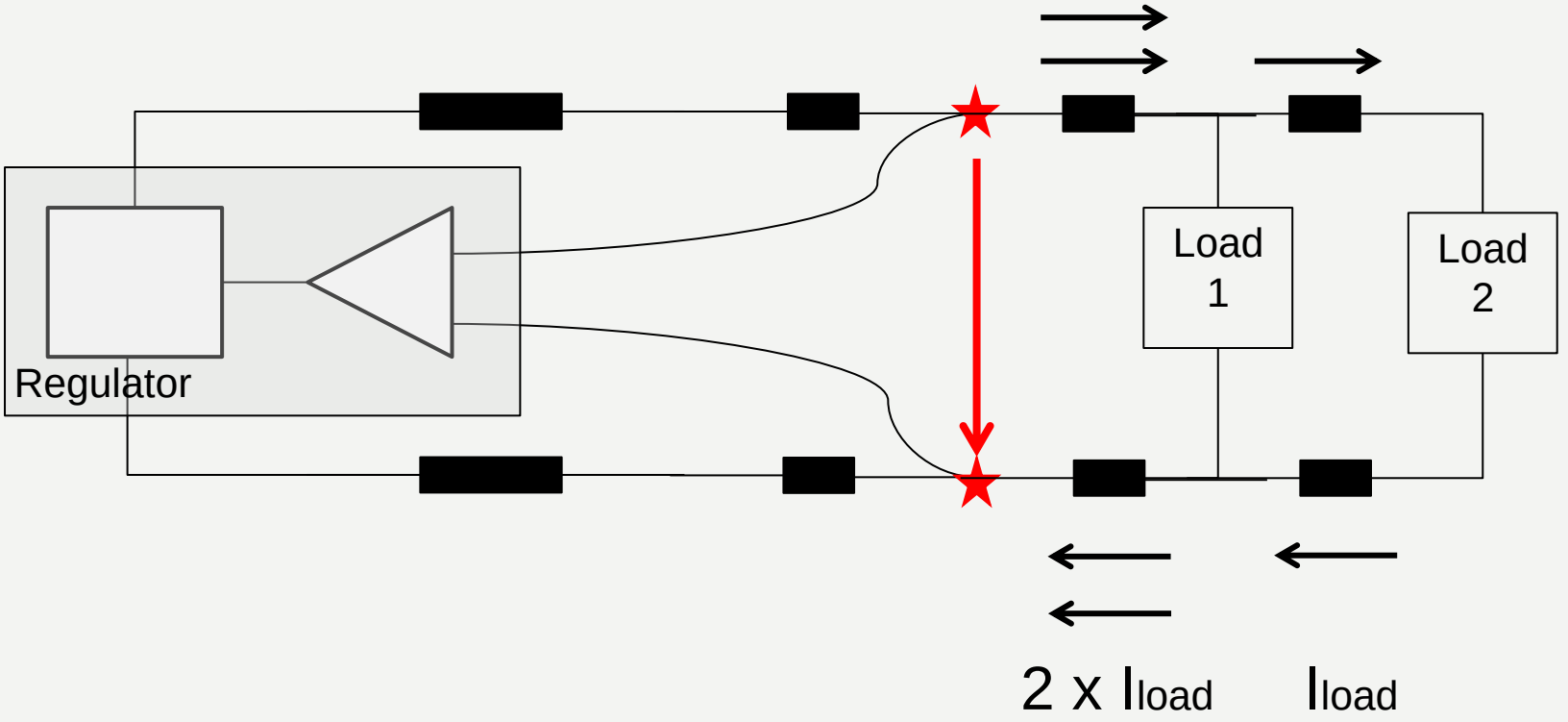
- A closer look to sensing: Sensing compensates the voltage drop till the marked point where the sense wires are connected



- 10mΩ Rmod will increase the DC output impedance from 0.2mΩ to 20.2mΩ!

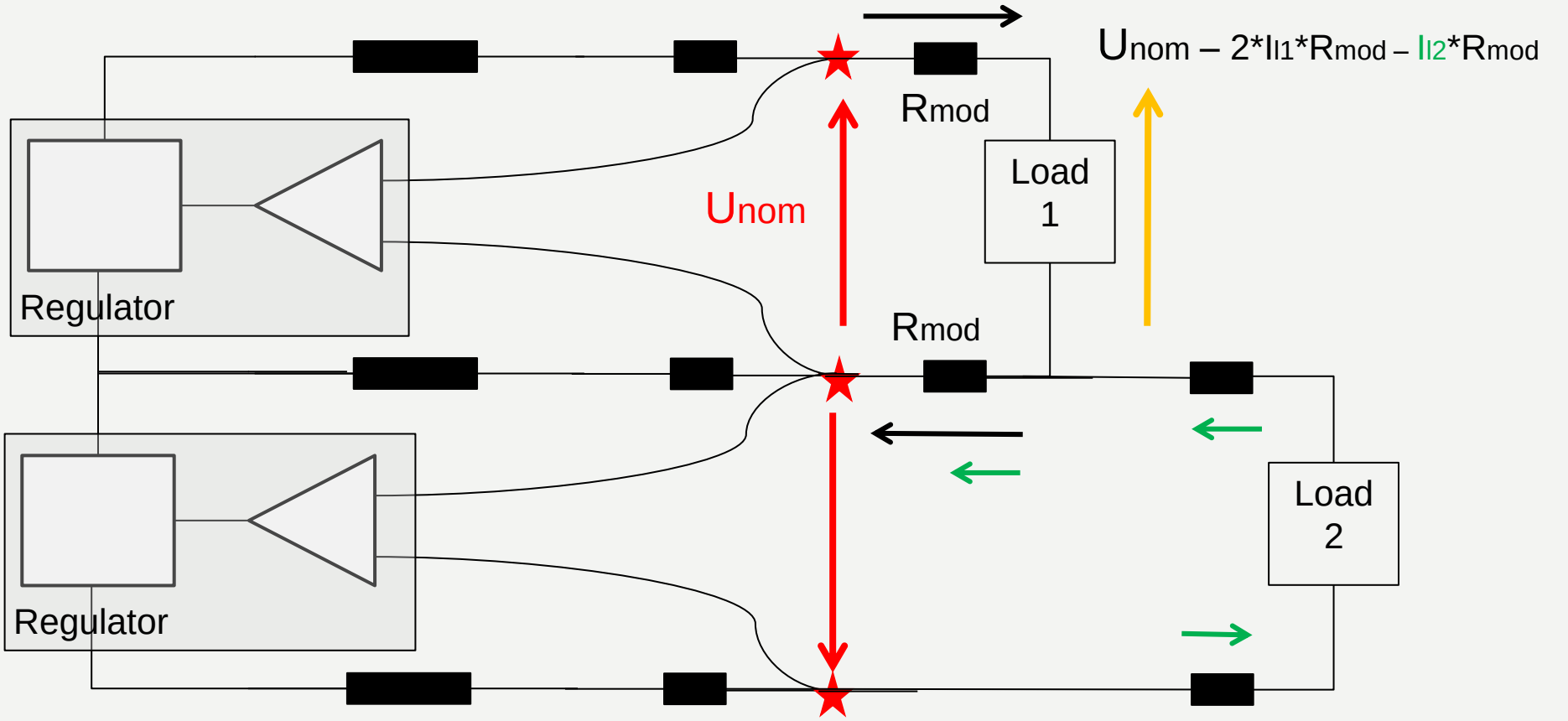
PS Operation – Load regulation

- A closer look to sensing: Series connections of loads



- In case of series connections the effect of increased output impedance gets more pronounced

PS Operation – Load regulation

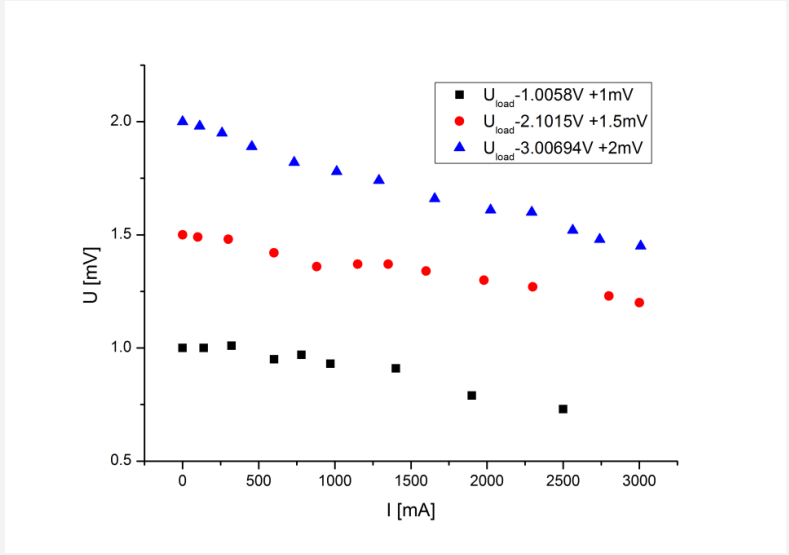


- Shared grounds add another component of potential deviations
- GND Sense wire is connected on PCB level not on Module in case of PXD6 Hybrid

PS Operation – Load regulation

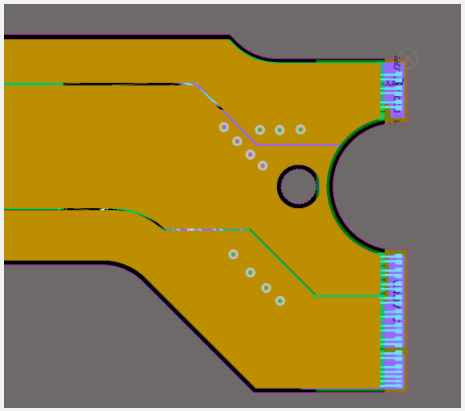
- DC output impedance is very sensitive to trace resistance downstream of the sense wire connection

→ Good PCB layout supports sensed operation



Services

Services - Kapton



- After lengthy discussions regarding fine tuning of the TML's impedance, production at Taiyo started in December
- Expected delivery time to KEK end of January
- In addition a German vendor has been qualified for a second backup test production

Next steps:

- Incorporate Capacitors into design
- Design of 4 types (Forward,Backward,Inner,Outer)

Summary

- Upgrade of Demonstrator is done
- Improvements in stability of firmware
- Preproduction is ongoing, after TB it will gain speed
- Kapton development is continued at MPI, first samples from Taiyo delivered end of January

Backup

Services – Patch Panel

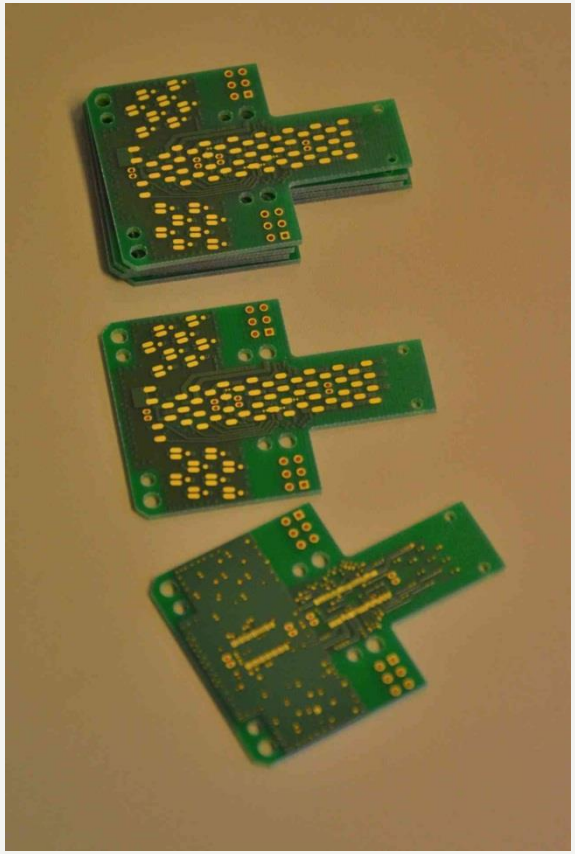
- Design of latest PP done

- Features:
  - Incorporates latest mechanical requirements
  - Solder pads for ALL cables
  - Samtec SS4/ST4 towards Kapton

- Design finished (8 Layers, Blind Vias)

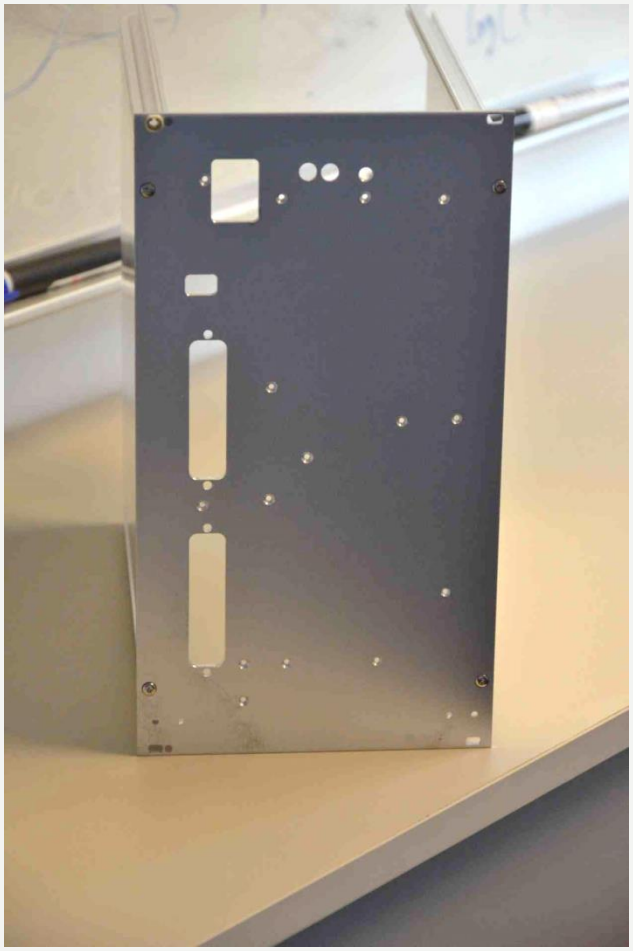
- Mechanical Dummy for solder tests has been produced
- Expected lead time 12WD for full production

→ Testing of assembly procedure crucial!



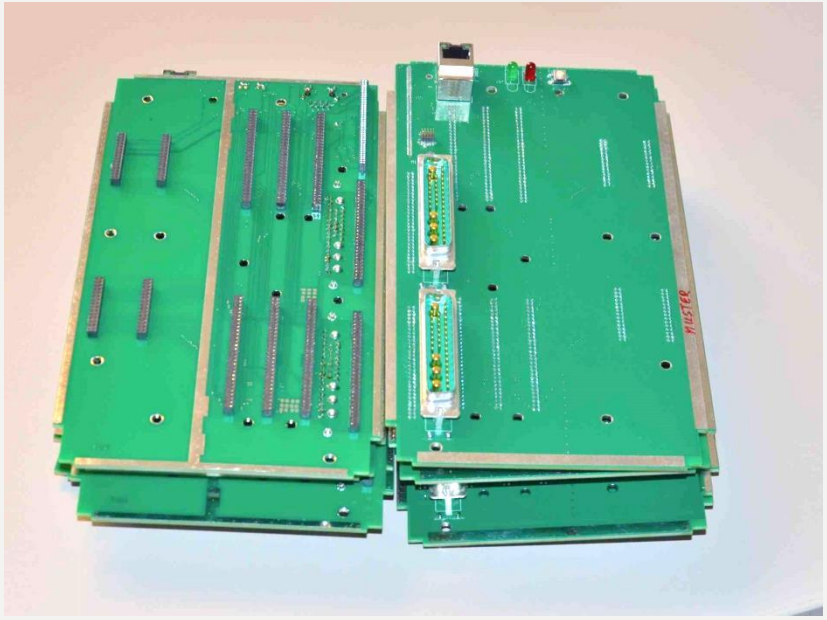
Preproduction status – Mechanics

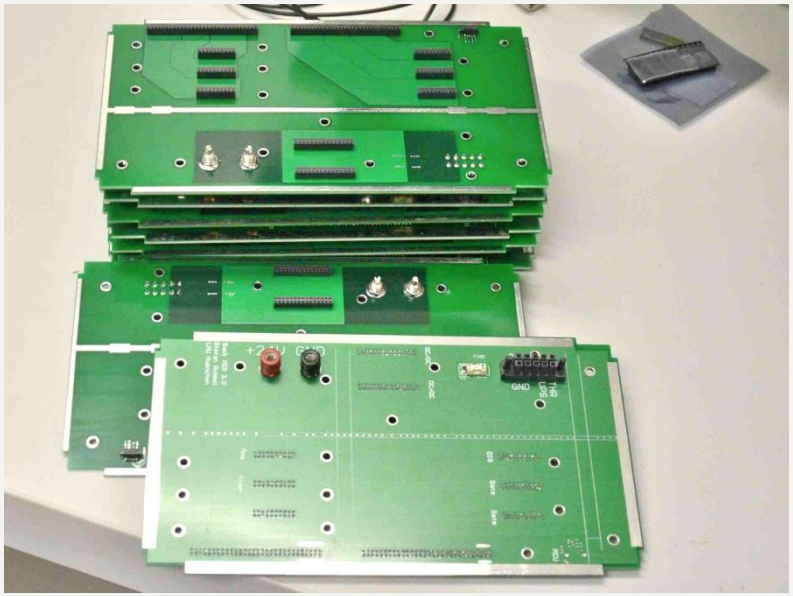
- Box designed and first sample produced
- Extra wide crate received



Preproduction status

- Several items are produced - Front PCB, Back PCB, empty OVP Card

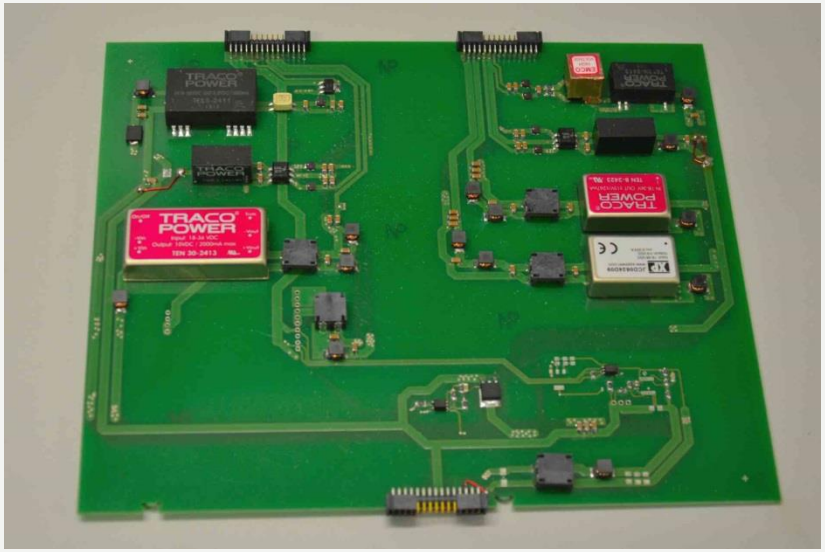


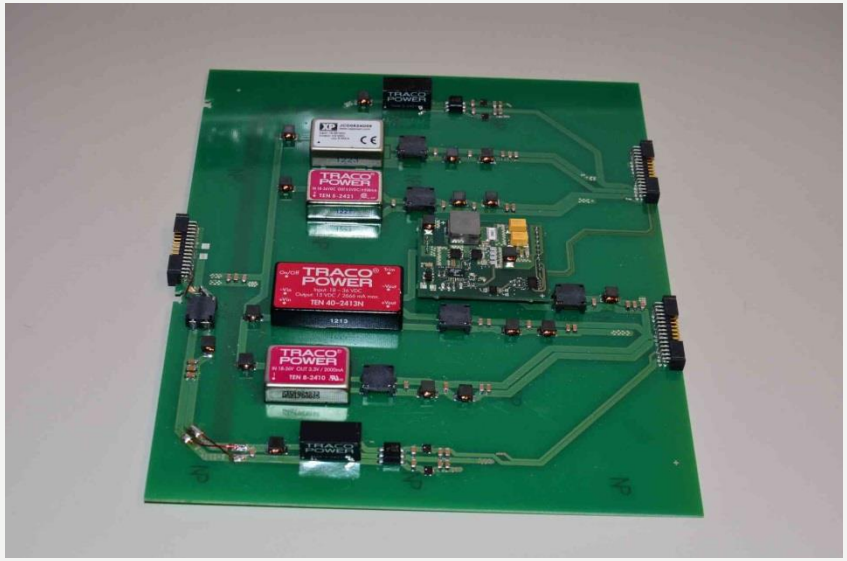


Preproduction status

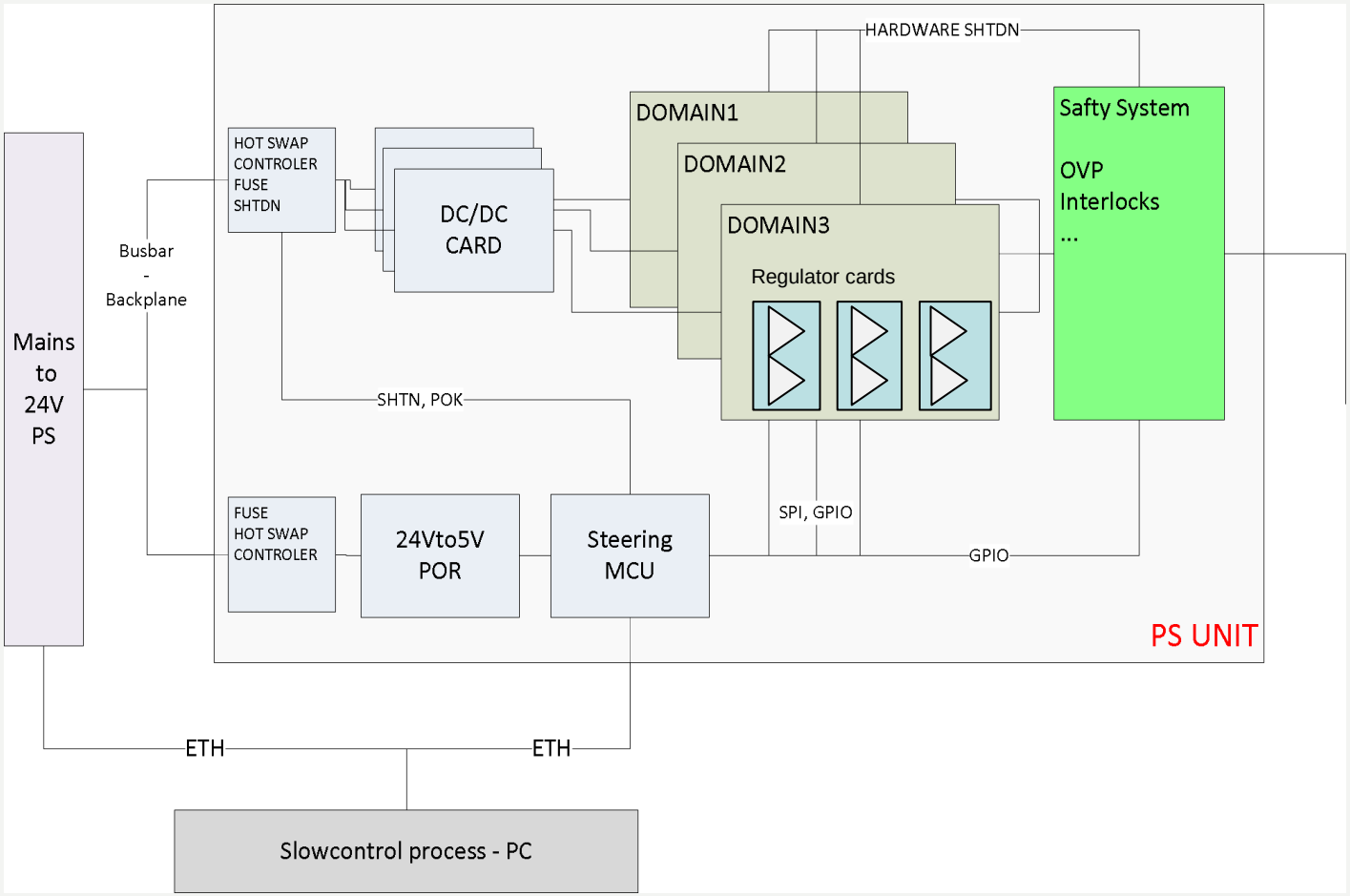
- Final DC/DC converter cards are tested, manually produced in two sets
- Step-down converter is finalized and successfully tested

→ Ready for production





PS System Layout



Demonstrator vs. Preproduction PS

	Demonstrator	Preproduction PS
# Channels	16 (up to 24)	24
Mechanics	21TE	28TE
Power distribution	37 pin D-SUB	Mixed Layout D-Sub, final cable
Output Power	DEPFET + 1 pair DCD/DHP	DEPFET + 4 pairs DCD/DHP
Slow control	Chromosome + EPICS	Chromosome + EPICS

Services – Dock Box

- Design man power kindly provided by MPI
- Layout according to our design rules
  - 100 Ohm
  - Resistance of power traces adapted to expected current
  - CMD filter capacitors

- Design is finished, received Gerber data last week
- Lead time ~12WD