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Data Handling Processor DHPT 1.0
Functional Test

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PXD/SVD Worksop, DESY, Januar 22-24, 2014

DHPT 1.0 Development

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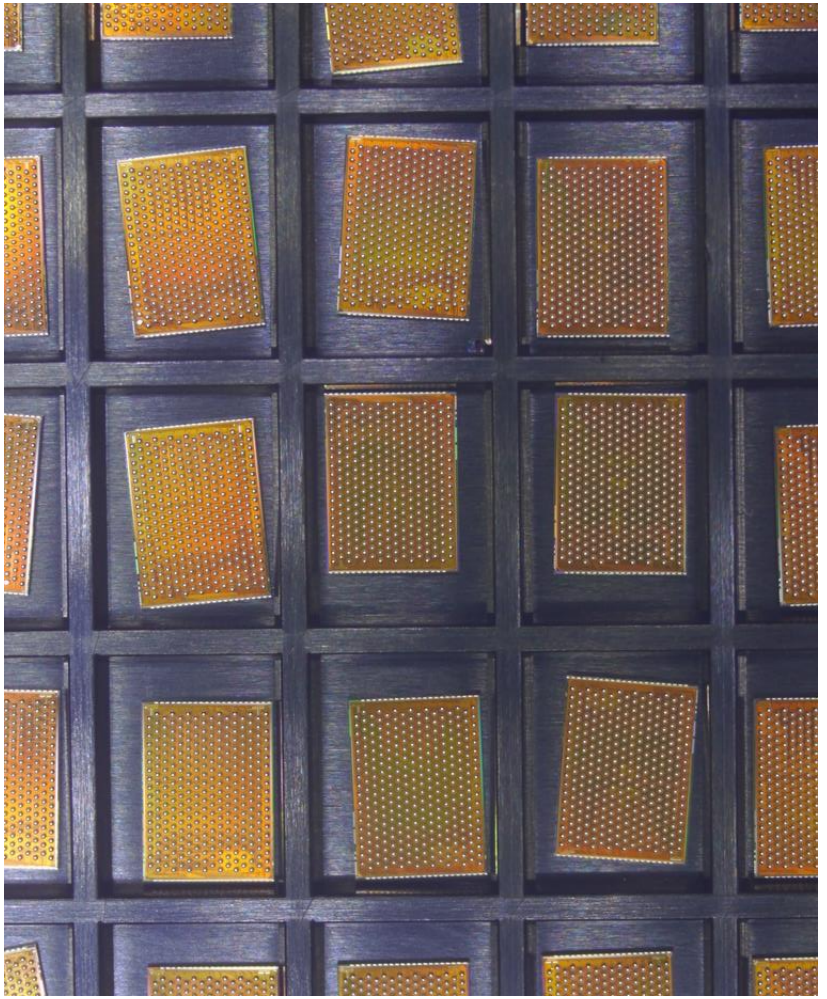
- DHPT 1.0, **first production version**
  - 12 mm^2 area, C4 bumps (SAC 305)
  - Mainly digital with analog IP blocks (PLL, serializer, Gbit link, LVDS …)
- MPW submission in Aug. 2013
- Delivery end of Nov. 2013
- 100 chips received (eq. one wafer)
- Turn-around: 3 months including bumping



Status of the Funcional Verification

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	IP Block / Task	Status	Comment
Custom IP	Gbit Link Driver	✓	
	PLL / Serializer	(✓)	Works with adjusted VCC / CLK freq.
	Temperature Sensor	✓	
	LVDS IO	✓	
	Interface DHP-DCD	TBD	Need new WB adapter (LVDS DCDCLK)
	Interface DHP-Switcher	TBD	
	Bias DAC, Currrent reference	✓	
Data Processing	Command Interface (Manchester encoded)	✓	
	Memory Access (via JTAG)	✓	
	Data Processing: Channel Masking	TBD	
	Double Precision Common Mode Processing	TBD	
	Overflow Handling	TBD	

Serializer Issue

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- Serializer works, but VCC and/or GCK have to be adjusted:
  - GCK= 80 MHz → VCC = 1.6V (works but should not be applied for a long time)
  - GCK= 60 MHz → VCC = 1.4V (ok)
- Simulation with typical process parameters is Ok
- Manufacturer test data ➔ wafer batch has „slow NMOS“ (too high threshold)

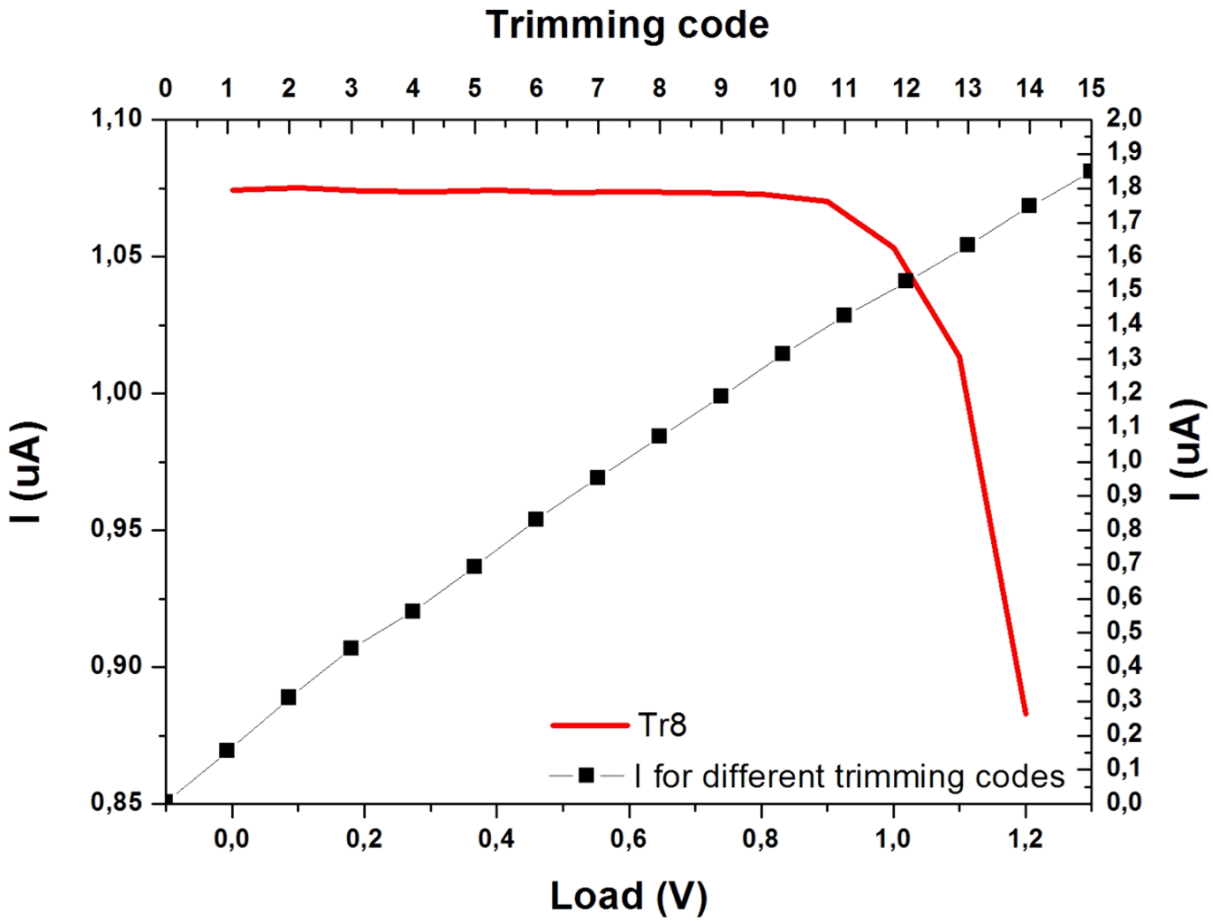
PARAMETER BY LOT:		SPEC LO	SPEC HI	MIN	MAX	MEAN	STD DEV
VTl_N4	(N/.3/.06/1)	0.300	0.490	0.368	0.490	0.423	0.029
Isof_N4	(N/.3/.06/1)	-1.400E-07	0.000	-8.958E-10	-3.833E-11	-2.339E-10	2.063E-10
Isat_N4	(N/.3/.06/1)	0.491	0.735	0.547	0.673	0.593	0.031

- Re-simulation with „slow NMOS“ corner reproduced the observed speed limitations
- Issue within the Serializer localized → can be fixed with a small design change

Analog Blocks – Current Reference

Temerature Independent Current Reference

- Compliance ✓
- Trimm functionality ✓
- Temeprature sensitivity TBD



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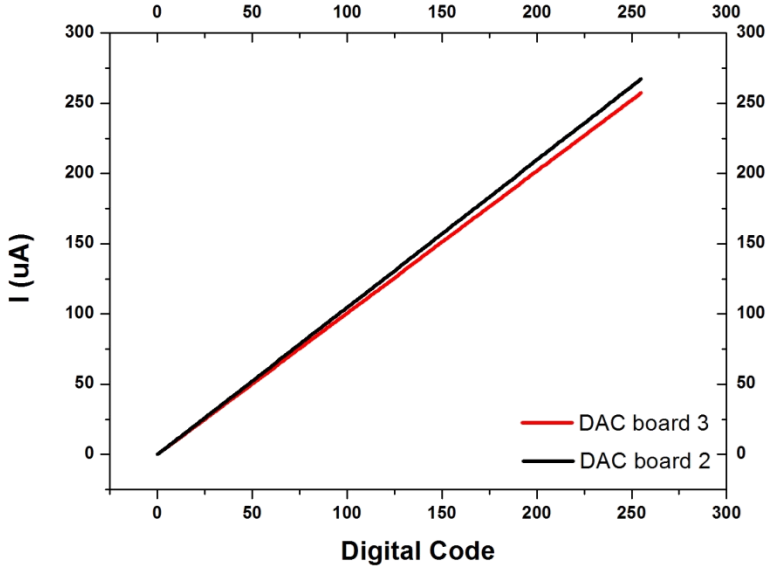
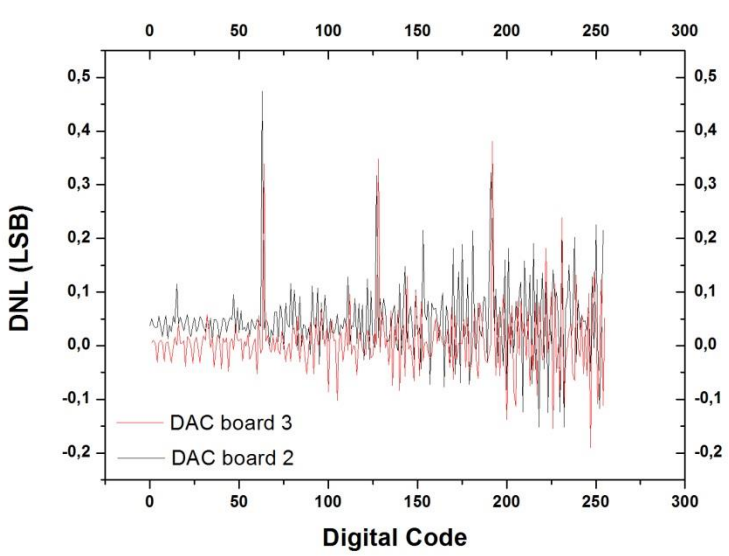
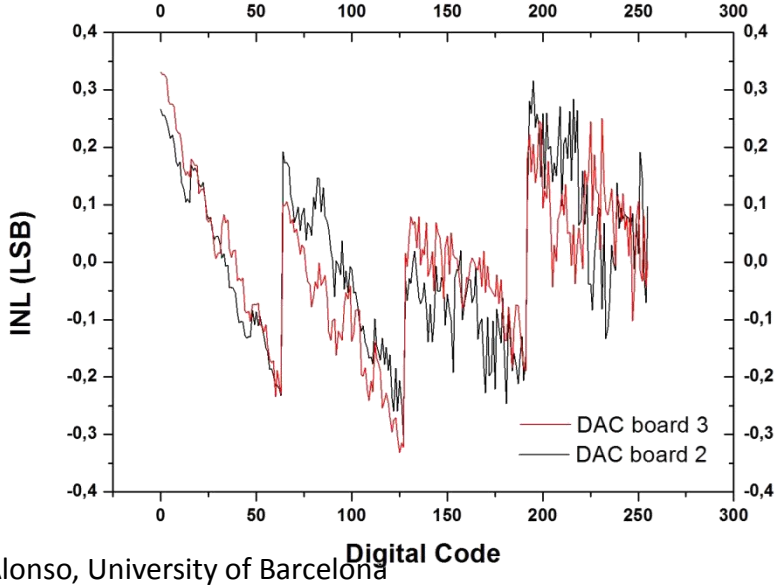
Analog Blocks – 8-bit DAC

8-bit DAC for bias current control

- Dynamic range ✓
- Linearity ✓







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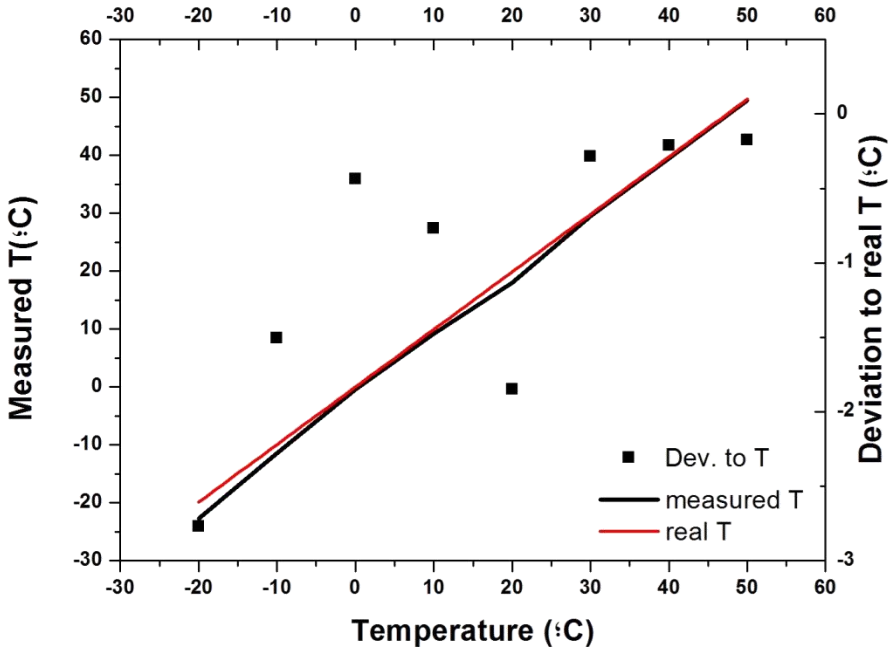
Analog Blocks – Temperature Sensor

Internal or external sensing diode + 16 bit Sigma-Delta ADC

- Measurement range -20°C ... +60°C ✓
- Accuracy ±1°C ✓



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Status & Outlook

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- Functional verification: DHPT 1.0 mounted on PCB with WB adapter→ ongoing
  - Analog blocks ✓
  - Digital signal processing → ✓, ongoing
  - Interface DCD, Switcher → TBD
  - Serializer needs non standard operation conditions
- Next verification steps
  - Full functional coverage with current PCB test setup
  - Probe station tests → known good die
  - System tests!!! (E-MCM…)
- Planned re-design DHPT 1.1
  - Serializer bug fix
  - Anything else that eventually shows up (Data processing, E-MCM operation …)
- DHPT 1.1 tentative schedule
  - Tape-out: April
  - Delivery: July
  - Tested production chips available starting from September

DHPT Production Details

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- MPW submission
  - Cost (12 mm^2, one wafer included): 59 TUSD + 12 TUSD for bumping ➔ 52 TEUR
  - Extra 12“ wafer (100 chips): 9 TUSD
  - Two MPW runs per month, turn-around ~12 weeks

- PXD production
  - Can be done with MPW production + extra wafers, no engineering run needed
  - 160 chips for 40 modules + overhead for E-MCM, test assemblies, production contigency etc.
  - How many „green“ chips do we need?

- DHPT (65nm only) production costs
  - 2x test chip (mini@sic DHPT 0.1 & DHPT 0.2) ➔ 45 TEUR
  - 2x MPW (DHPT 1.0 & possible redesign DHPT 1.1) + 5 extra wafers ➔ 140 TEUR