universitätbonn

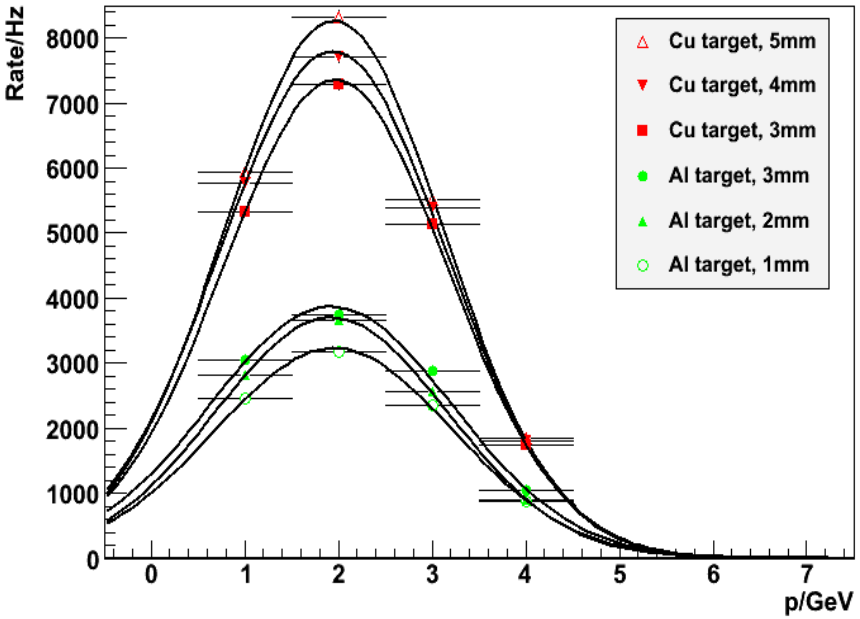
PXD TB Status

C. Marinas for the DEPFET Collaboration

cmarinas@uni-bonn.de

Introduction

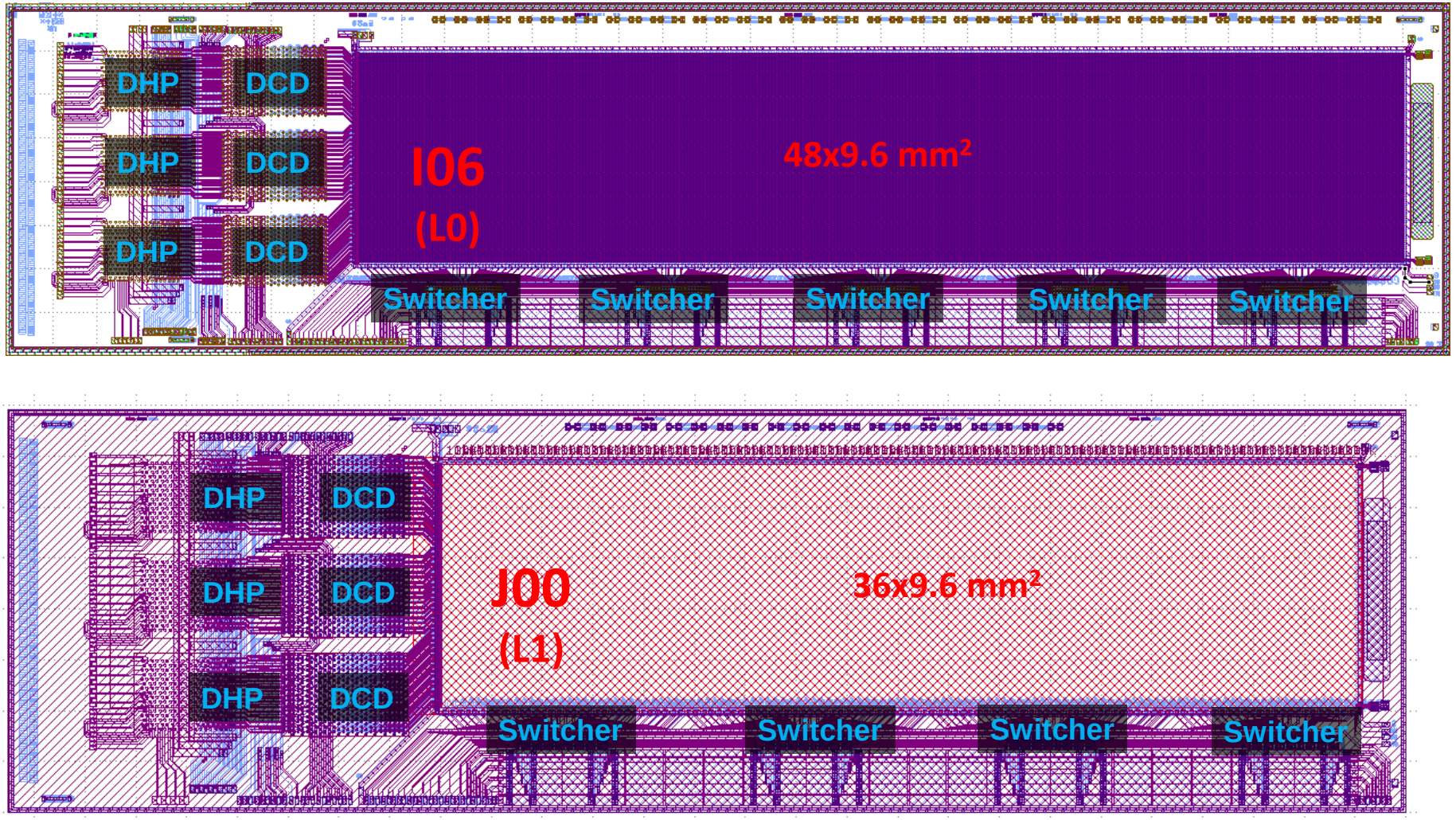
- VXD common test beam in January 2014 (4 weeks)
- Small sector of the close to final prototype detectors and ASICs
  2 PXD half ladders + 4 SVD single module layers
- Complete VXD readout chain: HLT, monitoring, event building, PocketDAQ
- CO_2 cooling, slow control, environmental sensors
- Illumination with (up to) 6 GeV e^- under solenoid magnetic field (PCMAG)
- Alignment, tracking algorithms, ROI



- **Goal**: System integration test

cmarinas@uni-bonn.de

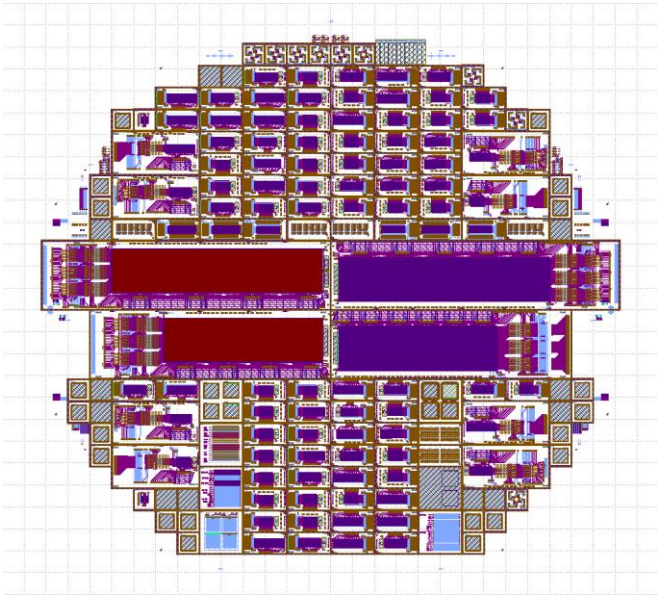
Long PXD6 – TB Devices Under Test



cmarinas@uni-bonn.de

Sensor Description

- **I06**
  Belle II Standard Design
  50x75 µm²
  768 drain lines (256x3 DCD/DHP)
  160 gate/clear lines (5 Switcher)

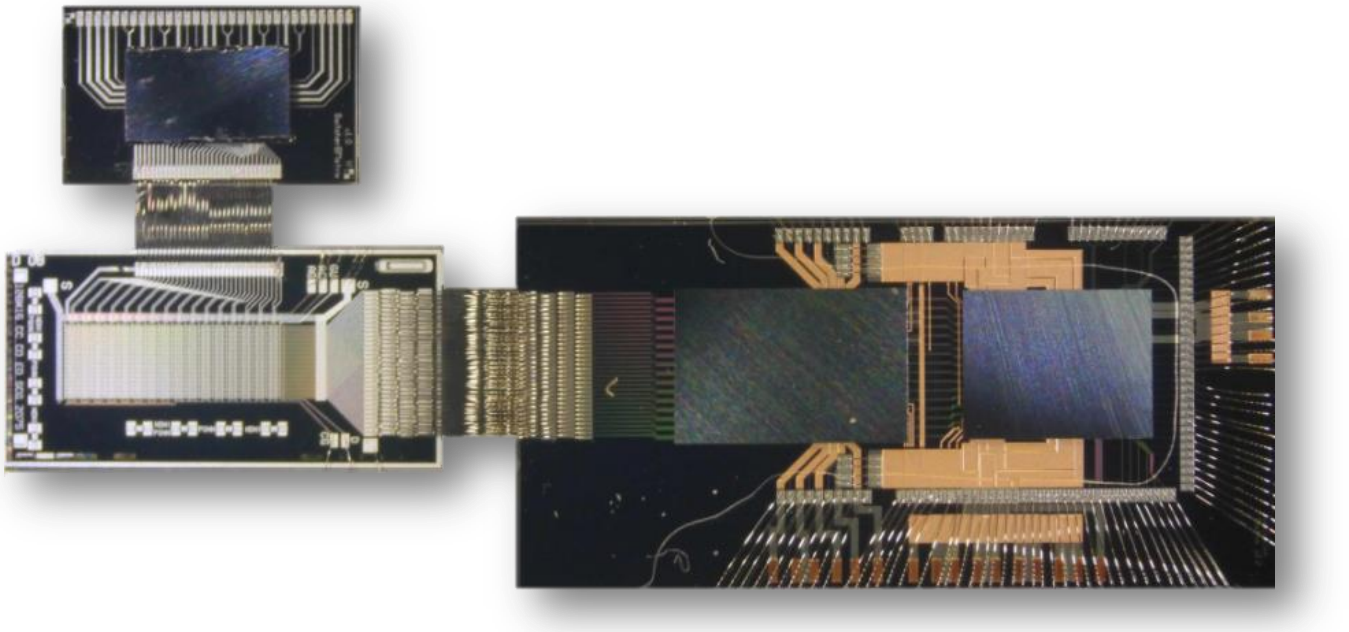


- **J00**
  Capacitive Coupled ClearGate
  50x75 µm²
  768 drain lines (256x3 DCD/DHP)
  120 gate/clear lines (4 Switcher)

- **ASICs**
  DCDBv2, DHP0.2, SwitcherB1.8G (in non gated mode)

cmarinas@uni-bonn.de

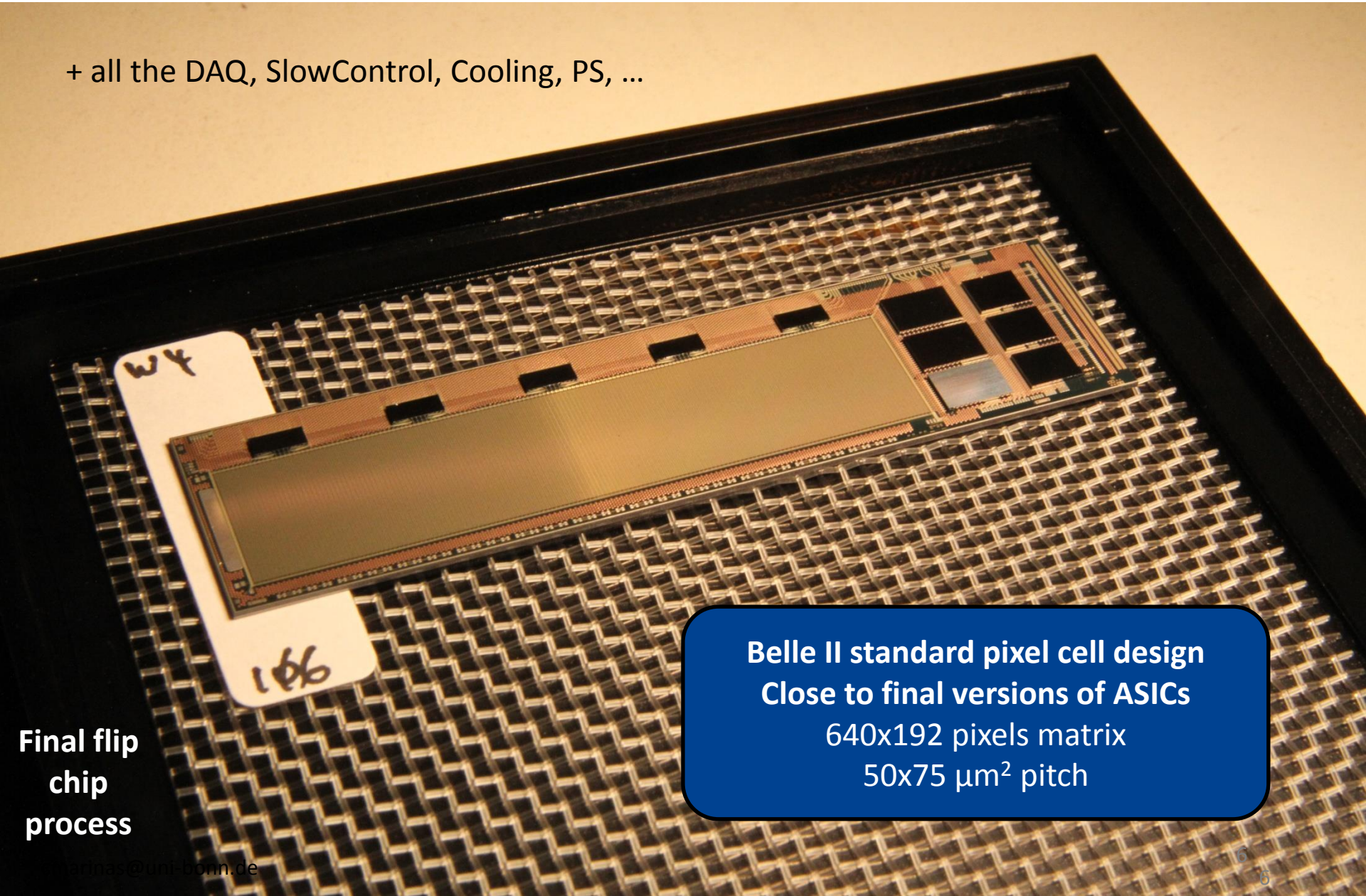
From this…



cmarinas@uni-bonn.de

… to this

+ all the DAQ, SlowControl, Cooling, PS, …

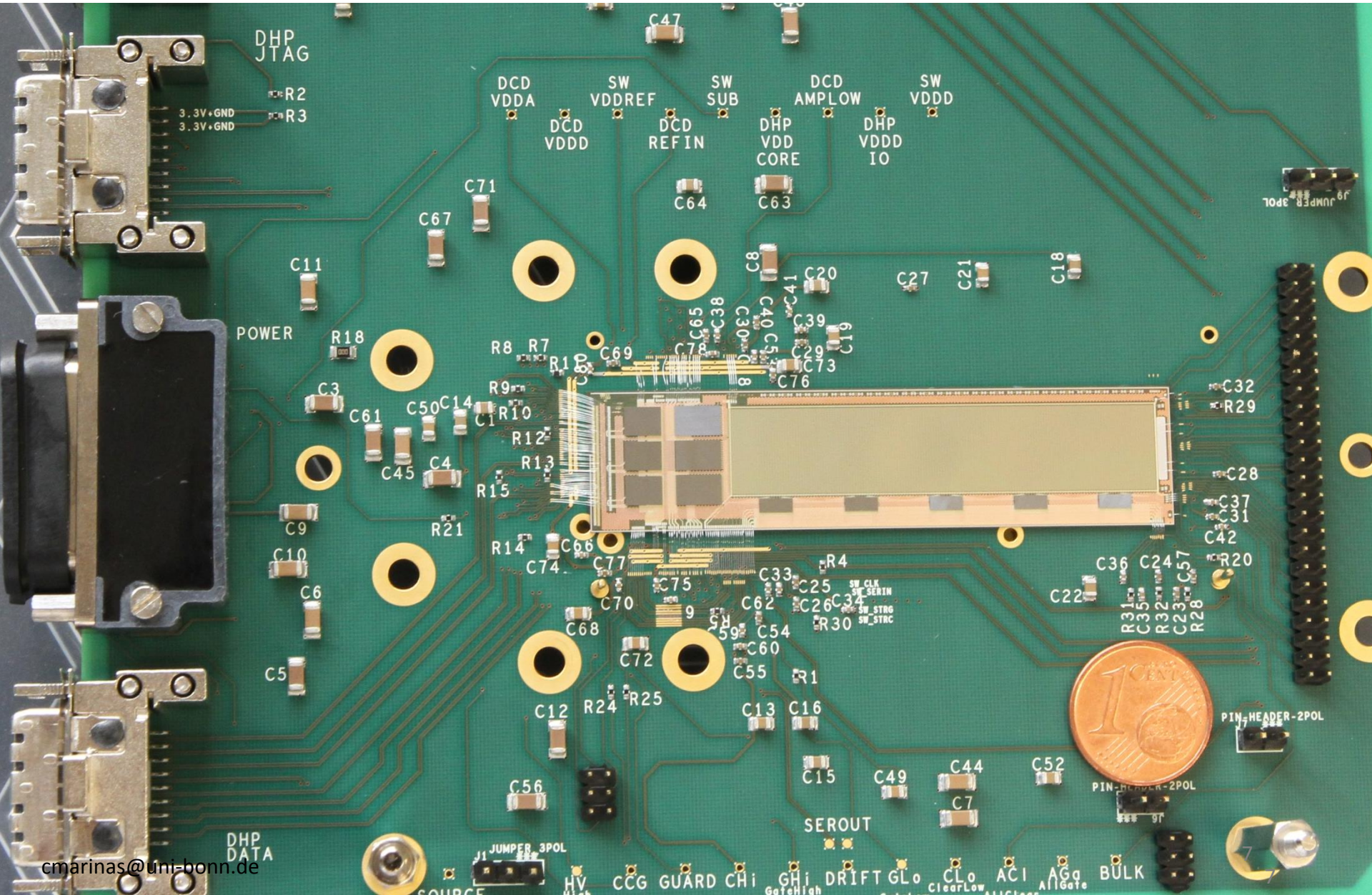


Belle II standard pixel cell design
Close to final versions of ASICs
640x192 pixels matrix
50x75 µm² pitch

Final flip chip process

harinas@uni-bonn.de

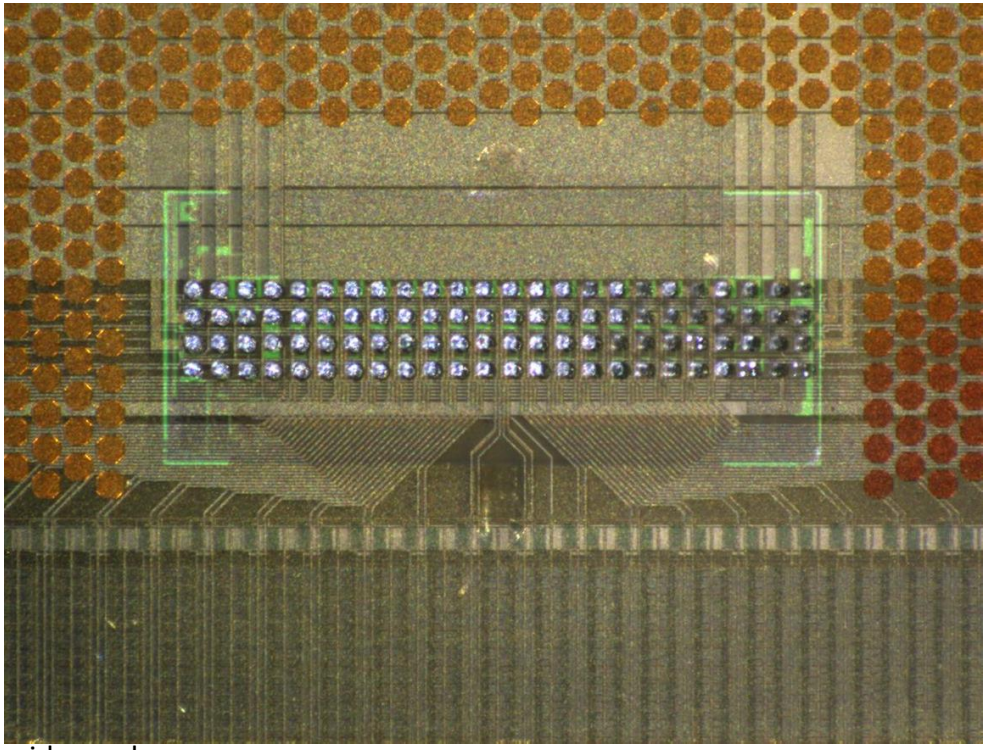
PXD6 on Hybrid6



cmarinas@uni-bonn.de

Damaged Detector

- Differential to single ended converter chip has been operated at 3.3 V
- The Switcher technology is designed to be operated at 1.8 V
- Protection diodes were activated
- Switchers did not show any power consumption (current flow)
- ASICs were powered through the JTAG bus/pins
- Switchers has been damaged → need to be replaced



Rework at Finetech

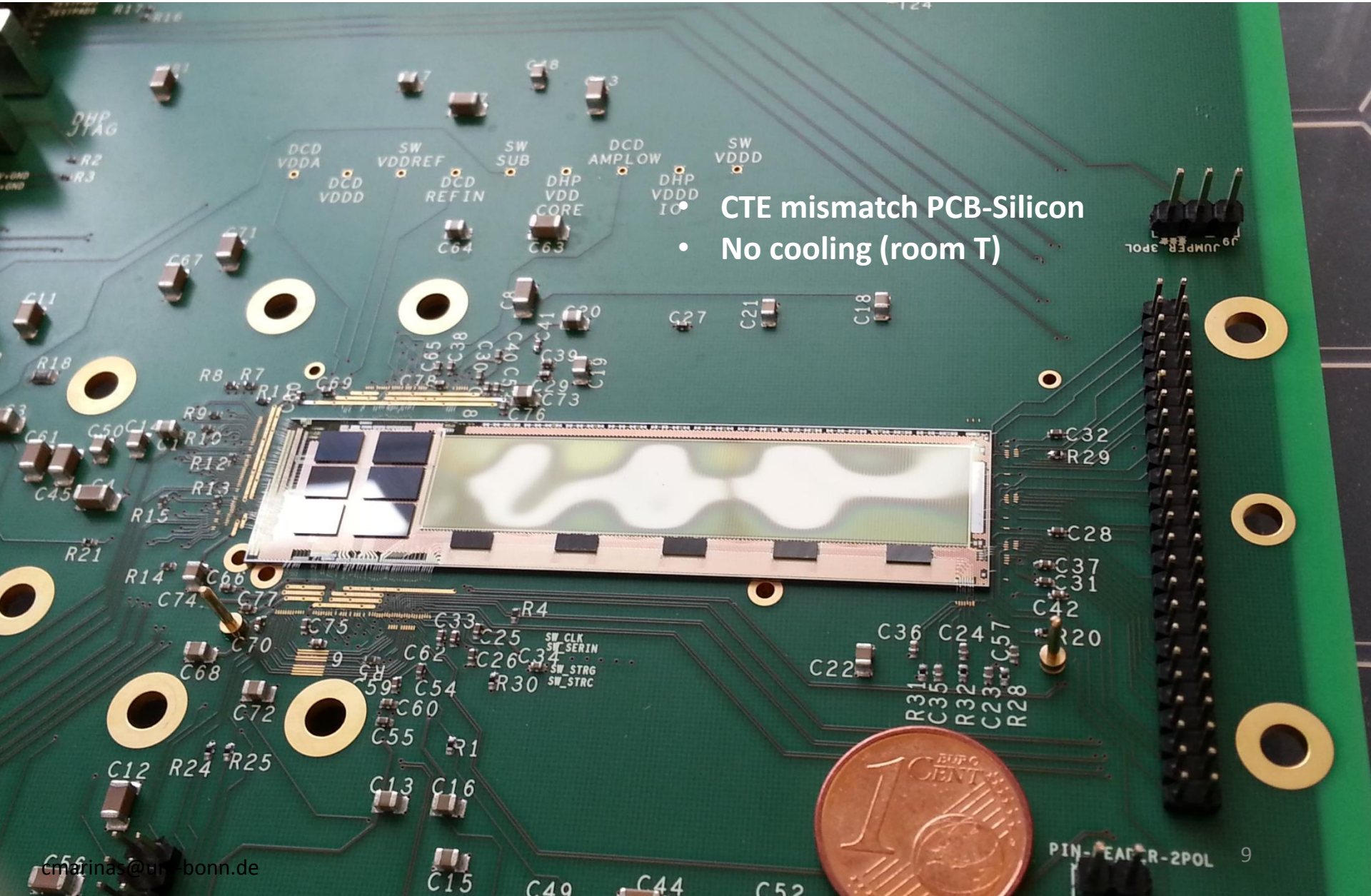
Switchers being replaced

Expected end of this week

EMCM with PXD6 and
Hybrid 5.0 as back up

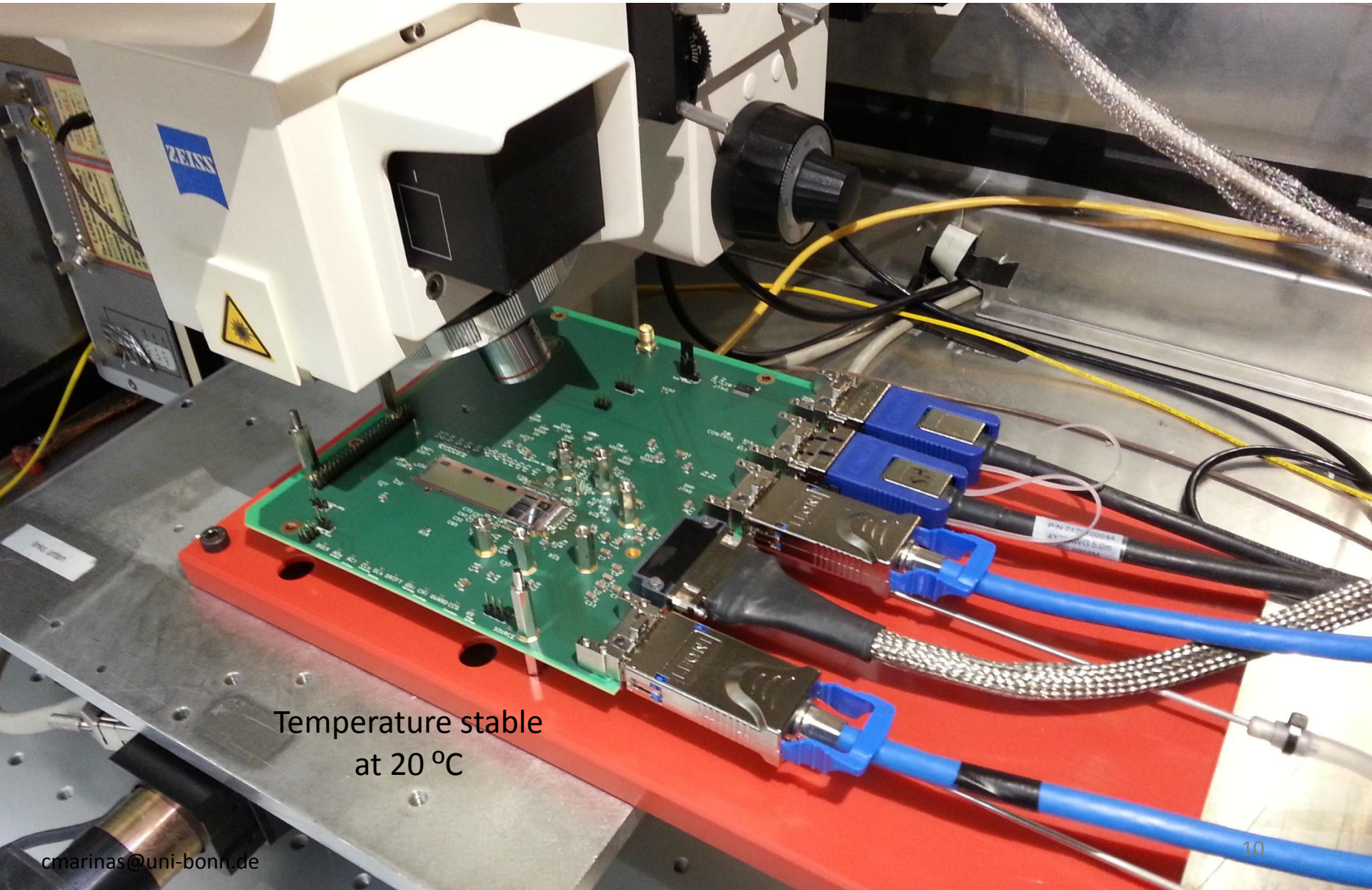
cmarinas@uni-bonn.de

Sensor Deformation



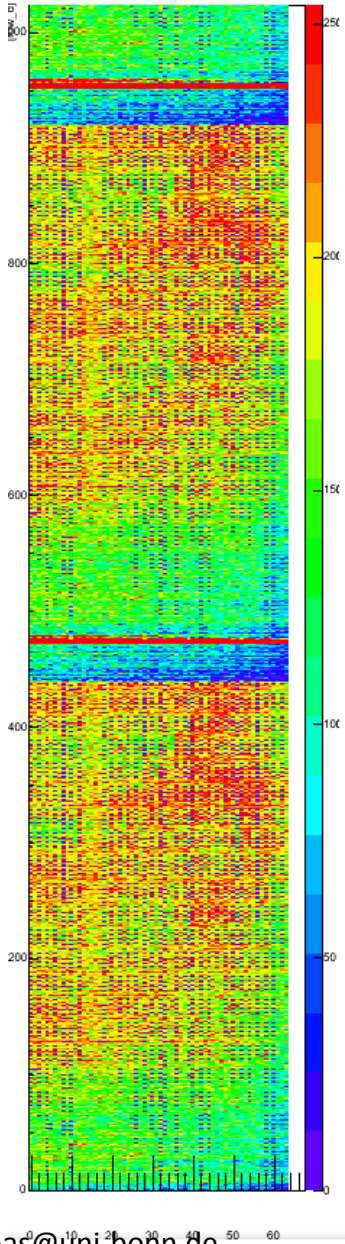
- CTE mismatch PCB-Silicon
- No cooling (room T)

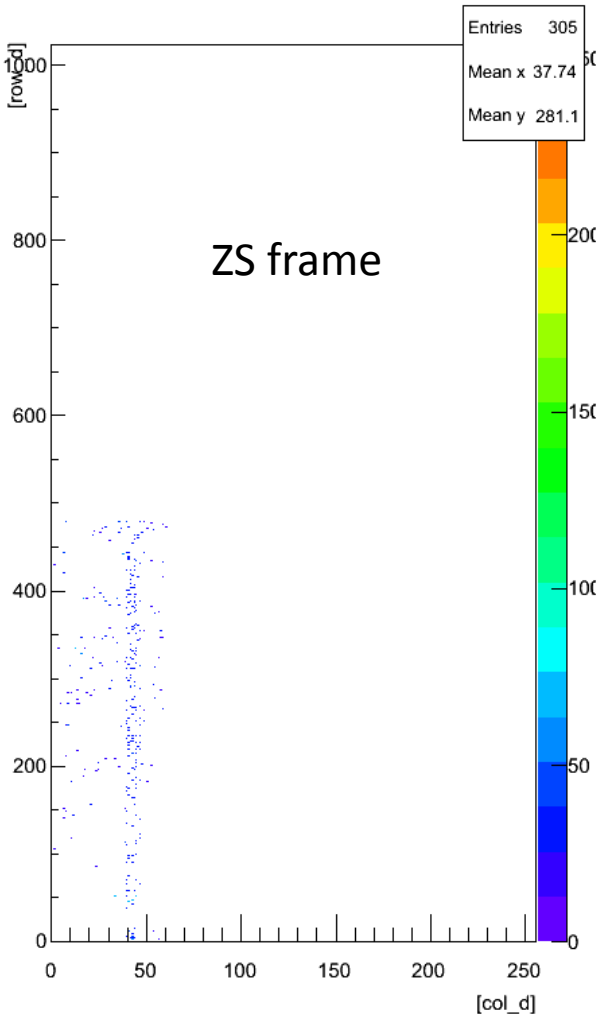
Laser Setup PXD6-J00



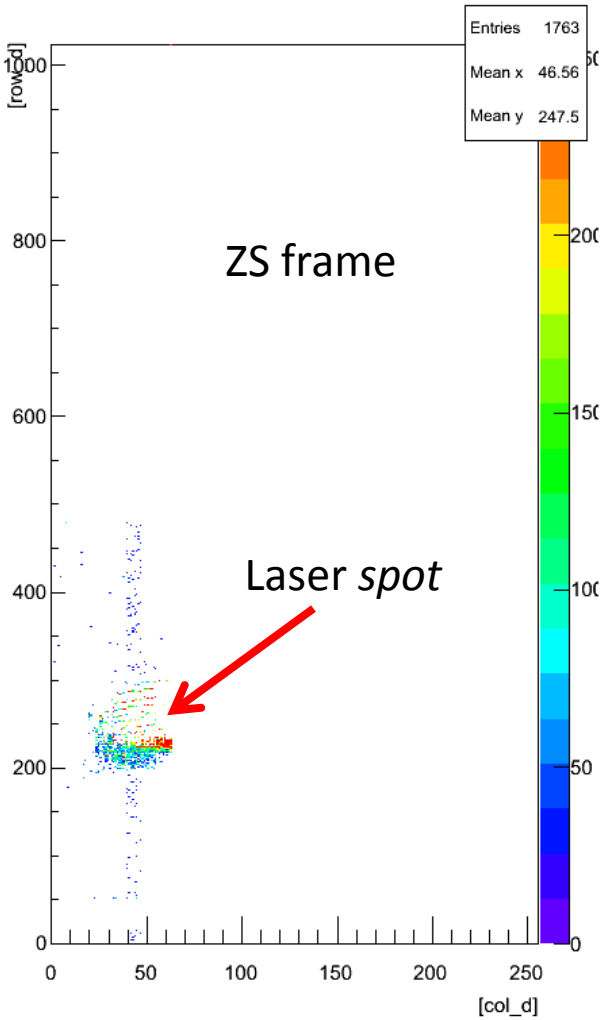
Temperature stable
at 20 ^{o}C

Pedestals and Signal





No optimization performed



Pedestal distribution (two frames) (64x480 pixels)

cmarinas@uni-bonn.de

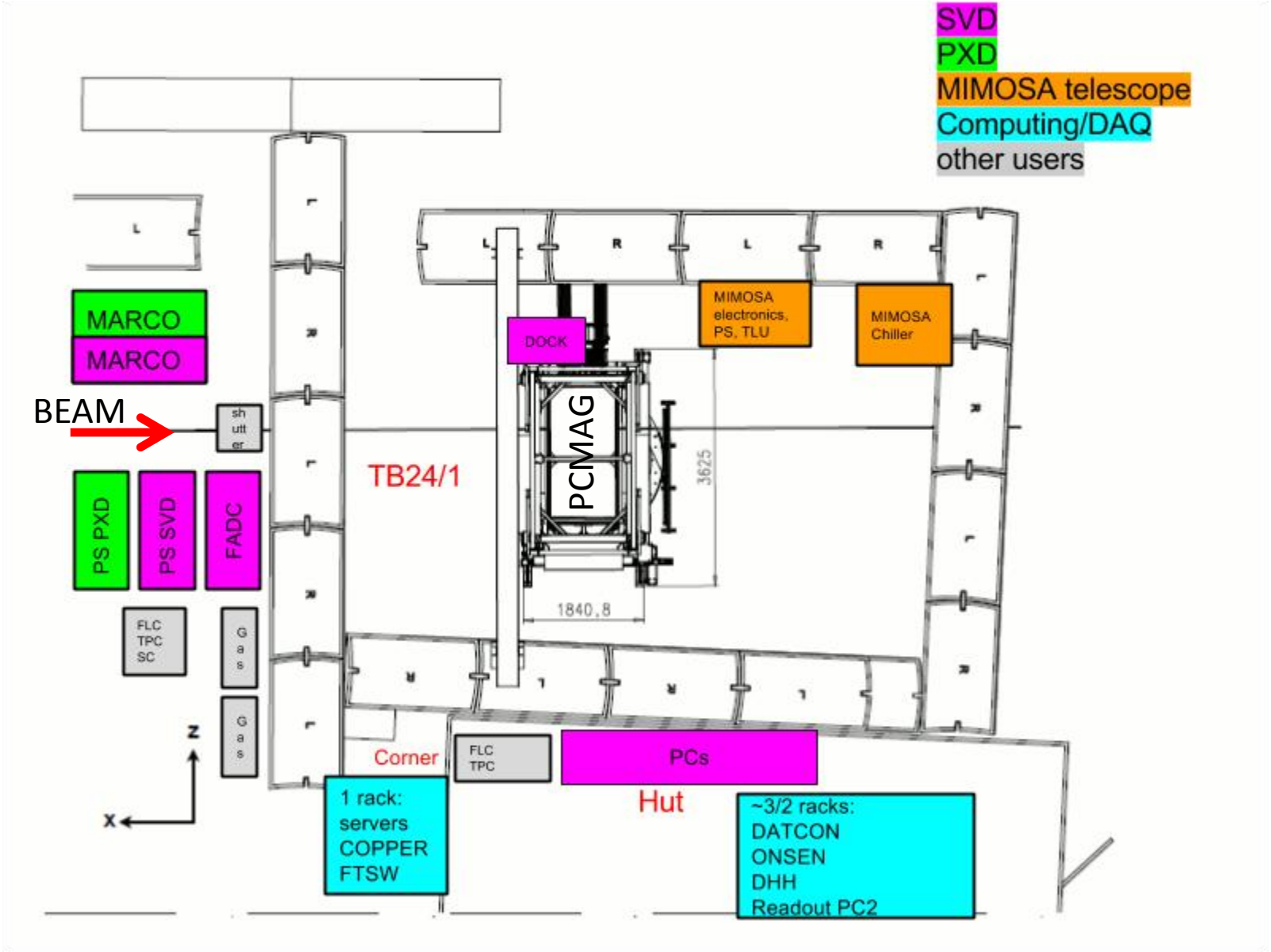
Schedule

14. Okt 13	42		CMS TrkPh2-J							announced
21. Okt 13	43		CLICpix	---	---	CALICE AHCAL	LorAngle	---	---	
28. Okt 13	44	no beam 2/11/2013	CMS FPIX	---	---	GSI-DIRC	LorAngle	---	---	
04. Nov 13	45		CMS Pix	---	---	GSI-DIRC	LorAngle	---	---	
11. Nov 13	46		ALICE ITS	---	APIX PPS	---		---	---	
18. Nov 13	47		CMS TrkPh2-E		APIX PPS					
25. Nov 13	48		CMS TrkPh2	---	APIX PPS	---	Belle-II Installation			
02. Dez 13	49		CLICpix	---	APIX PPS	---				
09. Dez 13	50		SiPM	---	---	CALICE AHCAL				
16. Dez 13	51	End of beam 19/12/2013 0800	---	---	---	---				
23. Dez 13	52									
2014										
6-Jan-14			FCAL	---	---	CALICE AHCAL	Belle II VXD			Announced
13-Jan-14	3		FCAL	---	---	CALICE AHCAL	Belle II VXD	---	---	
20-Jan-14	4		SBS GEM	---	APIX 3D		Belle II VXD	---	---	
27-Jan-14	5		SBS GEM	---	DIAPIX		Belle II VXD	---	---	
3-Feb-14	6		LHCb VELO	---	MuPix	---	LorAngle	---	---	
10-Feb-14	7		LHCb VELO	---	ATLAS Strip	---	---	---	PLUME	
17-Feb-14	8		ATLAS Lucid	---	ATLAS Strip	---	---	LCTPC Time	---	
24-Feb-14	9			SiPM	APIX PPS		---	LCTPC Time	---	
3-Mar-14	10		CMS TrkPh2-E		APIX PPS					

Test beam preparations at the experimental hall started end of November

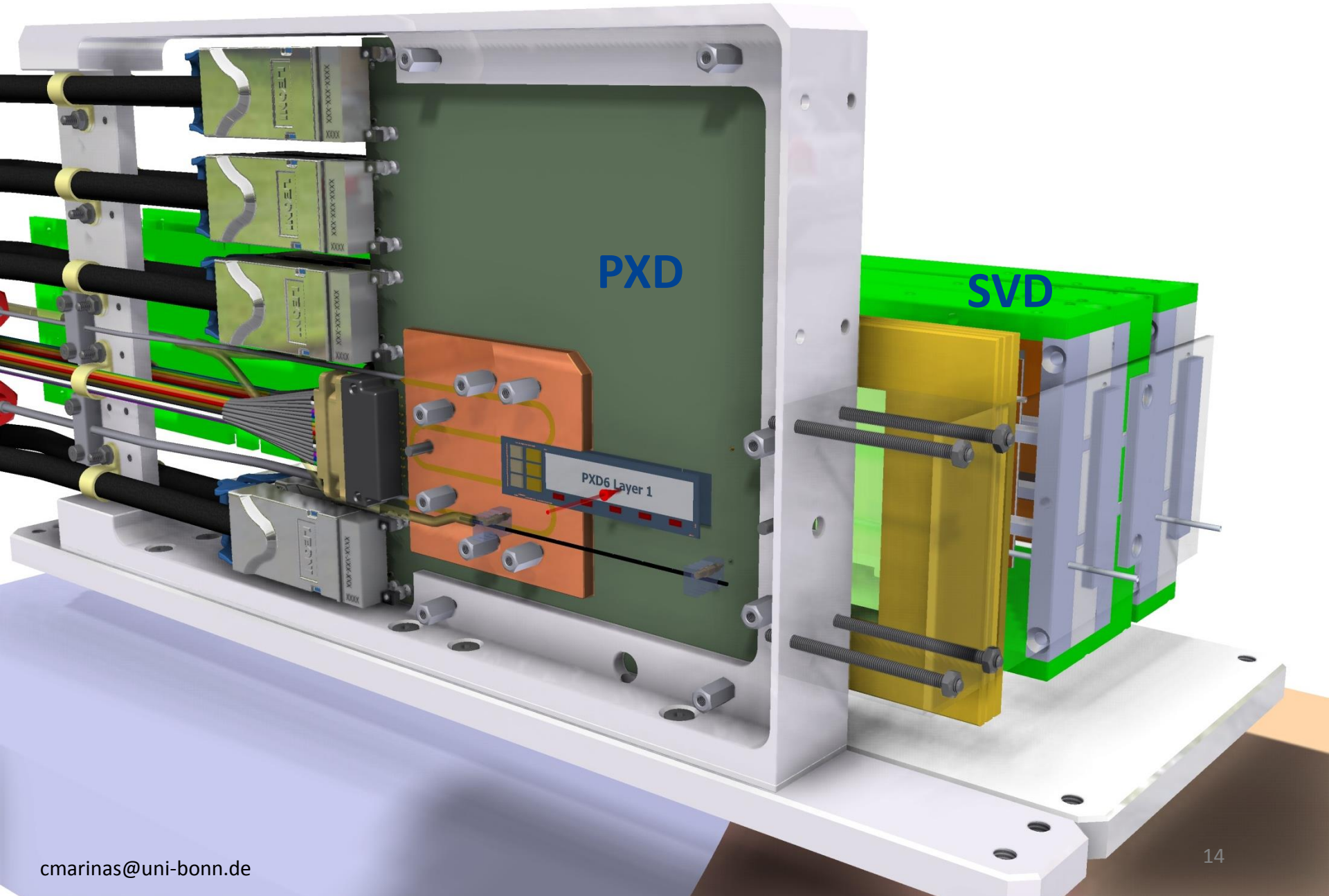
Two months of ‘test beam-like’ (*sort of*) life

General Layout



cmarinas@uni-bonn.de

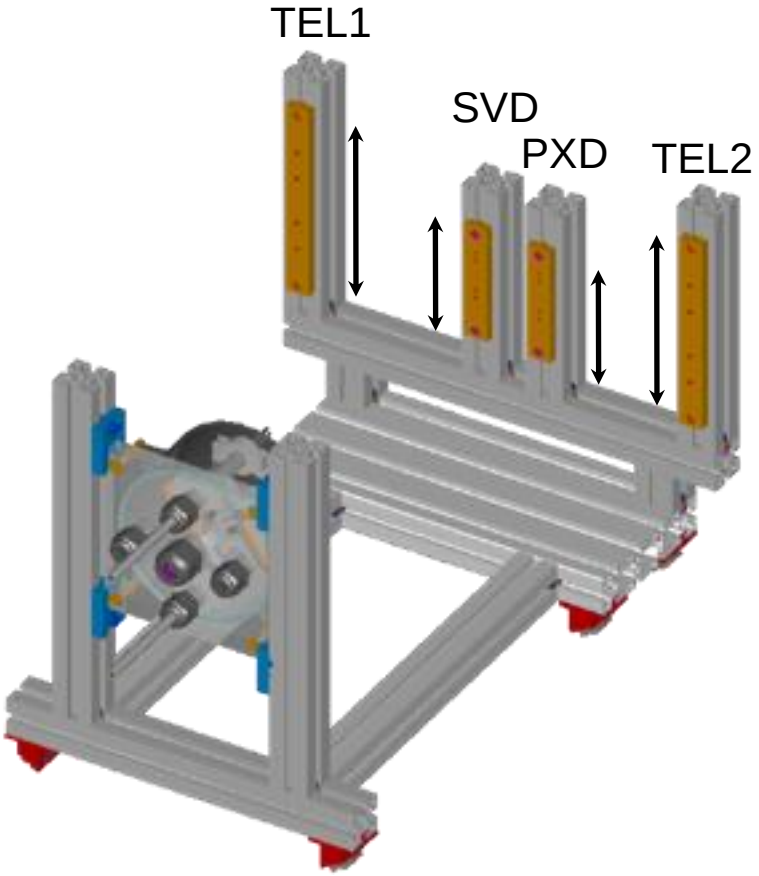
Mechanical Set-up



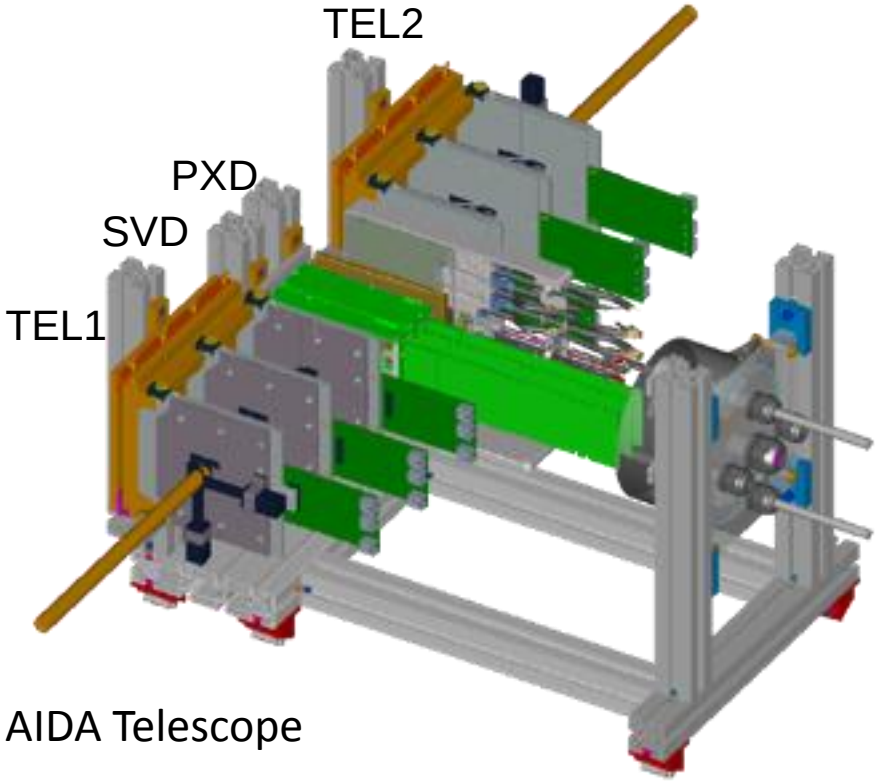
cmarinas@uni-bonn.de

VXD and AIDA Telescope

Four independent possibilities
to adjust height

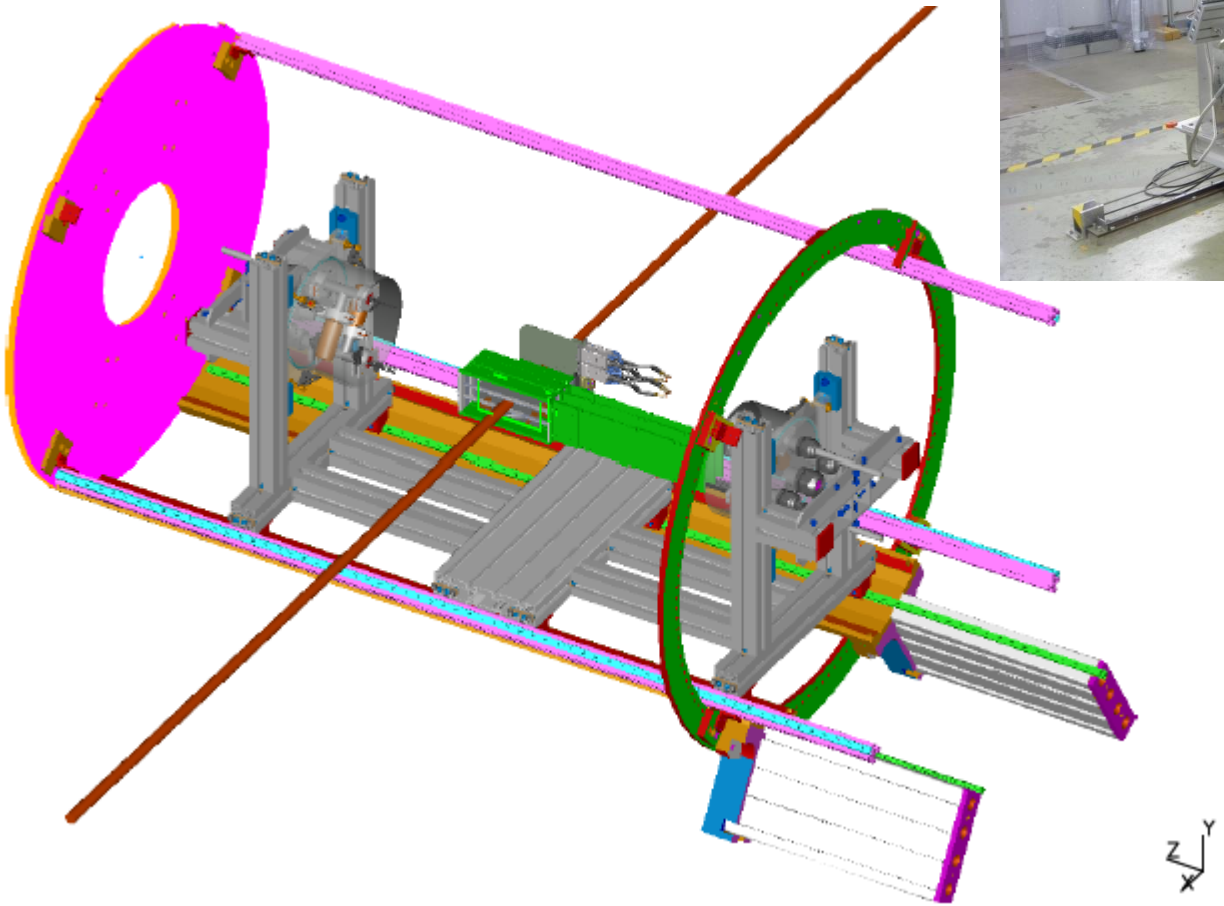


Support frame



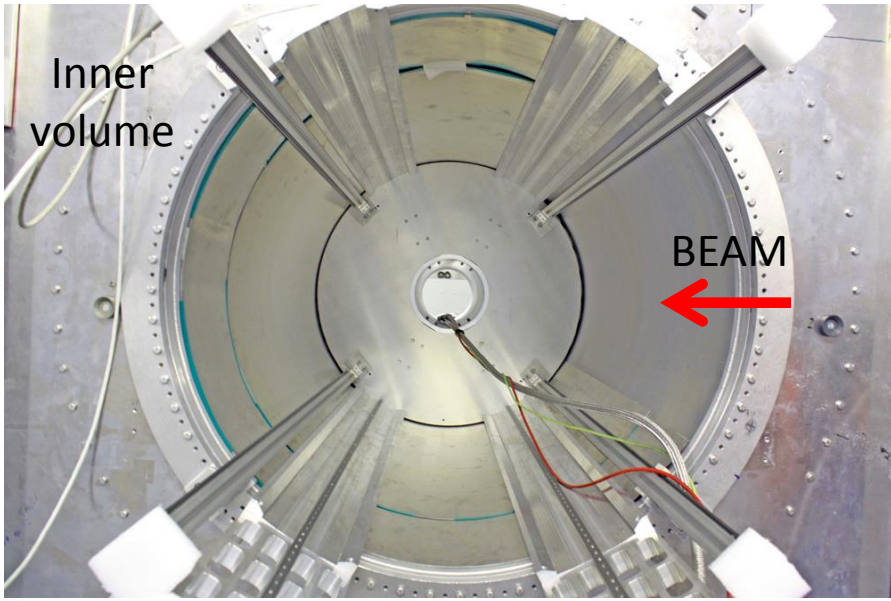
AIDA Telescope

Integration into the PCMAG

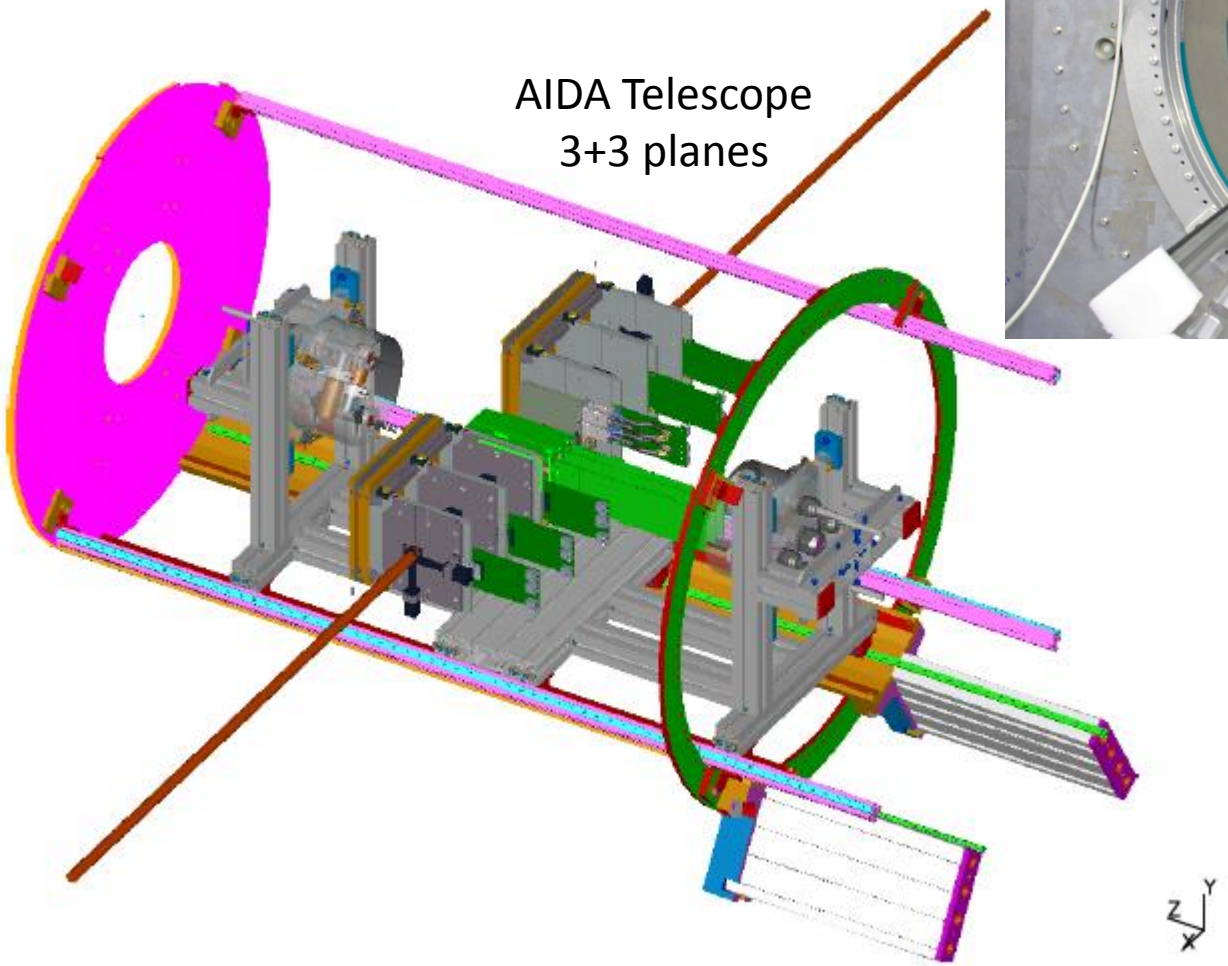


cmarinas@uni-bonn.de

Integration into the PCMAG

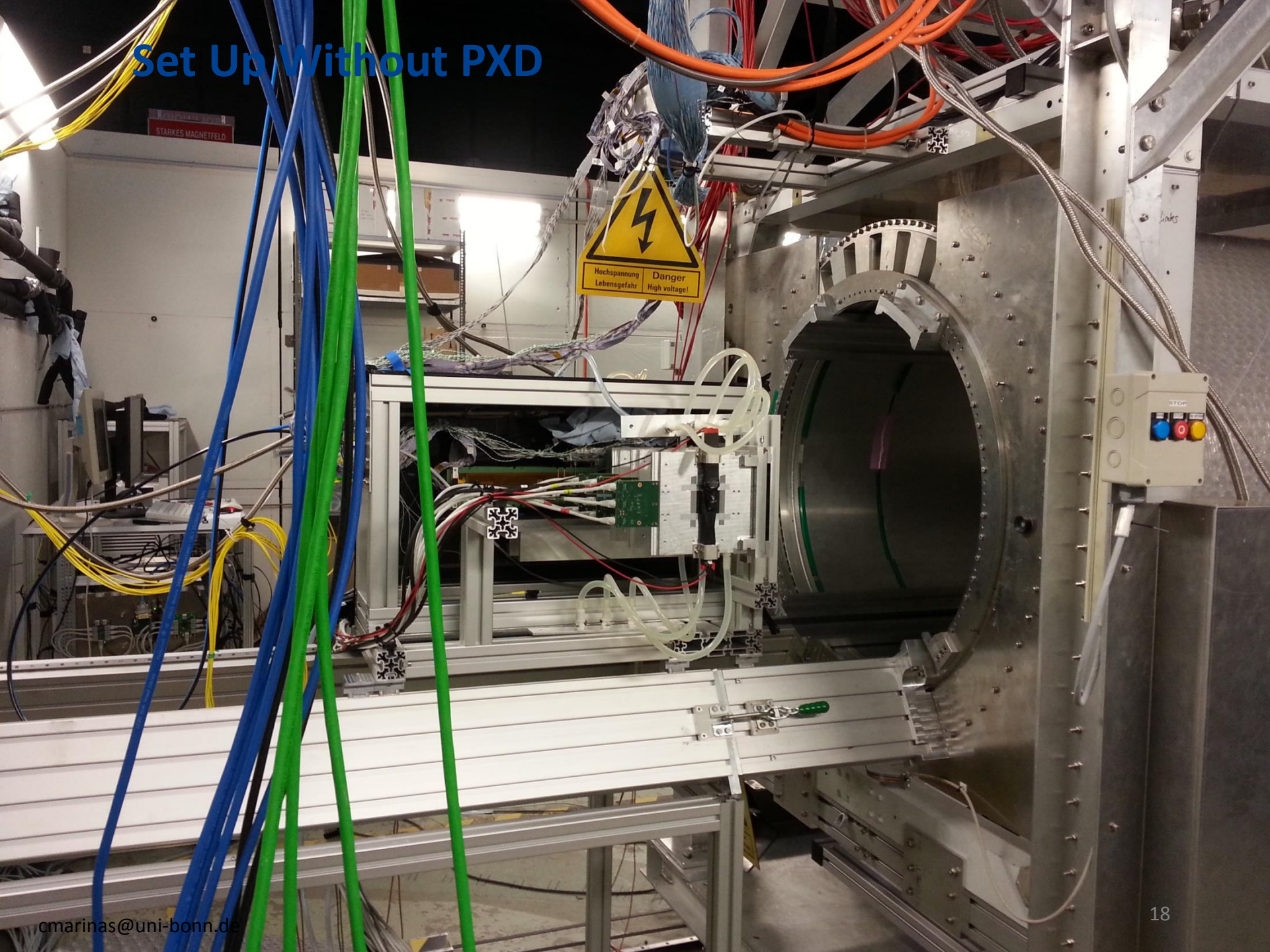


AIDA Telescope
3+3 planes

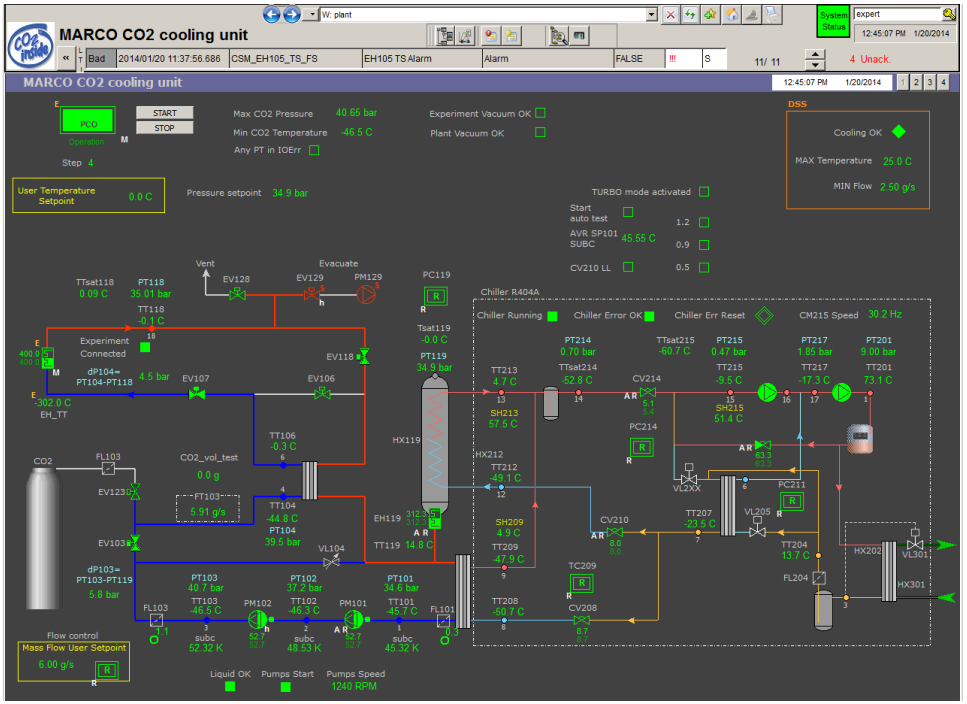


cmarinas@uni-bonn.de

Set Up Without PXD



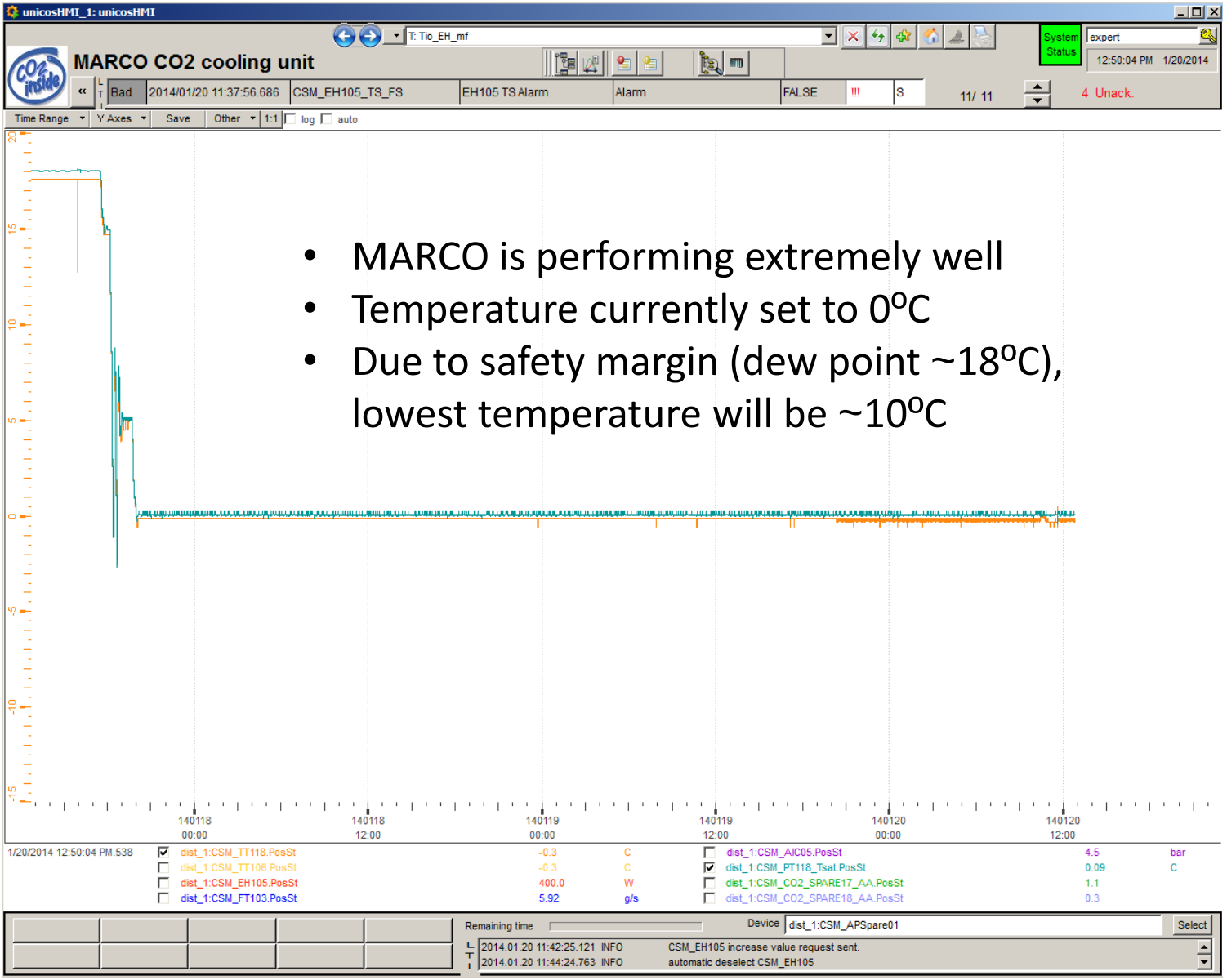
MARCO



- Connected (only) to the SVD
- Additional close loops with heaters for tuning

cmarinas@uni-bonn.de

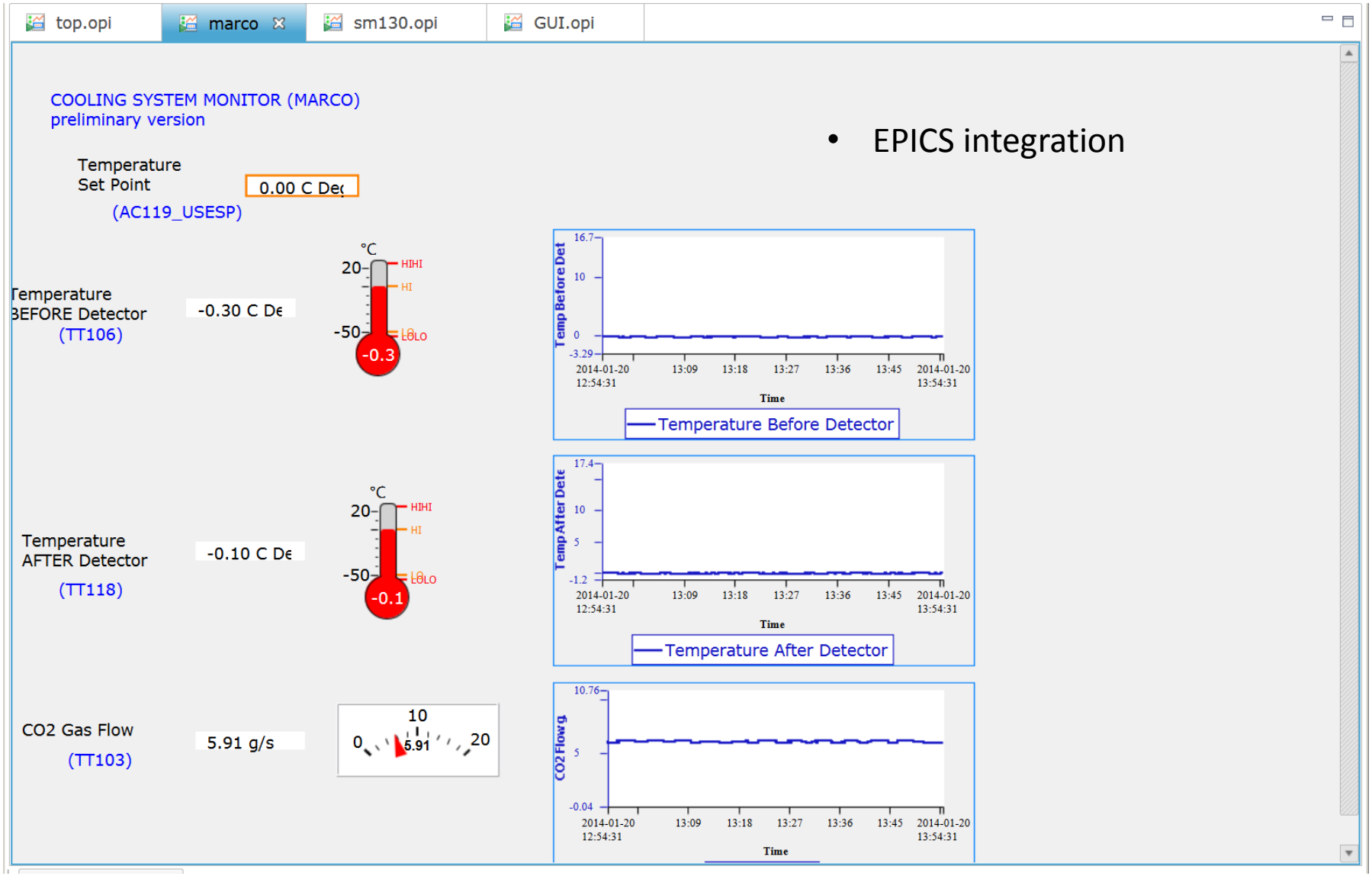
Temperature Stability



- MARCO is performing extremely well
- Temperature currently set to 0°C
- Due to safety margin (dew point ~18°C), lowest temperature will be ~10°C

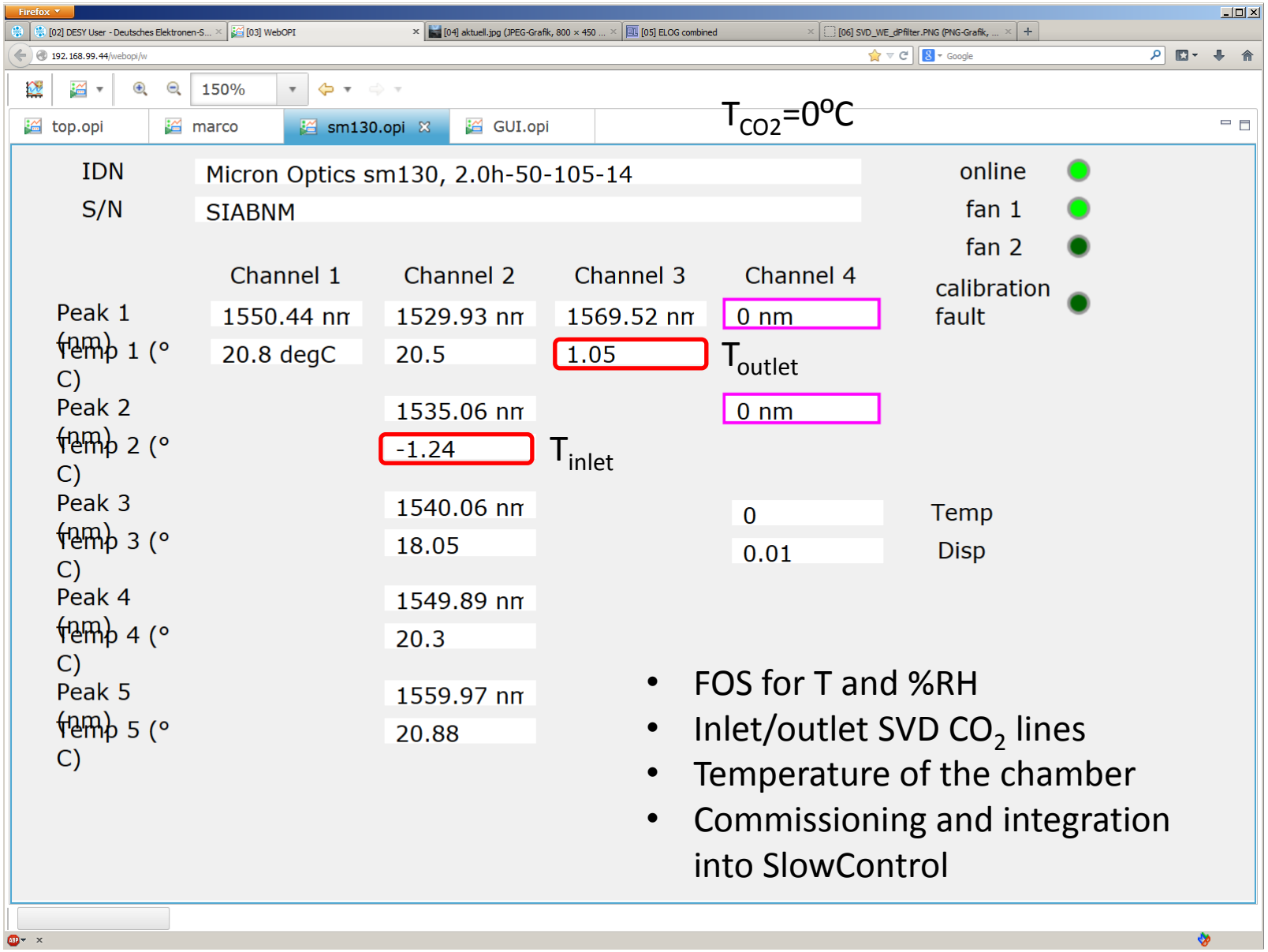
cmarinas@uni-bonn.de

MARCO Slow Control



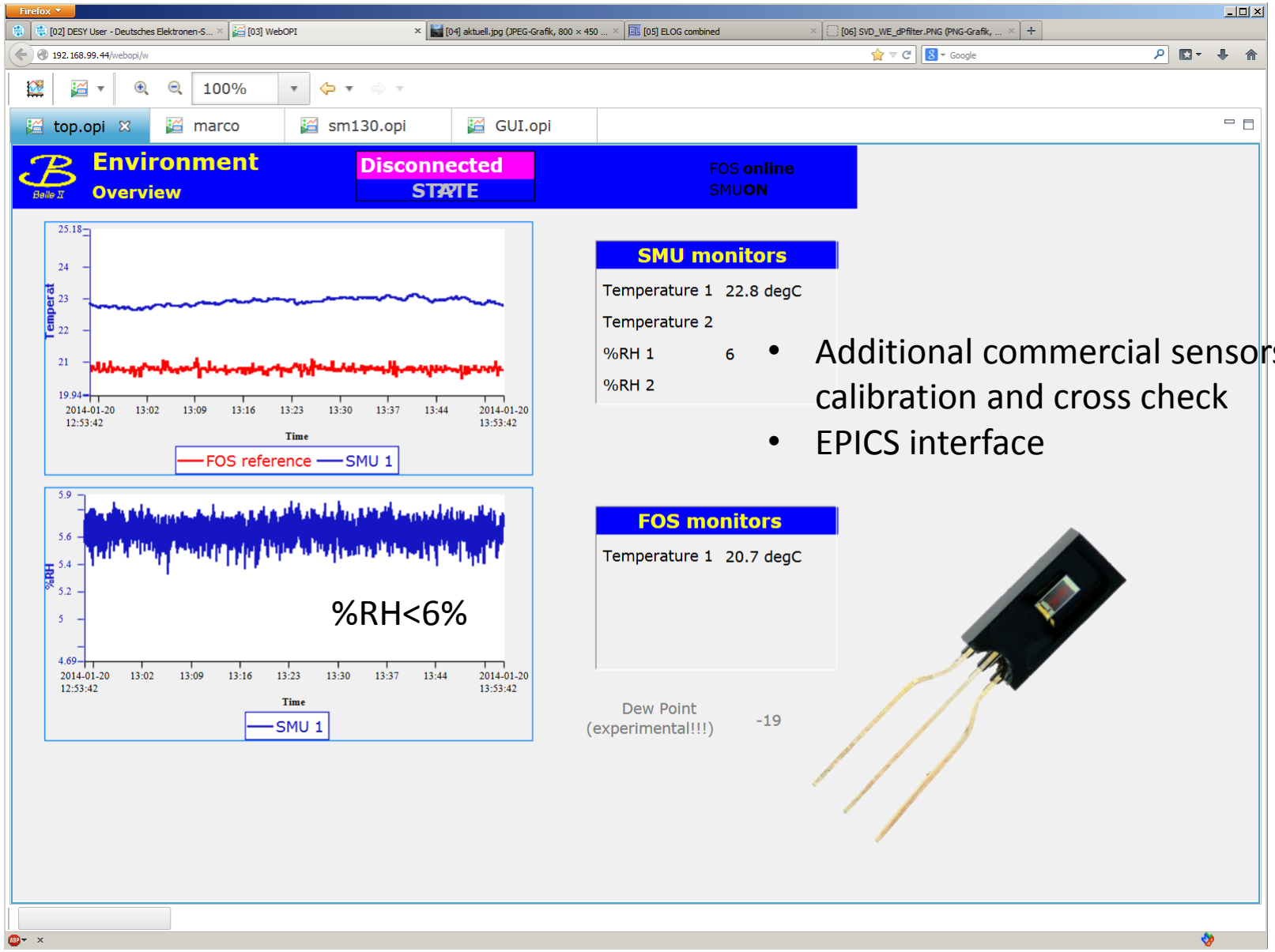
- EPICS integration

Environmental Monitors



cmarinas@uni-bonn.de

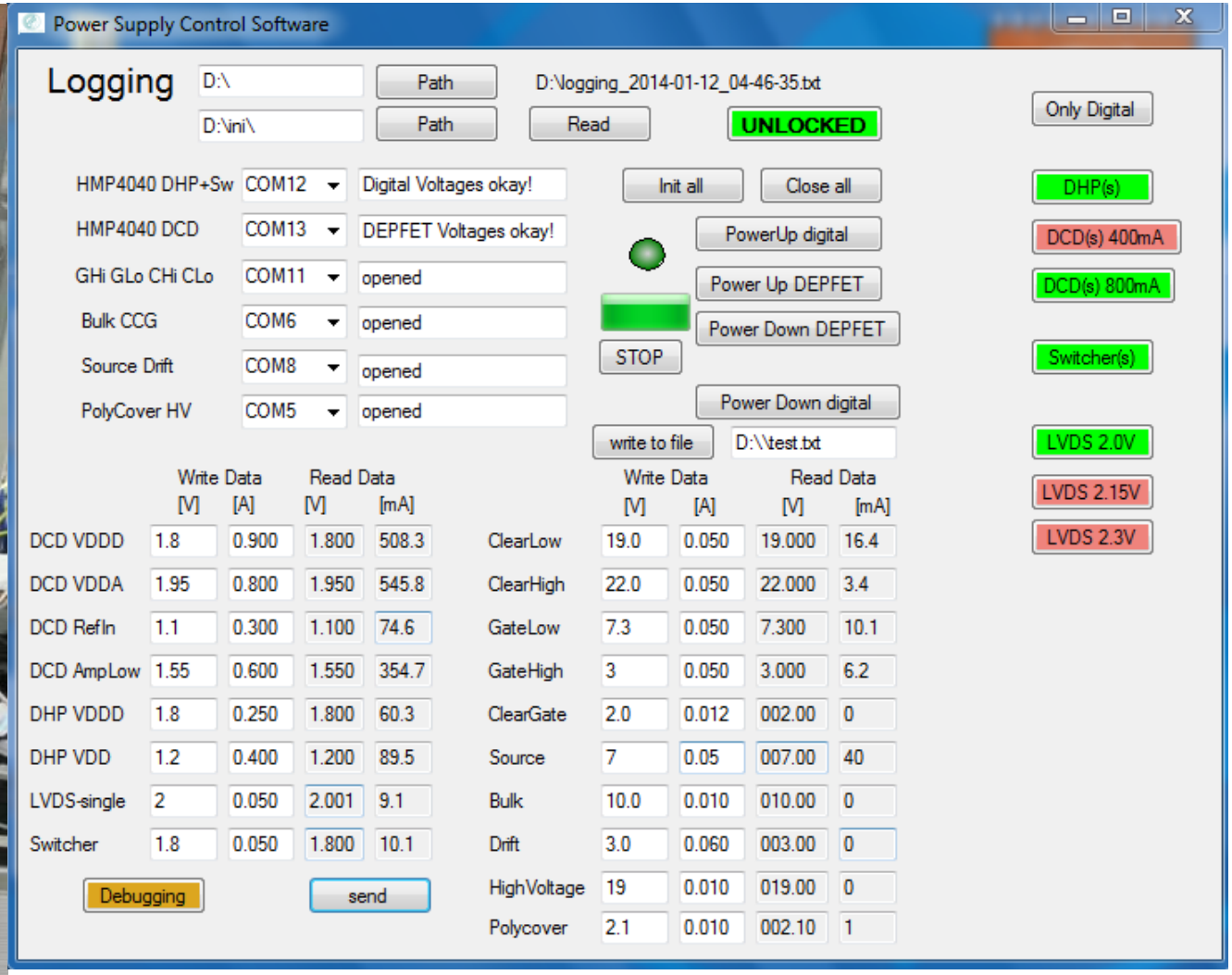
Environmental Monitors



- Additional commercial sensors for calibration and cross check
- EPICS interface

cmarinas@uni-bonn.de

Operation with Bench PS



- Specific power up/down sequences
- PS with sense lines → patch panel → 15 m cable → breakout board → Glenair → H6

cmarinas@uni-bonn.de

Belle II Power Supplies

- PS ready in TB24
- EPICS interface
- Interlock to MARCO
- Development of special power up sequence

Powersupply RUNNING $(DEVICE) Disconnect Disconnect

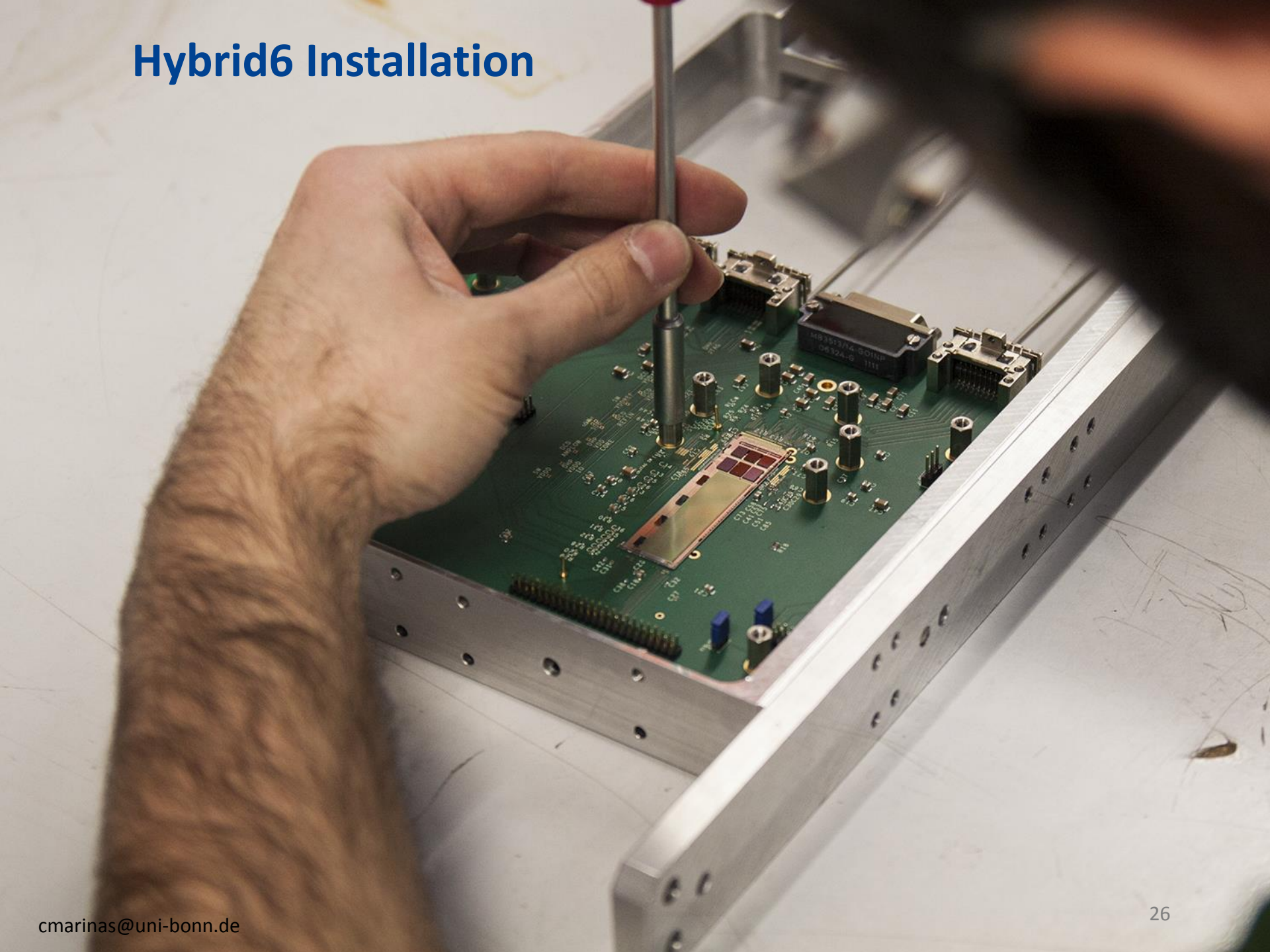
P03 Overview

ENABLED CONNECTED **RUNNING** OVP THERMAL UPS Emergency Shutdown

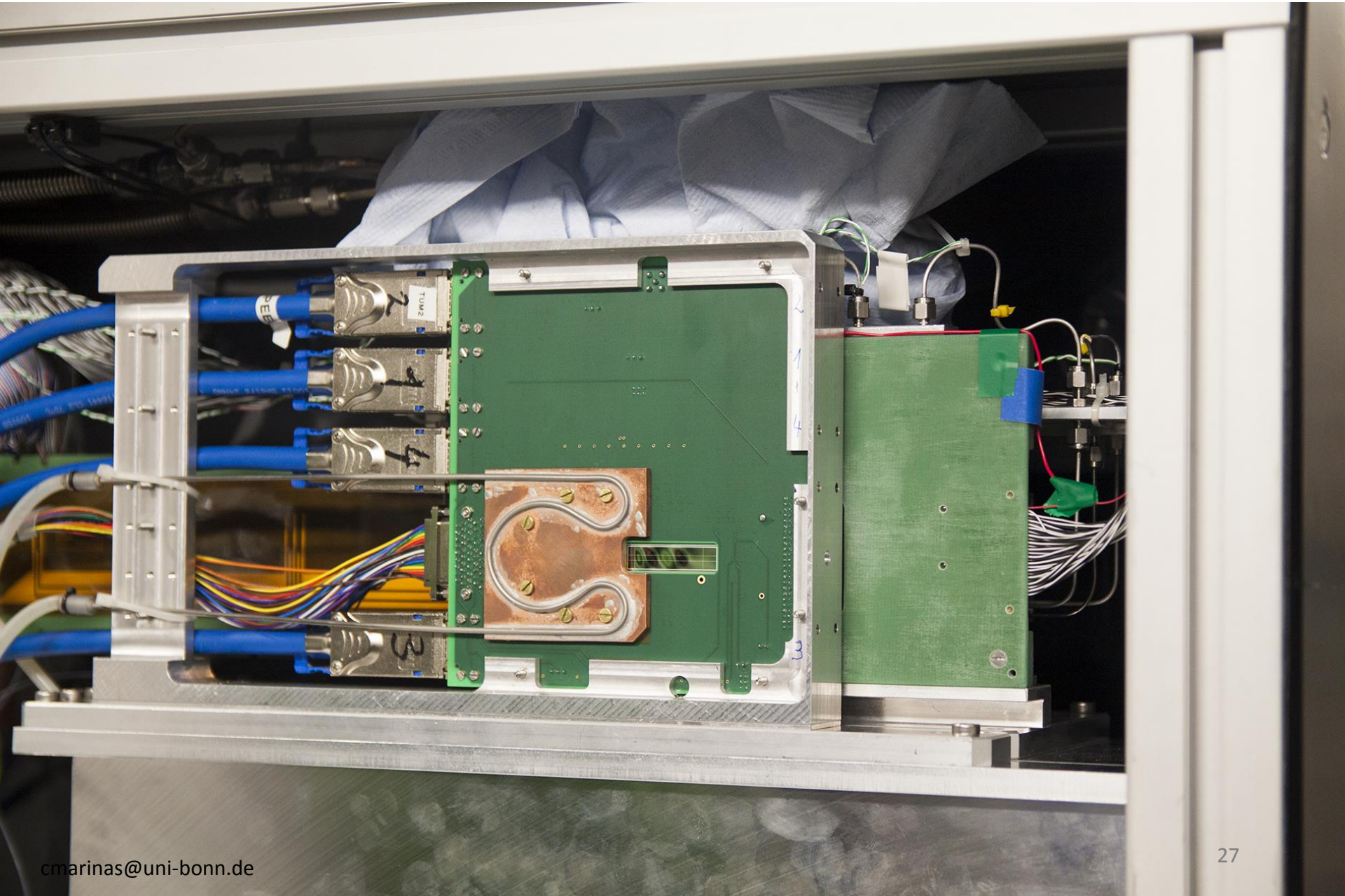
	Set Current	Set Voltage	Regulator Status	Voltage at Regulator	Voltage at Load	Current
NOT_USED_1	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_2	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_3	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_4	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_7	0 mA	0 mV	0	13 mV	6 mV	1 mA
NOT_USED_8	0 mA	0 mV	0	9 mV	12 mV	1 mA
buffer	50 mA	1800 mV	0	3 mV	0 mV	1 mA
bulk	10 mA	17000 mV	0	5 mV	7 mV	0 mA
ccg	10 mA	5000 mV	0	24 mV	-24 mV	8 mA
clear-off	30 mA	10000 mV	0	28 mV	29 mV	0 mA
clear-on	30 mA	29000 mV	0	27615 mV	-7559 mV	-3 mA
dcd-amplow	600 mA	350 mV	0	270 mV	-89 mV	0 mA
dcd-avdd	900 mA	1900 mV	0	406 mV	0 mV	7 mA
dcd-dvdd	800 mA	1800 mV	0	-5 mV	-3 mV	-1 mA
dcd-refin	400 mA	1100 mV	0	363 mV	-2 mV	8 mA
dhp-core	400 mA	1200 mV	0	-1 mV	9 mV	5 mA
dhp-io	400 mA	1800 mV	0	2 mV	6 mV	2 mA
drift	10 mA	4000 mV	0	0 mV	22 mV	0 mA
gate-off	30 mA	10000 mV	0	5 mV	6 mV	-1 mA
gate-on	30 mA	4000 mV	0	17 mV	13 mV	0 mA
hv	10 mA	-12000 mV	0	-34 mV	-13 mV	0 mA
polycover	10 mA	4900 mV	0	13 mV	8 mV	0 mA
source	50 mA	7000 mV	0	7366 mV	7000 mV	-1 mA
sw-dvdd	50 mA	1800 mV	0	51 mV	8 mV	3 mA

cmarinas@uni-bonn.de

Hybrid6 Installation

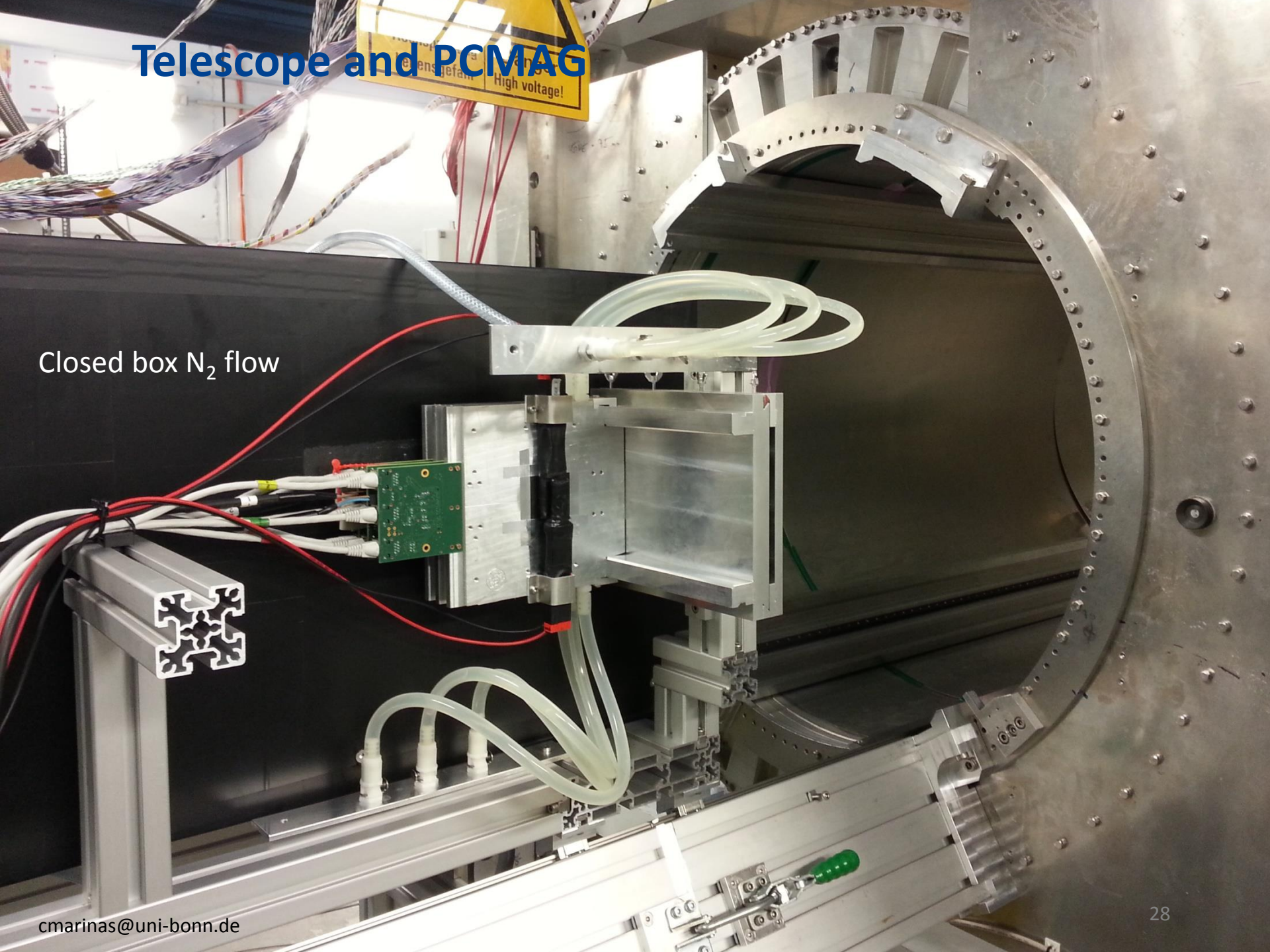


L1 Final Position



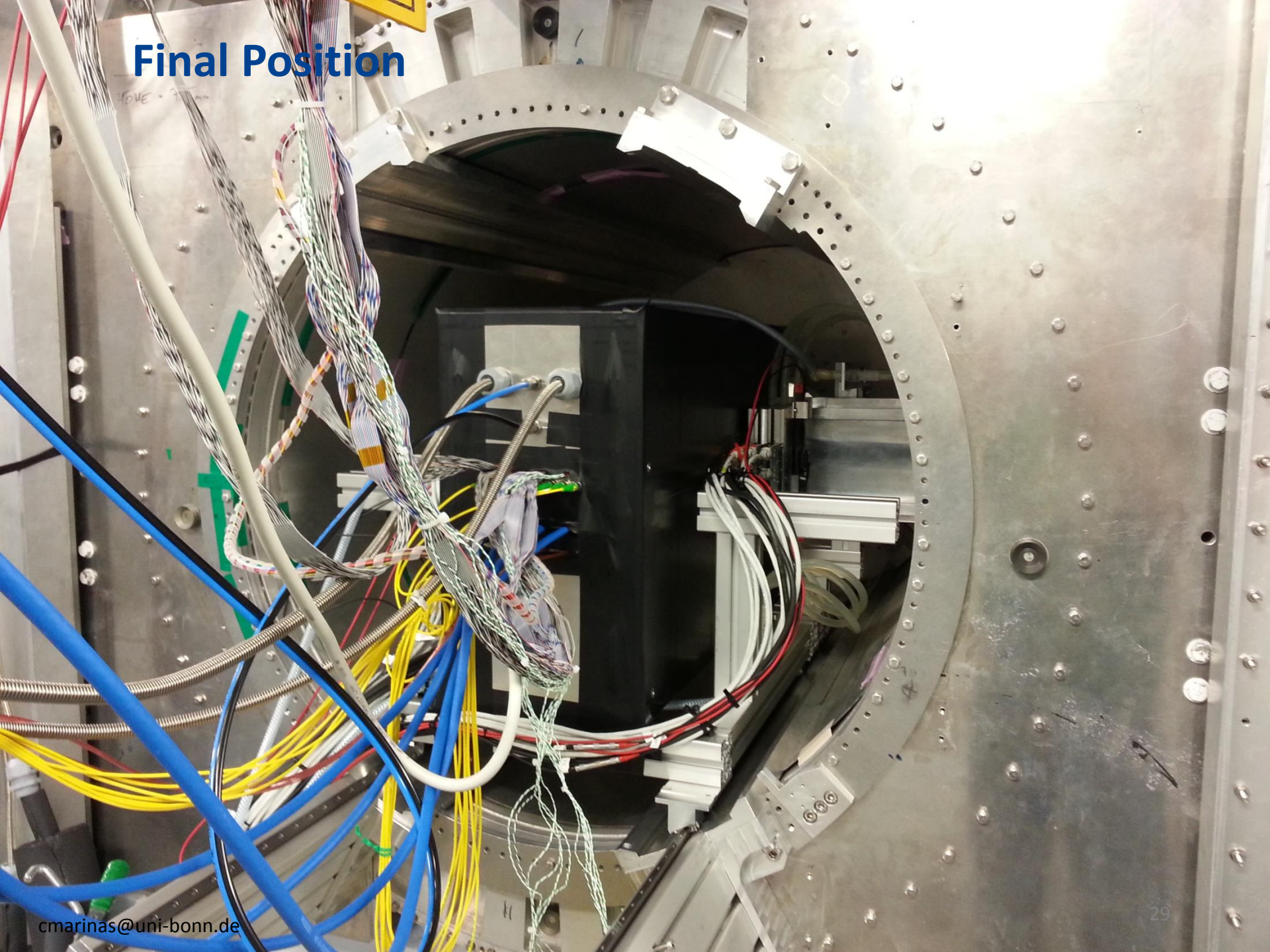
cmarinas@uni-bonn.de

Telescope and PCMAG

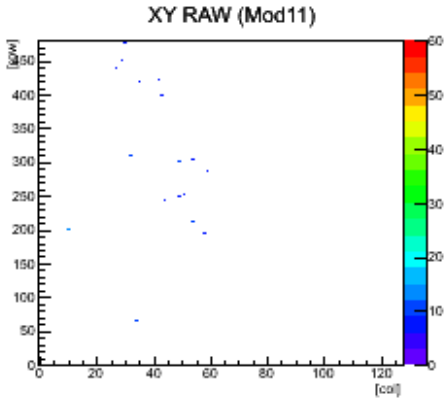


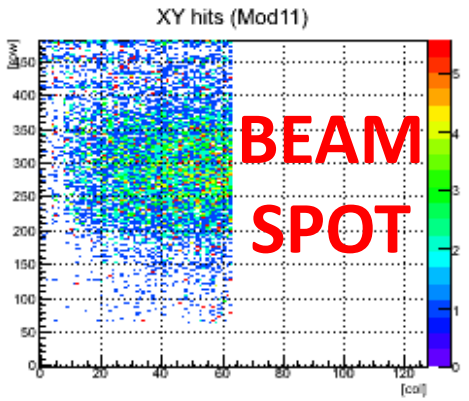
Closed box N_2 flow

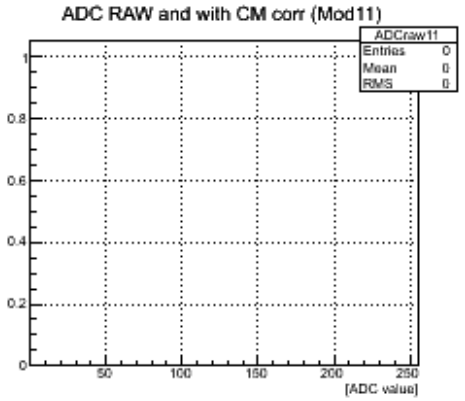
Final Position

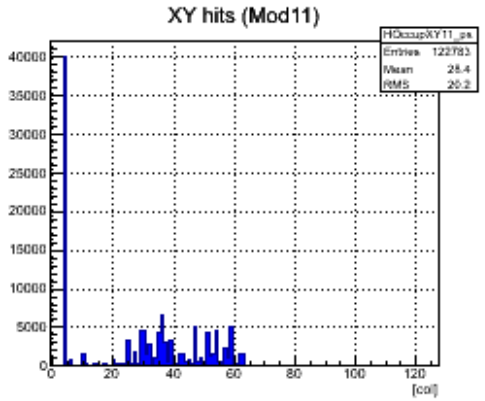


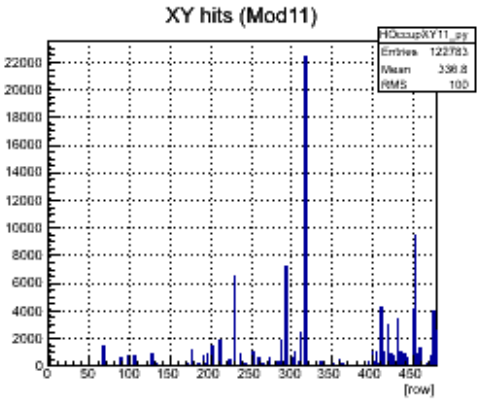
DAQ via BonnDAQ

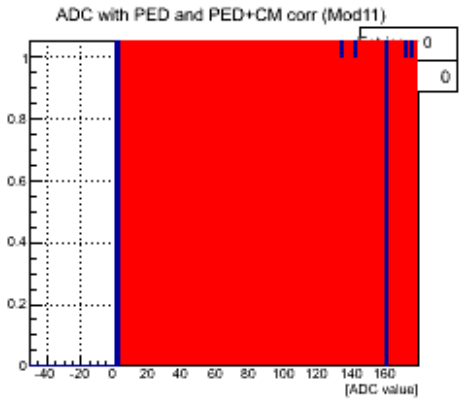


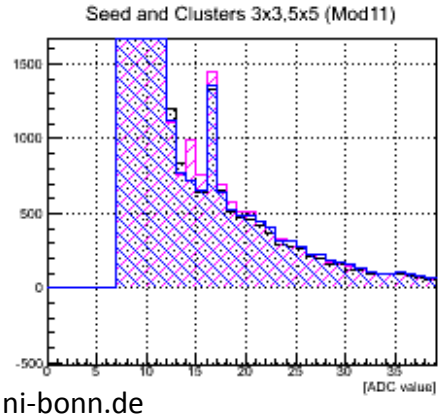


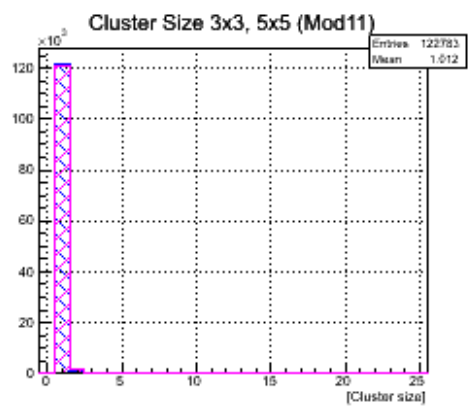


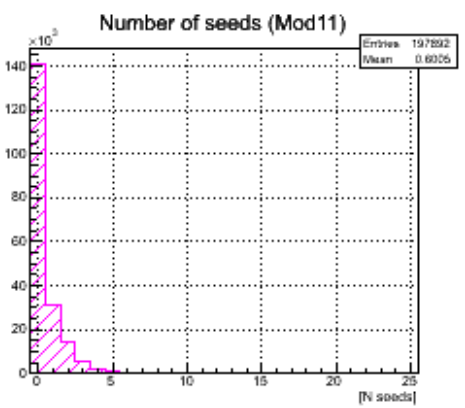






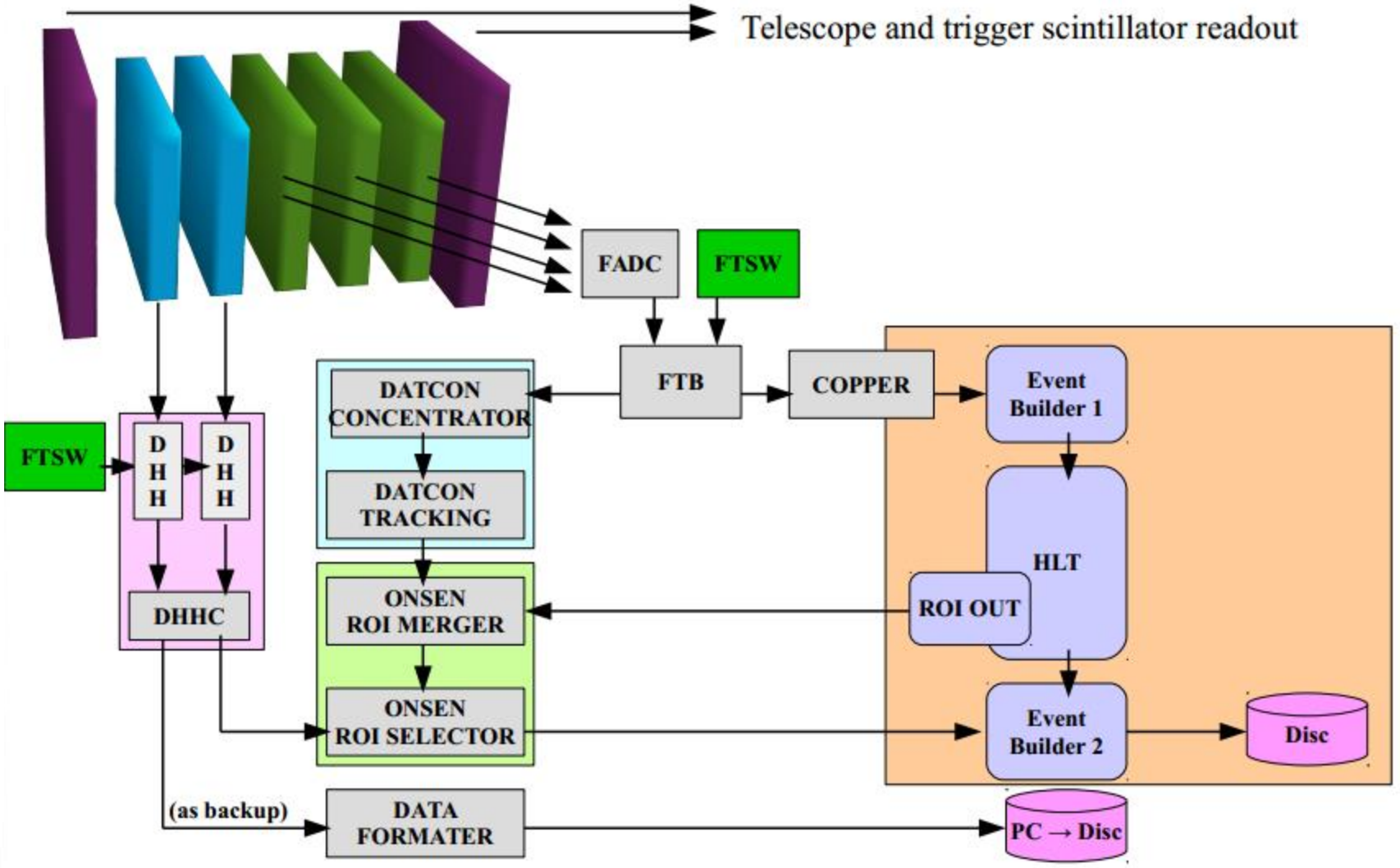






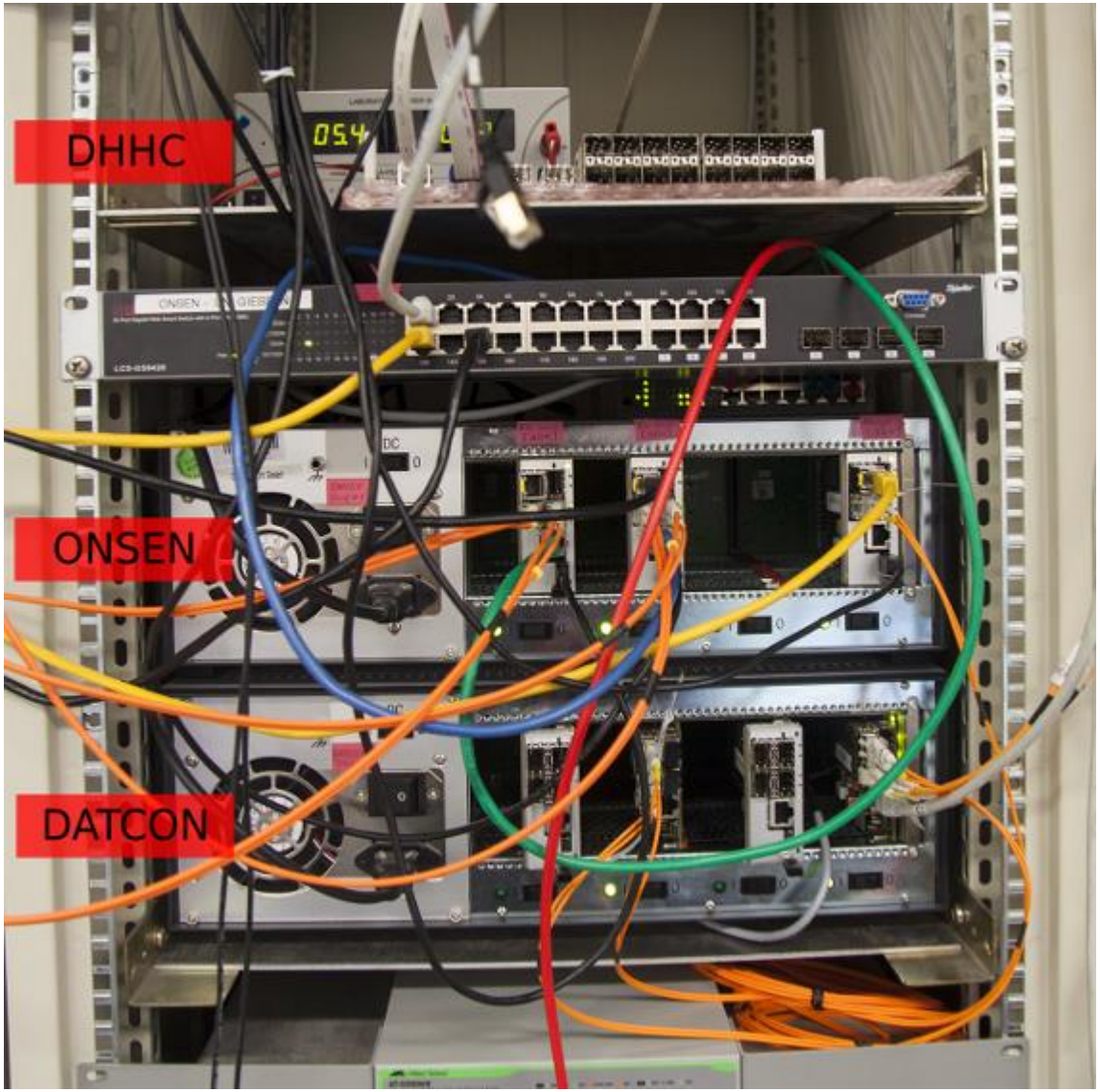
cmarinas@uni-bonn.de

Test Beam VXD DAQ Estructure



cmarinas@uni-bonn.de

PXD DAQ



DATCON

- Two AMC rev. 2:
  - Concentrator for receiving SVD data from FTB and preprocessing
  - Tracking for track extrapolation, ROI creation and transmitter to ONSEN

- Link between FTB and DATCON stable
- Proper decoding of zero-suppressed SVD data
- Correct coordinate translation
- Event and data management works
- Track extrapolation and ROI creation, functional

- Hough transformation and ROI management still not fully verified

cmarinas@uni-bonn.de

DHH and DHHC

- DESY test beam configuration : full readout chain
  - PXD matrix → 1(2)xDHH → DHHC → ONSEN
- DHH
  - Up to 4 x (DHP+DCD) + Switchers
  - Full EPICS control via IPBUS
  - Triggers+127MHz clock from DHHC via optical link
  - UDP for pedestal (full frame readout) and Bonn DAQ || PocketDAQ
- DHHC
  - FTSW interface
  - Interface to ONSEN @ 3.125 Gbps with backpressure flow control
  - Full EPICS control via IPBUS
  - Current firmware supports 2 DHH modules i.e. 2 detectors

→ System tested with the PXD6 detector @ 1kHz random trigger rate and 200 µs dead time. (Additional tests at higher rate ongoing)

cmarinas@uni-bonn.de

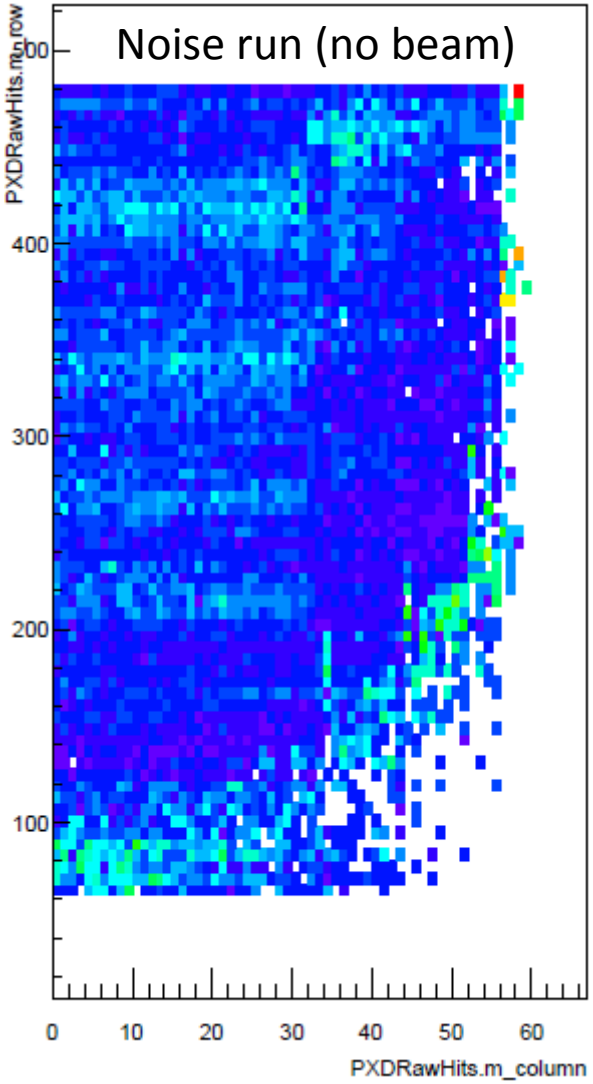
ONSEN

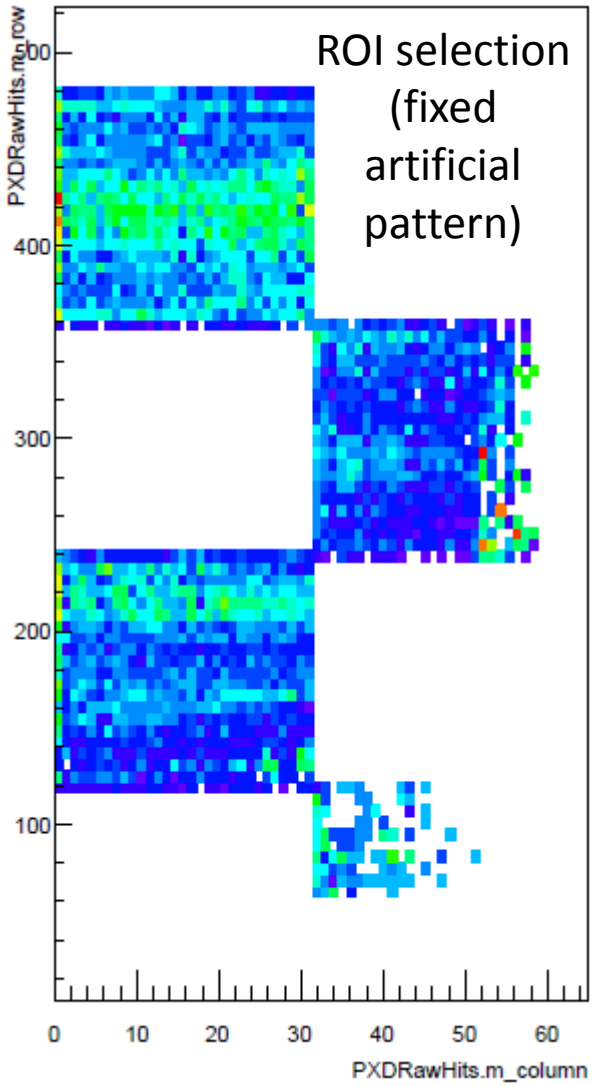
- "Pocket ONSEN" debugging system with four Compute Node cards is used.
  Running stably after initial troubles with most current firmware.

- First real data (with dummy ROIs) processed and written to EVB on Monday.

- Full DAQ chain is established: DEPFET → DHP → DHH → DHHC → ONSEN (← HLT) → EVB

Full Data Path with ROI Selection





cmarinas@uni-bonn.de

Conclusions

Although fine tuning is necessary, the test beam is already a **big success**!

All the PXD hardware, software and firmware is ready to declare run conditions

Decisive step forward towards the Belle II PXD

cmarinas@uni-bonn.de

Congratulations for the hard work!

cmarinas@uni-bonn.de

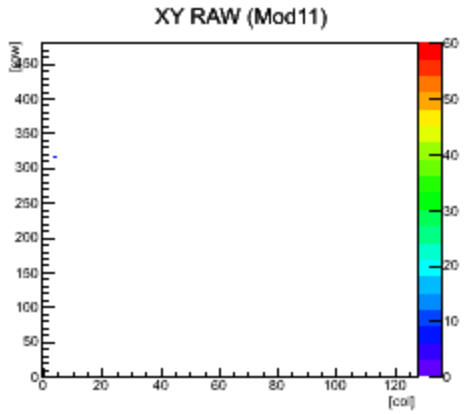
universitätbonn

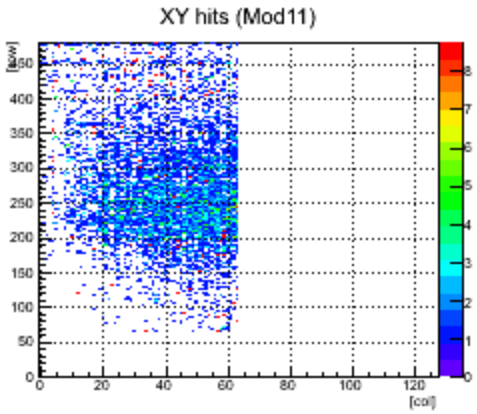
Thank you

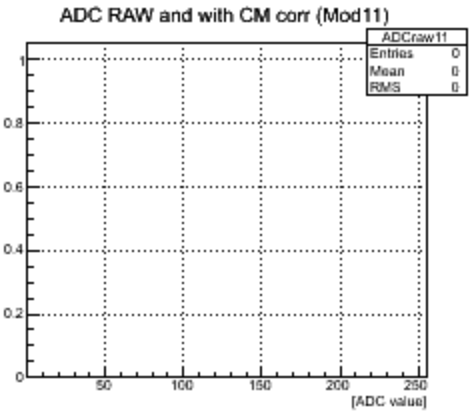
cmarinas@uni-bonn.de

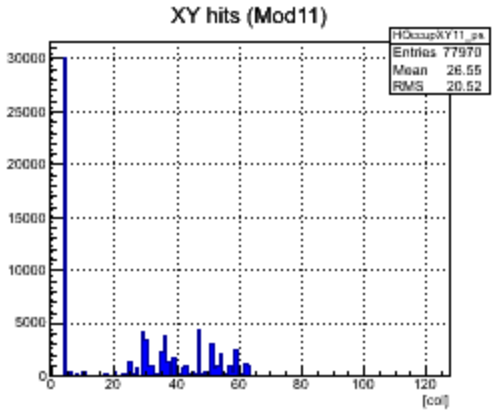
SILAB DQM

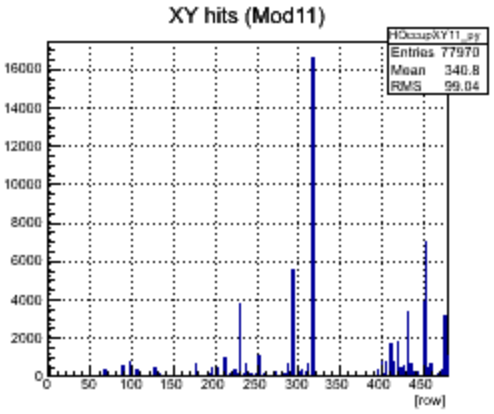
Trigg | Mod11 | Ped11

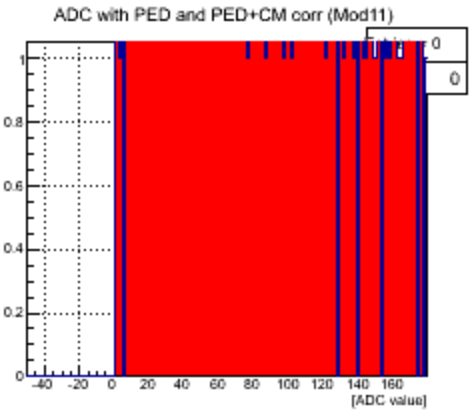


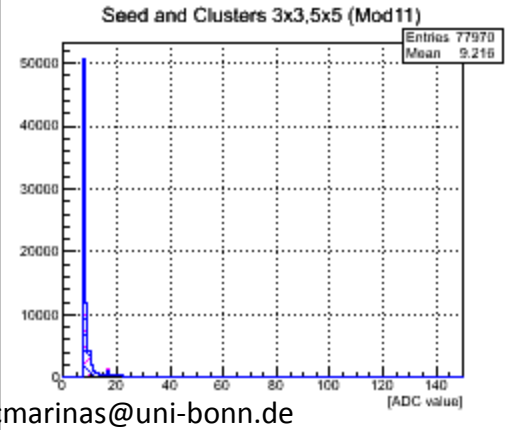


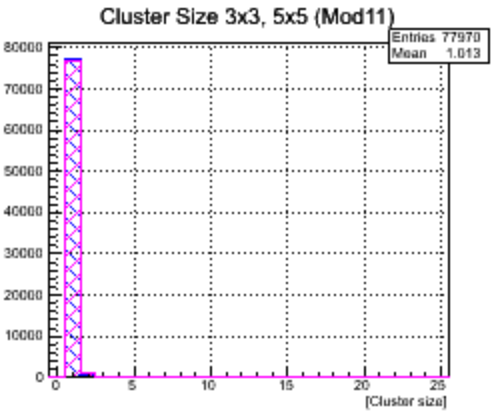


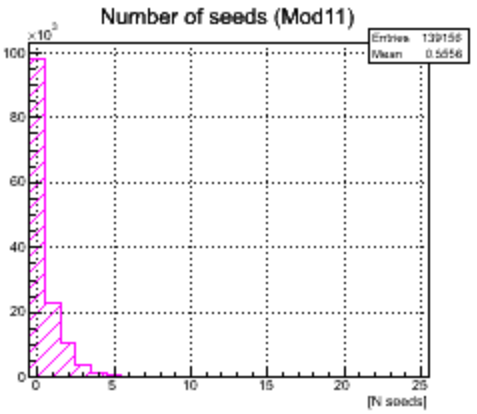












Run: 1007

Ped: -1

Ev: 67476

LU P 0.0 [Hz]

LU T 0.0 [Hz]

Seed[11]: 0.56

Temp= 0.00

Reset

Save

Correlation

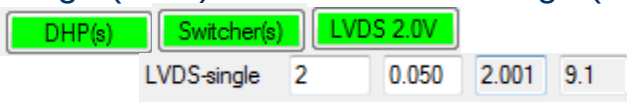
Resume

Exit

cmarinas@uni-bonn.de

Powering during Testbeam

Power Up sequence:

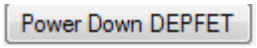
1. Apply DHP (IO 1.8V and Core 1.2V) & Switcher voltage (1.8V) and converter voltage (around 2.0V in order to switch it on => decrease to 1.8V) 

2. Configure DHPs (switch off clock for DCDs)
3. Apply DCD voltages (VDDD, VDDA, RefIn, Amplow, current limits at 400mA) 

4. Configure DCDs, switch off analog part of the DCDs
5. Increase the current limits (VDDD 800mA, VDDA 900mA, Amplow 600mA) 

6. Switch on DHP clocks and analog part of the DCDs
7. Switch on the DEPFET (in the normal sequence) [Bulk, Clearhigh, Clearlow, GateHi, Gatelow=0V, Source, Cleargate, Gatelow, Highvoltage/Backplane, Drift, Polycover) 

Power Down sequence:

1. Switch off DEPFET 

2. Switch off ASICs