PXD DAQ General Issues

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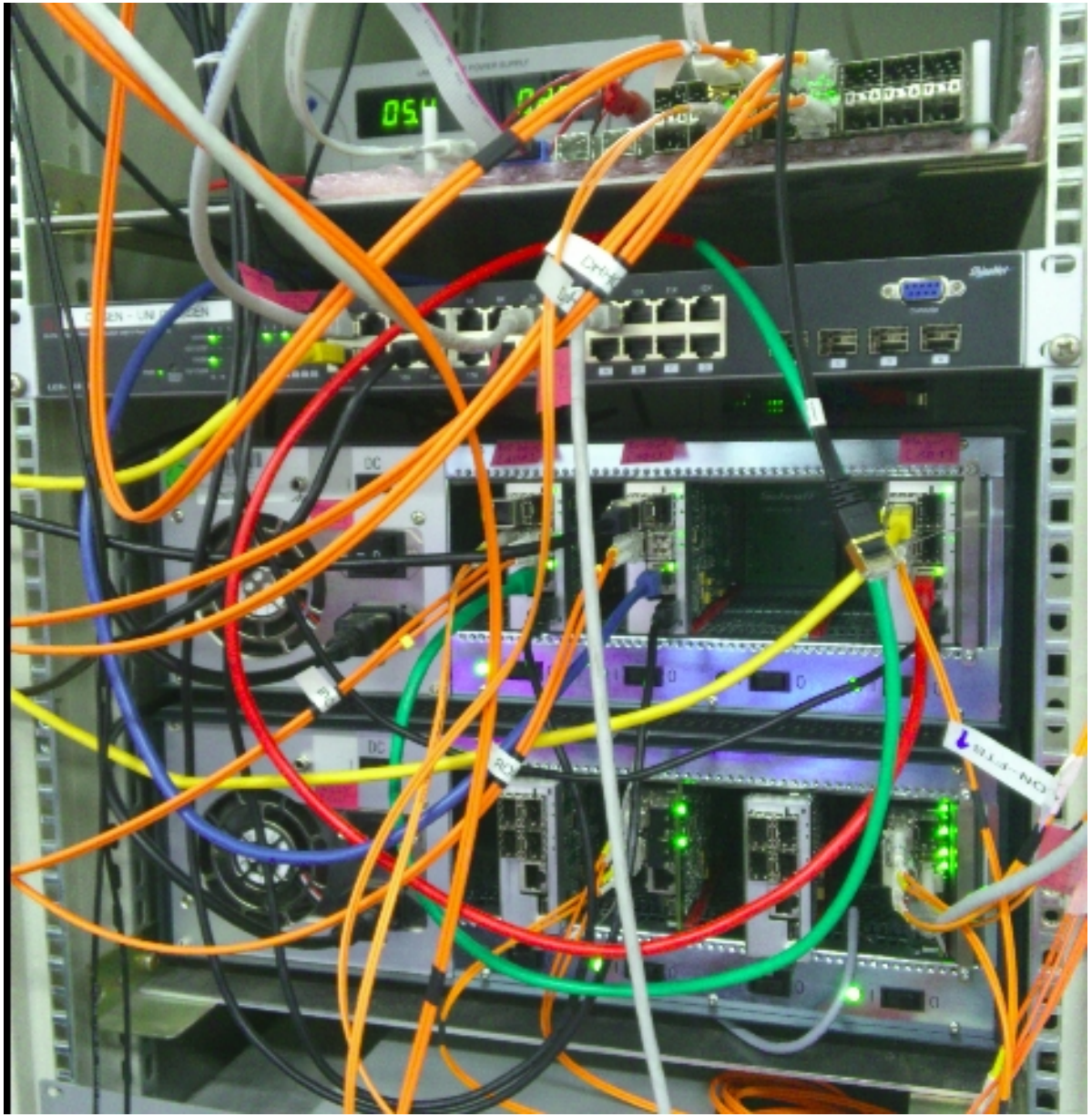
Belle II

Bundesministerium
für Bildung
und Forschung

Status of Onsen and DATCON Hardware

DESY Testbeam Setup Jan14



DHH

uTCA Systems
AMC cards

ONSEN

DATCON

8 new AMC cards (compute node v3) arrived at Giessen from IHEP on Monday 02.12.2013

new cards are being used for DESY test

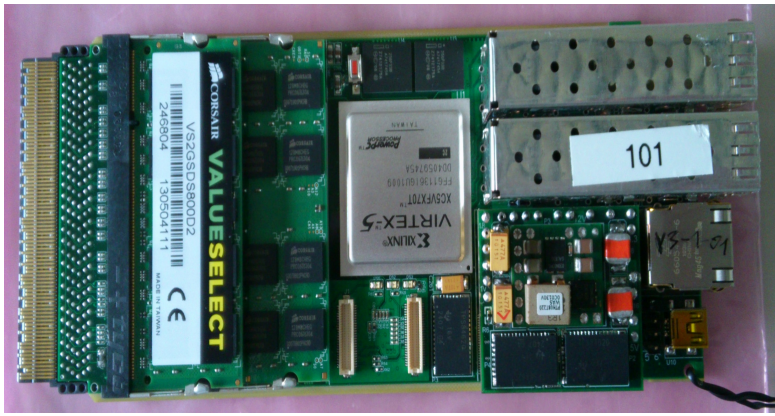
	1	2	3	4	5	6	7	8
Seriell	✓	✓	✓	✓	✓	✓	✓	✓
RAM1	✓	X	✓	✓	✓	✓	✓	✓
RAM2	✓	X	✓	✓	✓	✓	✓	✓
PPC	✓	✓	✓	✓	✓	✓	✓	✓
FLASH	✓	✓	✓	X	X	✓	✓	✓
PROM	✓	✓	✓	✓	✓	✓	✓	✓
OPT 1 (3.125 Gb/s)	-	-	-	-	-	-	✓	✓
OPT 2 (3.125 Gb/s)	✓	✓	✓	✓	✓	✓	✓	✓
OPT 3 (3.125 Gb/s)	-	-	-	-	-	-	✓	✓
OPT 4 (3.125 Gb/s)	✓	✓	✓	✓	✓	✓	✓	✓
Ethernet	✓	✓	✓	✓	✓	✓	✓	✓
Backplane (3.125Gb/s)	✓	✓	✓	✓	✓	✓	✓	✓
Linux (on PPC)	✓	✓	✓	✓	✓	✓	✓	✓

Tests, mostly done by Björn Spruck

Number of available Onsen AMC cards

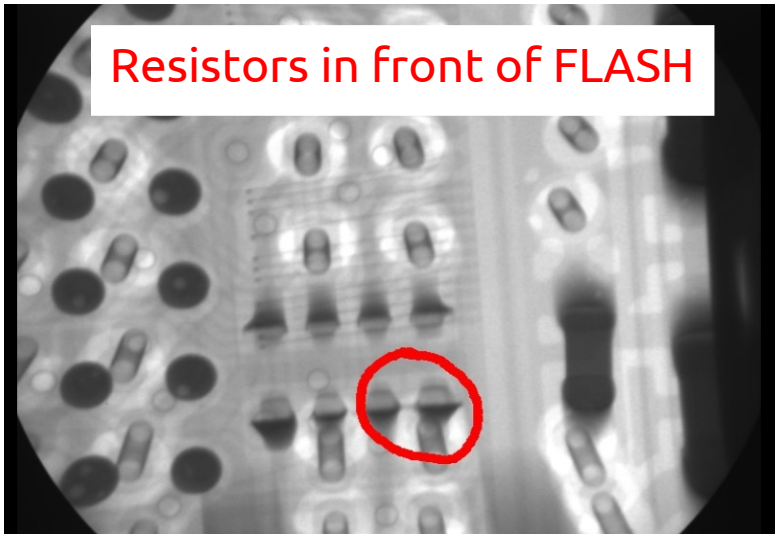
5 new boards are o.k.
2 have problems with FLASH,
1 has problem with RAM

investigation by microscope/ xray
→ shorts detected
but after re-soldering,
problems still persist



we have in total
5 + 3 working AMC v3
2 working AMC v2
(DESY DATCON, in operation)

final ONSEN system: 32 cards
→ what we have, is 25% of the final system
(but some cards are for Panda)



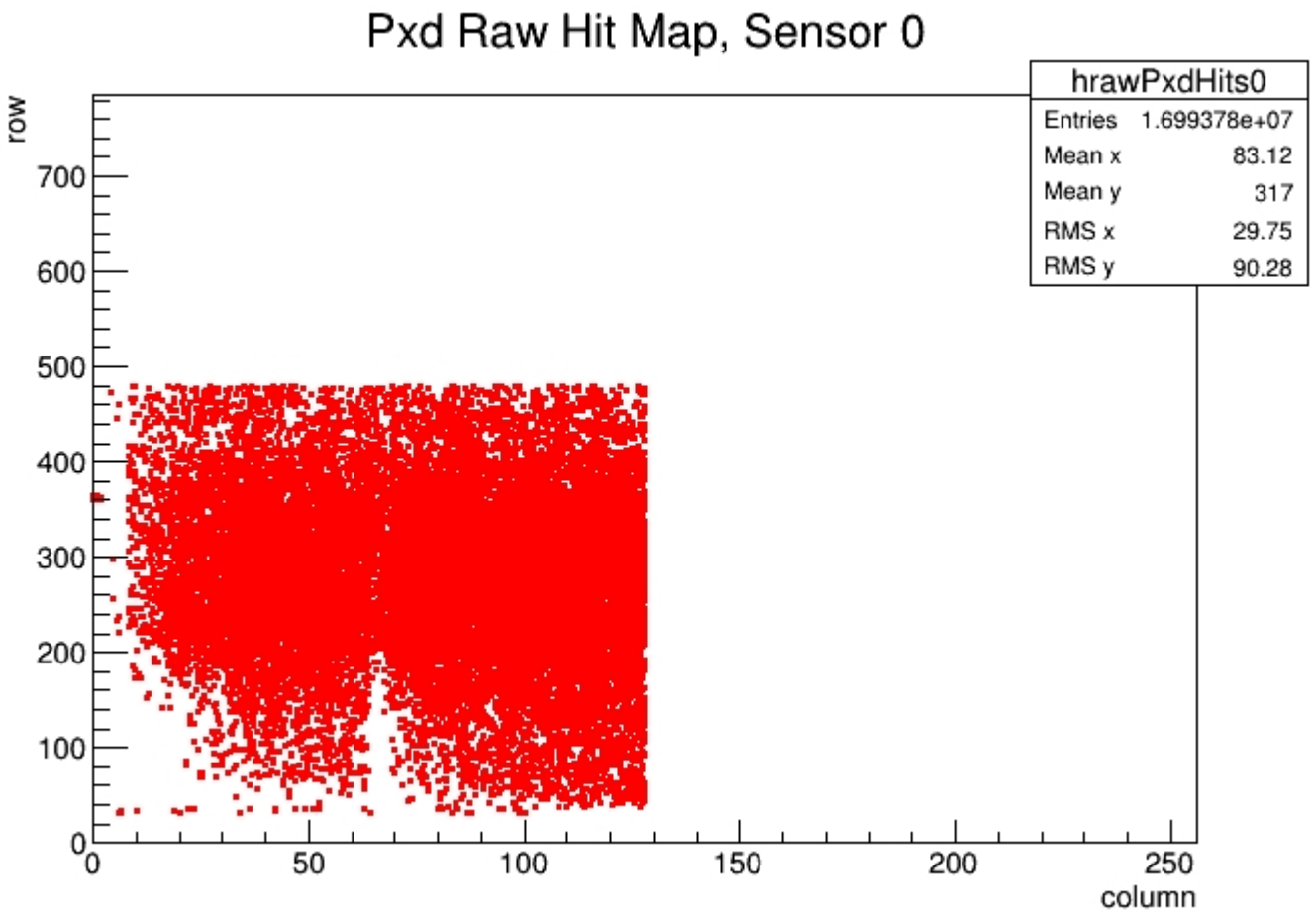
New hardware ordered, waiting for delivery

- 12-16 compute nodes (40.000,-)
- 32 transceivers optical 6 Gbps (3100,-)
- 32 transceivers optical/RJ45 (2360,-)
- 1 ATCA switch + CPU for in-shelf JTAG
- 3 uTCA shelfs

→ 3 Pocket-ONSEN Systems
1 for KEK
1 for DESY
(n.b. Belle II PocketDAQ w/ HLT and EVB will also stay at DESY)
1 for Giessen (mirror system, for parallel debugging)

DESY Testbeam

Lessons learned for PXD DAQ



run #443, THU Jan 23, 18:00-19:00
3 GeV, no field, Cu, 4mm collimator
SVD and PXD, with pedestals, ~1.5 Million events
no trigger ID mismatch

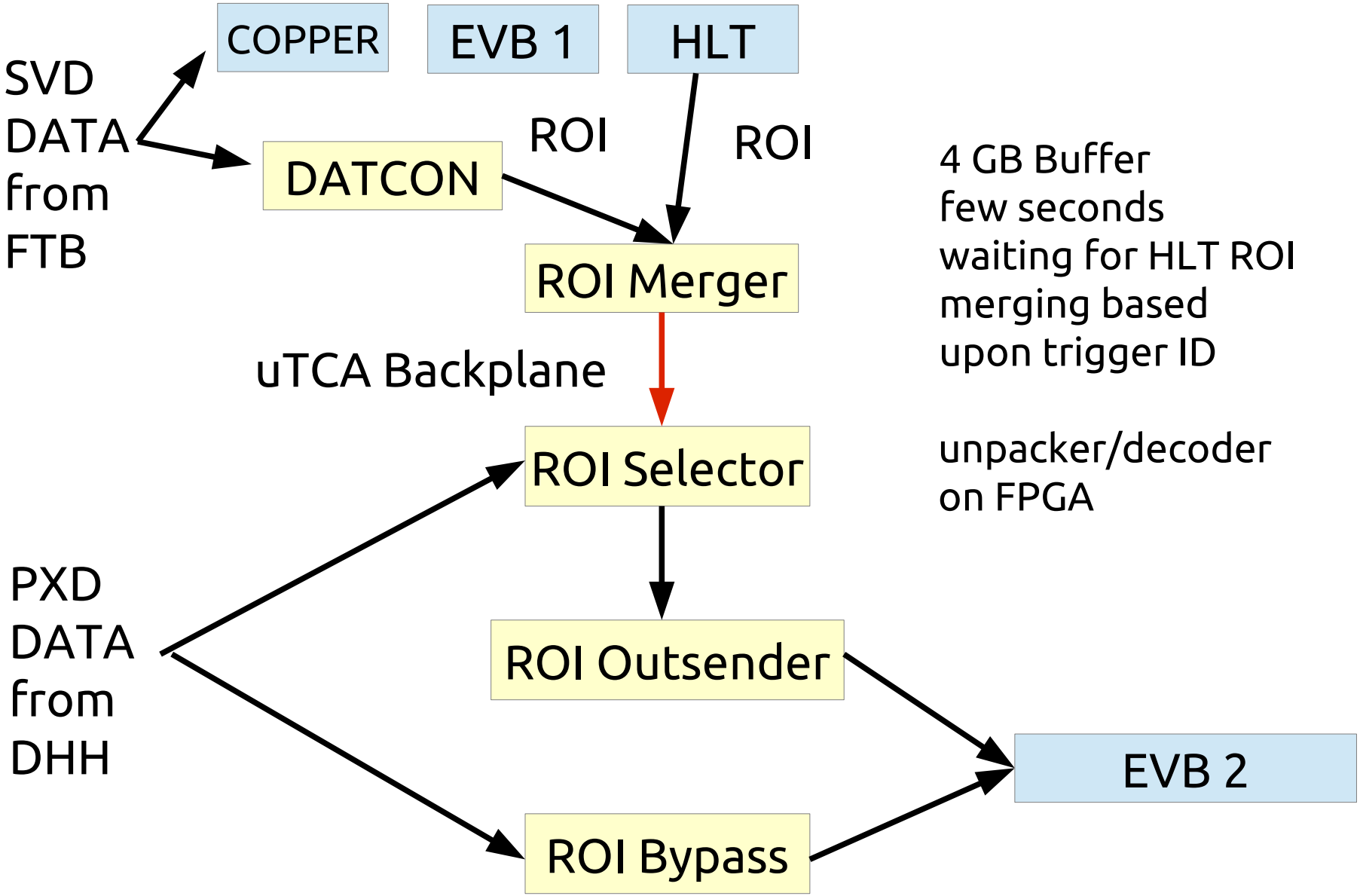
Testbeam DAQ integration, lessons learned

- work on interfaces between the subsystems needed
  („flush remaining HLT triggers at end of run“)
  → need more tests in this year

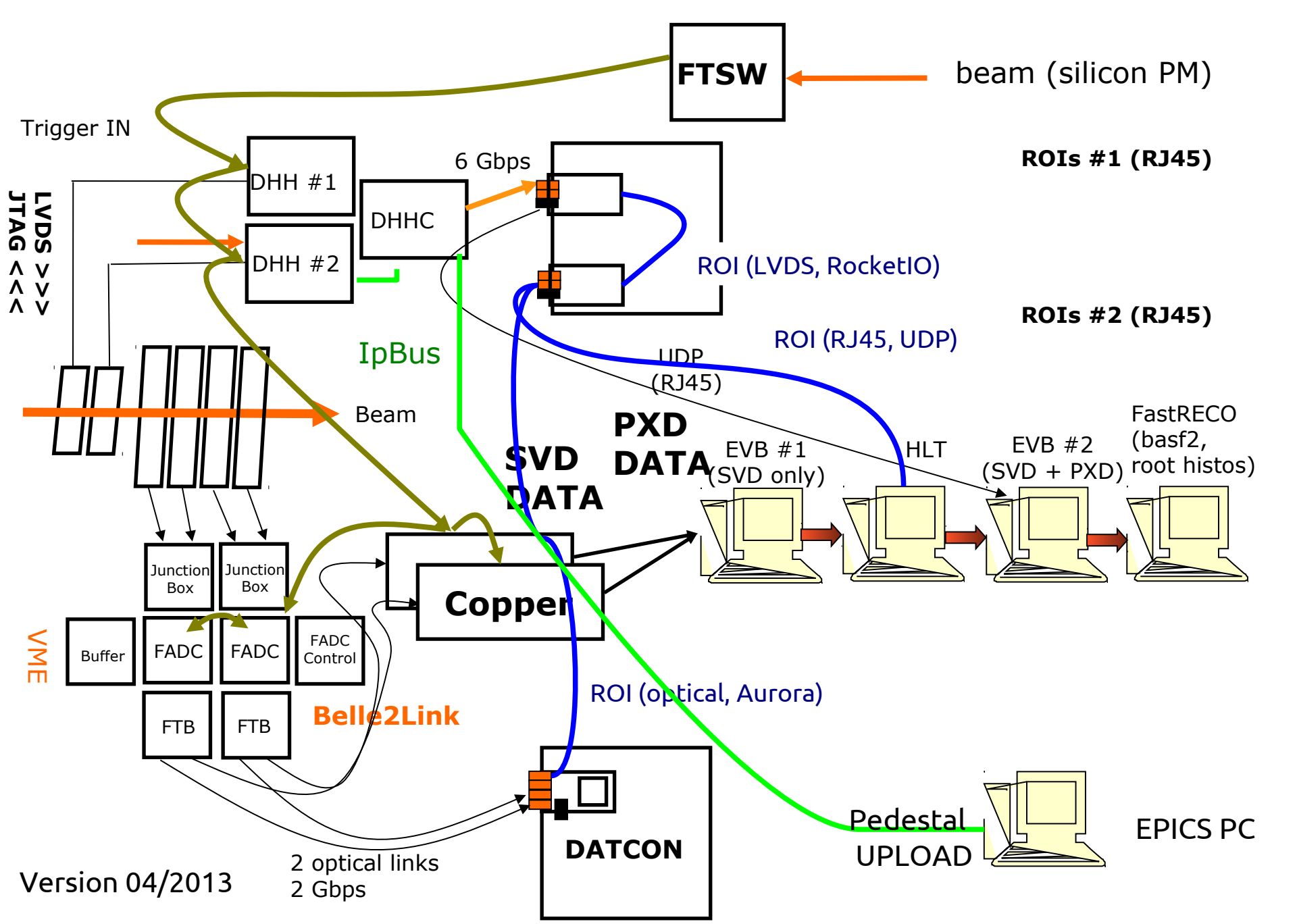
- basf2
  probability, that compile works after „svn update“
  is <50%
  → we need a stable branch

- DHP configure and pedestal upload
  ~45 min per 1 half-module, 3-4 x per day
  procedure of >50 steps by Florian

BACKUP



beige: FPGA compute nodes, blue: PCs


FTSW
beam (silicon PM)
Trigger IN
DHH #1
DHH #2
DHHC
6 Gbps
ROIs #1 (RJ45)
ROI (LVDS, RocketIO)
ROIs #2 (RJ45)
ROI (RJ45, UDP)
LVDS >>>
JTAG <<<
IpBus
UDP
(RJ45)
Beam
PXD
DATA
SVD
DATA
EVB #1
(SVD only)
HLT
EVB #2
(SVD + PXD)
FastRECO
(basf2,
root histos)
Junction
Box
Junction
Box
Copper
VME
Buffer
FADC
FADC
FADC
Control
FTB
FTB
Belle2Link
ROI (optical, Aurora)
DATCON
Pedestal
UPLOAD
EPICS PC
2 optical links
2 Gbps
Version 04/2013