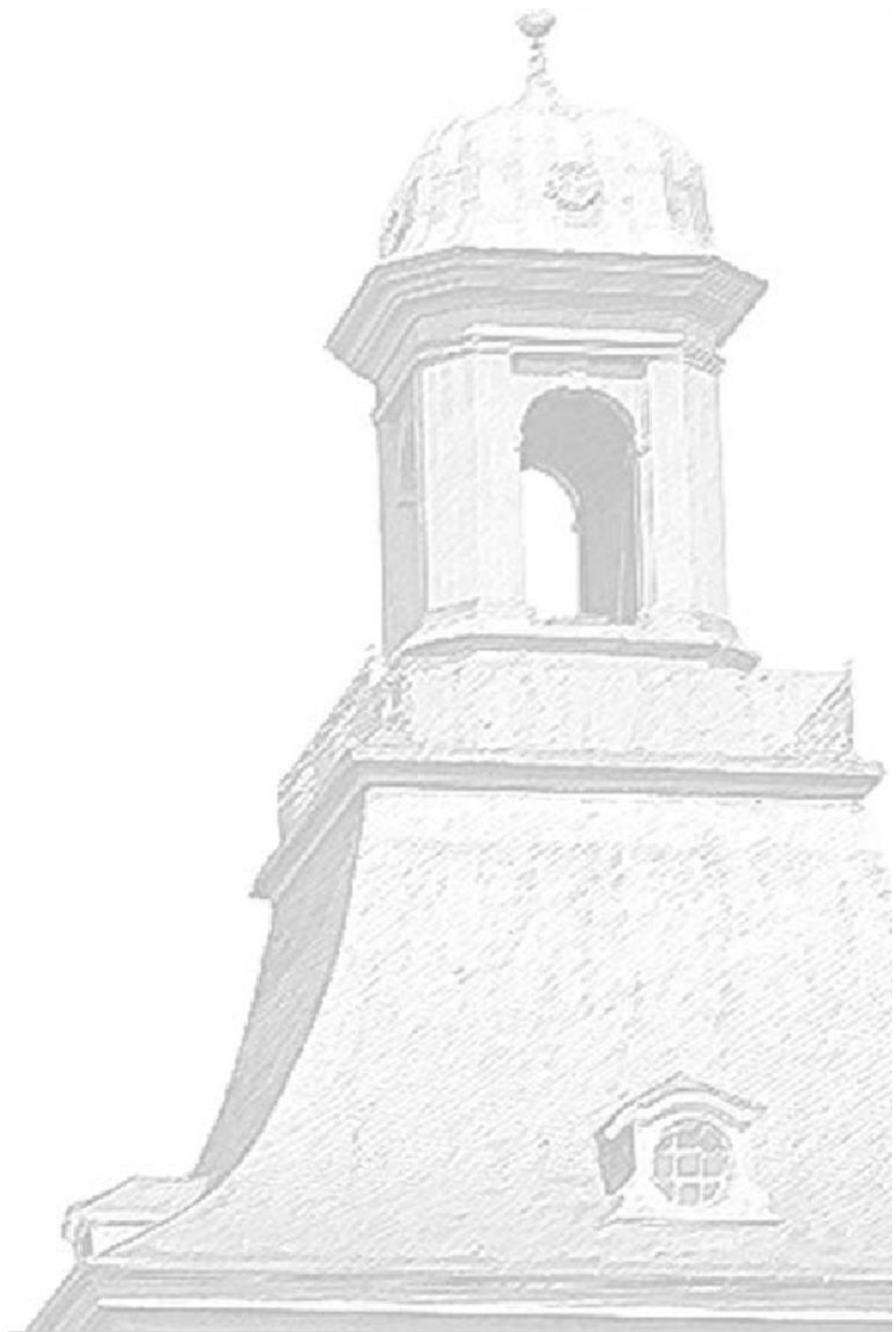


The Belle II Pixel Detector

Carlos Marinas
University of Bonn



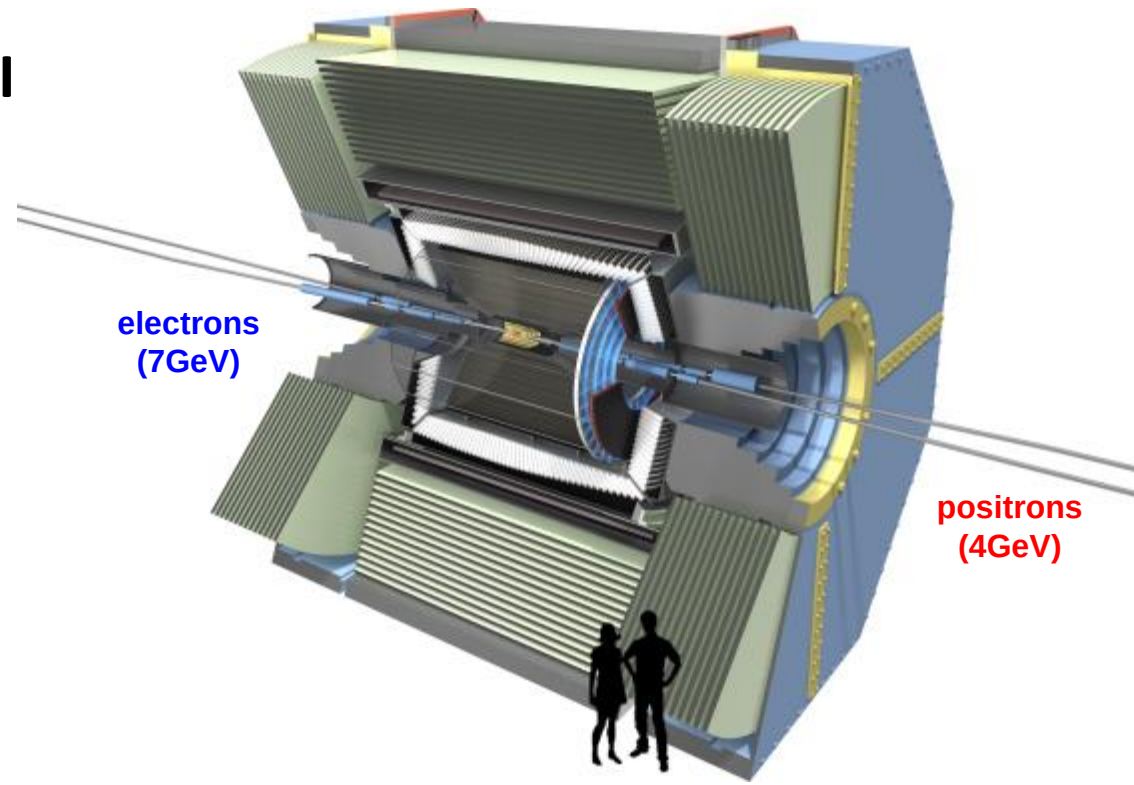
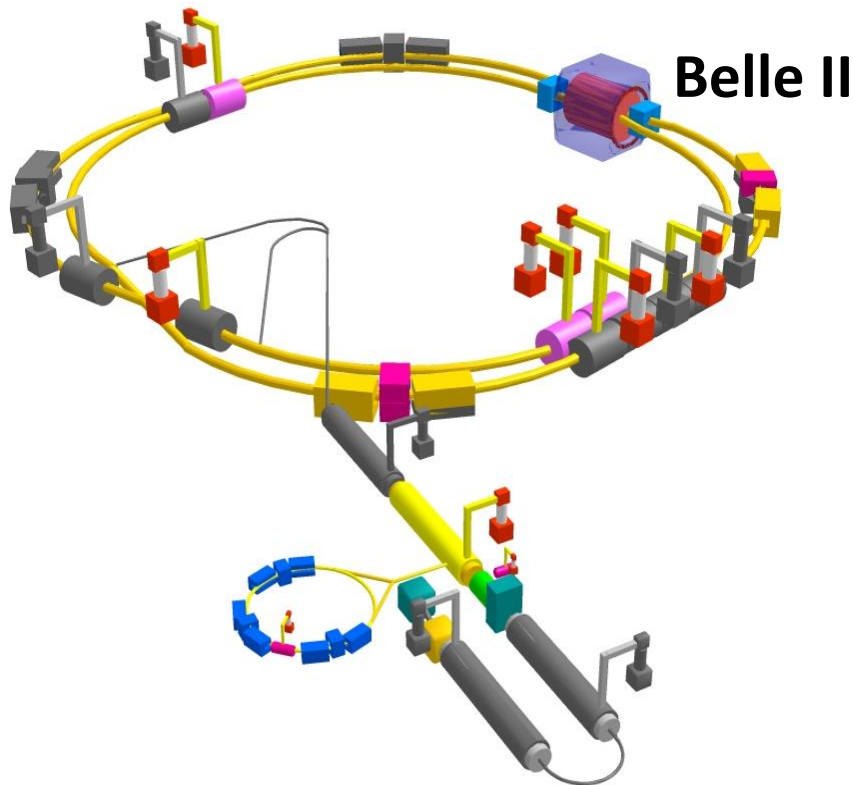
The DEPFET Collaboration

- Charles University, Prague
- DESY, Hamburg
- IFCA, Santander
- IFIC, Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- LMU Munich
- MPI, Munich
- HLL, Munich
- TU, Munich
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen



- SuperKEKB and Belle II Upgrade
 - Pixel detector
- DEPFET System Aspects
 - Sensor and ASICs status
- Latest results
 - Lab and beam tests

The KEKB Upgrade



- SuperKEKB: Asymmetric energy e^+e^- collider
 $E_{\text{cm}} = m(\Upsilon(4S)) = 10.58 \text{ GeV}$
- Final luminosity: $\mathcal{L} = 8 \cdot 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ (x40 higher than KEKB)
- Luminosity: Beam size reduction (nm) and higher current

- Larger backgrounds: higher occupancy and radiation damage
- Higher event rate: faster trigger and DAQ
- Decreased boost ($\beta\gamma=0.28$) $\rightarrow$ Better vertexing required
- Ready for Physics run in 2016

SuperKEKB accelerator Japan

Mt. Tsukuba

SuperKEKB ring (HER+LER)

Belle II detector

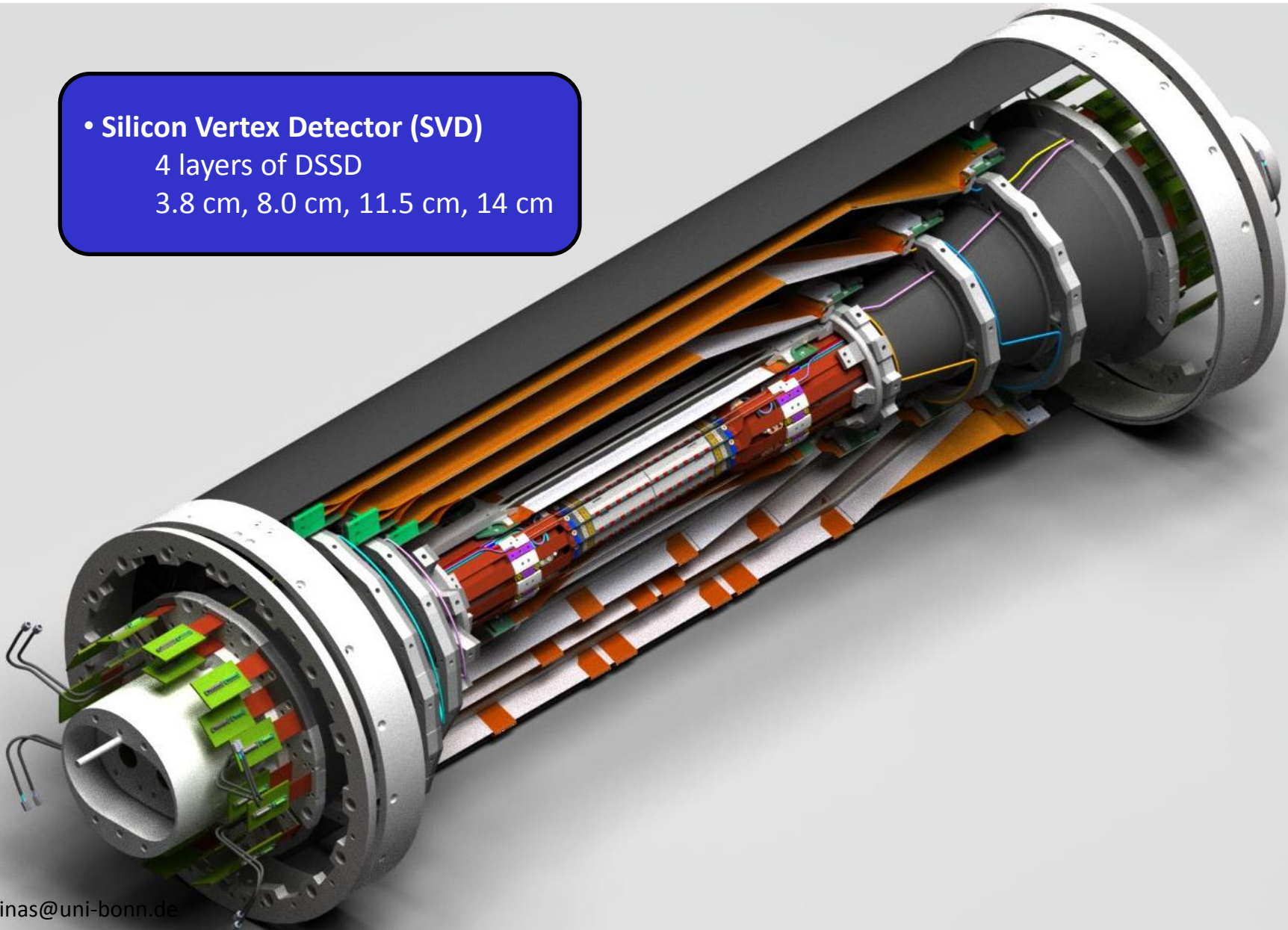
Linac

KEK - Tsukuba

- **Silicon Vertex Detector (SVD)**

4 layers of DSSD

3.8 cm, 8.0 cm, 11.5 cm, 14 cm



- **Silicon Vertex Detector (SVD)**

4 layers of DSSD

3.8 cm, 8.0 cm, 11.5 cm, 14 cm

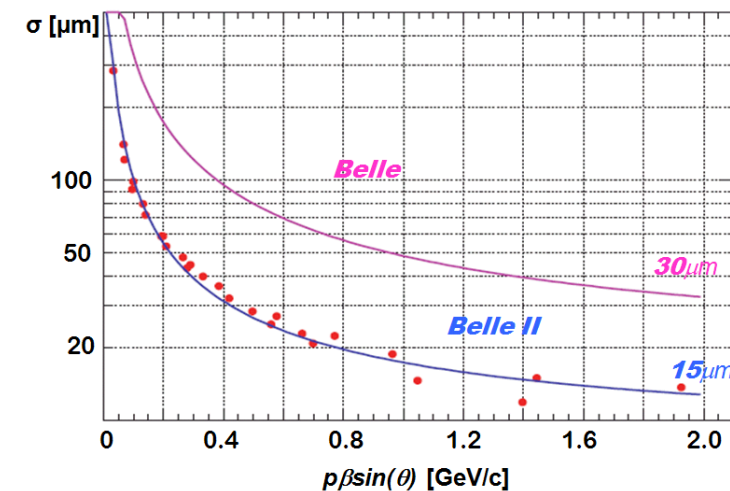
- **Pixel Detector (PXD)**

2 layers of DEPFET pixels

1.4 cm, 2.2 cm

New !

	Belle II
Occupancy	0.4 hits/ $\mu\text{m}^2/\text{s}$
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Duty cycle	1
Frame time	20 μs
Momentum range	Low momentum (< 1 GeV)
Acceptance	17° - 155°
Material budget	0.21% X_0 per layer
Resolution	15 μm ($50 \times 75 \mu\text{m}^2$)



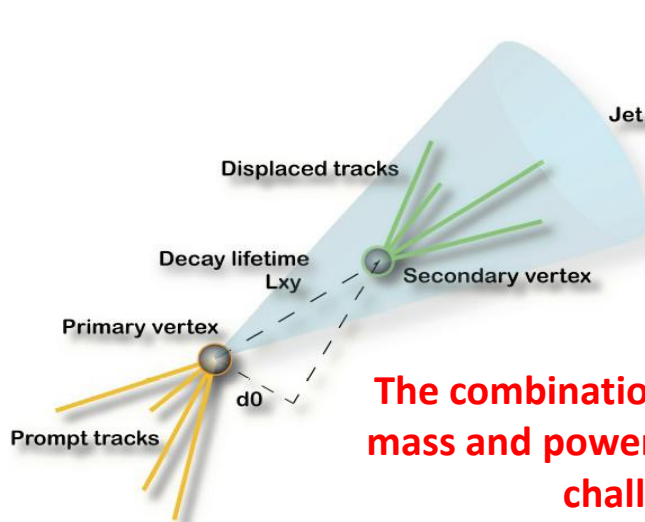
- Modest resolution (15 μm), dominated by M.S. $\rightarrow$ Pixel size ($50 \times 75 \mu\text{m}^2$)
- Lowest possible material budget (0.2% X_0/layer)

- DEPFET is one of the candidates** for the ILC vertex detector

	Belle II	ILC
Occupancy	0.4 hits/ $\mu\text{m}^2/\text{s}$	0.13 hits/ $\mu\text{m}^2/\text{s}$
Radiation	2 Mrad/year	< 100 krad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year	10^{11} 1 MeV n_{eq} per year
Duty cycle	1	1/200
Frame time	20 μs	25-100 μs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	17°-155°	6°-174°
Material budget	0.21% X_0 per layer	0.12% X_0 per layer
Resolution	15 μm (50x75 μm^2)	5 μm (20x20 μm^2)

→ Belle II presents more severe challenges than ILC in many different aspects

** Novel detector concepts for e+e- physics (P. Roloff)



The combination of resolution, mass and power is a substantial challenge

$$\sigma_{d0} \approx \sqrt{\frac{r_2^2 \sigma_1^2 + r_1^2 \sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{p \sin^{\frac{3}{2}} \theta} 13.6 \text{ MeV} \sqrt{\frac{x}{X_0}}$$

	a (μm)	b (μm GeV c ⁻¹)
SLD	9	33
LEP	25	70
LHC	12	70
SuperKEKB	8.5	10
ILC	5	10

Common vertex detector requirements

- First layer close to the IP
- Low material budget
 - Reduced services
 - Low power dissipation
- High granularity
 - Good spatial resolution
- Fast readout
- Radiation hardness



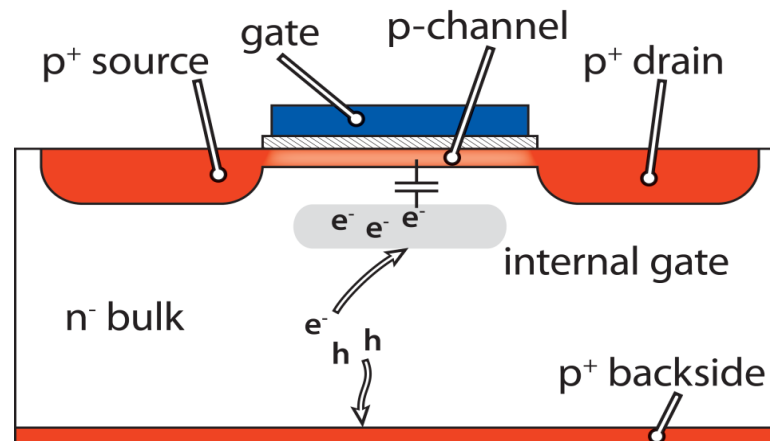
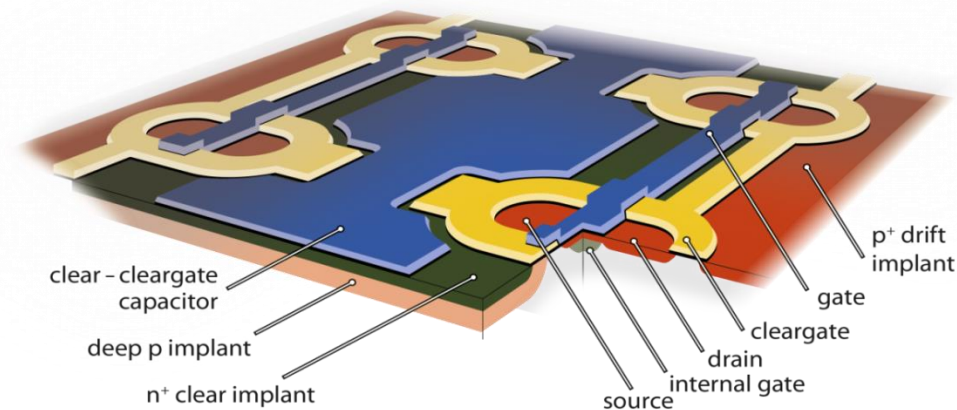
Highly pixelated



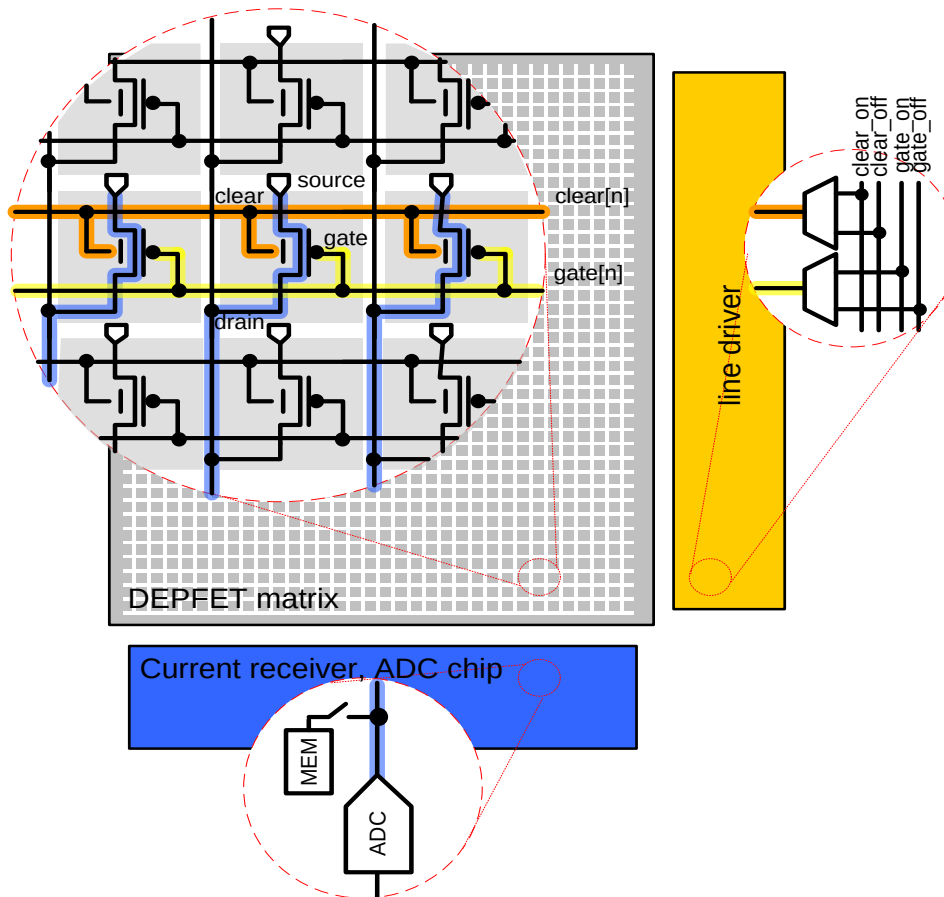
Transparent

DEPFET – DEpleted Field Effect Transistor**

- Concept: amplifying transistors in a fully depleted bulk
- Internal gate forms potential minimum for e^-
- Stored charge modulates the channel current
- Small intrinsic noise
- Sensitive off-state, no power consumption
- Internal amplification $g_q \sim 0.3 - 1.0 \text{ nA}/e^-$



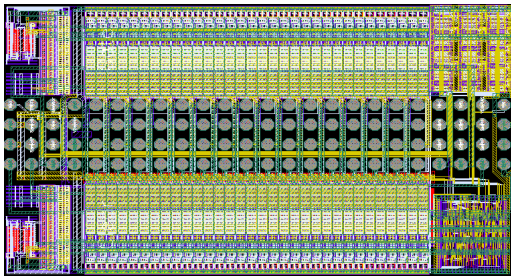
** DEPFET APS - recent developments and new applications (L. Andricek)



- Pixels are arranged in a matrix
- Row wise readout (4 rows at a time)
- Gate, clear lines need Switcher steering chip
- Long drain readout lines to keep material out of the acceptance region
- Only 'activated' rows consume power
 - The others are still sensitive to charge
 - Low power consumption

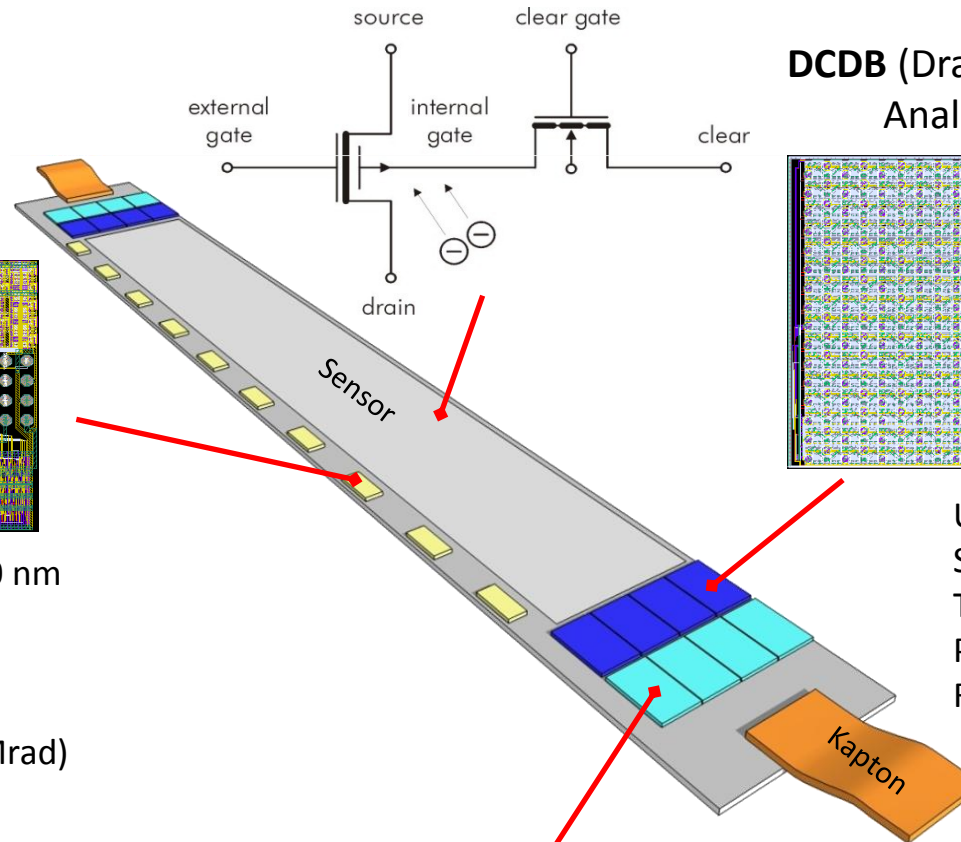
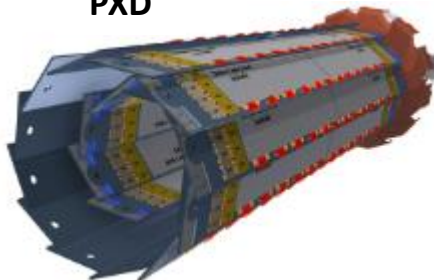
SwitcherB

Row control



AMS/IBM HVCMOS 180 nm
Size $3.6 \times 1.5 \text{ mm}^2$
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

PXD

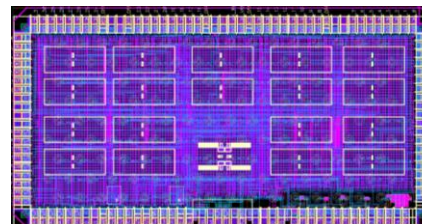


DCDB (Drain Current Digitizer) Analog frontend



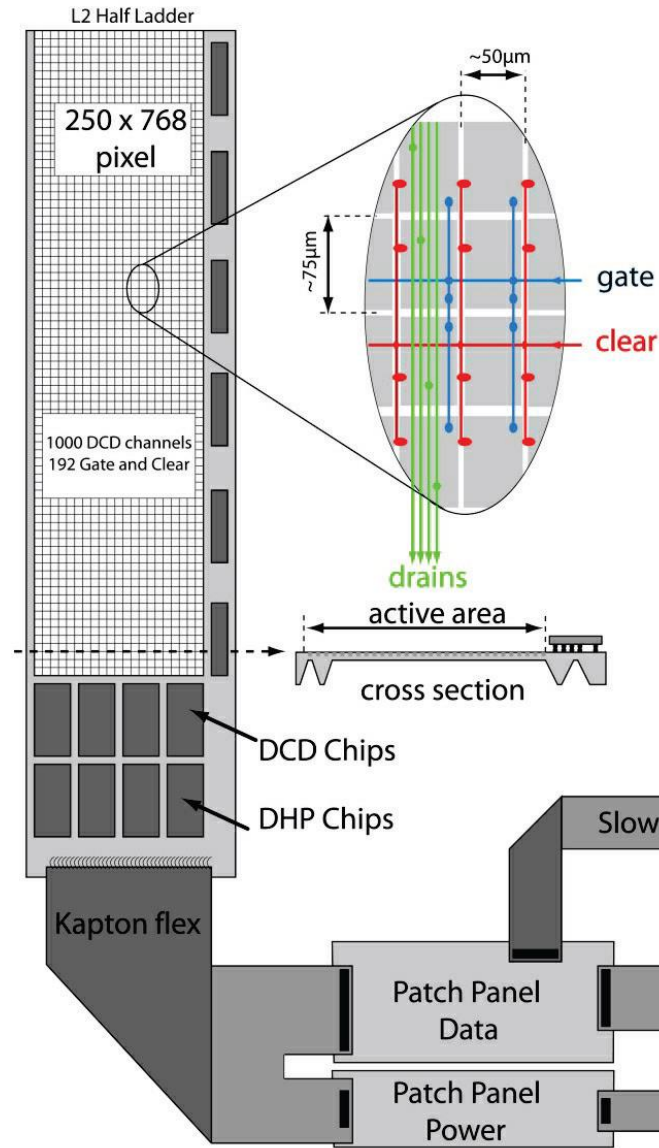
UMC 180 nm
Size $5.0 \times 3.2 \text{ mm}^2$
TIA and ADC
Pedestal compensation
Rad. Hard proved (20 Mrad)

DHP (Data Handling Processor) First data compression

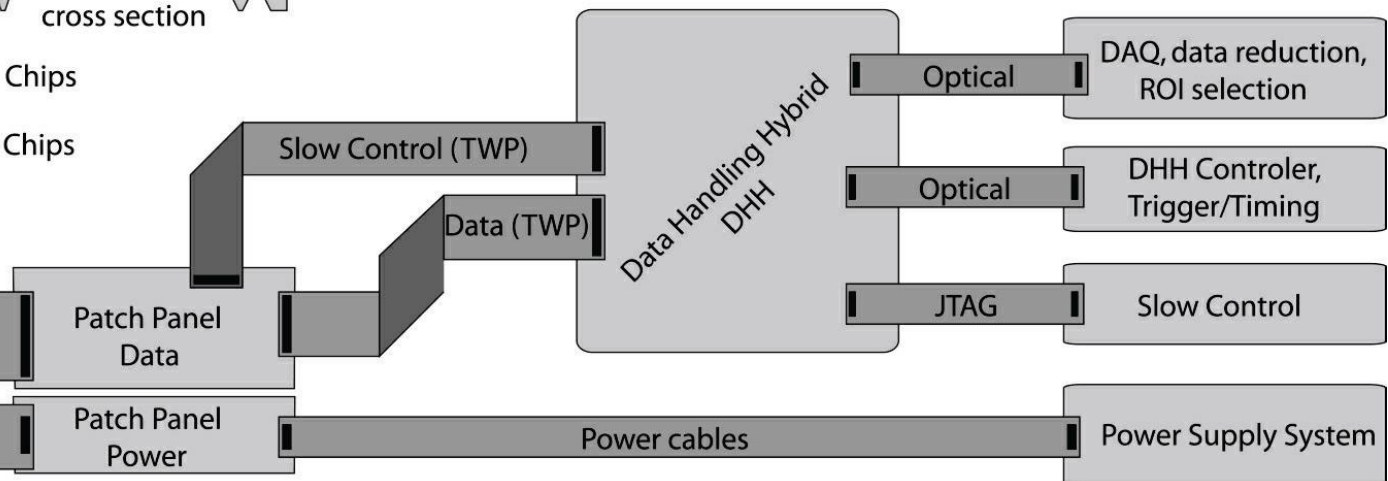


IBM CMOS 90 nm (TSMC 65 nm)
Size $4.0 \times 3.2 \text{ mm}^2$
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

** PXD DAQ System (S. Lange)

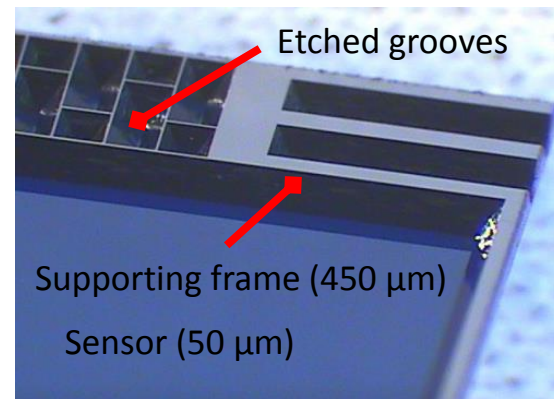
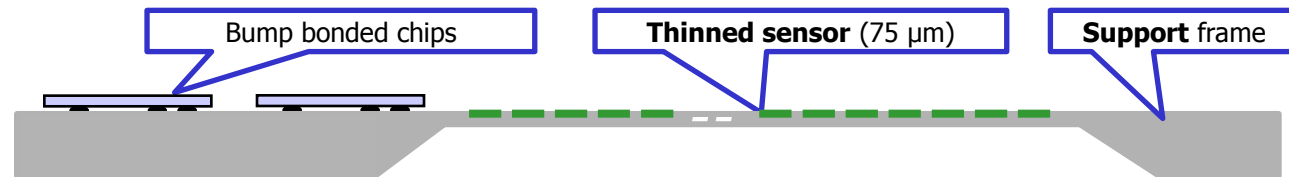
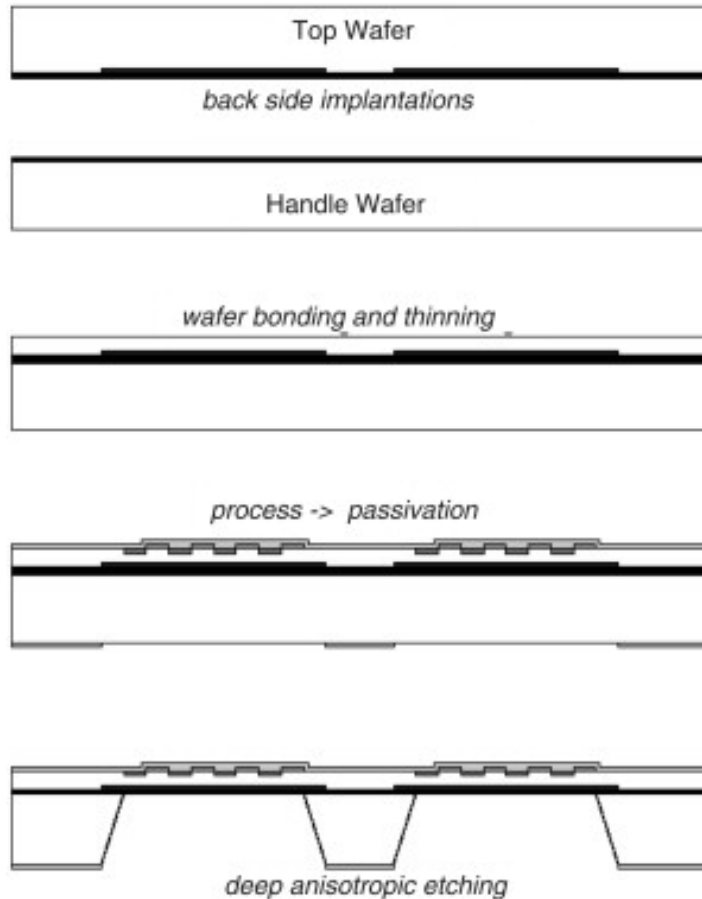


- **DHH (Data Handling Hybrid)**
Electrical - optical interface
Slow control master (JTAG)
- **ONSEN**
Data buffer
Reduction via ROI selection (DatCon, HLT)



Thin DEPFET Sensors**

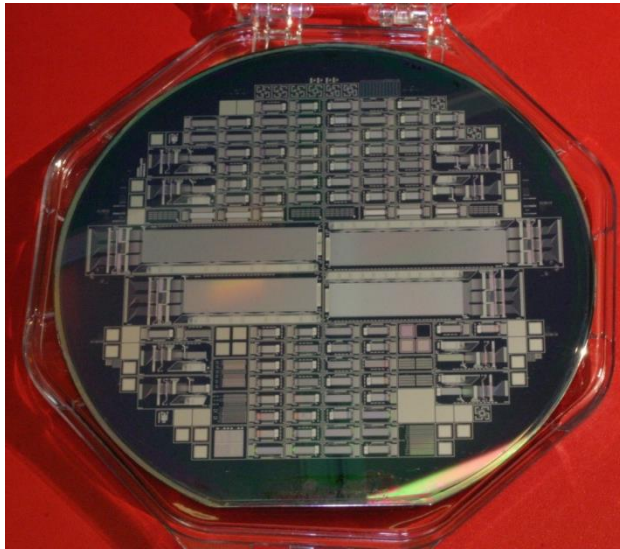
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor
→ One material: uniform and small thermal expansion



** DEPFET APS - recent developments and new applications (L. Andricek)



PXD6 DEPFET Latest Prototype Production



- 8 SOI wafers with 50 μm thin sensors (400 μm handle)
- Small test matrices to test different pixel sizes (50-200 μm)
- Design variations: short gate lengths, clear structures, drift
- Full size sensors –half ladders for prototyping
- Technology variations on the wafer level

90 steps fabrication process:

9 Implantations

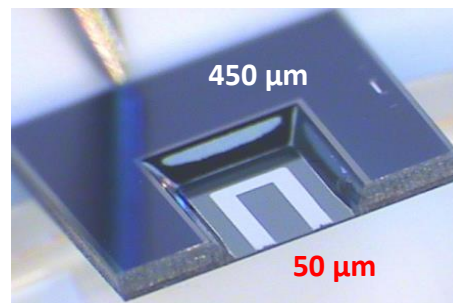
19 Lithographies

2 Poly-layers

2 Alu-layers

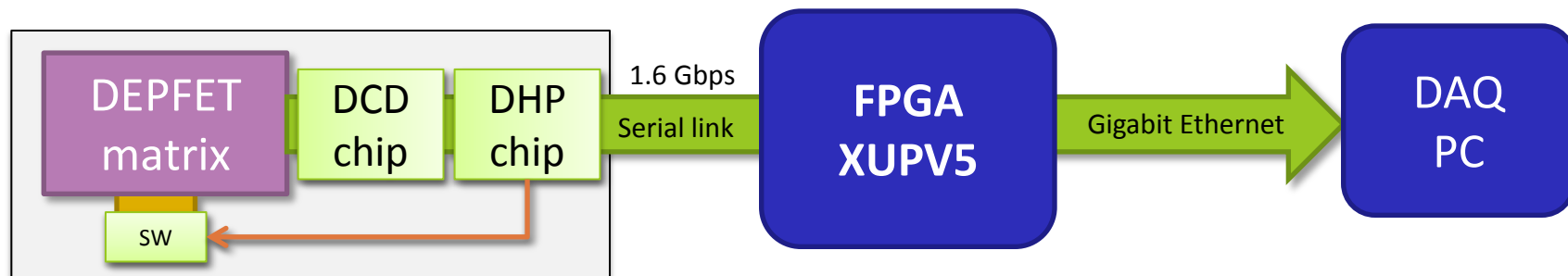
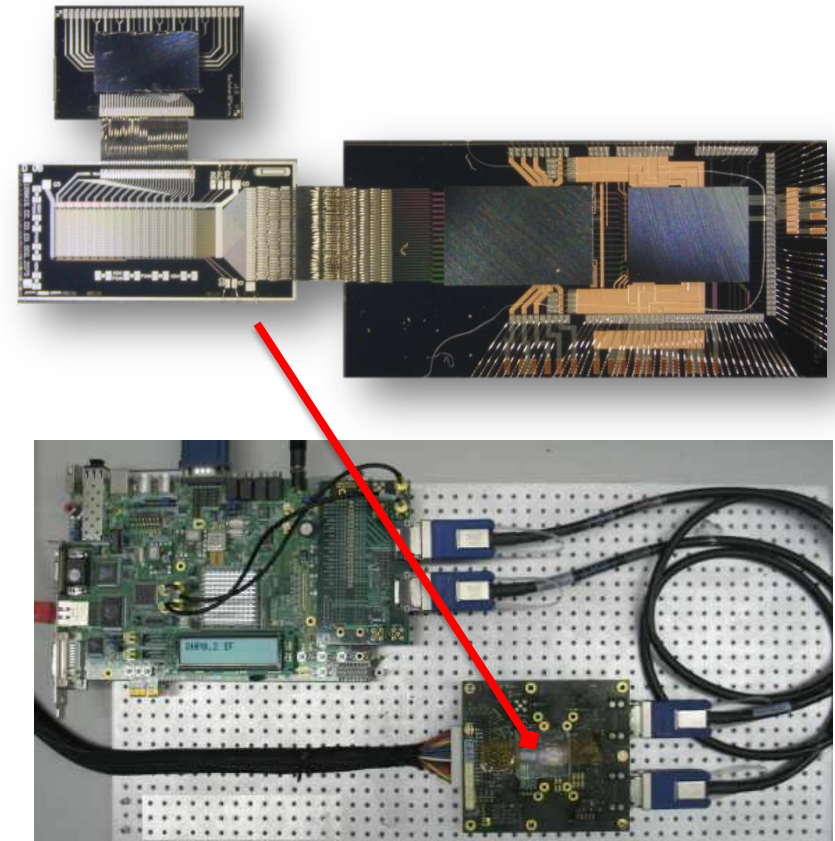
1 Copper layer

Back side processing

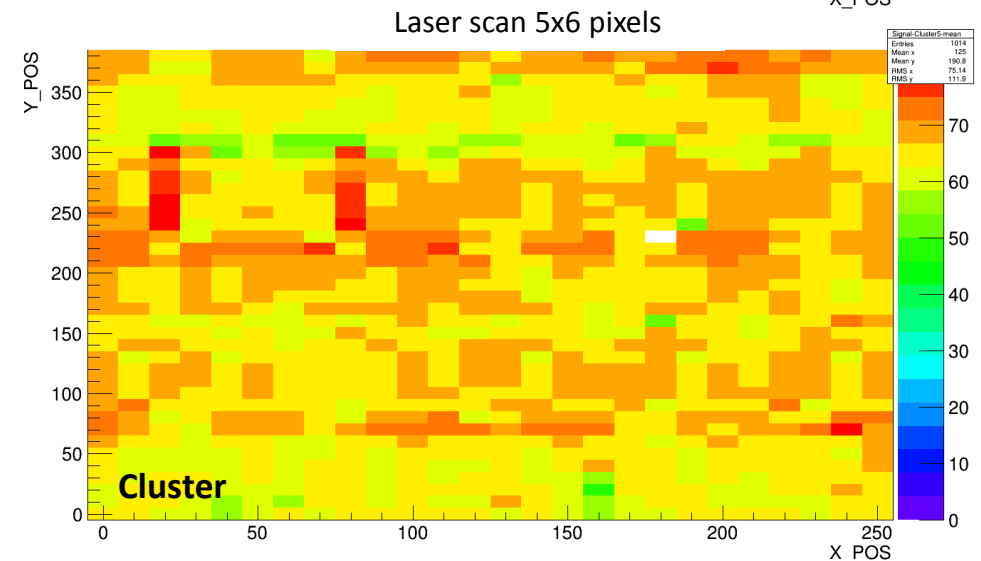
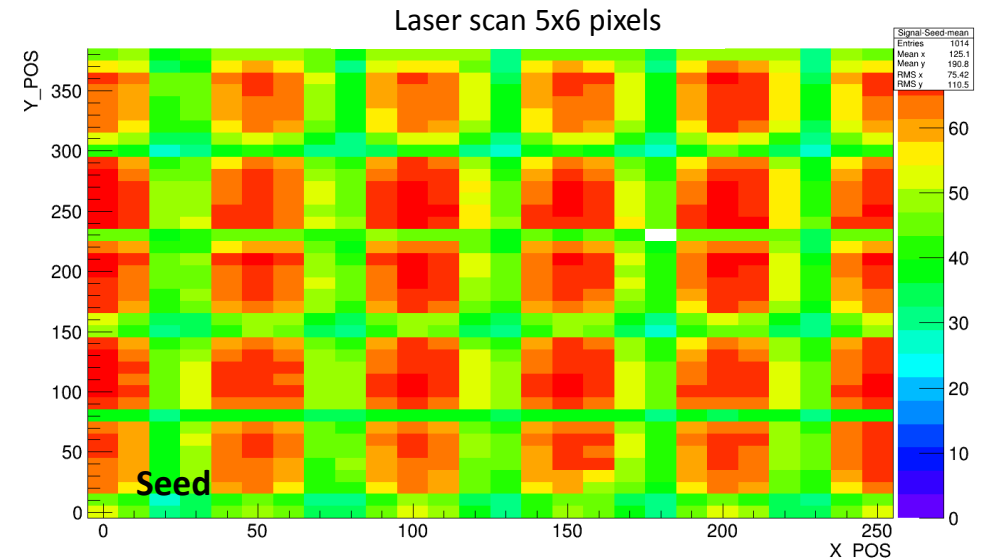
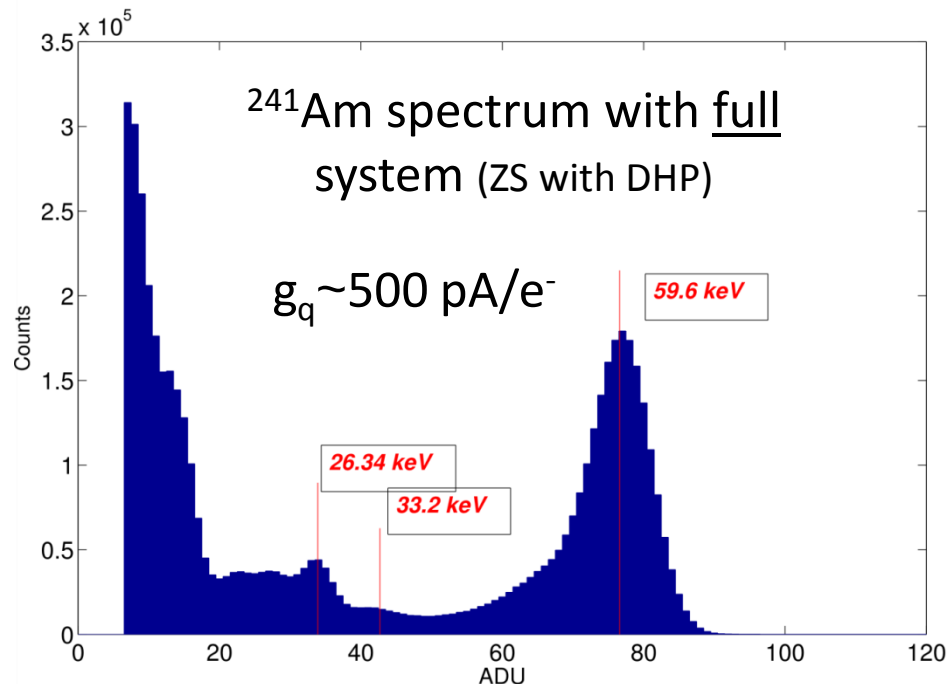


First 50 μm thin DEPFET sensors produced!

- Zero suppressed readout with the minimum necessary amount of components:
 - One Switcher-B
 - One DCDBv2
 - One DHP 0.2
 - Small thin matrix: Belle II SD PXD6 type, 16x128 pixels, 50x75 μm^2 pitch
- Frame rate: 300 kHz (small matrix)

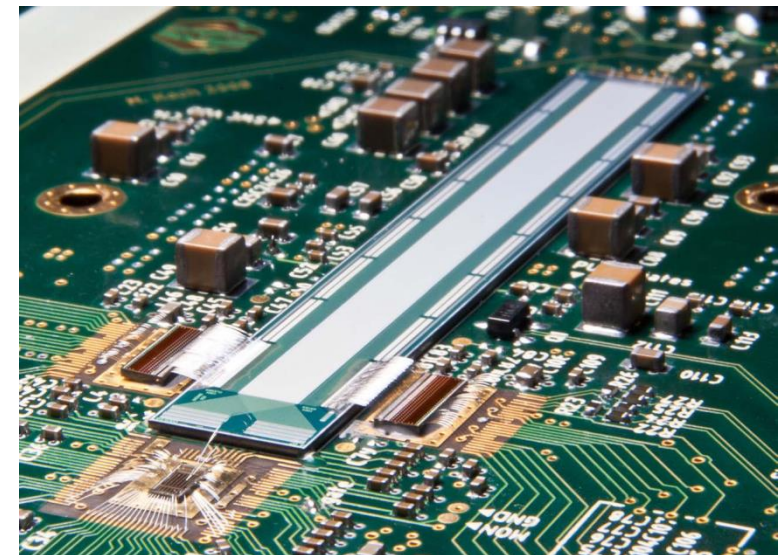
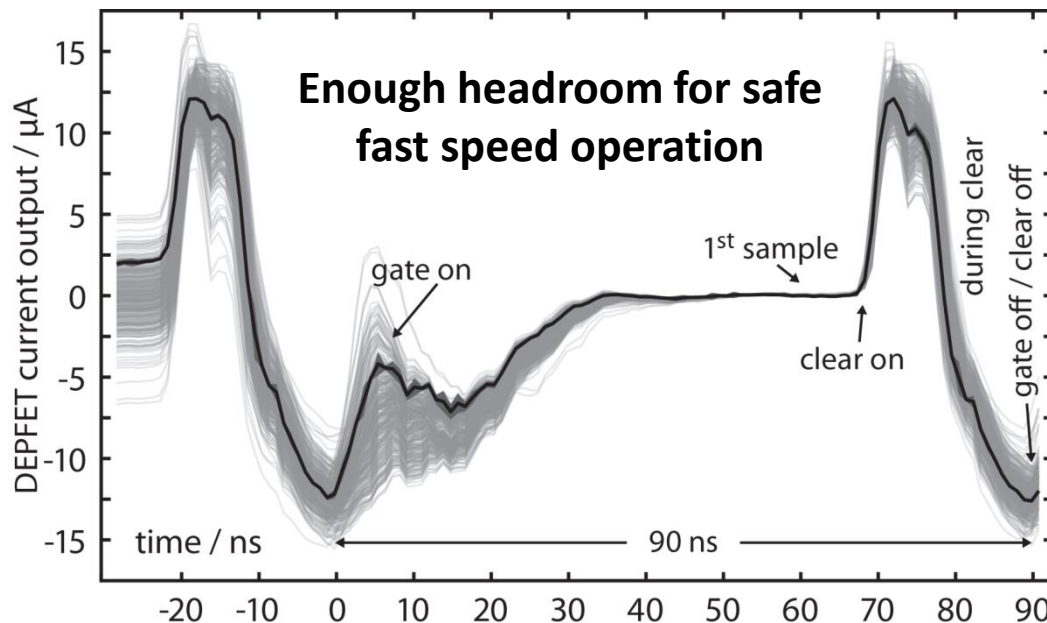
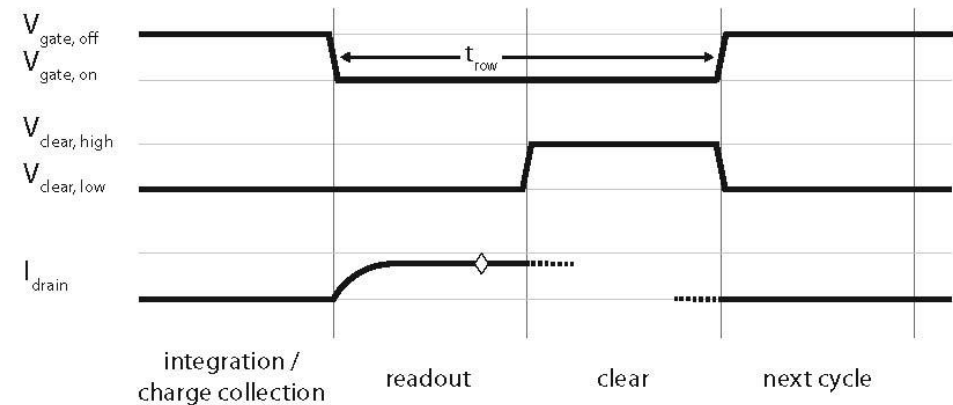


- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
Charge collection homogeneity
In pixel studies
- Radioactive source
System calibration



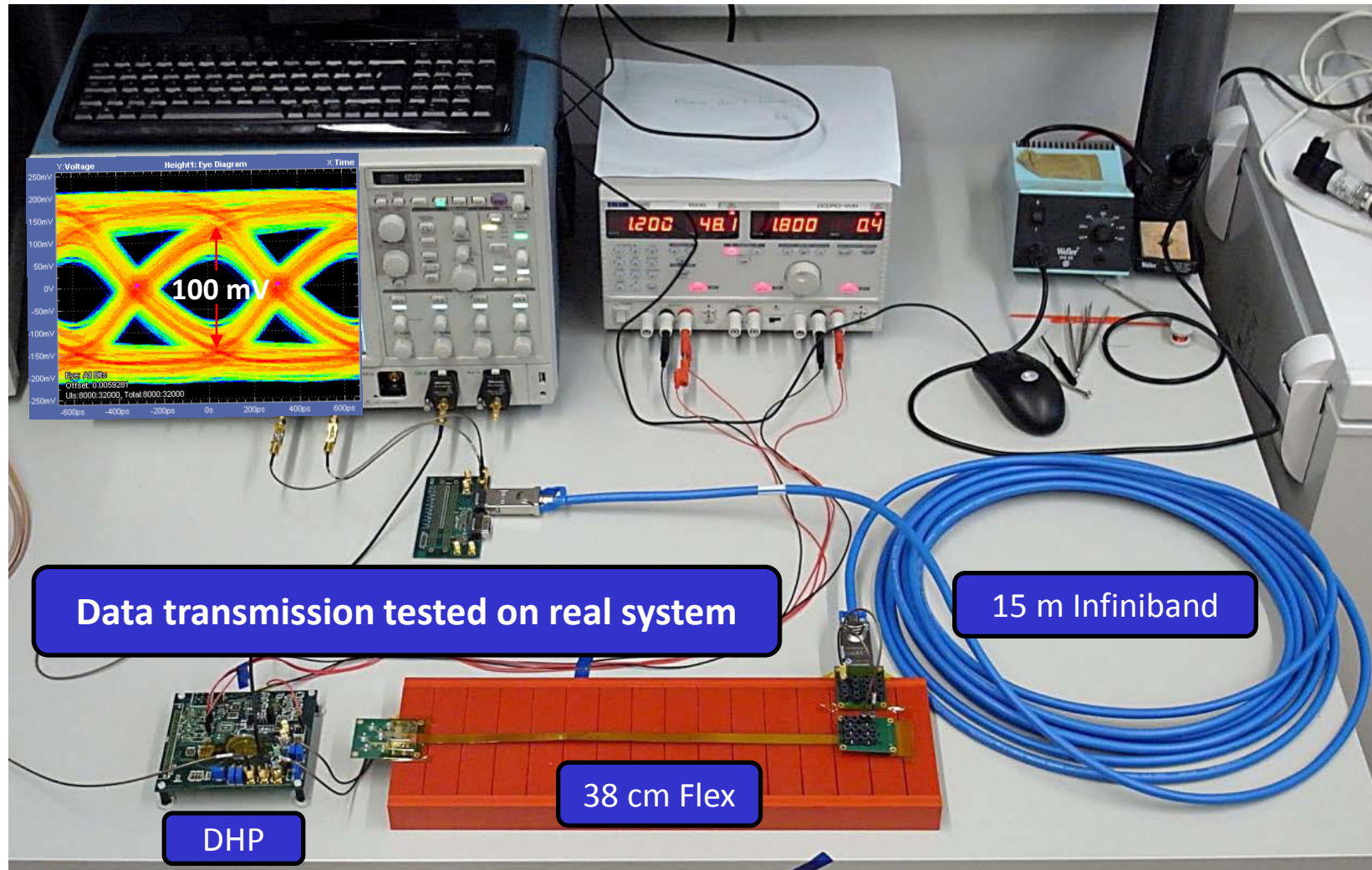
Homogeneous charge collection

- DCD dynamic measurements
Readout speed with single sampling
- Belle II PXD frame readout: 20 μs
(50 KHz frame rate)
- Read-clear cycle: 100 ns
(768 rows, 4 fold readout)



Long drain lines $\sim 60 \text{ pF}$ parasitic capacitance

Laboratory Tests: DHP Serial Link



+ pre-emphasis

**Irradiated (100 Mrad) DHPT 0.1, can drive
15 m of Infiniband cable**

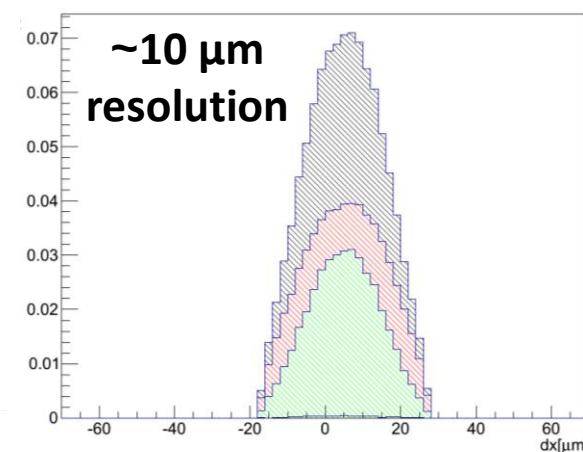
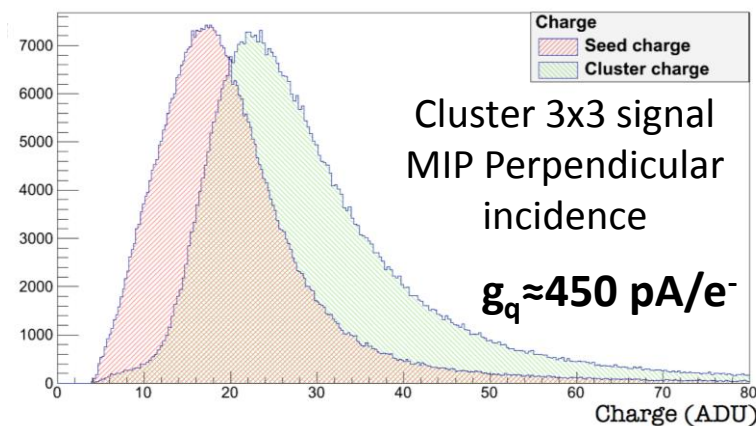
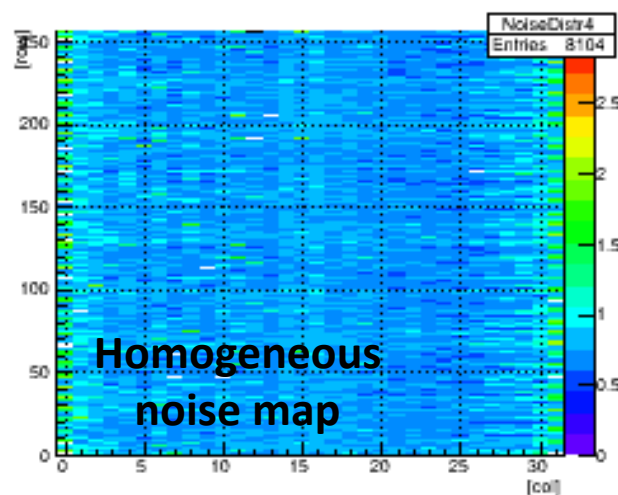
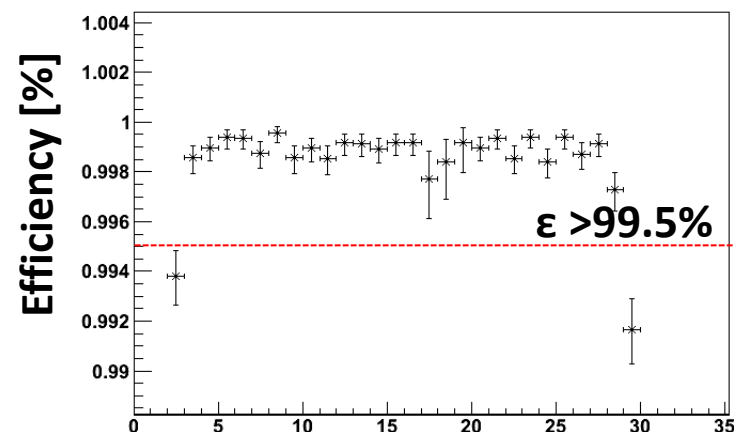
PXD6 Belle II design

Thin 50 μm sensor

Pitch 50x75 μm^2

Targeted speed readout

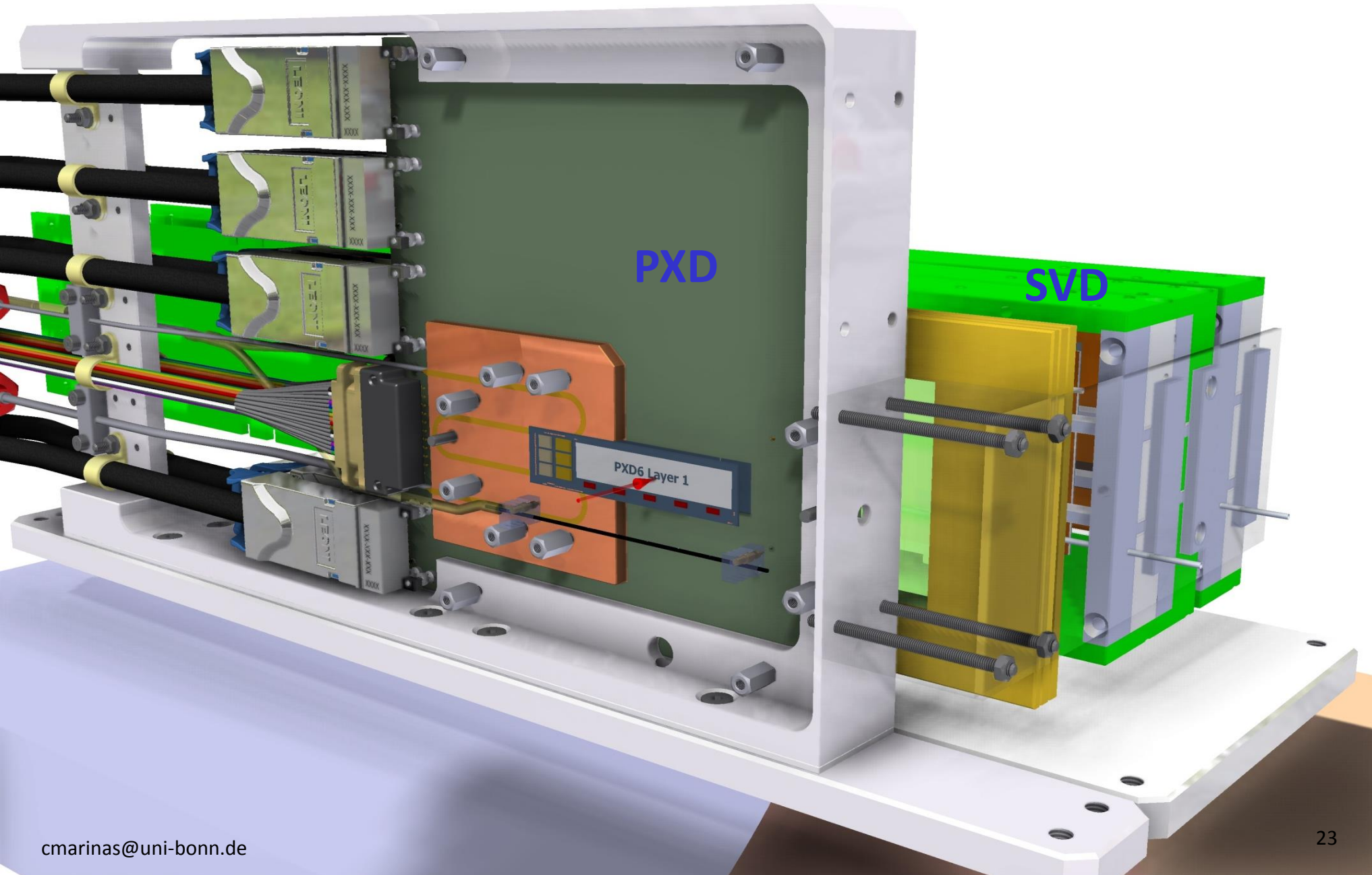
Belle II prototype power supply



Prove of principle demonstrated in many test beam campaigns over the past years

- VXD common test beam in January 2014 (4 weeks)
 - Small sector of the close to final prototype detectors and ASICs
PXD half ladder + 4 SVD single module layers
 - Complete VXD readout chain: HLT, monitoring, event building
 - CO₂ cooling, slow control, environmental sensors
 - Illumination with (up to) 6 GeV e⁻ under 1 T solenoid magnetic field
 - Alignment, tracking algorithms, ROI
- **Goal: System integration test**

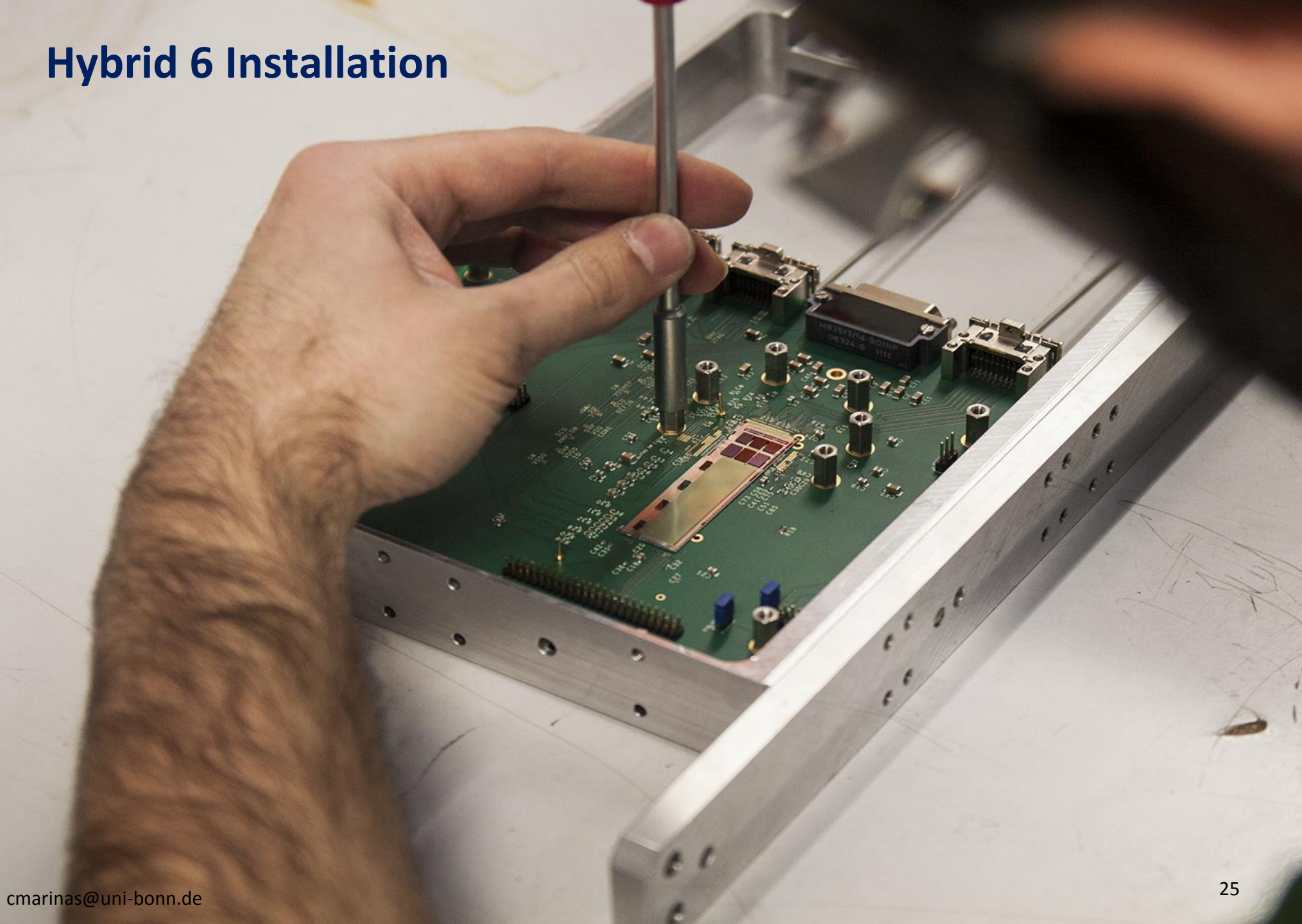
Test Beam Set-up

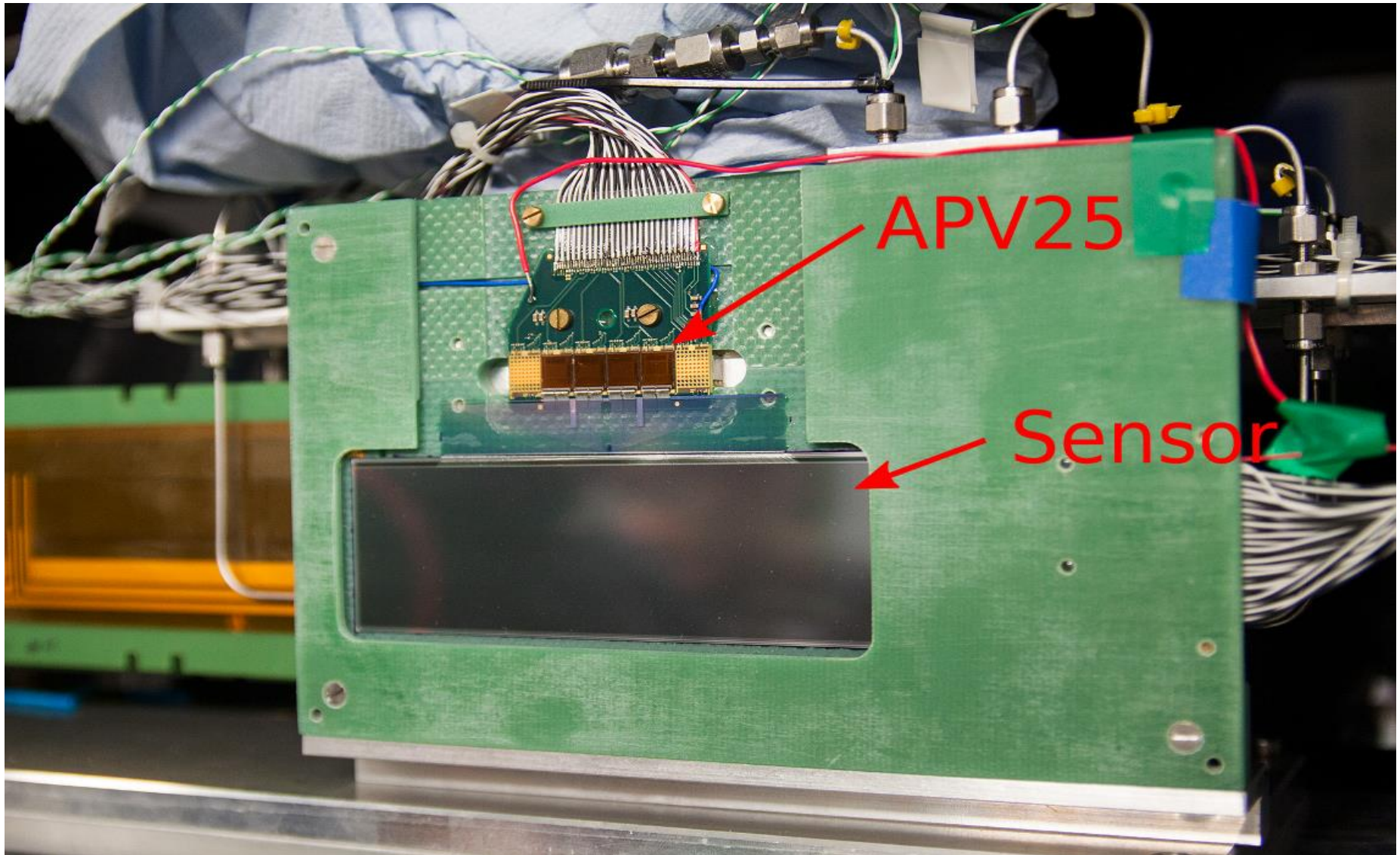


Belle II standard pixel cell design
Close to final versions of ASICs
640x192 pixels matrix
50x75x50 μm^3 pixel cells

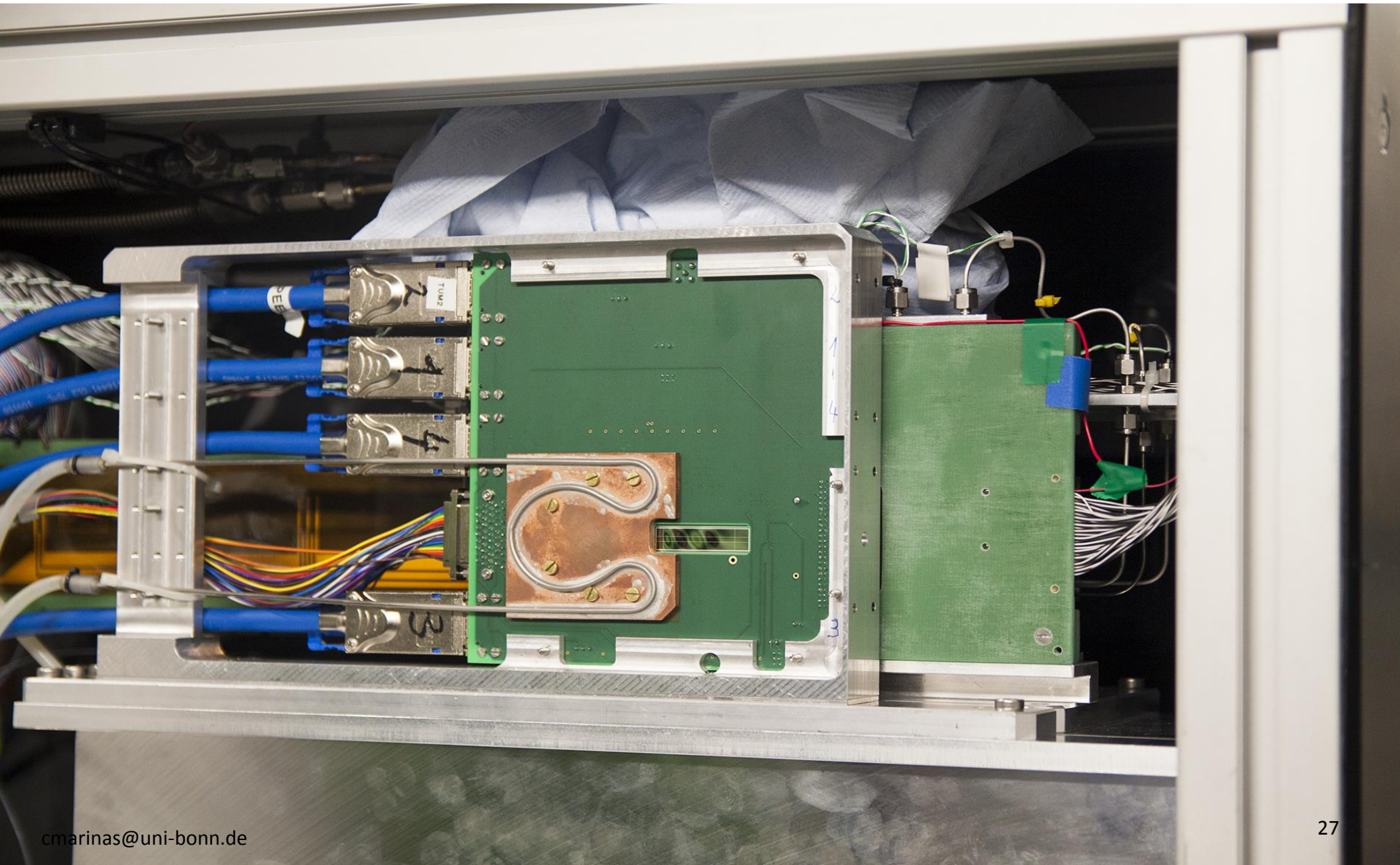
First time that a large, thin, multi-chip module
has been produced and operated

Hybrid 6 Installation

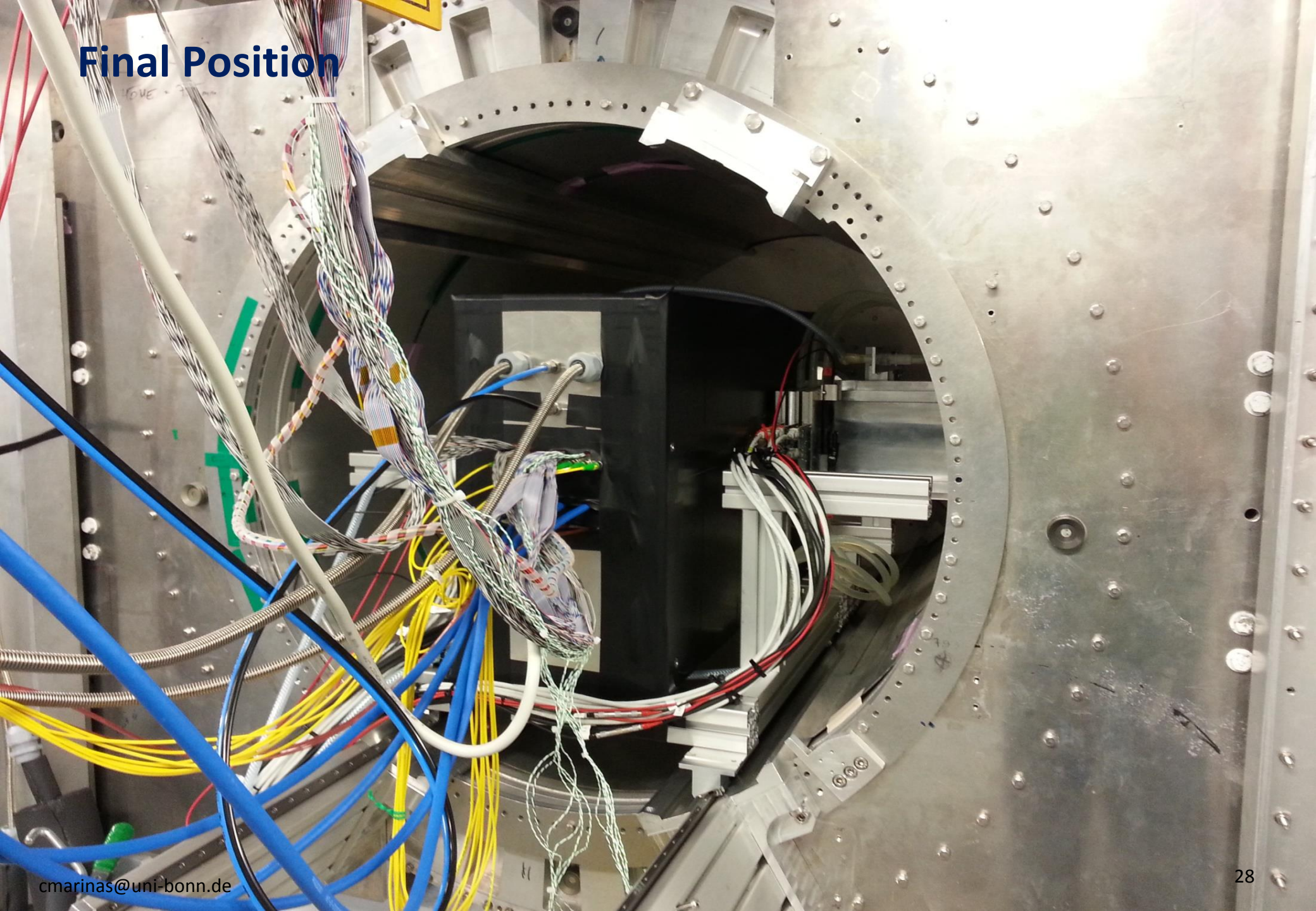




DEPFET Detector Installed

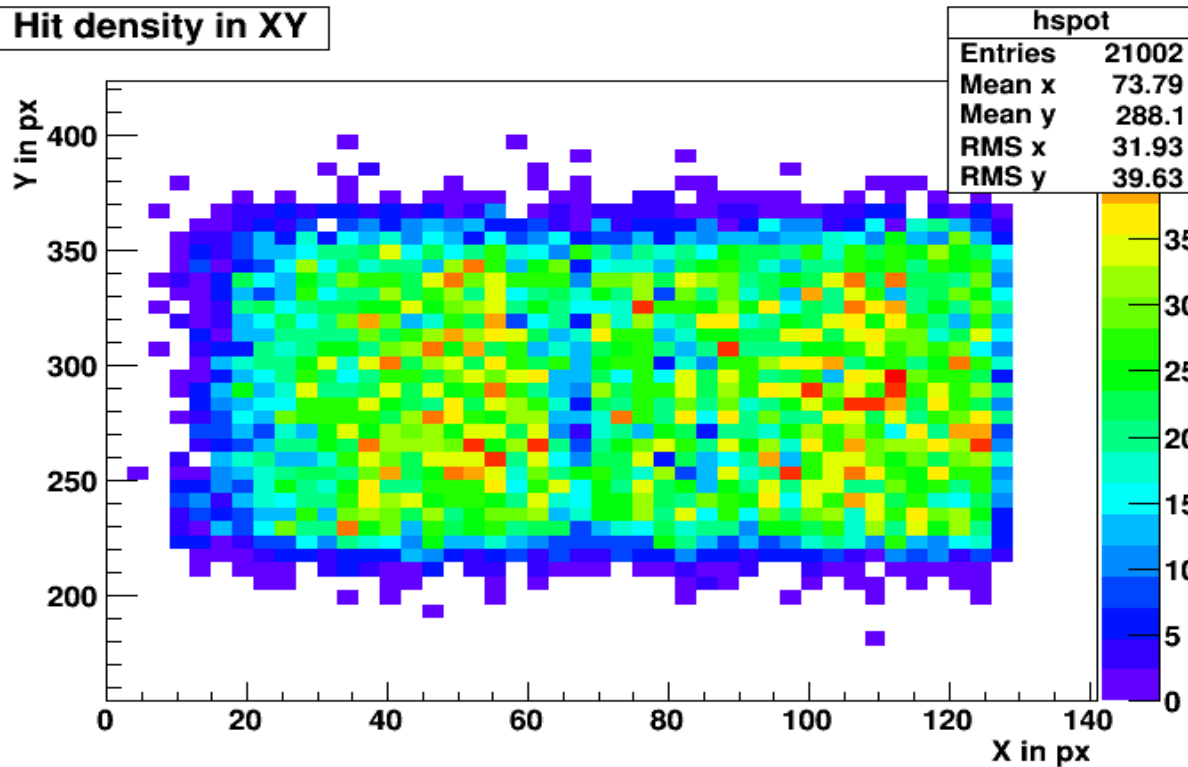


Final Position

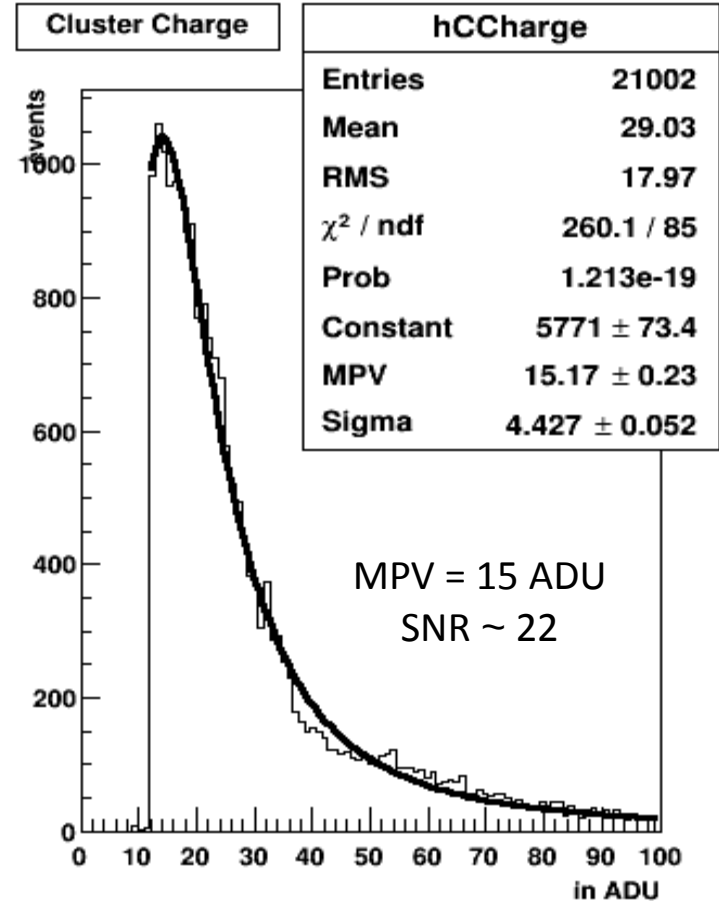


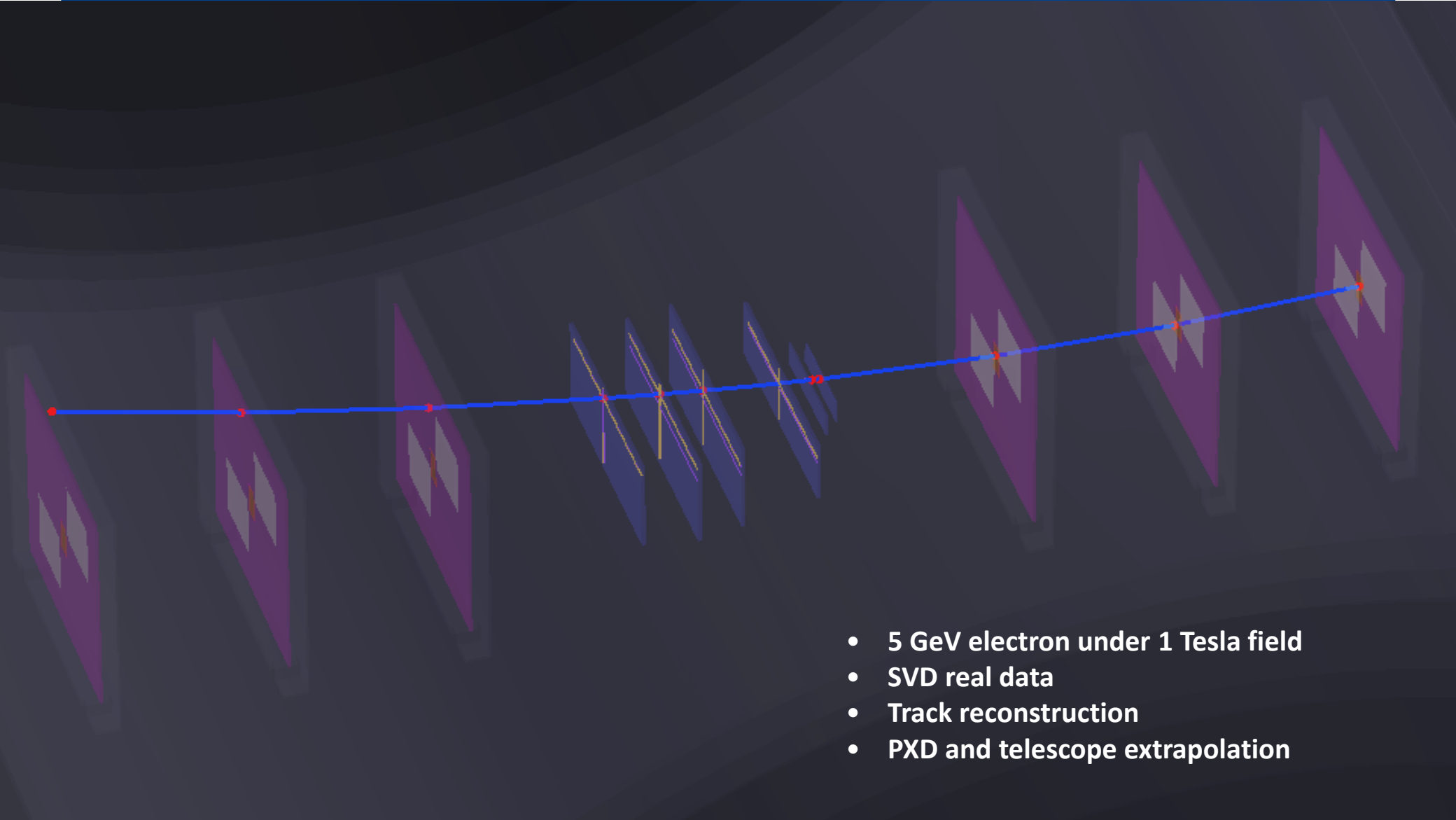
PXD HitMap and Cluster Signal

Hit density in XY



Beam spot 11x6 mm²





- The DEPFET Collaboration is developing ultra-transparent pixel sensors with integrated amplification for the Belle II vertex detector
- The good performance of the detector system (sensor+ASICs+DAQ) in terms of SNR, spatial resolution and speed is demonstrated
- Building and integrating a real system: Every detail (although not covered here) is being considered
 - Cooling, mechanics, DAQ, interlocks, env. monitor, alignment, ...

Thank you

