Calorimetry
Active Elements & Mechanics

Terascale Detector WS
Göttingen, March 2014

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Calorimeter for ILC

Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

Outline

- Introduction
- Active Elements
  - The Photon Sensor
  - The Scintillator Tiles
  - The Electronics
- Calorimetry Mechanics
  - Cassettes
  - Absorber Structures
- Conclusions

Introduction: Calorimeters for PFA

- The detectors where PFA “happens” - Quite different than calorimeter systems at current experiments in terms of granularity: Segmentation finer than the typical structures in particle showers
  - ECAL: X_0, ρ_M (length scale & width of shower)
  - HCAL: length scale ~ λ_I, but em subshowers impose requirements not too much different than in ECAL

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Depends on material:
- in W: X_0 ~ 3 mm, ρ_M ~ 9 mm
- in Fe: X_0 ~ 20 mm, ρ_M ~ 30 mm

NB: Best separation for narrow showers particularly important in ECAL
➩ Use W in ECAL!

When adding active elements: ~ 0.5 cm^3 segmentation in ECAL, ~ 3 - 25 cm^3 in HCAL

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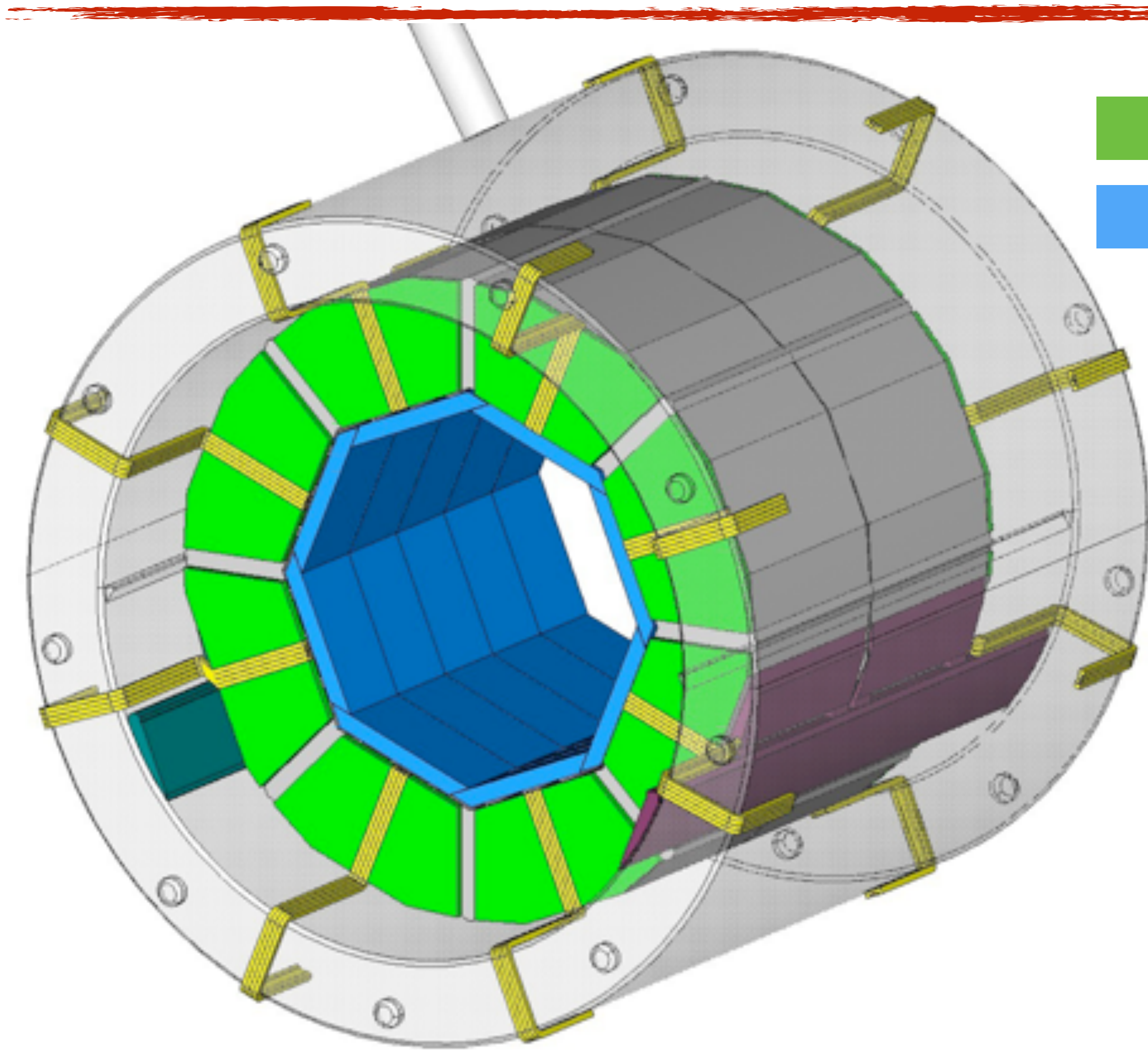
Several technological options both in ILD and SiD:
- ECAL: Tungsten absorbers, Si or Scintillator with SiPMs as active medium
- HCAL: Steel absorbers
  - analog: Scintillator tiles with SiPMs
  - digital or semi-digital: RPCs, GEMs, μMegas (digital or semi-digital)

Introduction: Design Overview



HCAL
ECAL

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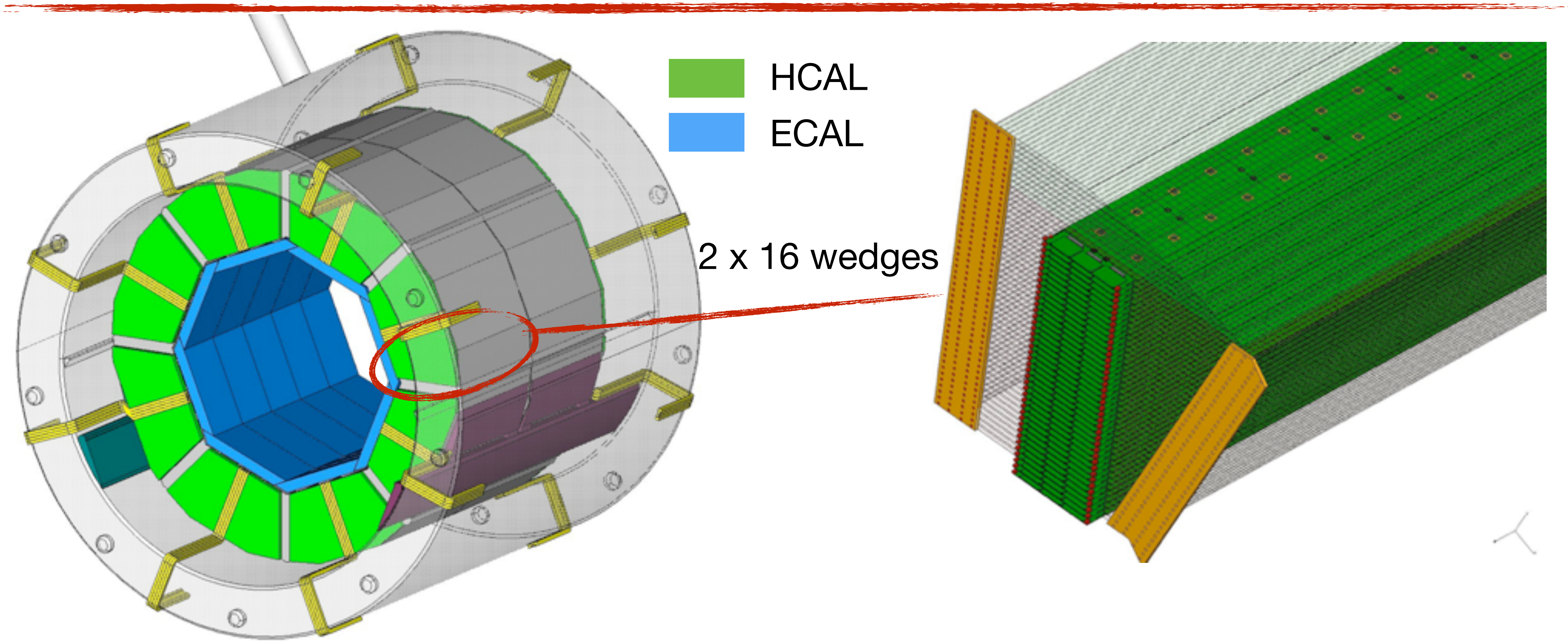

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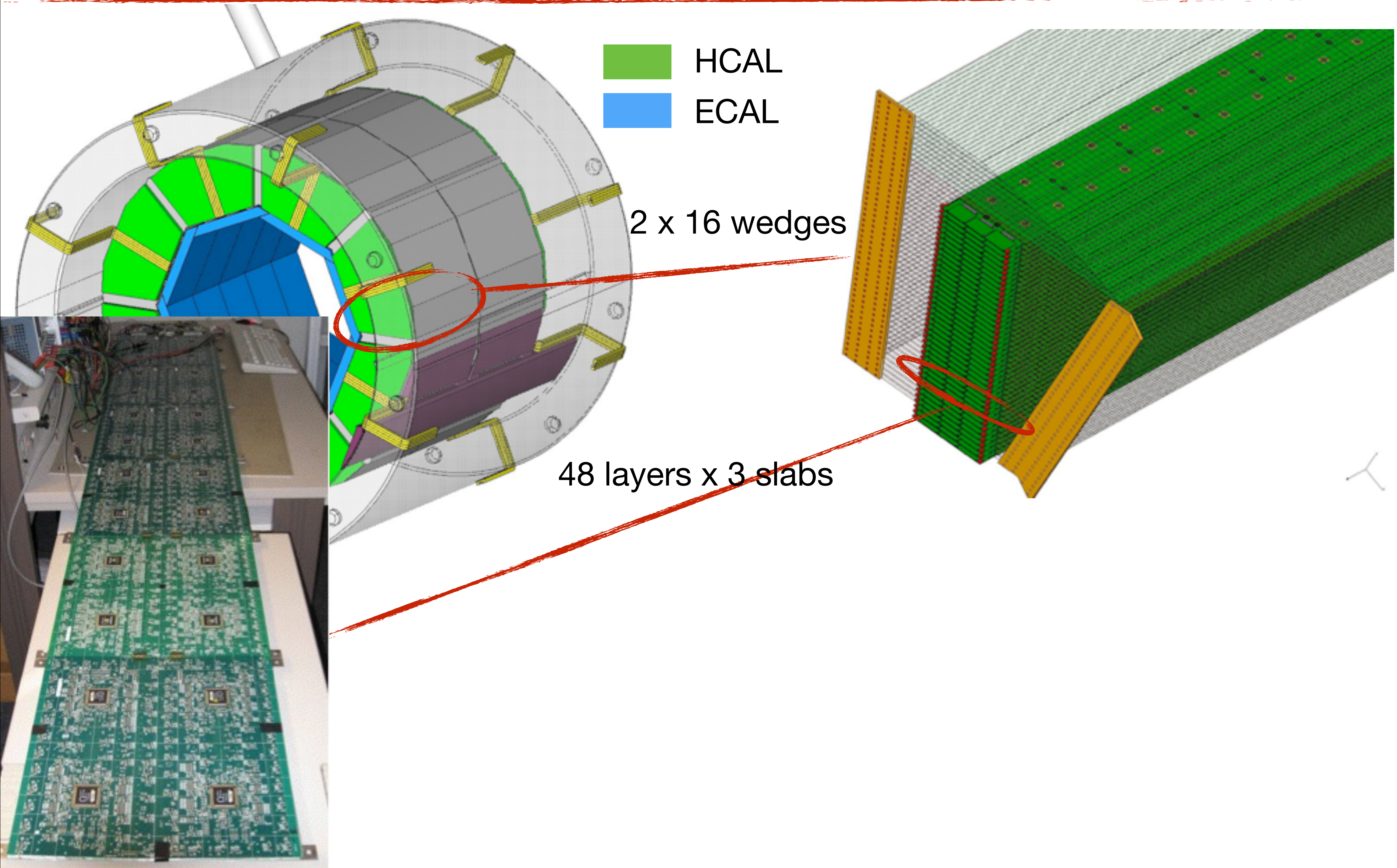

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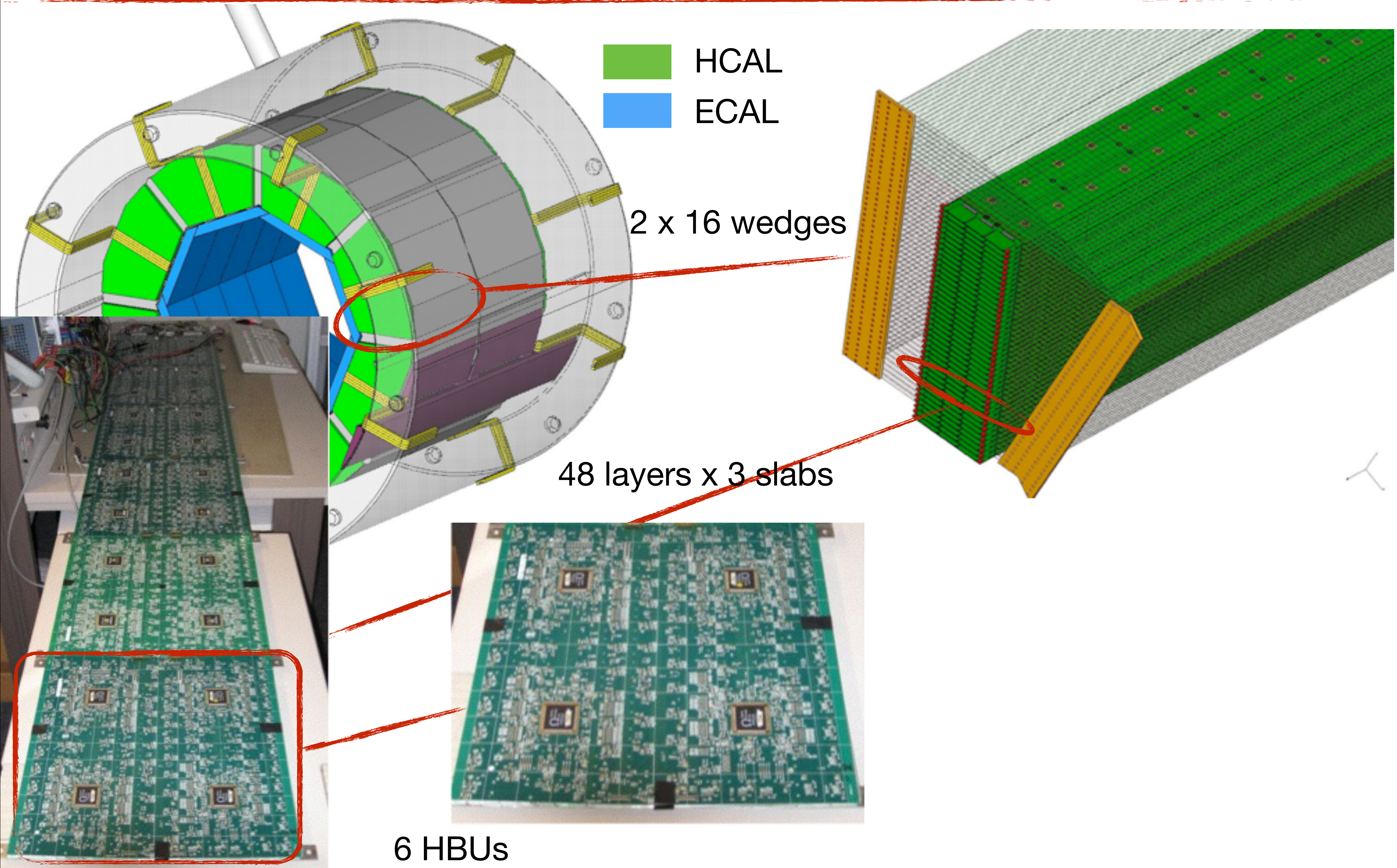

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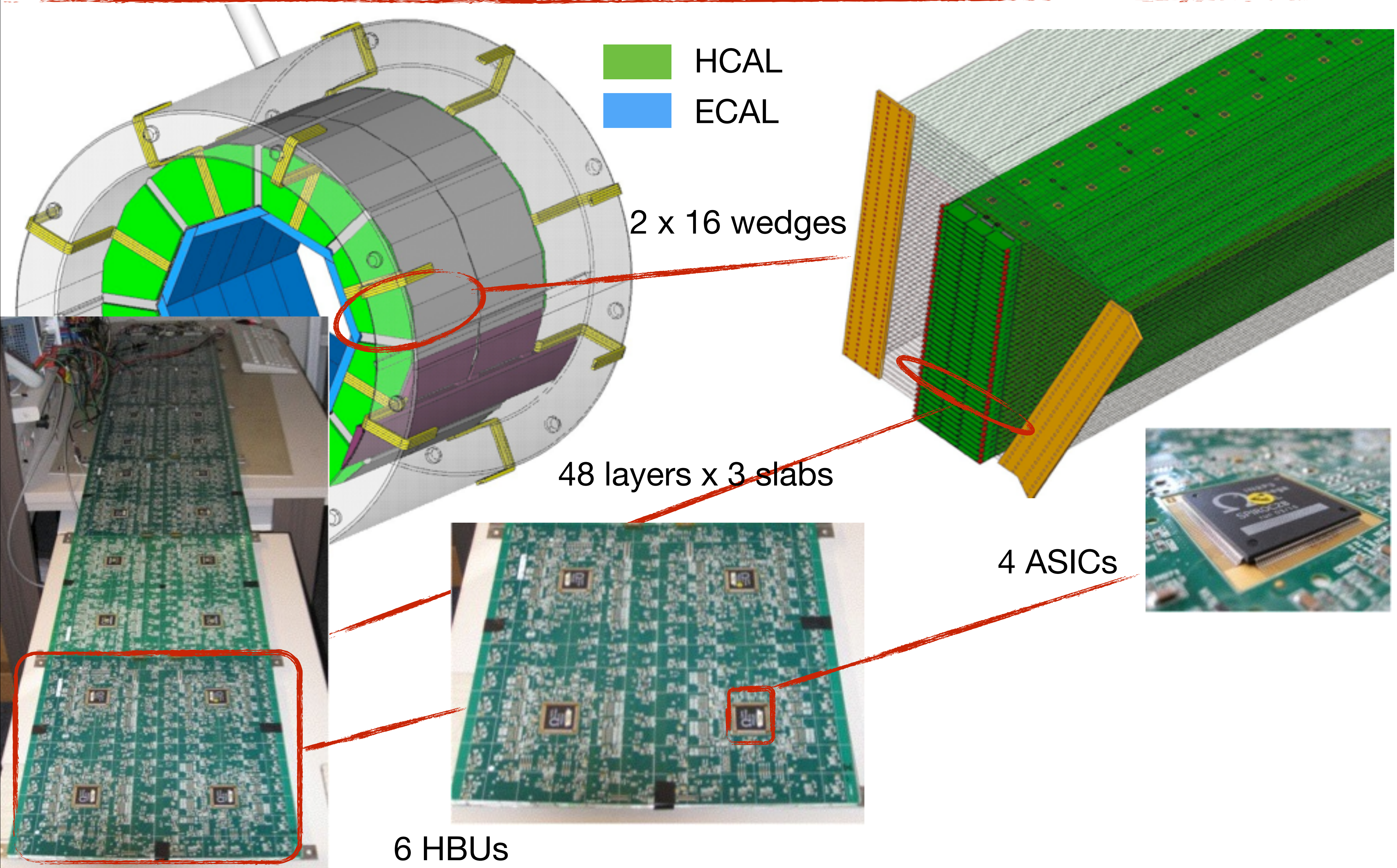

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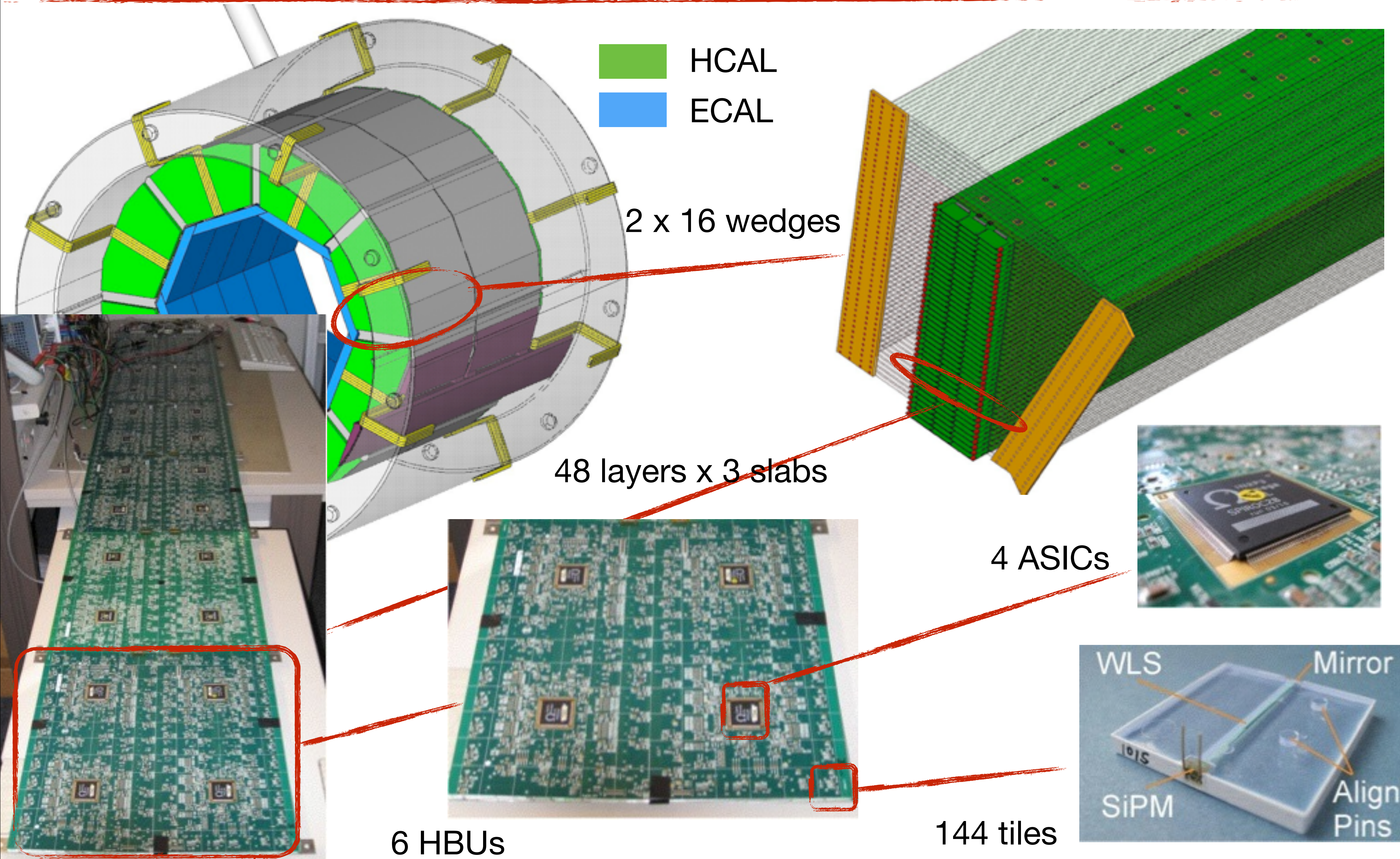
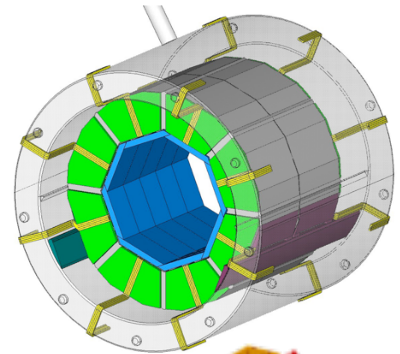


The Active Elements

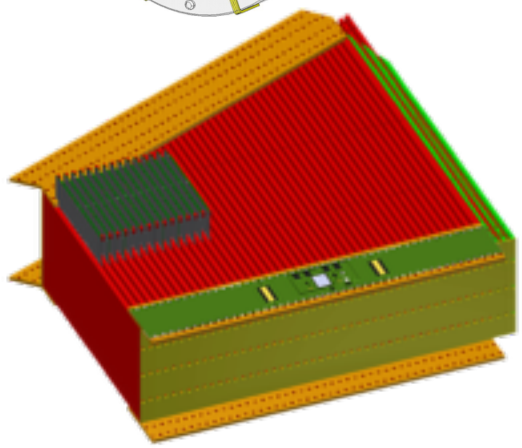
- From the generation of the signals and the detection of the photons to signal processing and acquisition

The Challenges of Large Numbers

- 1 calorimeter
  (barrel + 2 end-caps)

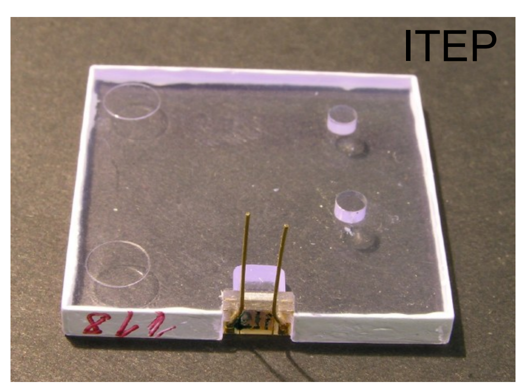


- 60 sub-modules



- 3 000 layers

- 60 000 HBUs
- 200 000 ASICs
- 8 000 000 Tiles + SiPMs



- 1 working year
- 46 weeks
- 230 days
- 2 000 hours
- 100 000 minutes
- 7 000 000 seconds

The Photon Sensor

- The CALICE AHCAL was the first large-scale use of SiPMs!

  … and the technology has evolved quite a bit since then - now used “everywhere”, with many possible producers.

- What we need:
  - Decent efficiency
  - Reasonable noise rate
  - Reasonable dynamic range
  - Low cost

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Packaging is important:
- Compactness to reduce dead area
- Long-term stability of materials (on the level of decades!)
- Robustness for installation / storage before further assembly
- ▸ Need experience with producers (and experienced producers! - Bad surprises recently)

Photon Sensor: Noise Limits

- The requirements change substantially when moving to realistic detectors: Auto-trigger - Have to avoid accidental signals at the ~ 0.2 - 0.4 MIP level! (no problem with external beam trigger, of course…)

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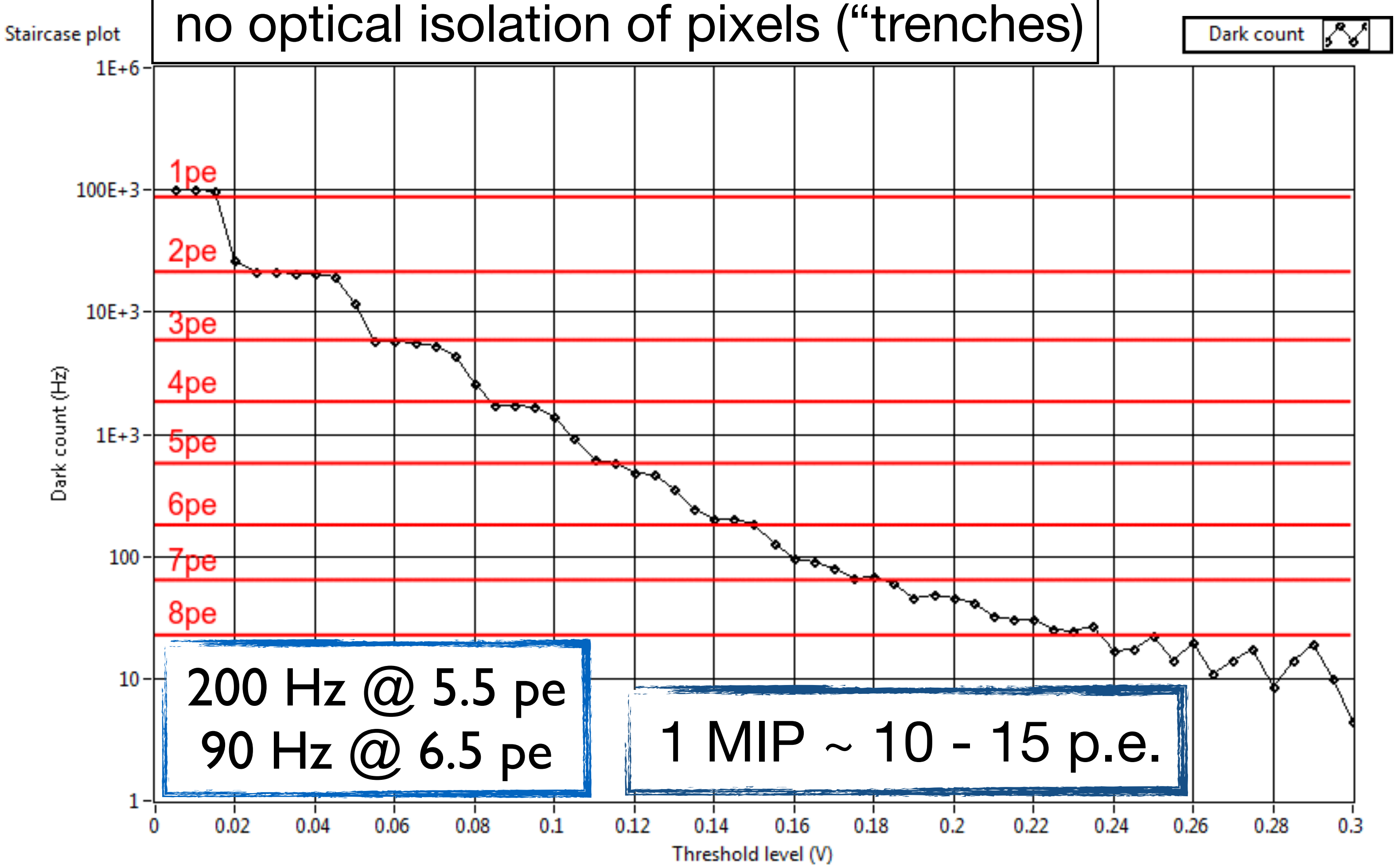

MPPC cross-talk level:
~ 25% - 30%

KETEK PM1125, with "trenches"
(used at UHH)
cross-talk level: ~ 5%
results in 0.1 Hz noise rate
at 0.2 MIP with UHH tiles

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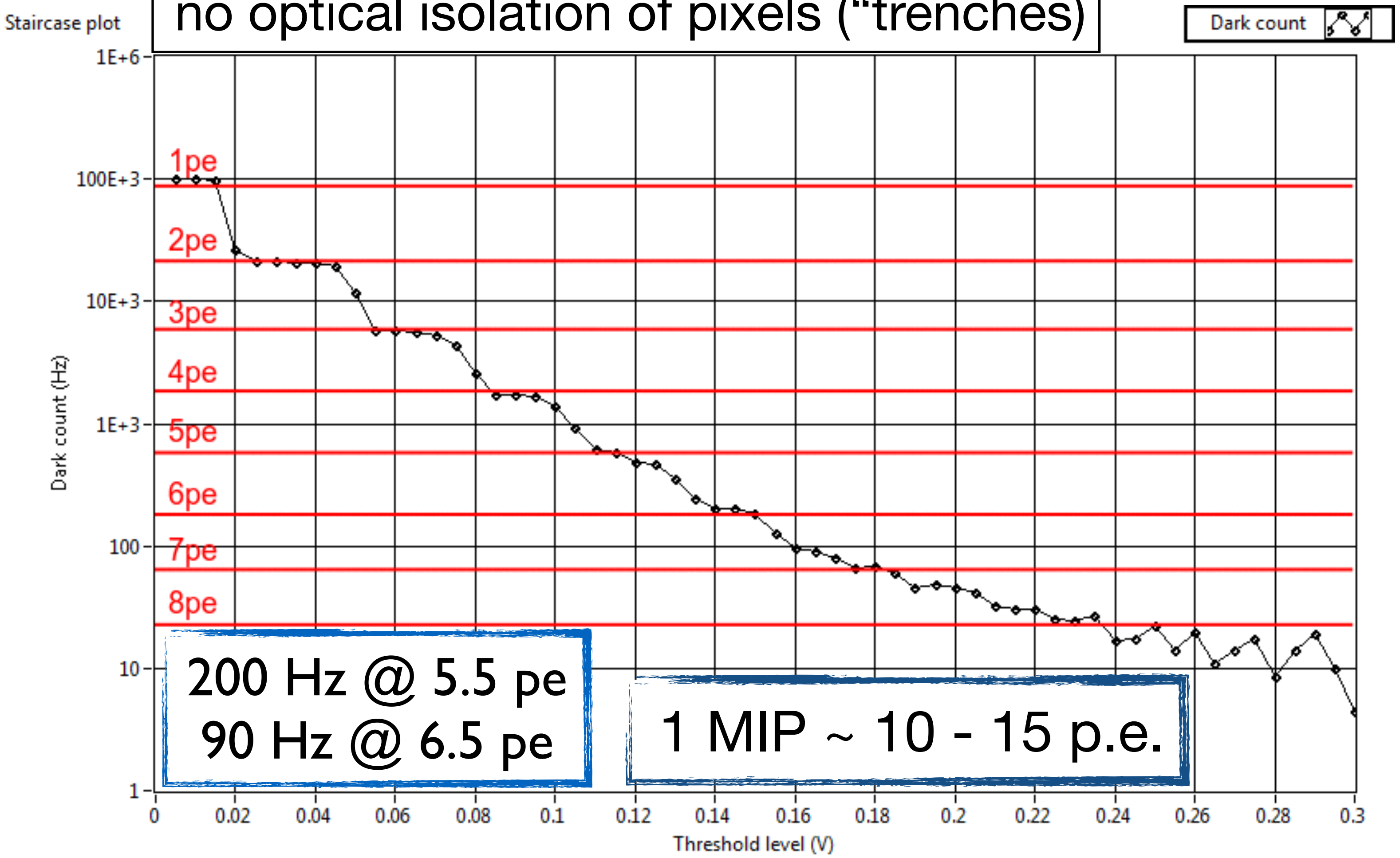

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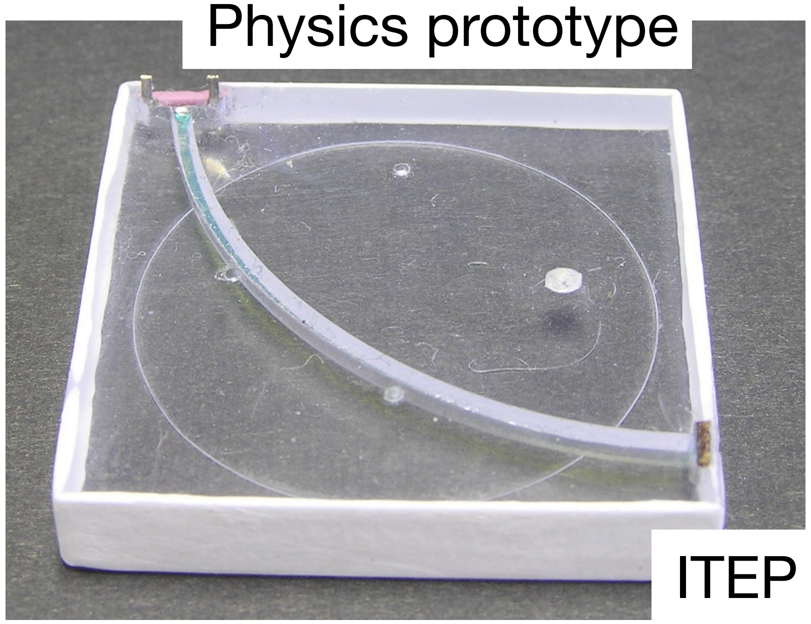
NB: Cross-talk depends on operating conditions. Impact depends on active area of sensor!

The Scintillator Tiles

- The smallest “building block” of the Calorimeter (with integrated SiPM) - Mass production and mass testing important!
  - Has undergone quite some evolution since first prototype:

Physics prototype



ITEP

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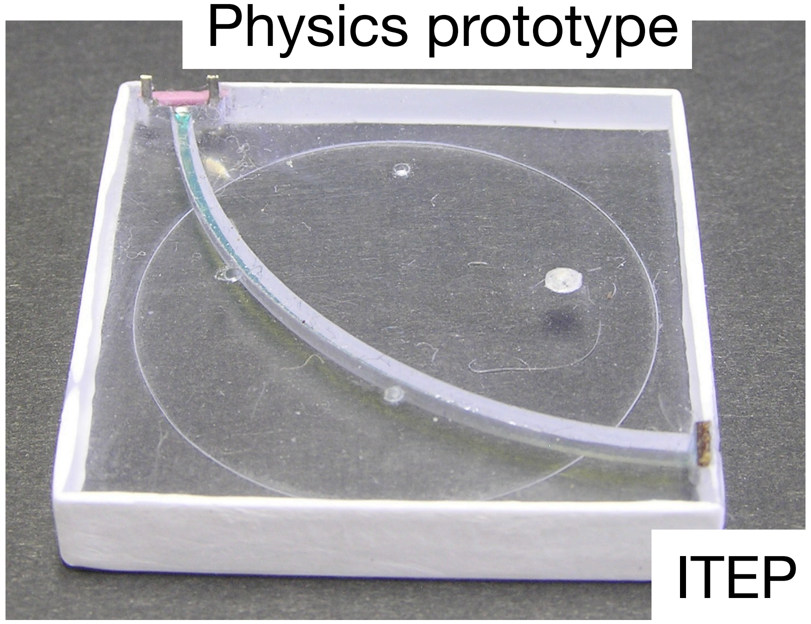
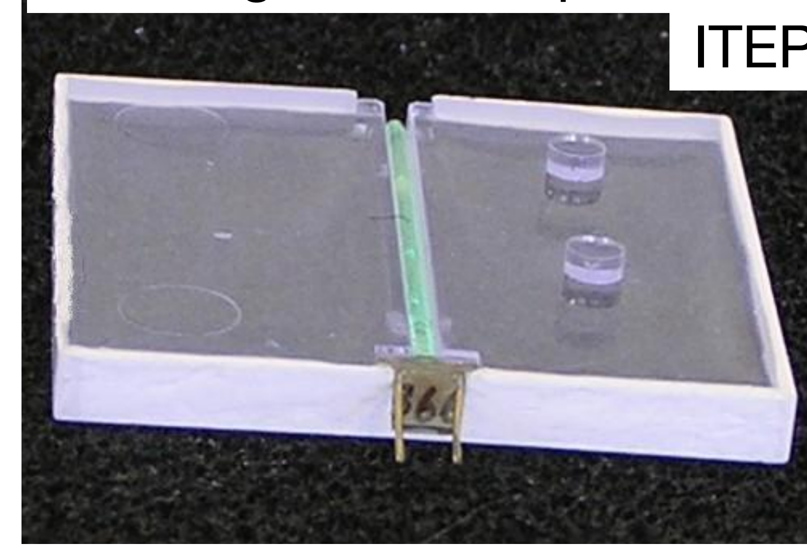


ITEP

easier tile assembly, mounting pins for placement on HBU

1st design for tech. prototype



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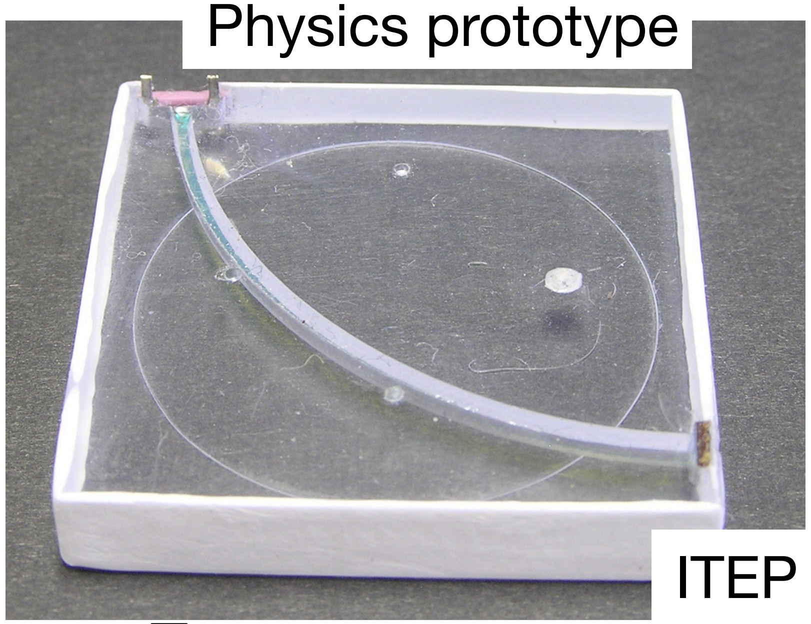

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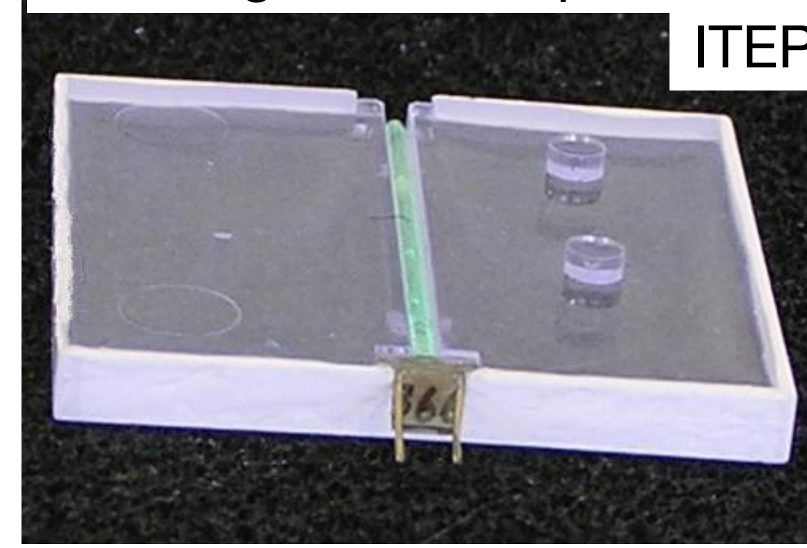
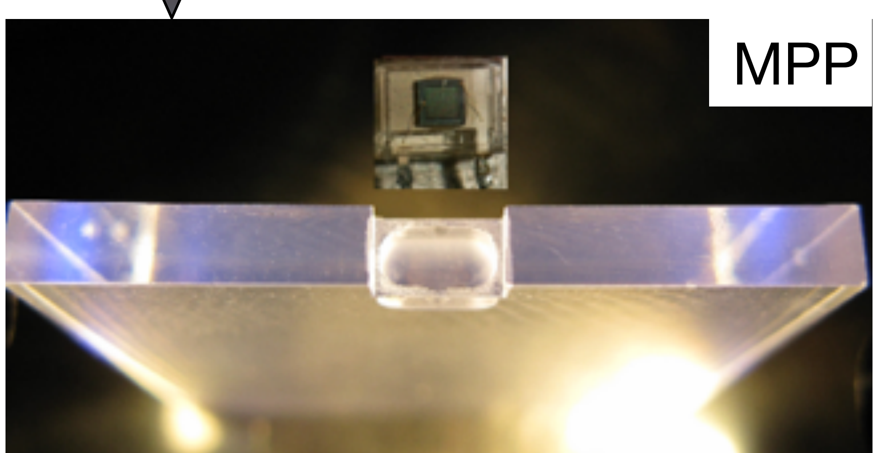


ITEP

fiberless coupling: easier manufacturing, increased tolerances



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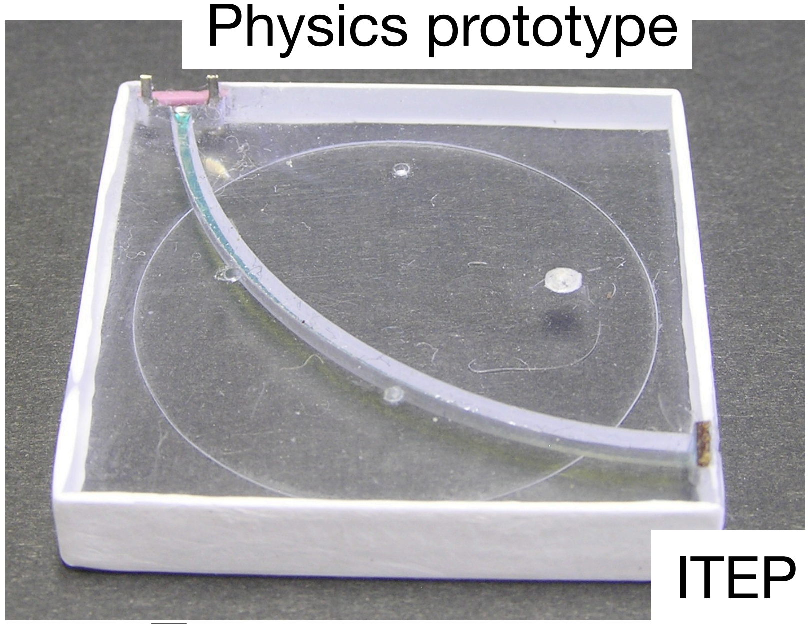

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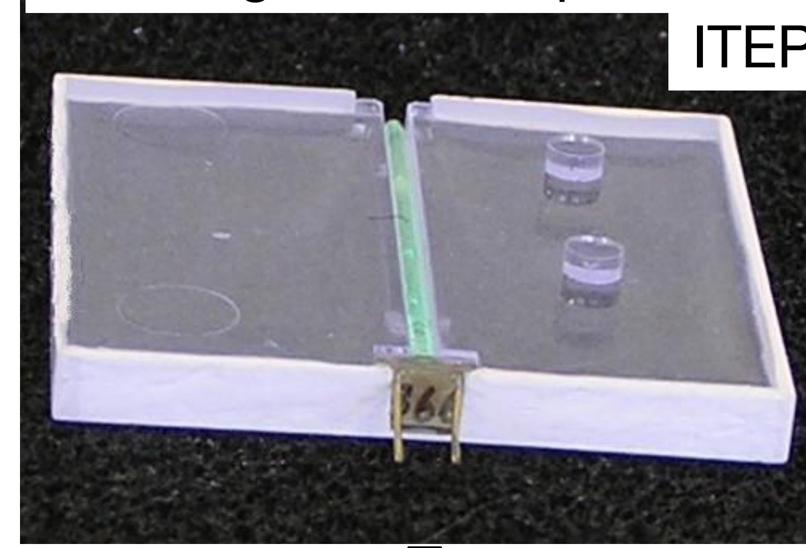

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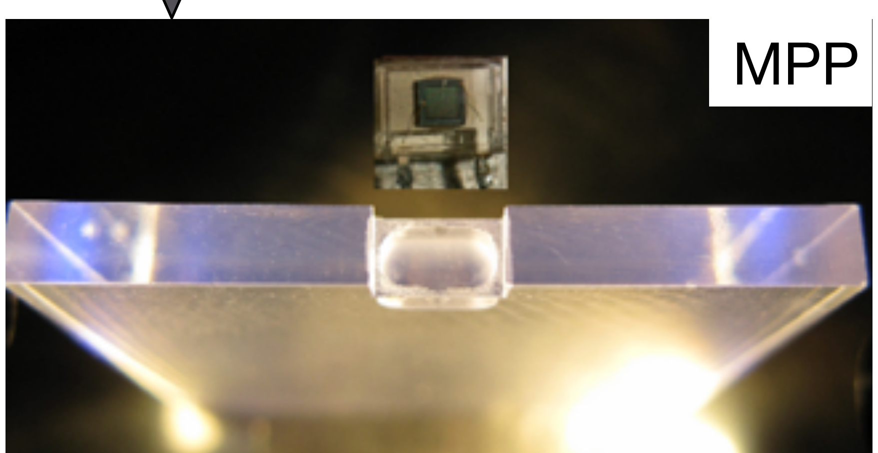
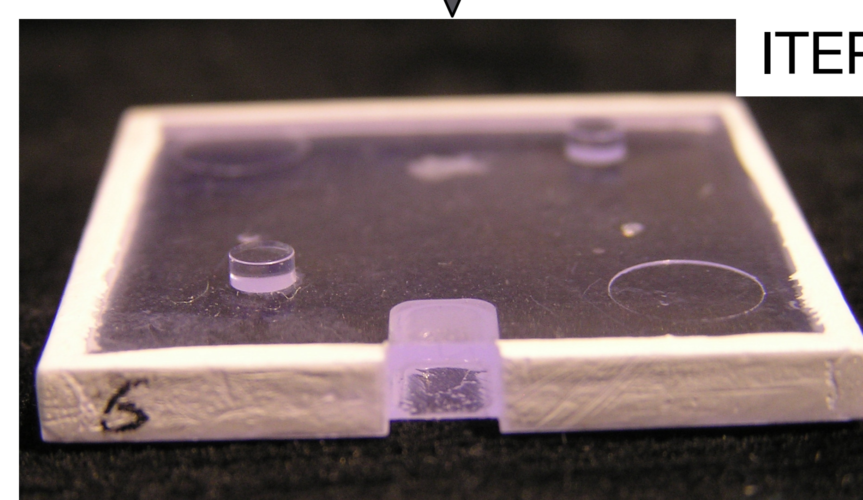
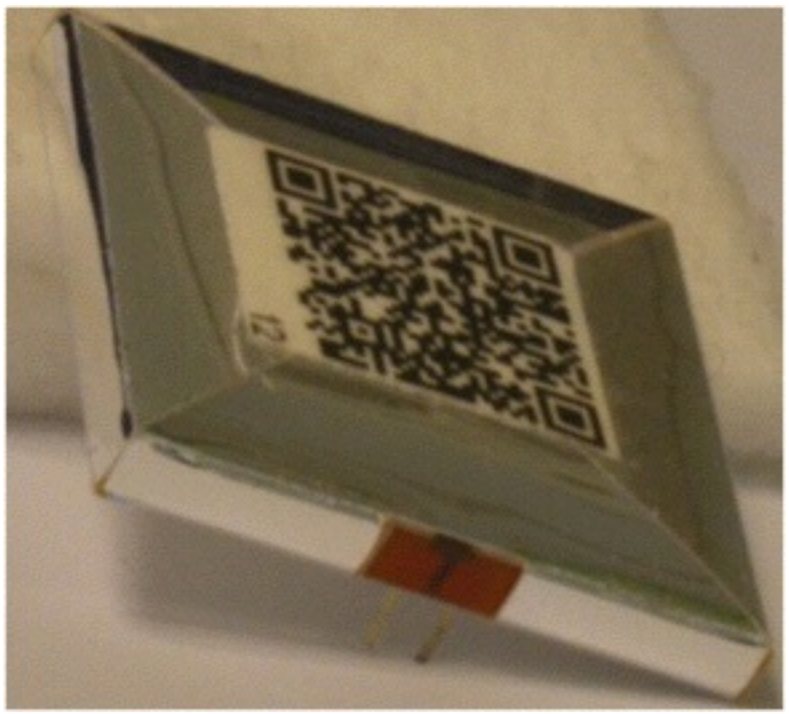
proof of principle: fiberless coupling, injection molding

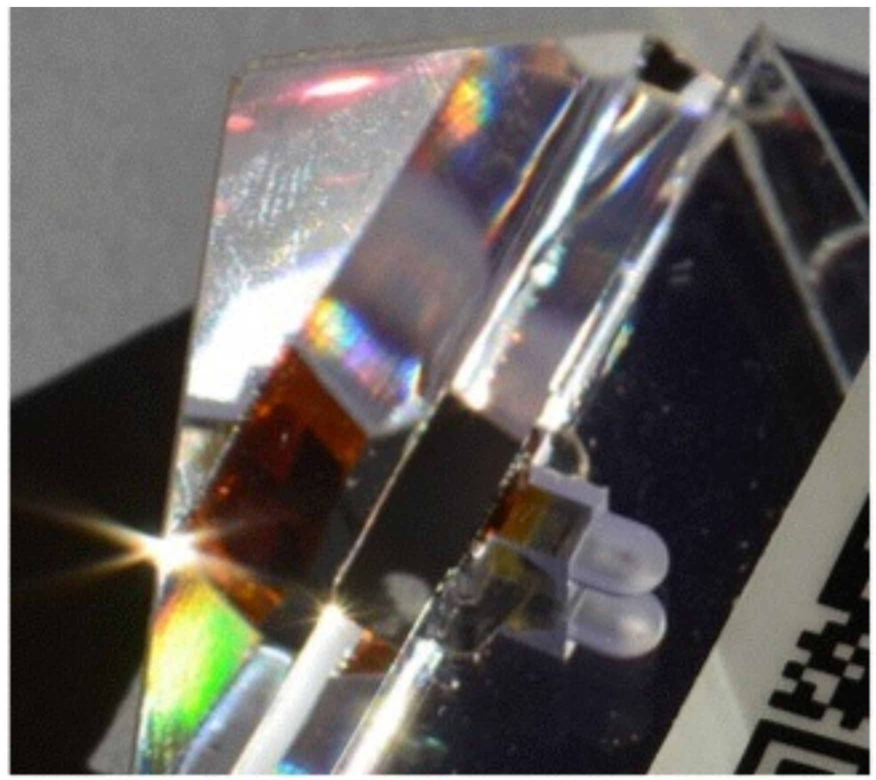




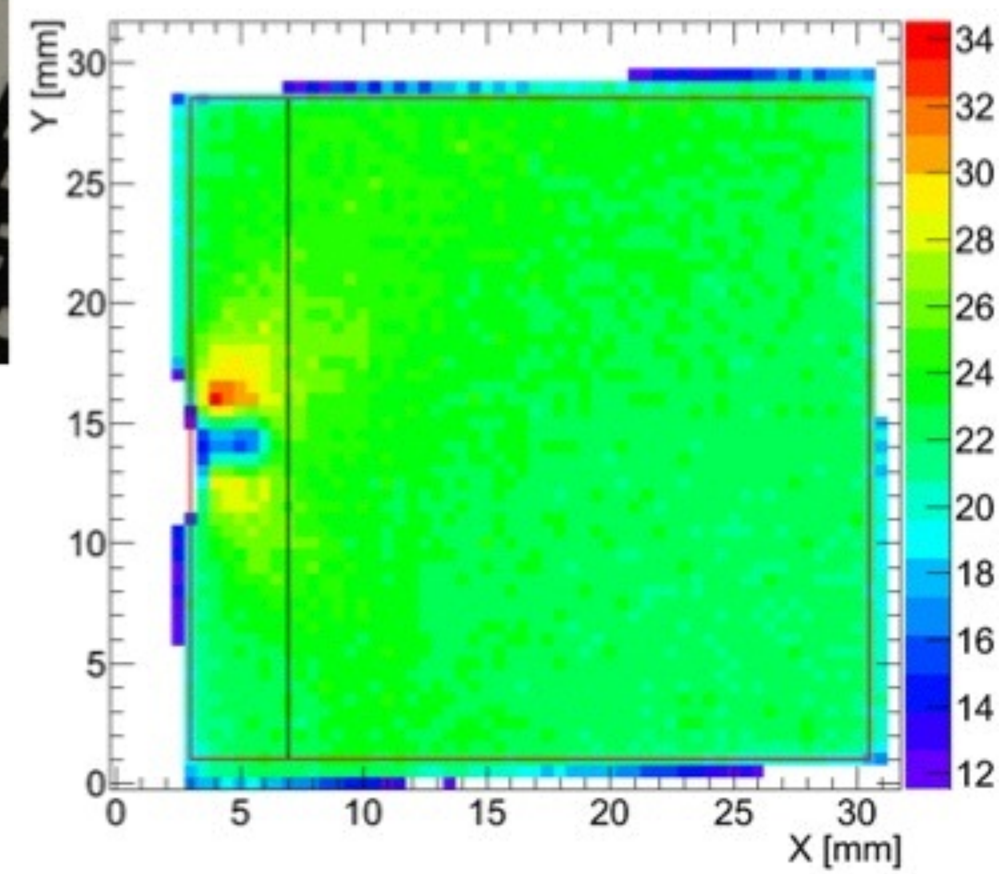
Large-Scale Tile Productions…

- Larger batches (several 100) of fiber and fiberless tiles have been produced at ITEP
- Ongoing production at UHH -> machining with slightly adapted MPP design
  - semi-automatic packaging of tiles in laser-cut (non-adhesive) reflector foil



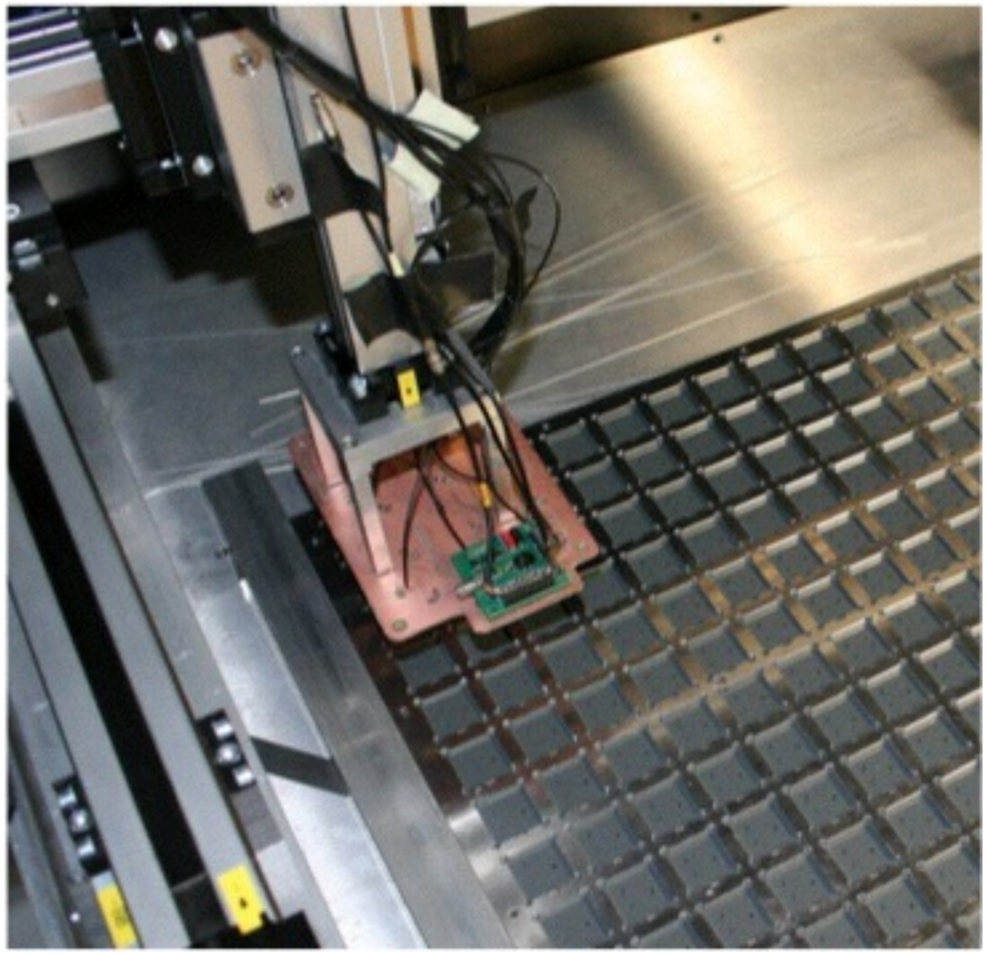


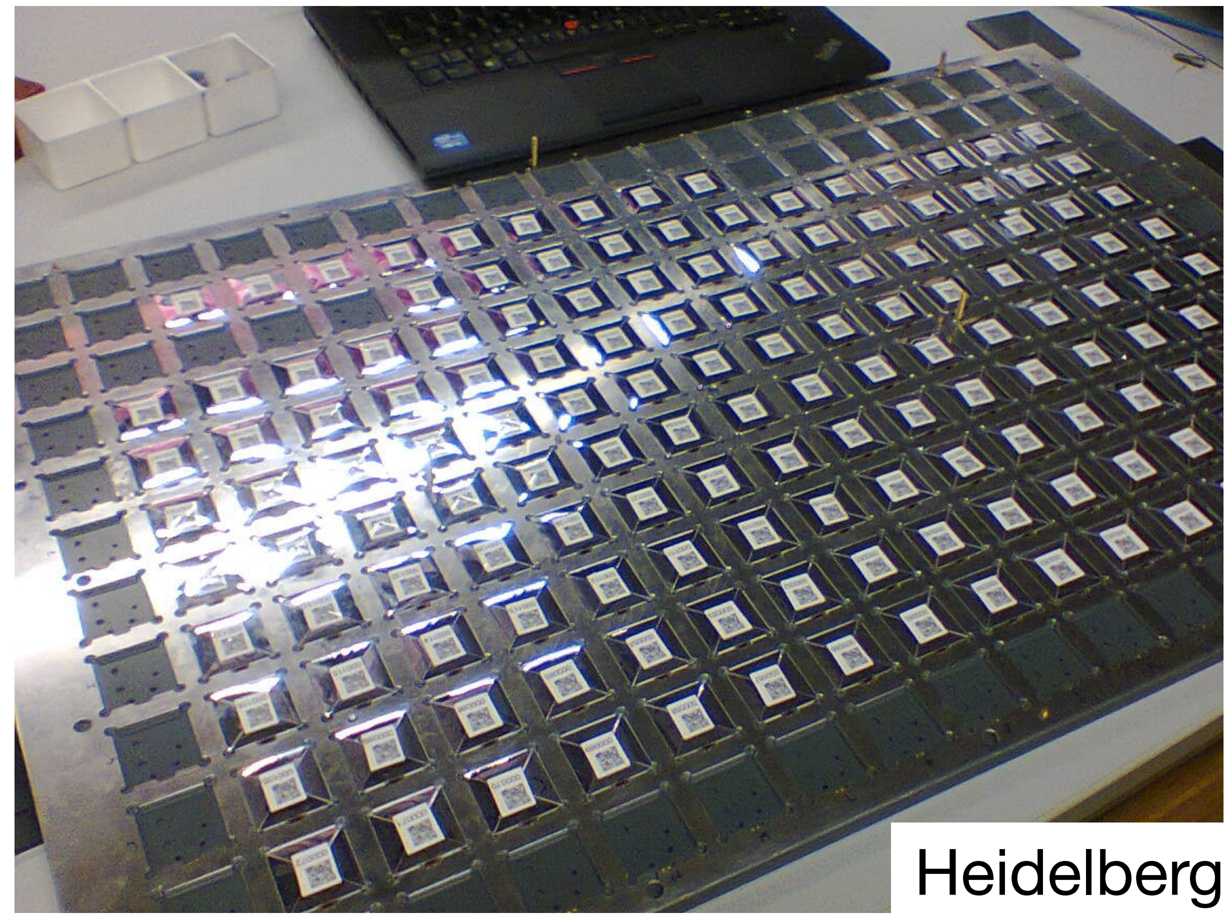
- New generation of KETEK SiPMs: High light yield
- High degree of response uniformity



… and large-scale Testing

- Fast testing of tiles prior to installation - basic functionality test with LED (measure gain, cross-check light collection from tile)





- Several 100 tiles already tested - currently with 15 point voltage scan
  - ▸ 2 minutes for 12 tiles (measured in parallel), then repositioning of head

Automated Assembly

- Large number of tiles require automatic assembly of full HBUs
  - ▸ Requires precise placement of Tiles with SiPMs in HBU boards, followed by soldering

Challenge 1: Placement precision and tolerances

- ▸ Higher stability expected w/o alignment pins: Precise placement of SiPM pins, tile fixed by fast-curing glue put on board via screen printing prior to tile placement

extensively studied at Mainz

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Challenge 2: Soldering of pre-assembled and heat-sensitive components

- Have to avoid detachment of HBU SMD components, heat damage of tiles

▸ Two options to study
  - Selective (point-by-point) soldering - disadvantage: rather slow, can be sped up by multi-point head, would profit from symmetric soldering positions
  - Wave soldering - fast, but heats up everything: Needs thermal protection mask, special requirements for clearance between tile solder points and components

extensively studied at Mainz

Re-thinking the Tile Design

- Current default approach: SiPM + Tile form a unit - Requires complex assembly

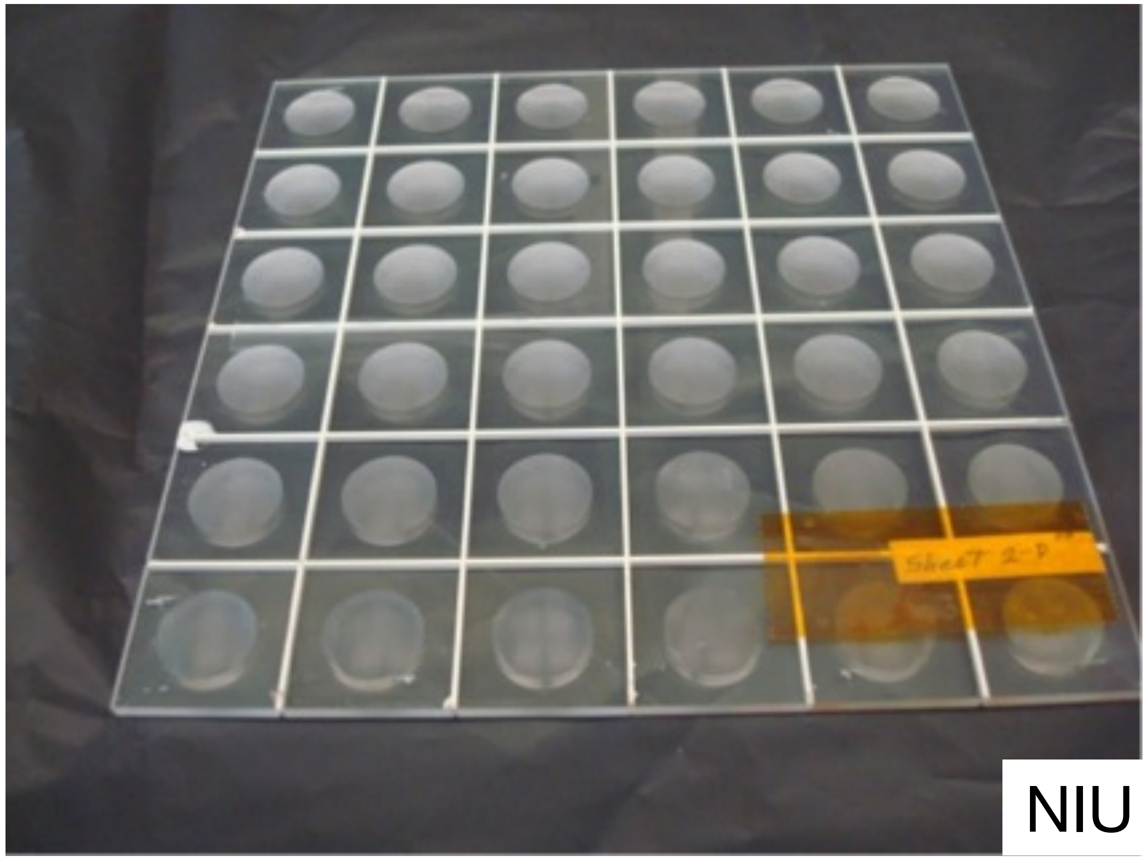
▸ Alternative: SiPMs on electronics, tiles coupled via bottom - avoids soldering with tiles

Proven to work with the first design of directly coupled tiles from NIU:

▸ Adaptations now studied at ITEP and Mainz

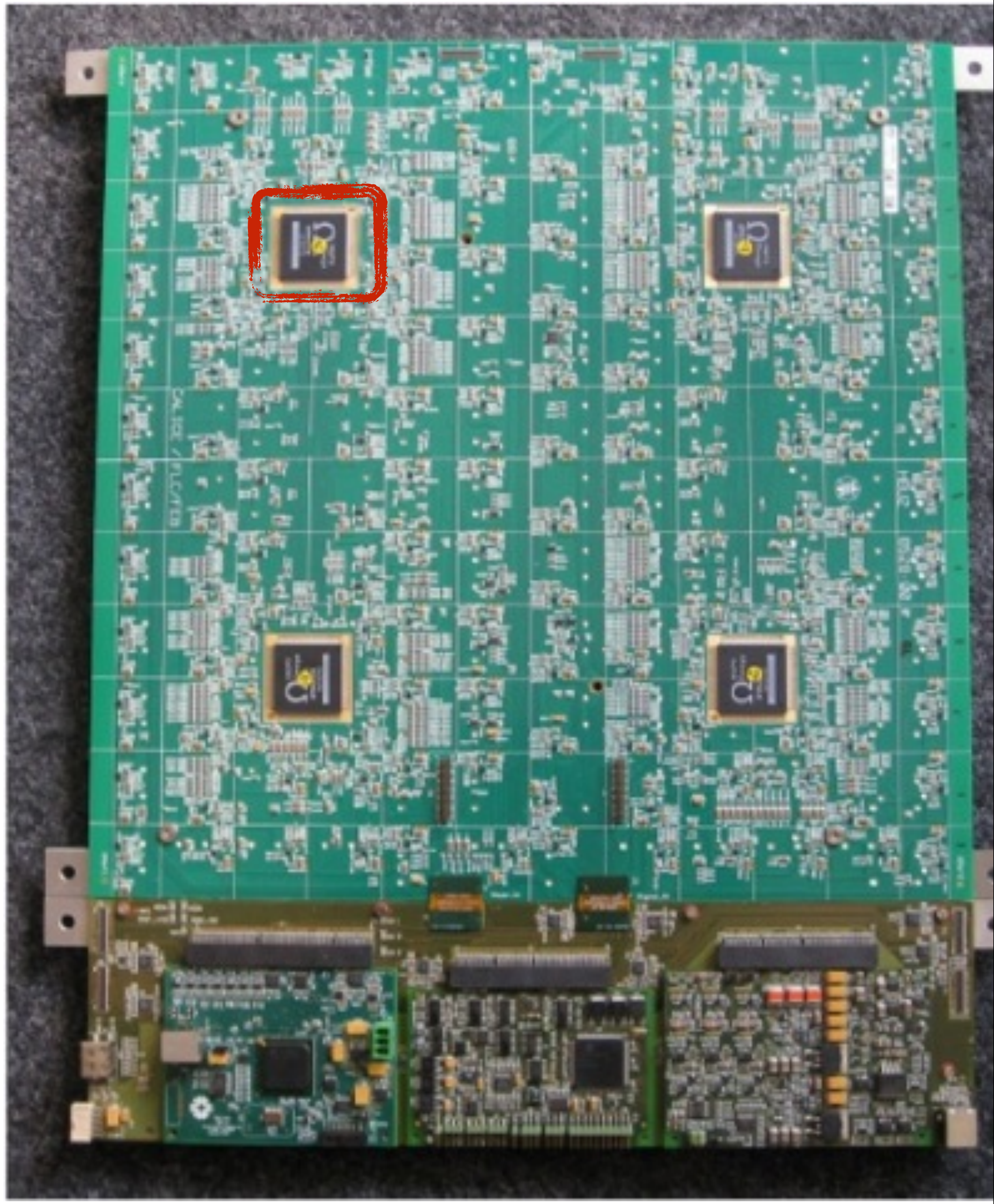
Challenges: MIP signal amplitude (can be overcome with larger SiPMs) and uniformity - Proven to be good with large dimple

- More radical approach: Megatiles - Reducing the number of individual units by ~ 2 ordes of magnitude
  - Requires concepts for light isolation between cells - and an assessment of the potential impact of light cross-talk


NIU

Reading It Out…

- Need a versatile front-end chip
  - sub-p.e. resolution for calibration, large dynamic range for sub-MIP to > 100 MIP signals
  - ns - level time stamping (background rejection for CLIC, exploit time structure in clustering, …)
  - Cell-by-cell auto-trigger: Triggerless readout
  - Powerpulsing: Compact layer!
  - SPIROC ASIC - Alternative analog part: KlauS, ADC currently being developed



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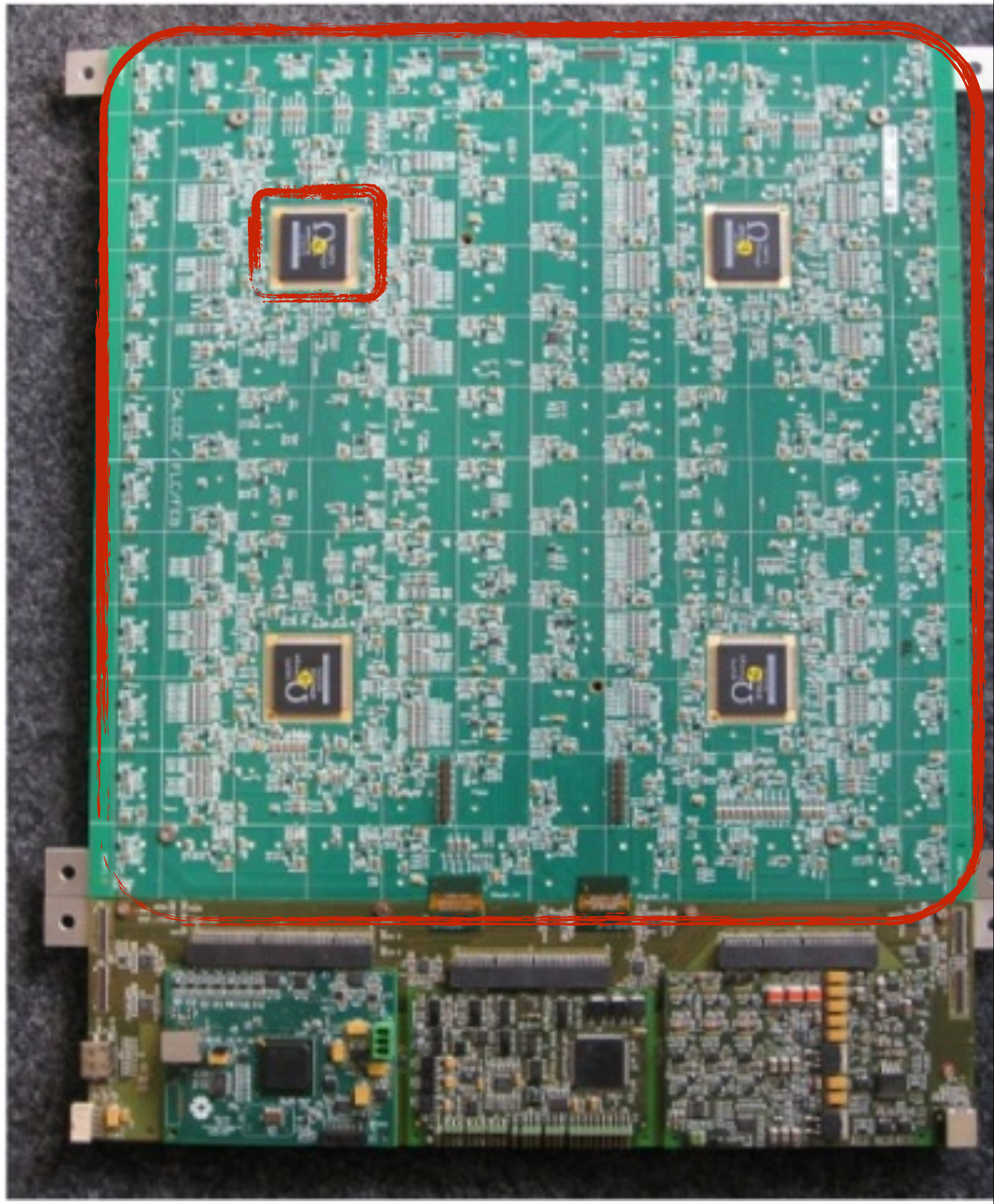
- 1 HBU - 4 Chips, 144 channels, including calibration LED for each cell



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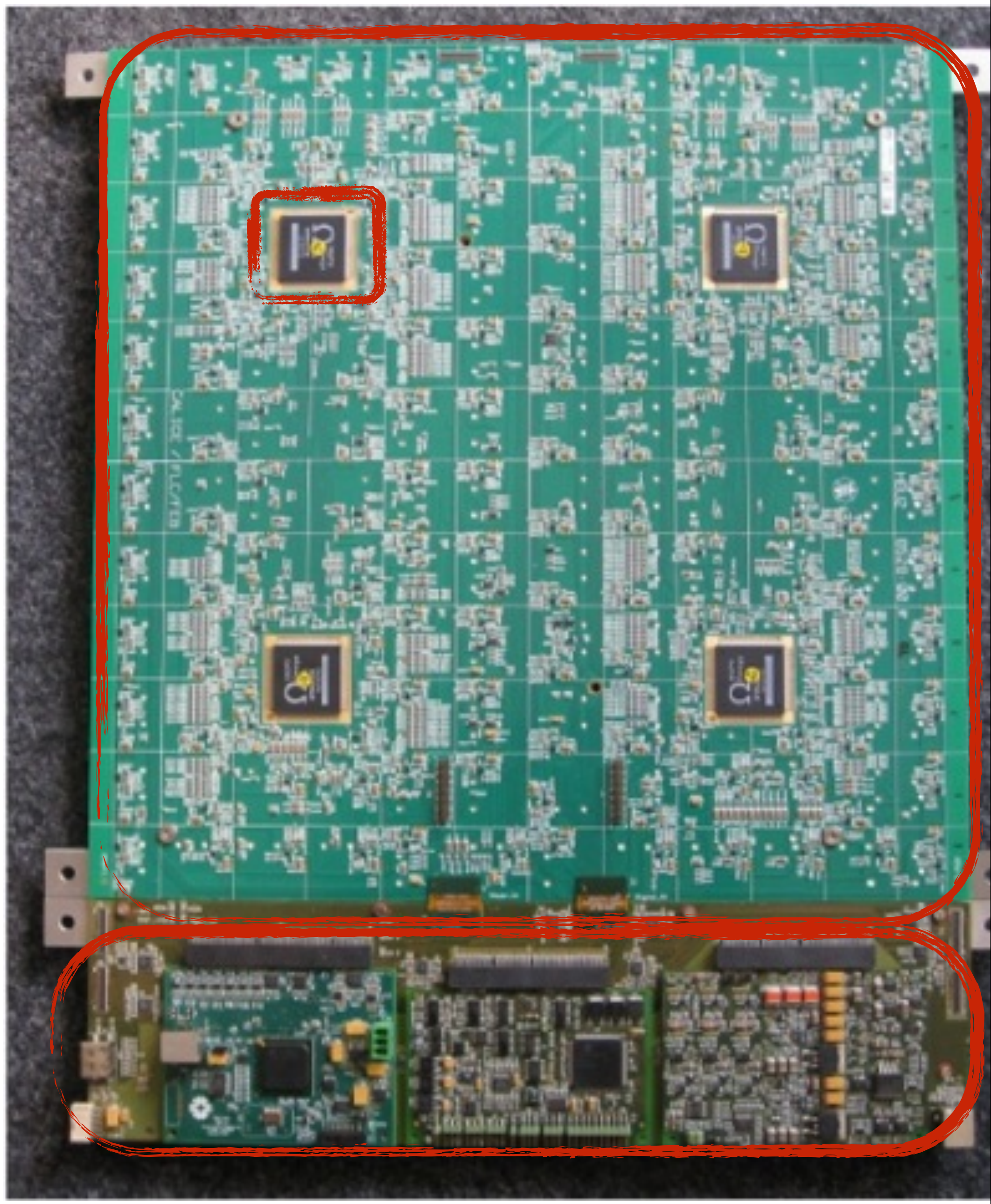
- 1 HBU - 4 Chips, 144 channels, including calibration LED for each cell
- Control of a full layer (3 x 1 string of up to 6 HBUs): Control & Interface Board CIB
  - DAQ Interface
  - Calibration and trigger controller
  - Power



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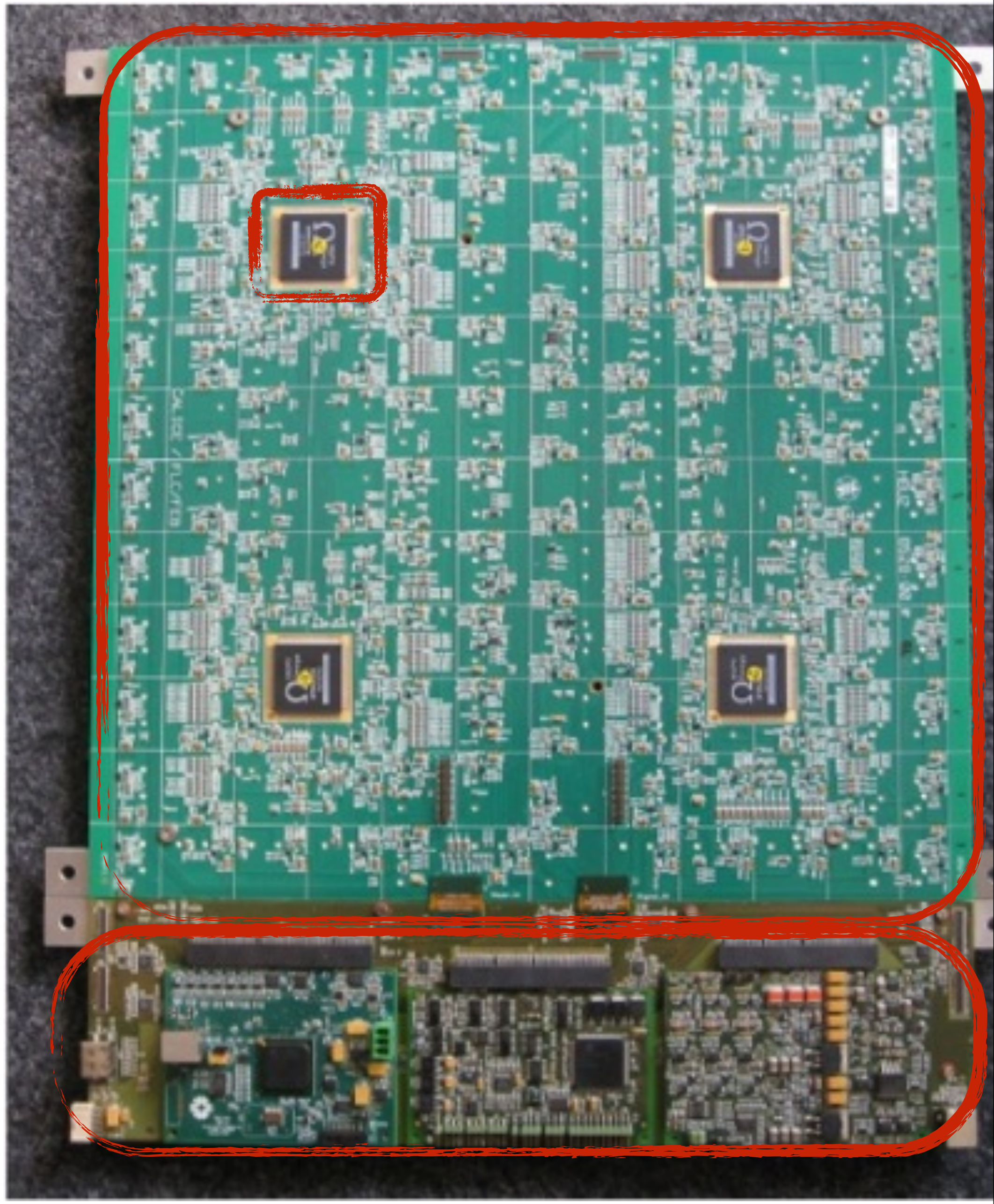
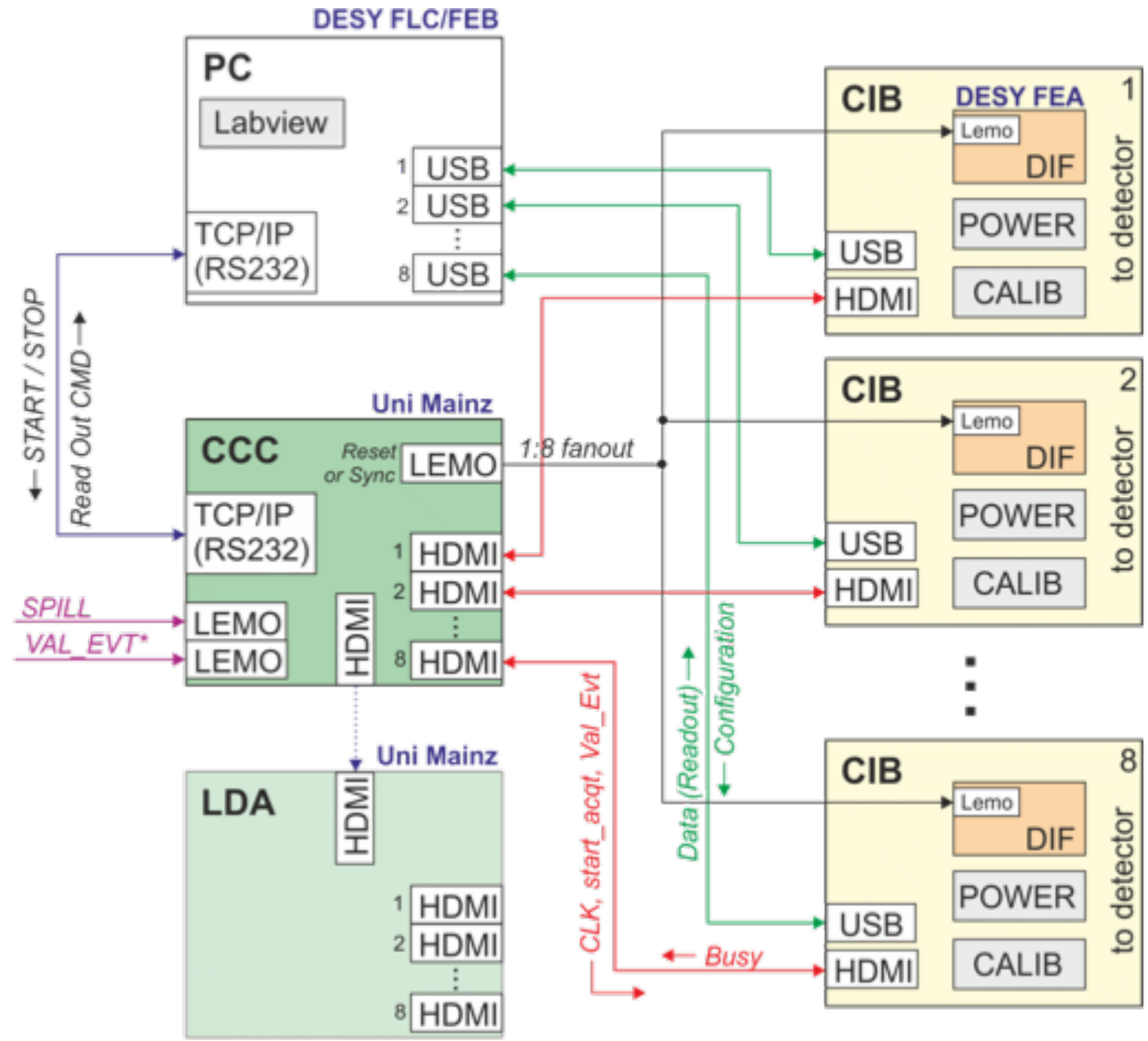
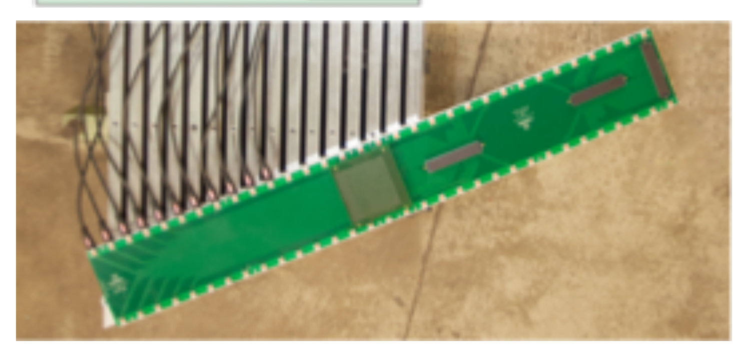


Identical requirements for scintillator ECAL - with x2 higher channel density: More complex PCB layout, same functionality

… and getting it on Tape

- Complete, flexible system:
  - can integrate other CALICE calorimeters
  - provides possible starting point for full experiment DAQ
  - Based on original CALICE DAQ, further development of second-generation DAQ
- DAQ Interface: DIF - part of CIB
- Fist signal distribution: CCC
- Data aggregation: LDA





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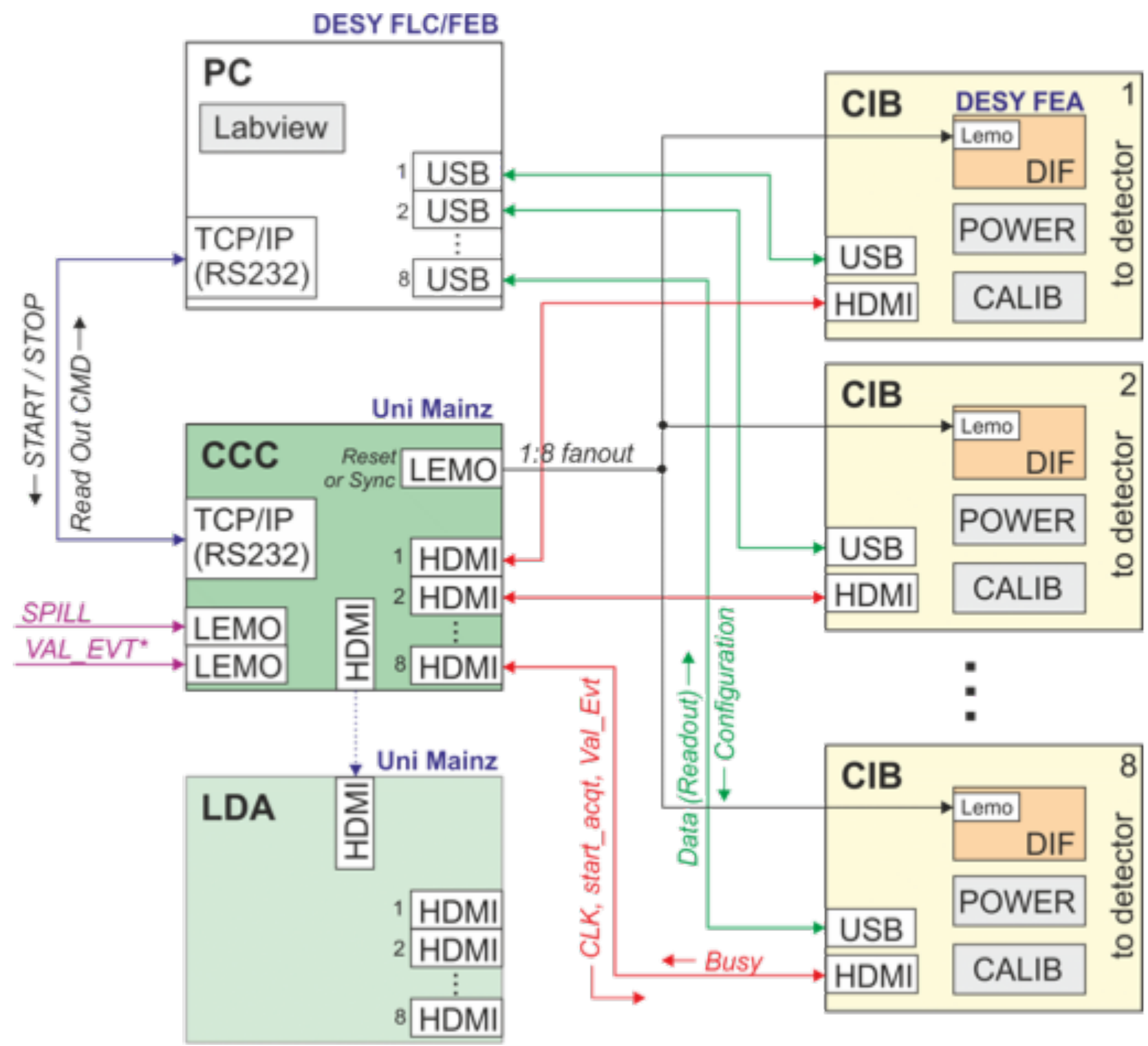
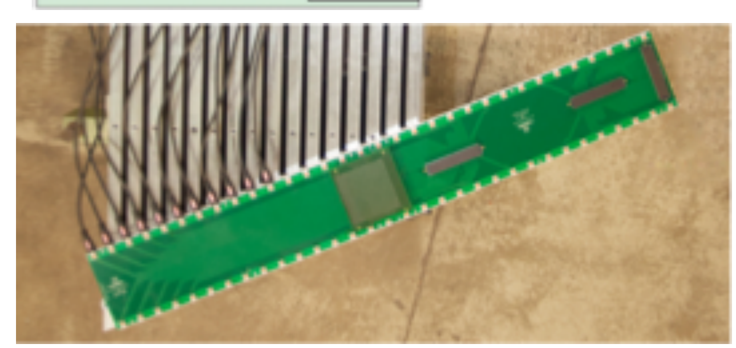


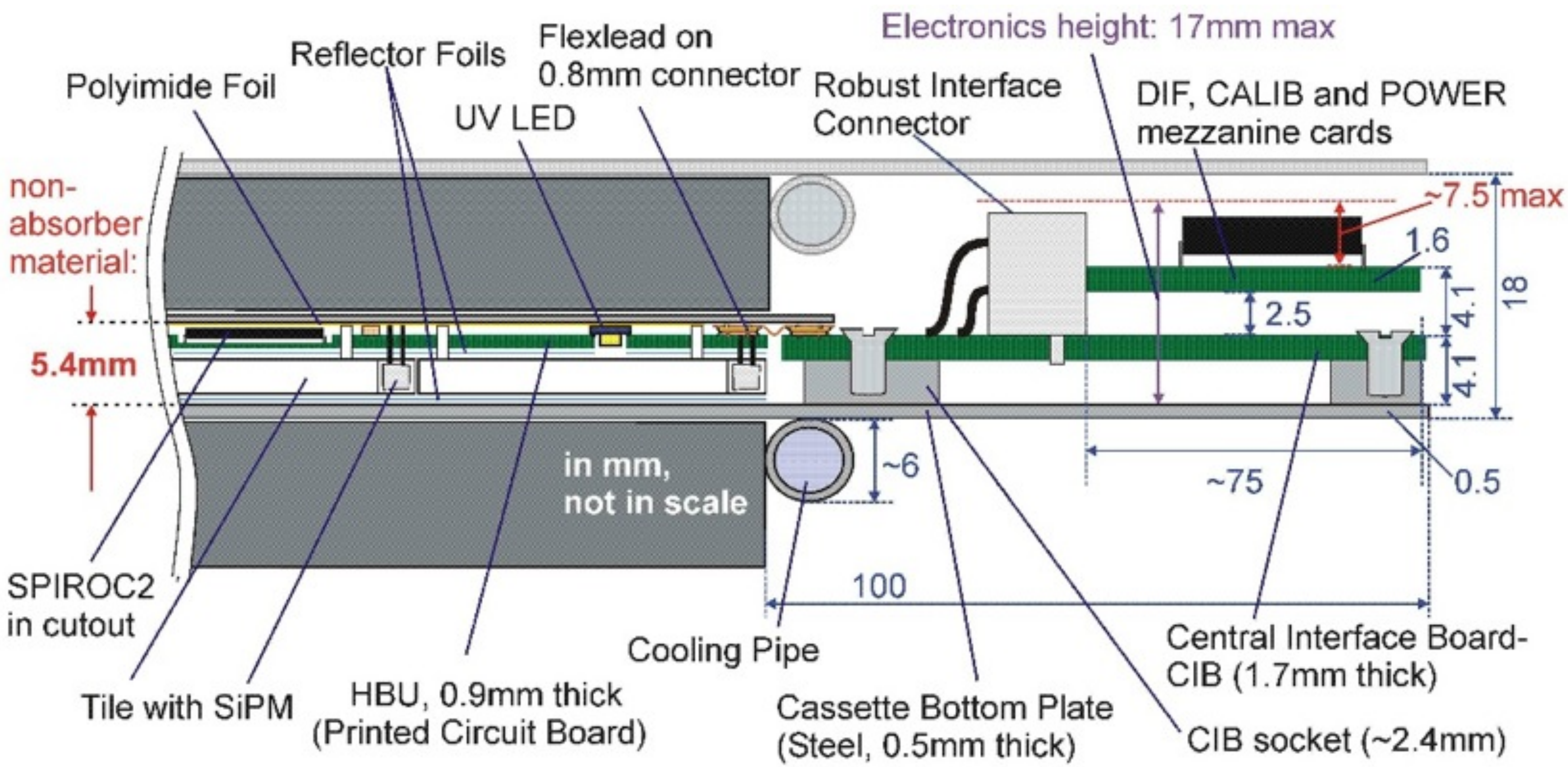
Successfully used for single and multiple HBUs, stepwise development to full scale ongoing



The Mechanics

- The absorber structure - provides the mechanical structure of the calorimeter, support for other detectors and the housing of the readout hardware

Overview

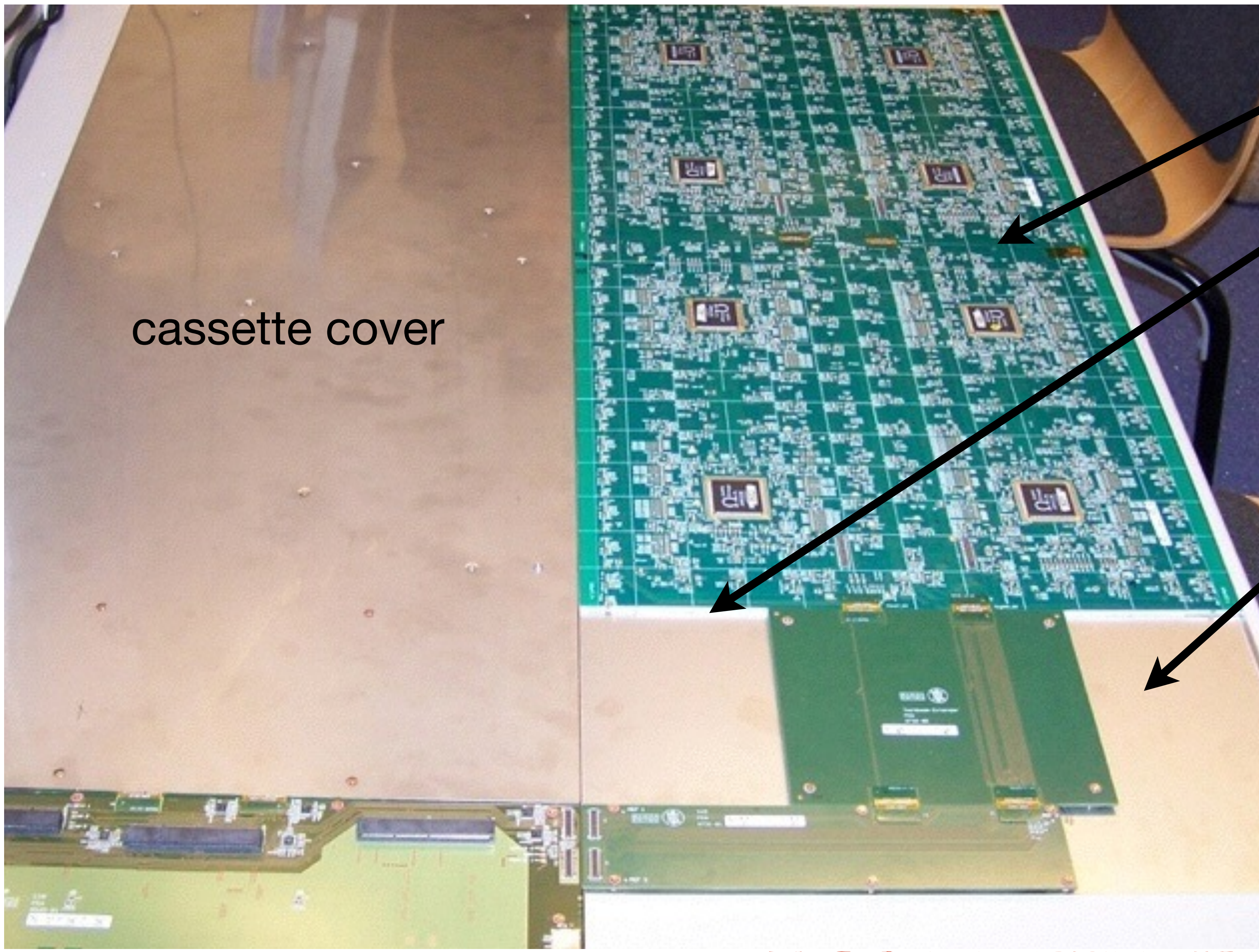


- Total absorber material per layer: 20 mm - 1 mm out of this in top and bottom plates of cassettes housing electronics + scintillator
- Key for maximum compactness: As little as possible non-absorber material: thin electronics, small tolerances, compact construction

Cassettes

- Provide mechanical stability and protection to HBUs with tiles - Creates insertable readout layers

  Proof of principle: Cassettes for technological prototype - designed at DESY, manufactured at Munich using precision welding



integrated electronics

scintillator tiles (3 mm thick)

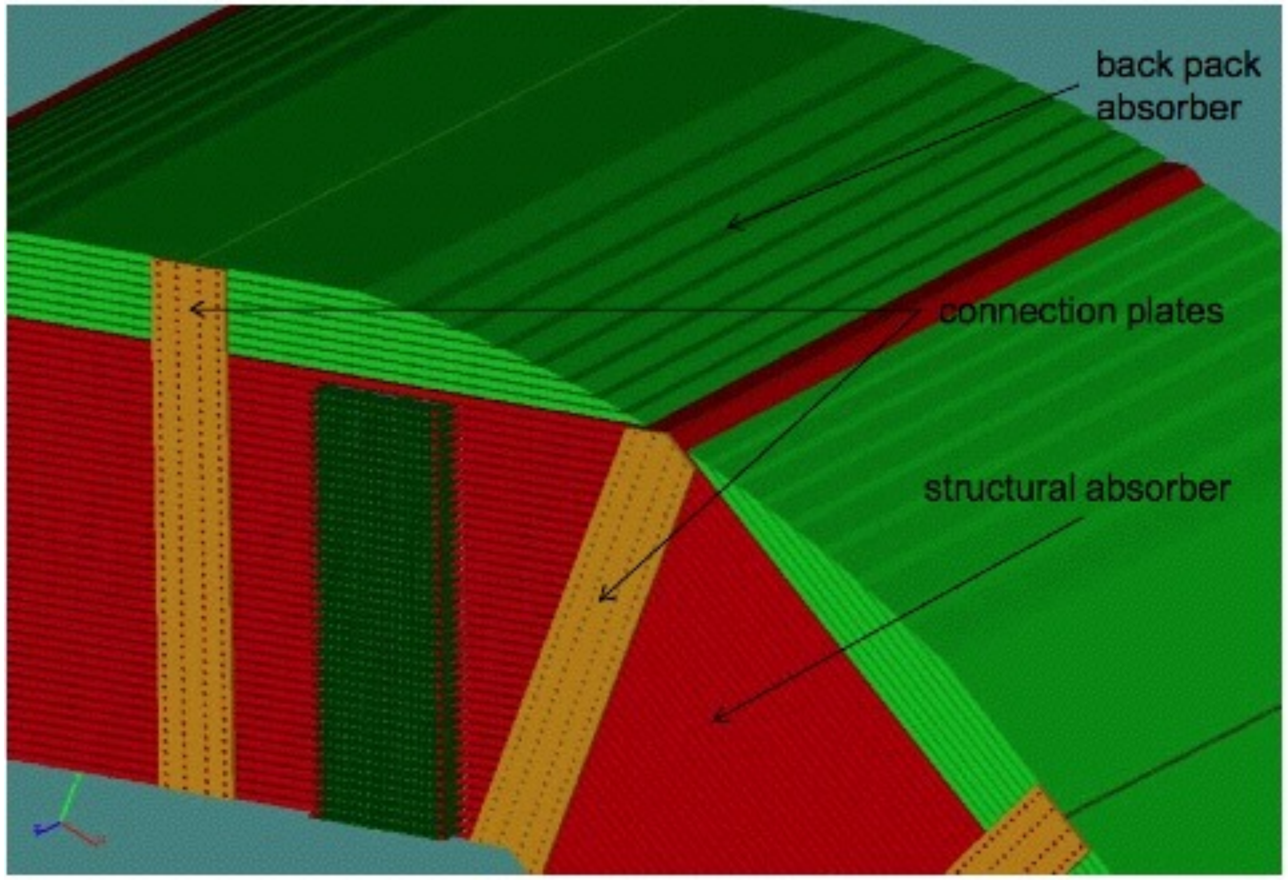
cassette base with precision pins

4.5 mm

Total thickness of unit:
6.5 mm (incl. 1 mm steel)

Absorber Structure

- Octagonal structure, 19 mm thick stainless steel plates



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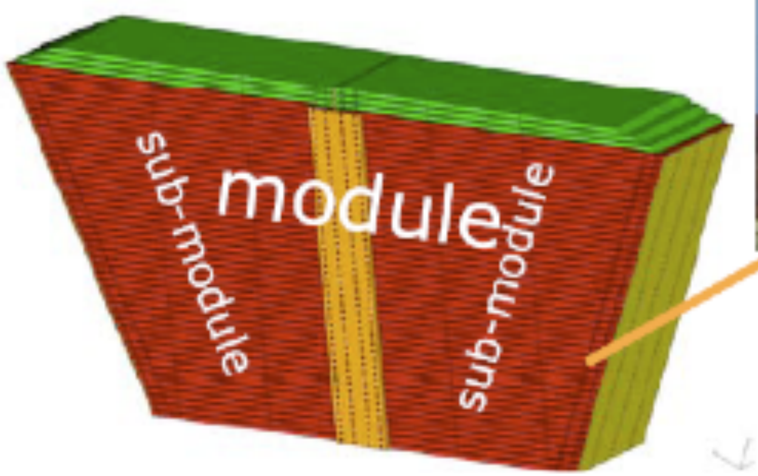


Prototypes:

- one HBU-deep full 48 layer stack
- full size 4-layer unit

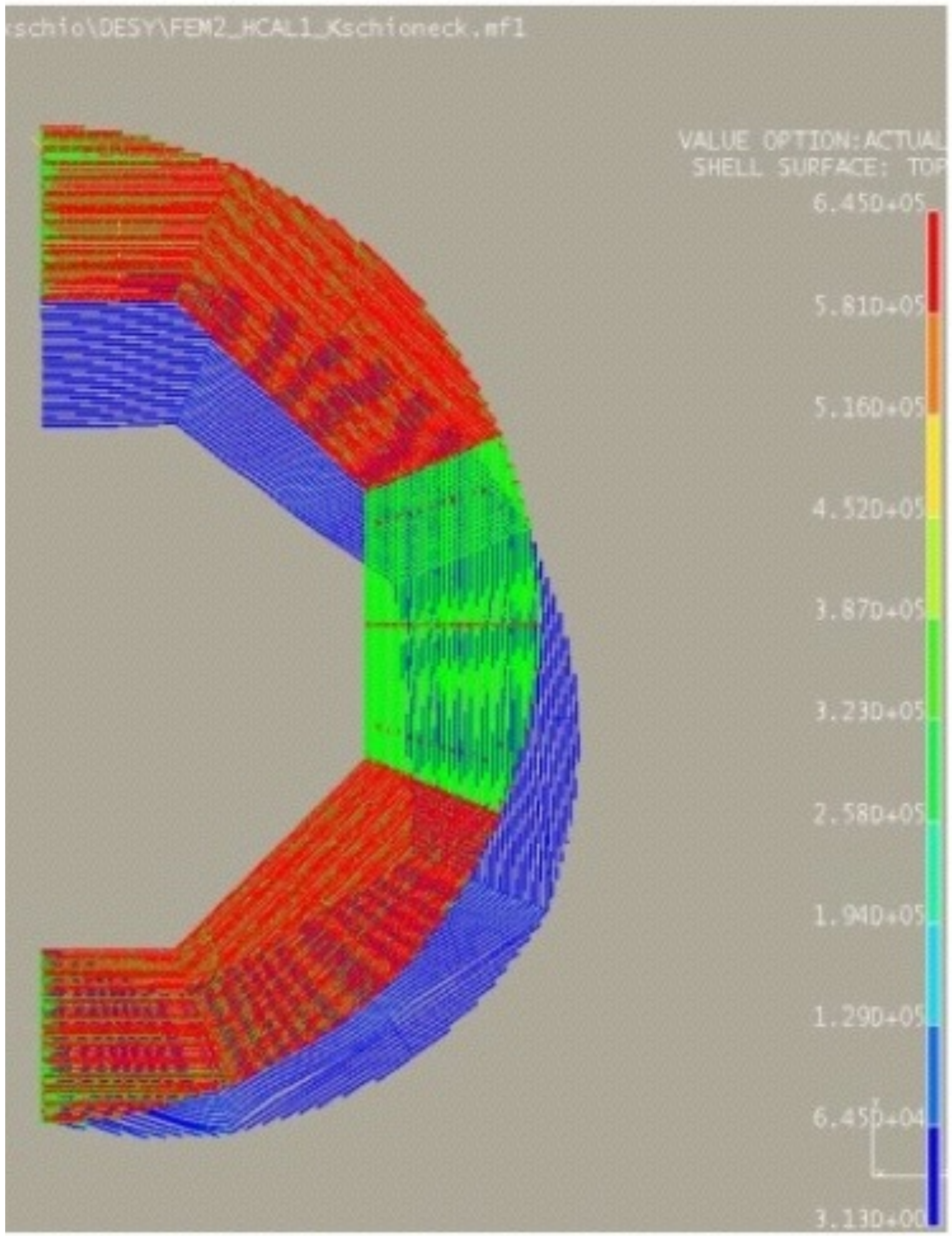
Steel plates from manufactures are far from the flatness requirements

- Flatness better than 1 mm over full length reached with roller levelling - substantially cheaper than machining

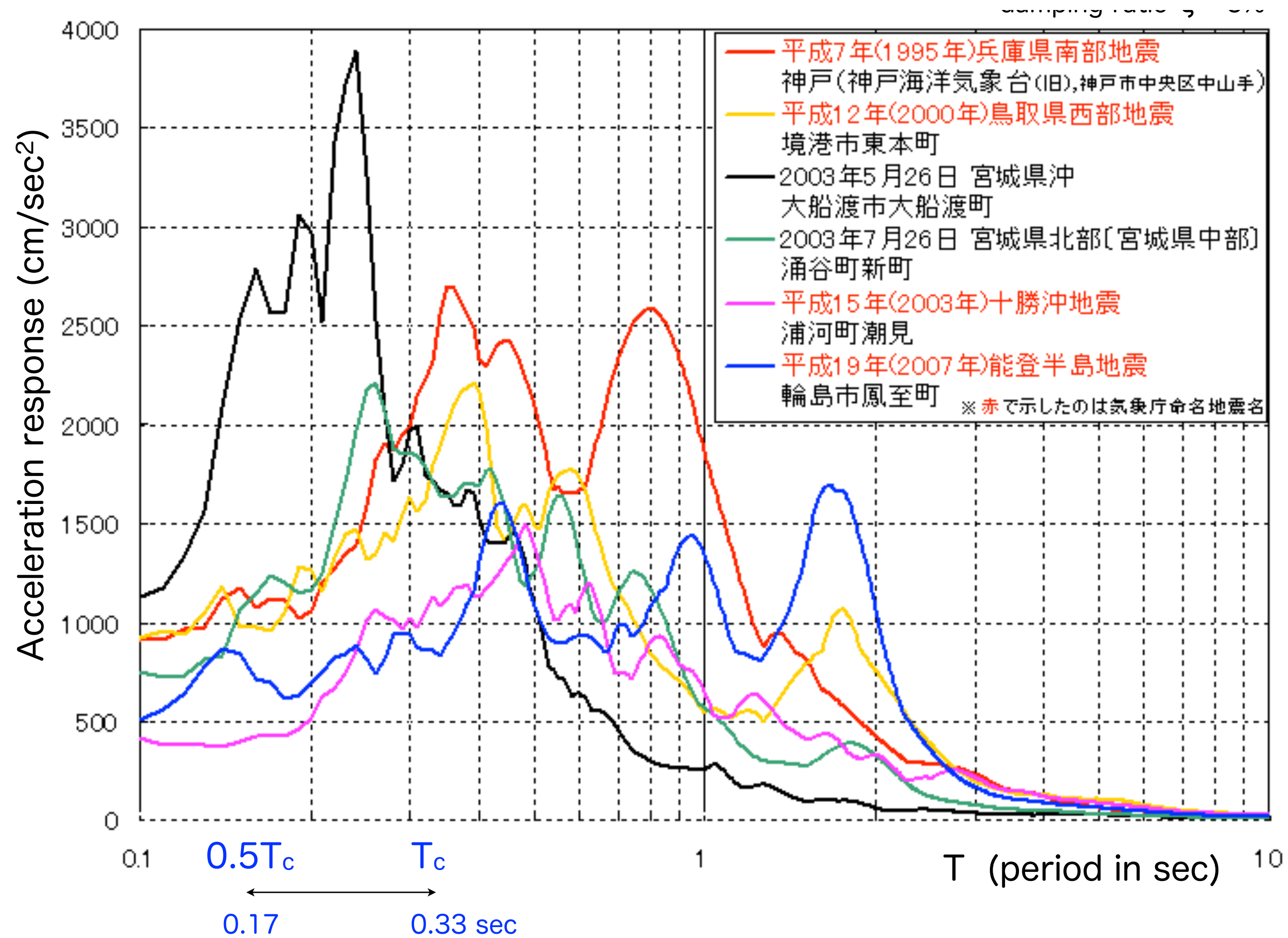
Getting realistic

- HCAL barrel plays an important structural task: Stability has to be understood, also in view of earth quakes in Japan

FEM calculations of structure stability



… need to be coupled with expectations for earthquakes in Kitakami region



Can we rely fully on calculations - or do we need larger mechanical prototypes?

A Strong Community in Germany

- Germany is leading the activities on analog hadron calorimetry for Linear Colliders: Activities spread over many institutes

DESY HH	LS integration; electronics, …
U Hamburg	SiPM & tile optimization,…
U Heidelberg	ASICS; SiPM simulation; tile tester
U Mainz	Data acquisition; HBU production
MPP Munich	SiPM & tile optimization; mechanics, …
U Wuppertal	LED calibration system

+ Analysis, Simulation, Reconstruction

synergies with ECAL activities - common electronics, DAQ, SiPMs and related scintillator challenges

Additional calorimeter activities:

DESY Zeuthen	Forward calorimetry

Summary and Outlook

- Full design for AHCAL for an ILC detector established - Prototypes for all major pieces
  - Scintillator tiles & photon sensors
  - Front-end ASICs and electronics
  - DAQ interfaces and control
  - Mechanics of active elements
  - Absorber structure
- First studies of large-scale test and assembly strategies
  - Rapid, automatic tile testing with LEDs
  - Automatic HBU assembly

Major roles of German institutes in all aspects of the detector

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Major roles of German institutes in all aspects of the detector

- Test-beam activities over the coming years will establish performance of technical prototypes - gradual build-up to larger systems
- Re-thinking some of the design choices: Investigating alternative tile concepts, ASICs, … - there is enough time for that!