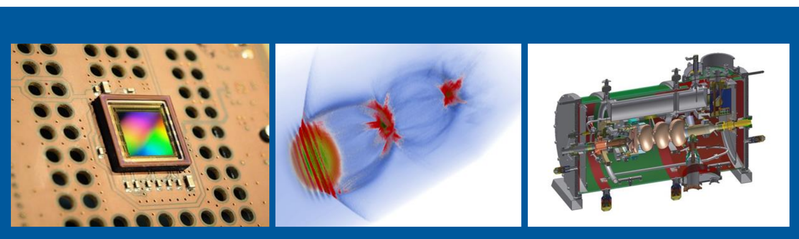
Programme Matter and Technologies

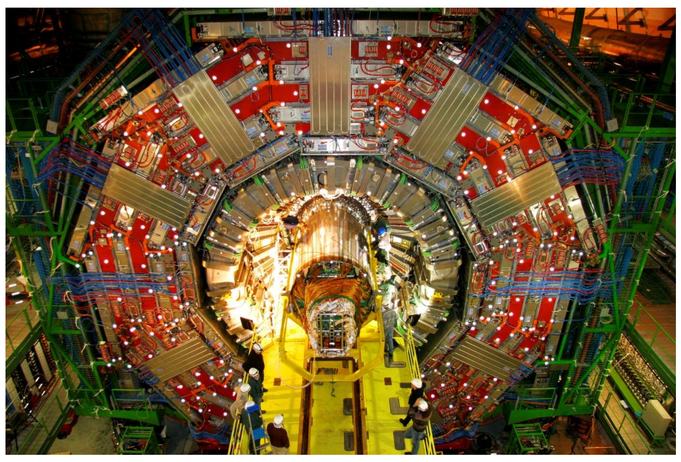
# CMS Level 1 Track Trigger for HL-LHC

DTS - An AM-based Trigger Approach

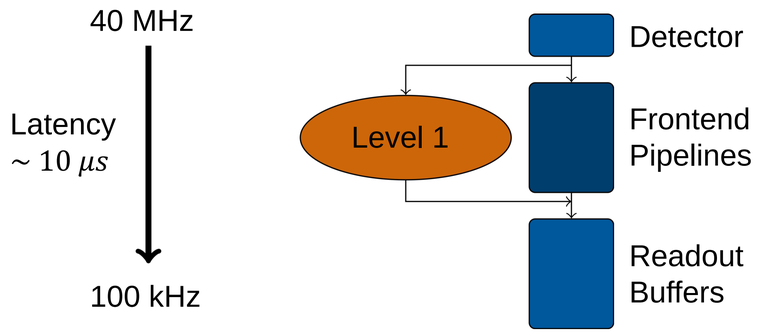


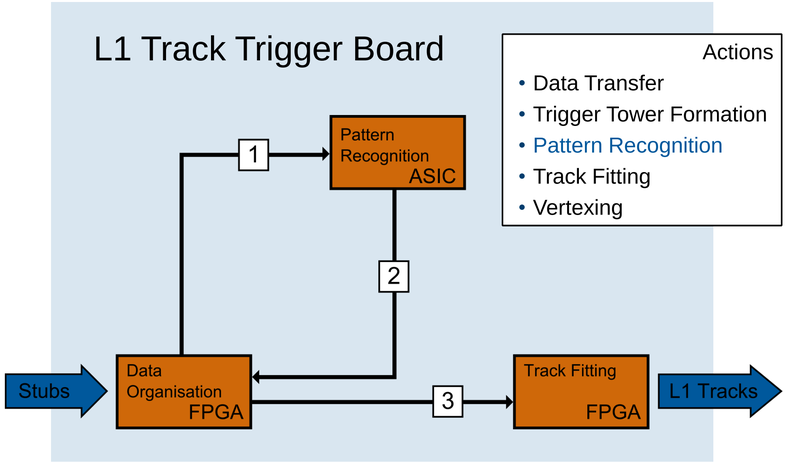
Tanja Harbaum (KIT)

## System Overview

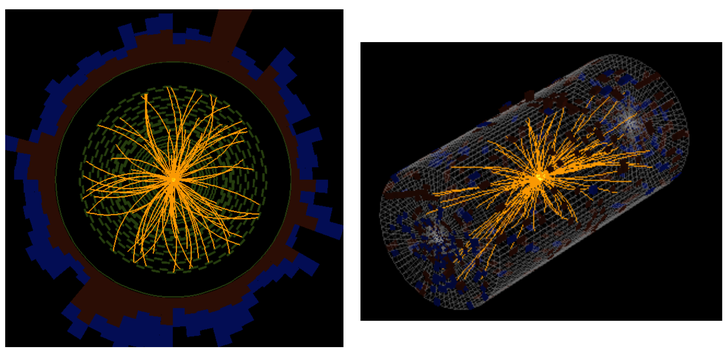


- 10000 tracks per collision
- 400 billion tracks per second



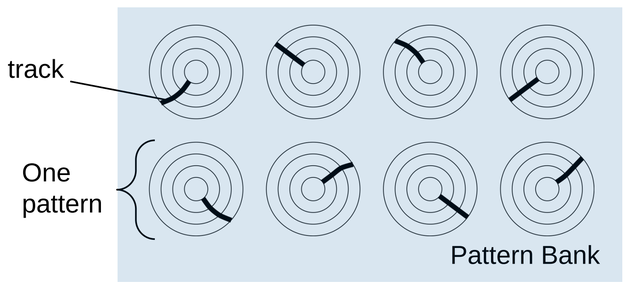

## Pattern Recognition - Approach



**How can we find a needle in this haystack within 10 $\mu s$ ?**

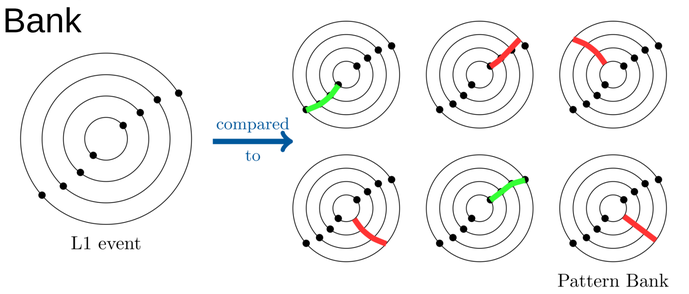
We know how interesting particles look like:

**Let‘s make some pictures of them !**

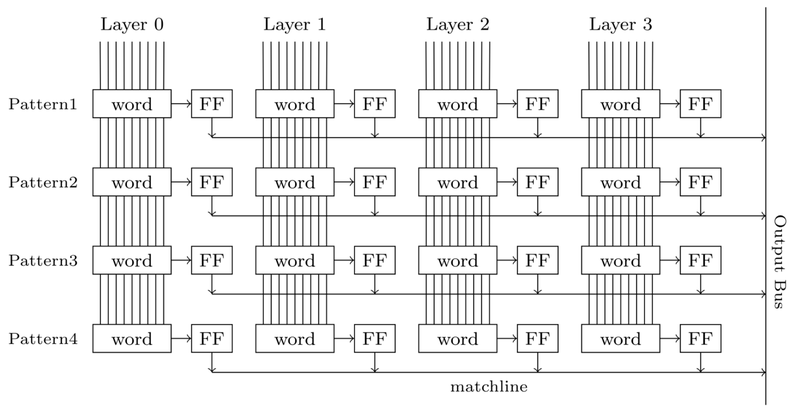



Pattern Recognition

- Generated Pattern Bank of interesting tracks
- One pattern defines a road into the tracker
- Compare the incoming data to the Pattern Bank



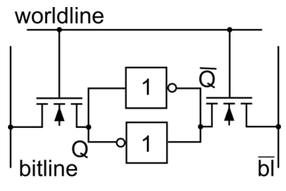

## Implementation



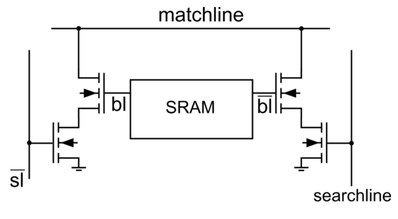

Content Addressable Memory (CAM)

- Provide hit result within one clock cycle

SRAM cell




CAM cell




128 Bits per Pattern

- Set of 8 layers
- 16 Bits per superstrip address
- Specify a low granularity tracker strip

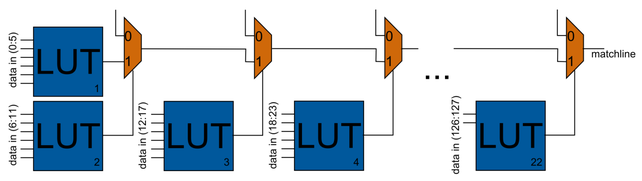
~100 M Patterns overall

- > 1 Gbyte data has to be loaded and compared within microseconds
- DDR3-SDRAM: bit rate 34 Gbyte/s is not enough

## FPGA based Approach

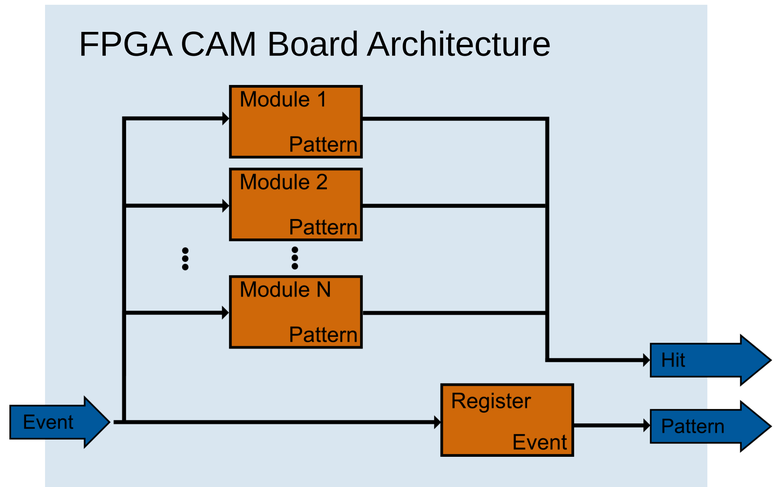
Efficient utilization of FPGA structure

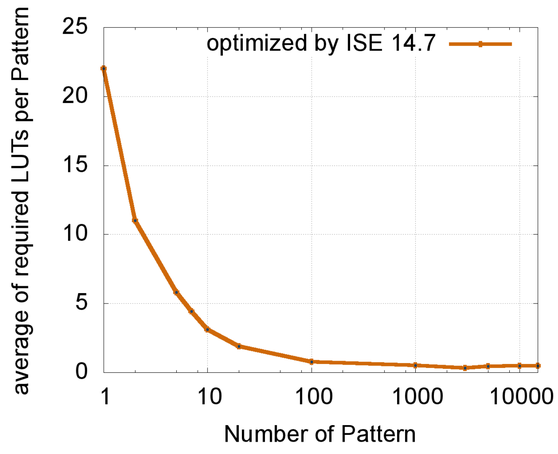
- Port Associative Read only Memory features




Minimization by logic

- Decrease number of LUTs per Pattern
- Depends on the composition of the Pattern Bank
- Utilise FGPA vendor tools




Extensive minimization accessible

- 15000 pattern -> 7300 LUTs
- 3.5% of xc7v330t

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