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A Fast and Low Power Readout ASIC

Front-End Performance

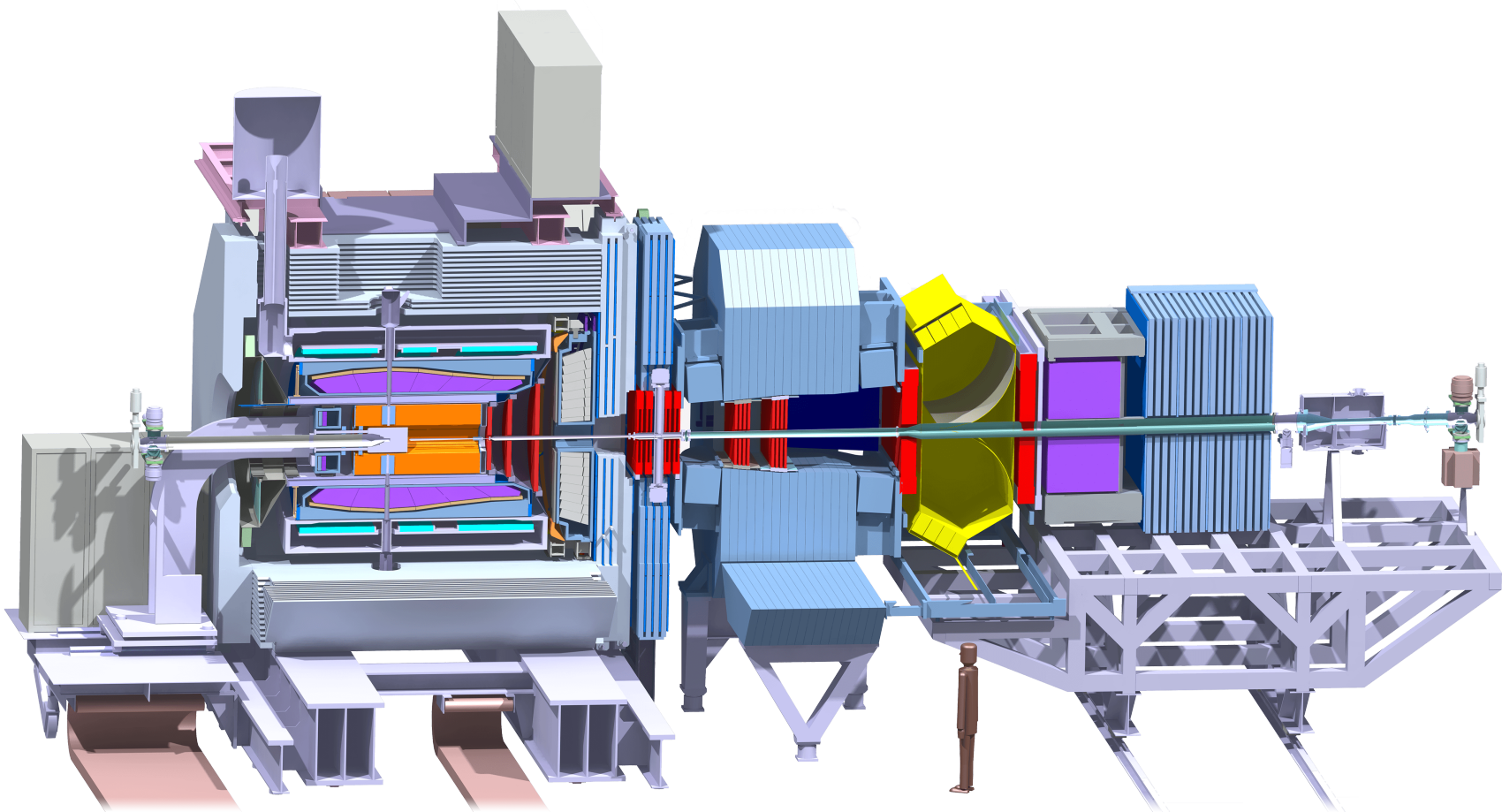
- High rate 100,000 /s/ch
- Time binning 50-200 ps
- Charge resol. 8 bit (dyn. range) \*
- Low power < 4 mW/ch \*
- Pitch 60 μm/ch
- Radiation dose 100 kGy \*

\* Design Goal

Close cooperation  
with INFN Torino

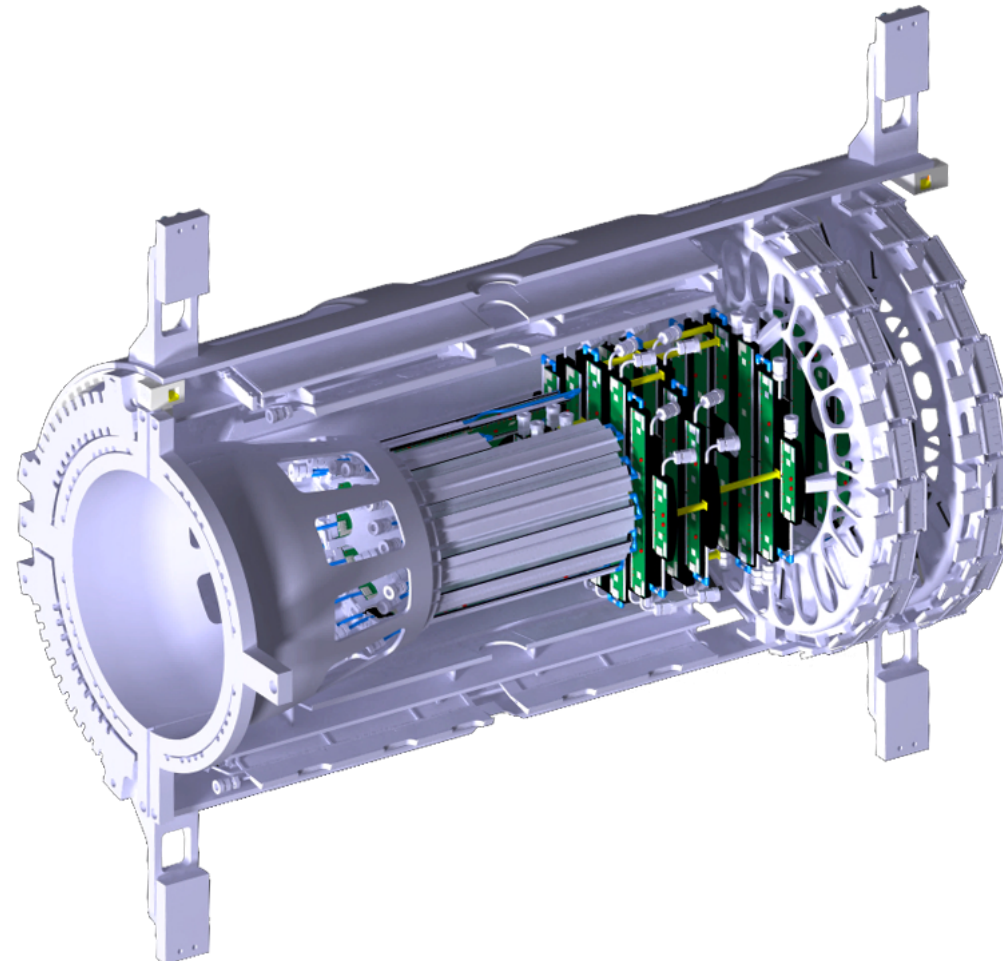


Possible Application



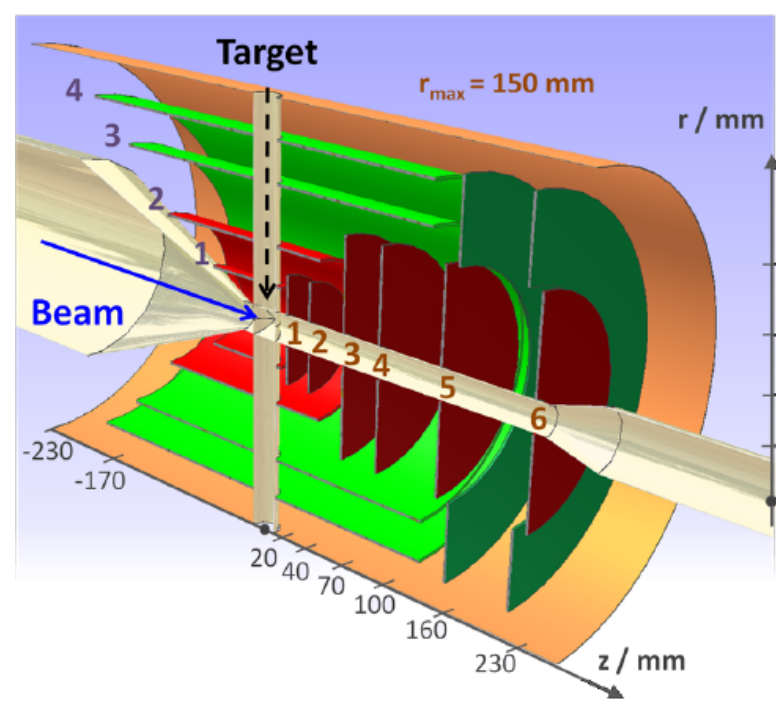
PANDA  
Antiproton Annihilation Darmstadt

Micro Vertex Detector (MVD)



Innermost detector for vertex tracking

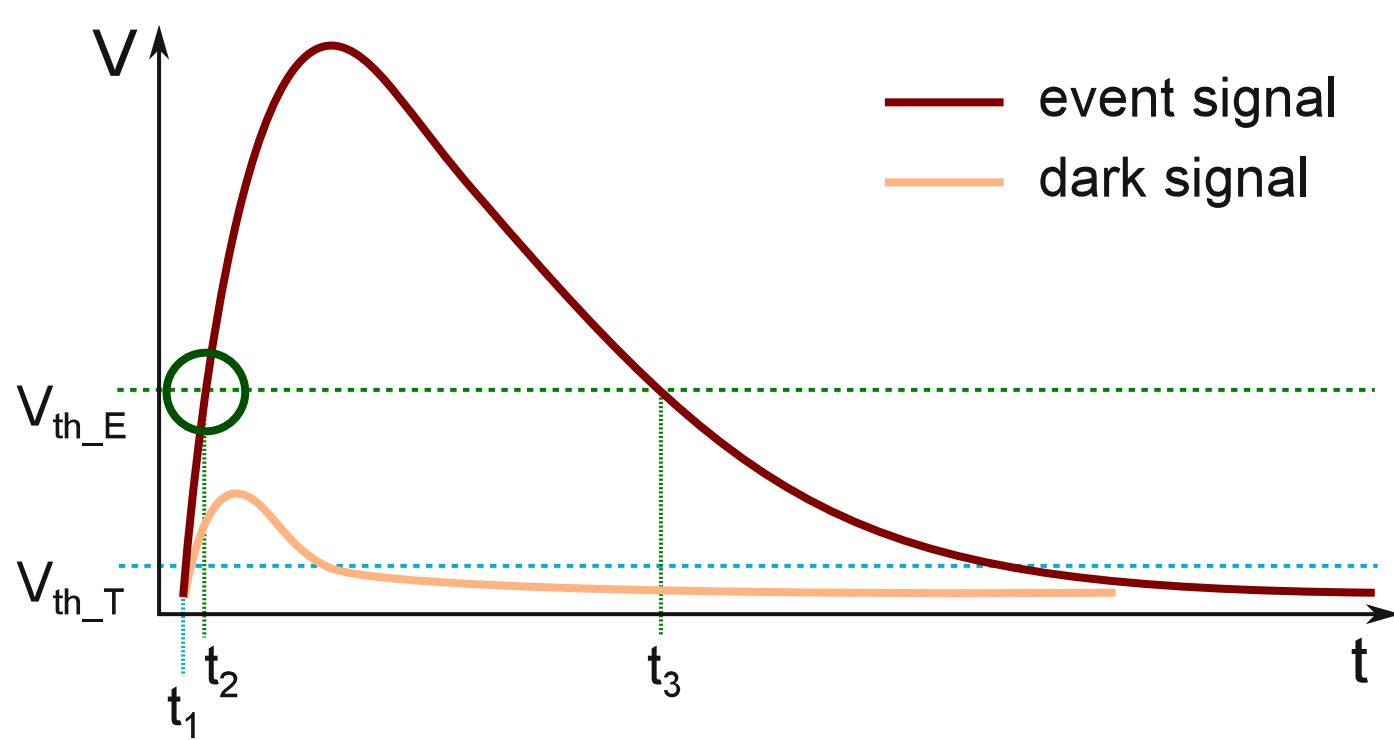
pixel:  $10^7$ ch



strips:  $2 \cdot 10^5$ ch

The PANDA Strip ASIC (PASTA)

Measurement Concept

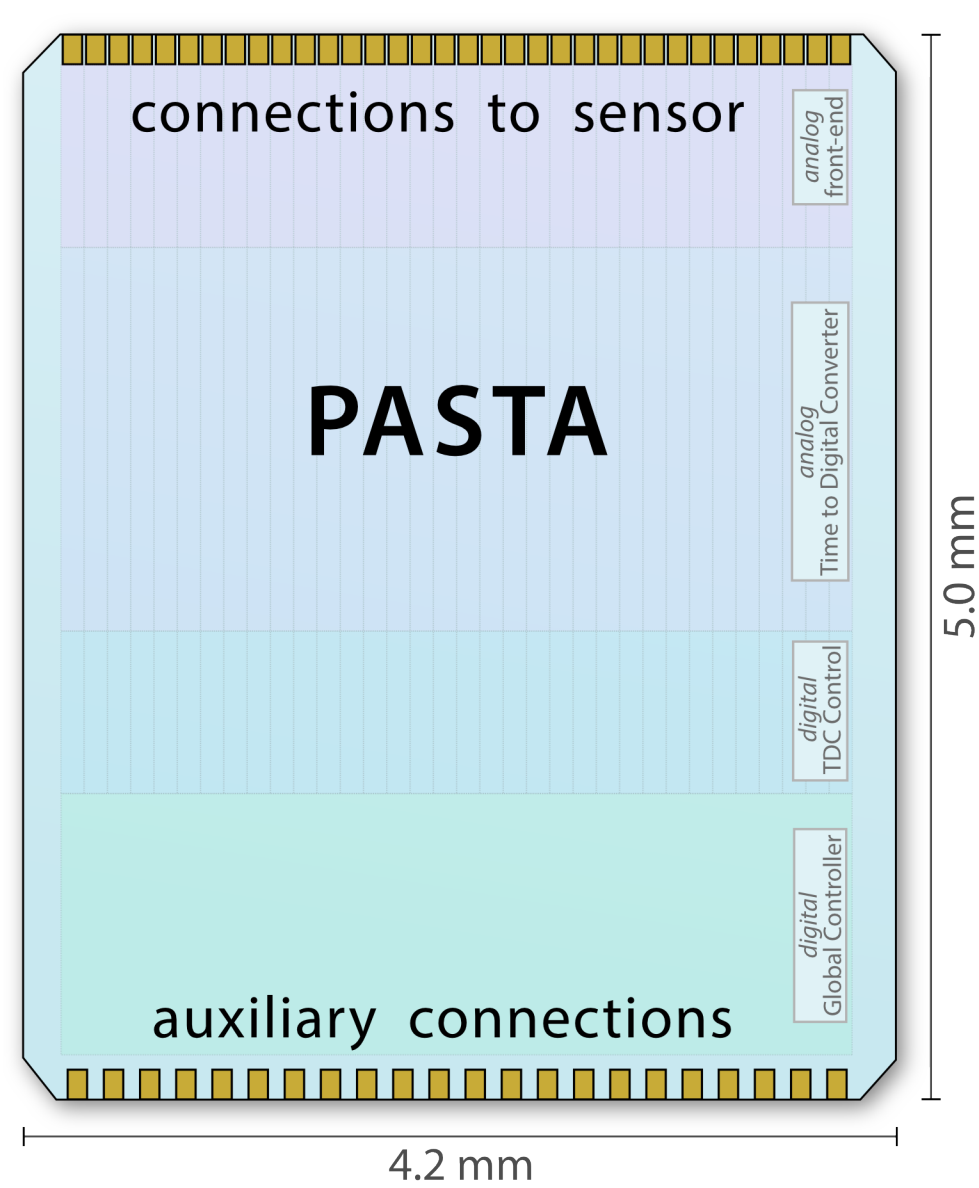


Readout

Timestamps (50 ps res.)  
Time over threshold  
Data driven (no LVL1-Trig.)

Concept based on TOFPET ASIC

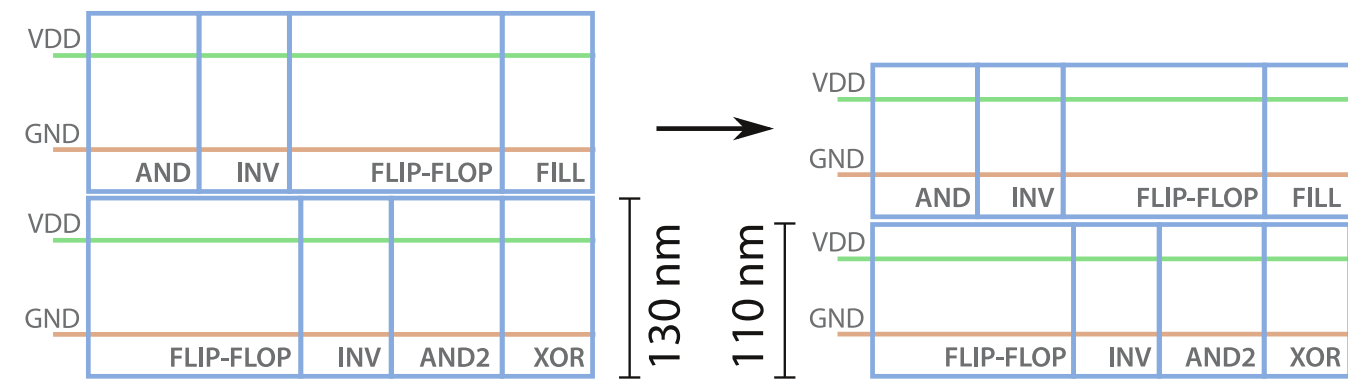
Components in the ASIC



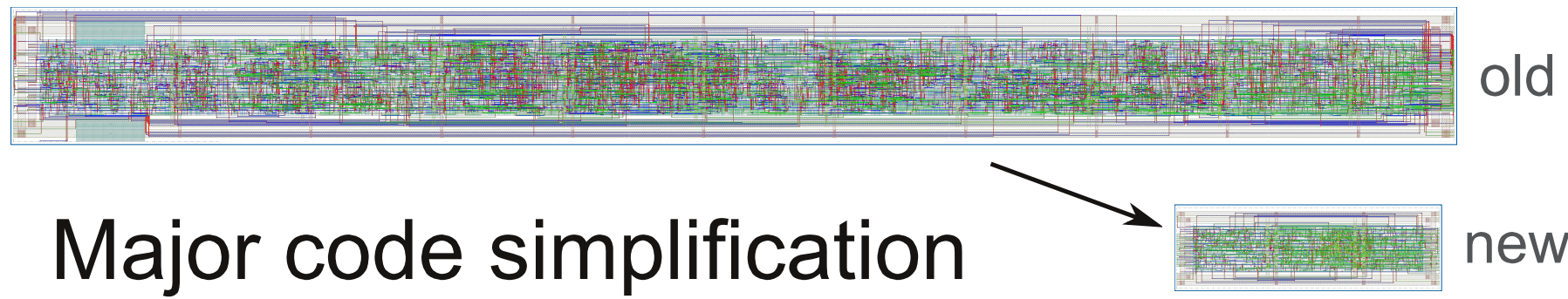
1. Amplification & discrimination
2. Time interpolation, Wilkinson ADC
3. Control charging, initiate storing
4. Handling config. & channel data

From TOFPET to PASTA

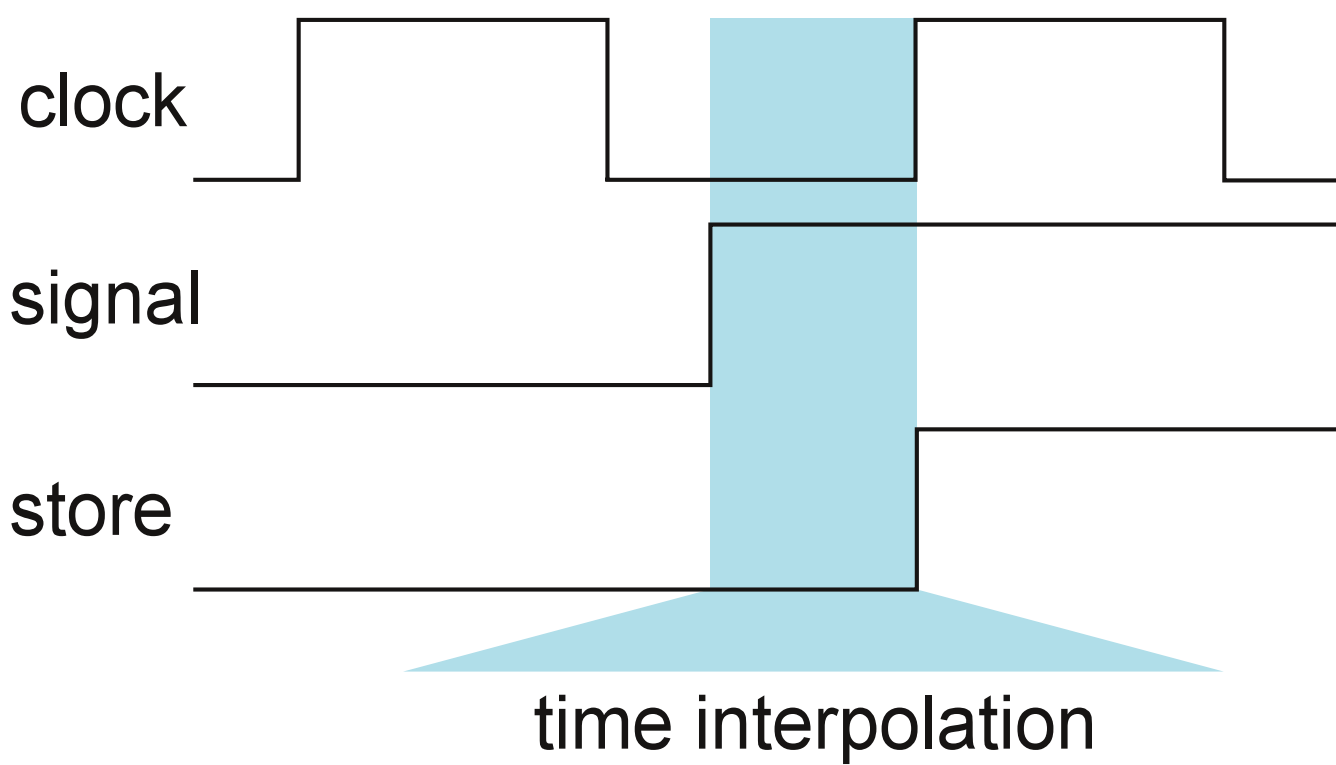
Technology Change



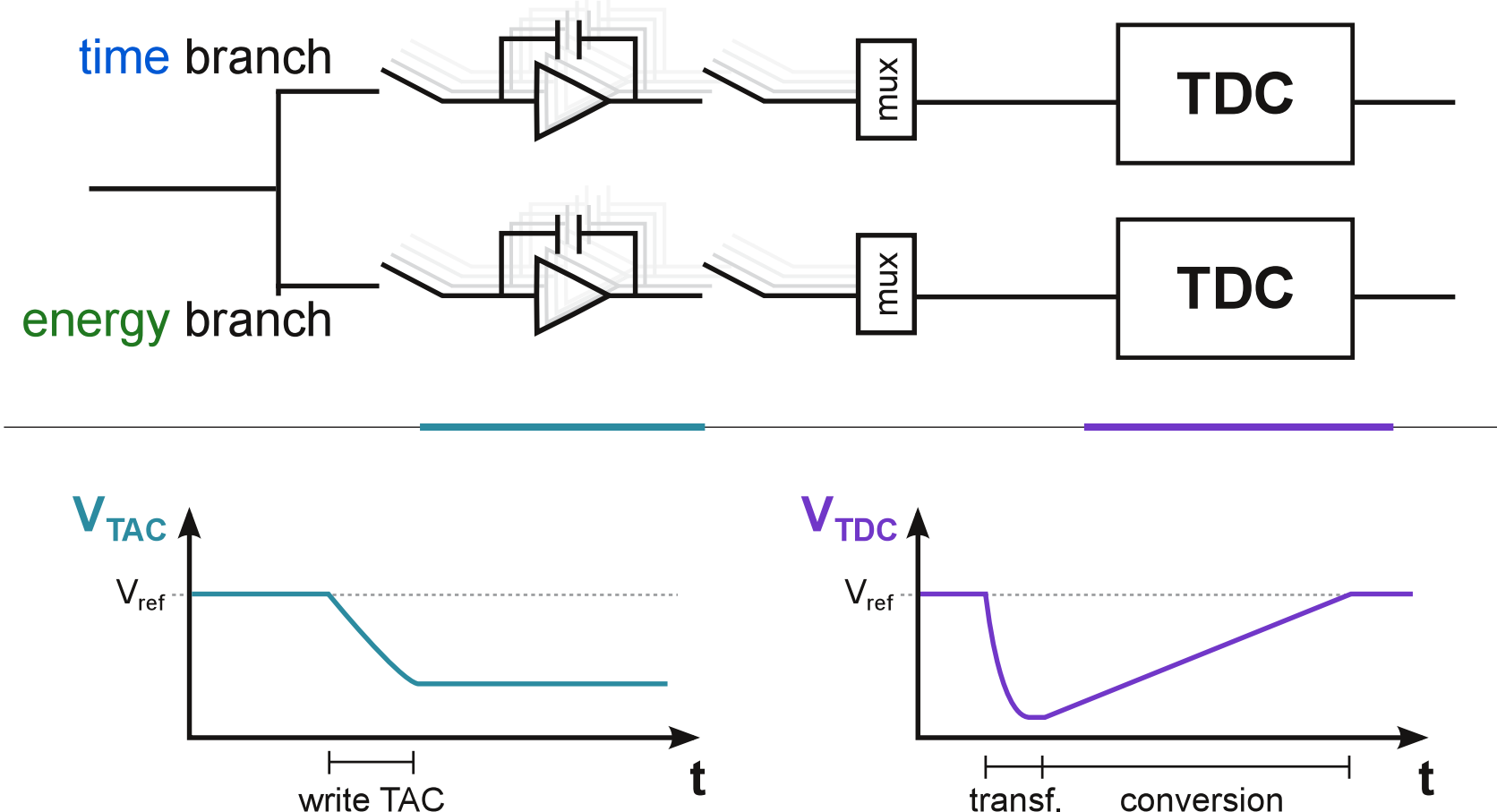
New TDC Control



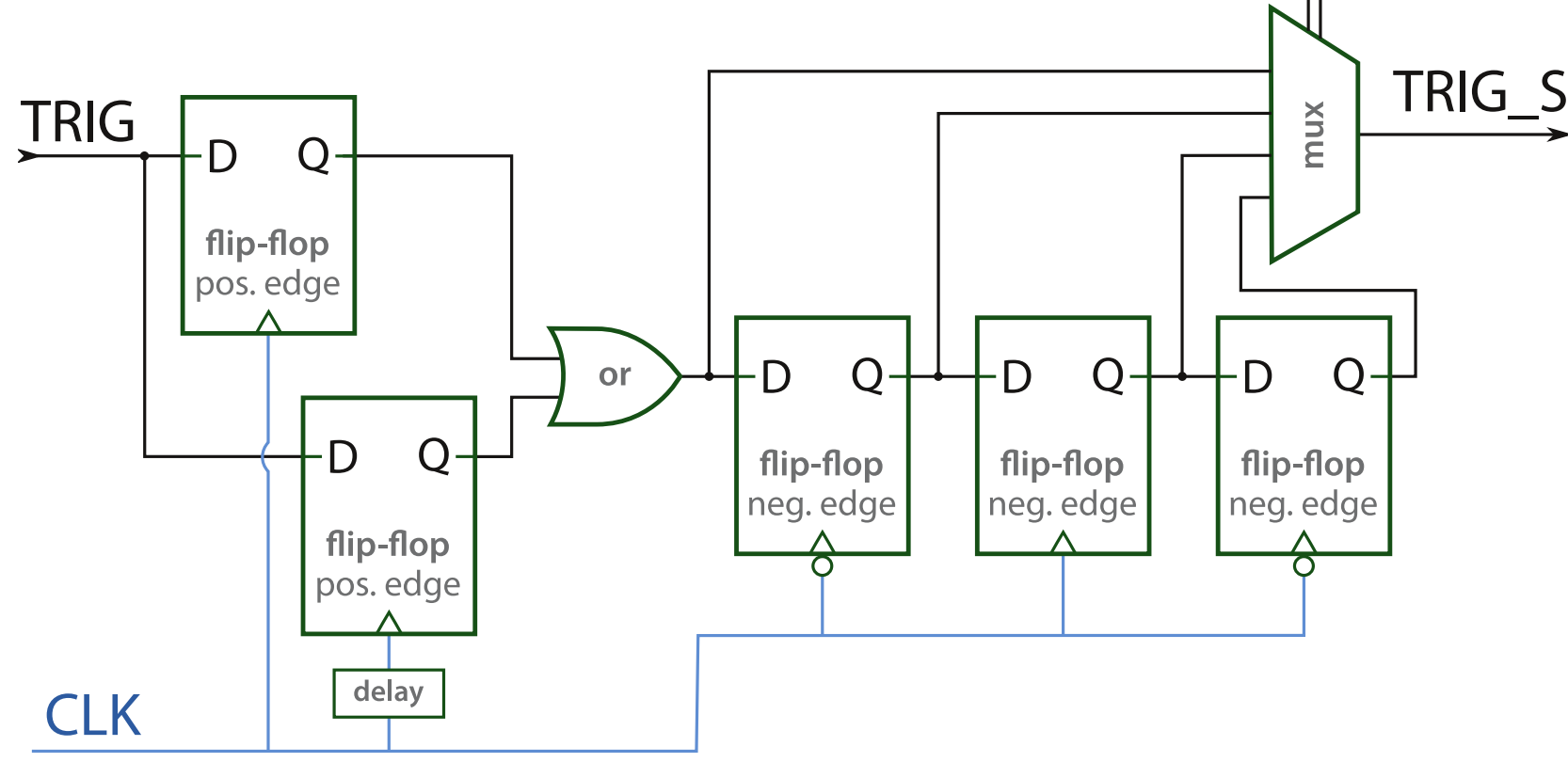
Time Interpolation



Time Interpolation in TDC



Synchronization Chain



Current Status

TDC Controller

- Second version finished
  - All improvements implemented
  - New code fully functional
- Single Event Upset protection of operation critical components

TDC Parameter:

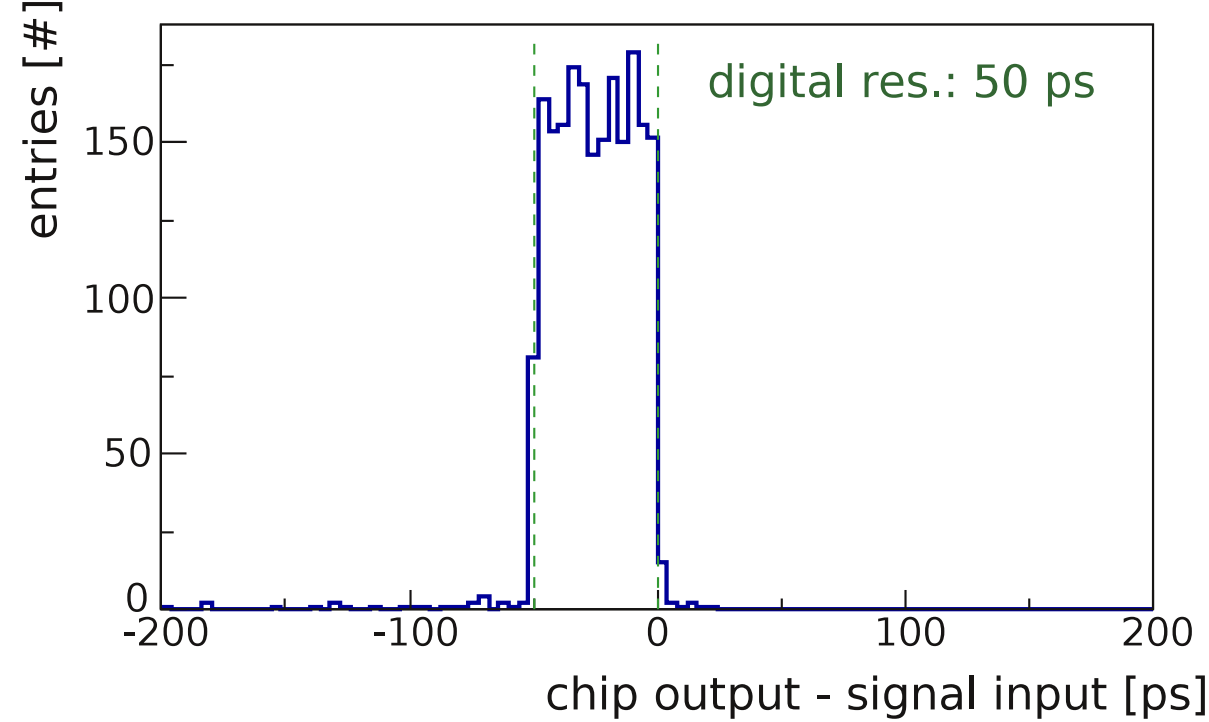
Area Occupation  
84.8% → **6.5%**  
Power [mW/ch]  
1.57 → **0.07**

Complete TOFPET: ~8 mW/ch

Global Controller

- Adapted to TDC control v2
- Implementation of Single Event Upset protection started

ASIC Time Mismatch



Conclusions & Outlook

Conclusion

- PASTA in development
- Time-based readout (based on TOFPET)
- Fast, simple, and low power consumption
- Adapted to microstrip readout
- New TDC controller, radiation protection

Outlook

- Combine analog and digital designs
- Submit design (summer 2014)
- Test first PASTA chip