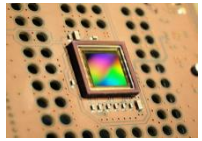
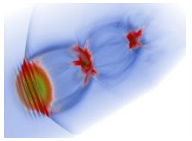
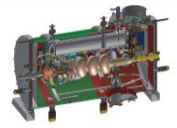
Matter and Technologies

Ultra-fast data acquisition system for ps – fs beam diagnostic

IPE: M. Caselle, S. Cilingaryan, A. Kopmann, M. Schleicher, M. Vogelgesang, M. Weber

IMS: J. Raasch, S. Wuensch, M. Siegel

LAS – ANKA: M. Brosi, V. Judin, A.-S. Müller, N. J. Smale, J. Steinmann

2th ARD ST3 Workshop: fs-ps electron and photon beams, 26-27 February 2014 - HZDR

Detector technology and systems

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Requirements for CSR measurements

To detect and study of the emission characteristics of CSR in the THz range → requires very fast detector operating in a spectrum range of hundred GHz -> Terahertz

Cryogenic HEB detector IR1 - ANKA

Cryogenic detectors:

- ✓ HEB (niobium nitride detectors)
- ✓ YBCO (Yttrium barium copper oxide)

→ *See J. Raasch's talk "Fast THz detectors"*

Room temperature detectors:

- ✓ Zero Biased Schottky Diode @ different spectrum ranges (200, 400 GHz ..)

Picosecond time resolution → Very wideband electronic

Turn-to-turn & bunch-to-bunch measurements of CSR with high energy & temporal resolutions

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What about readout electronic and acquisition system ?

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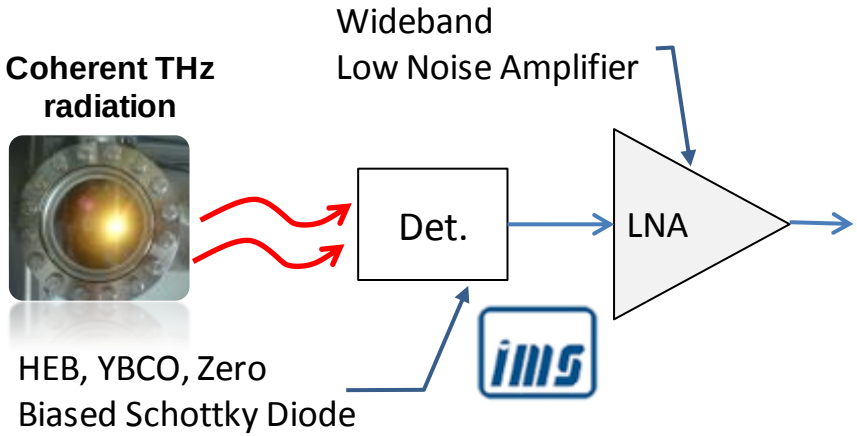
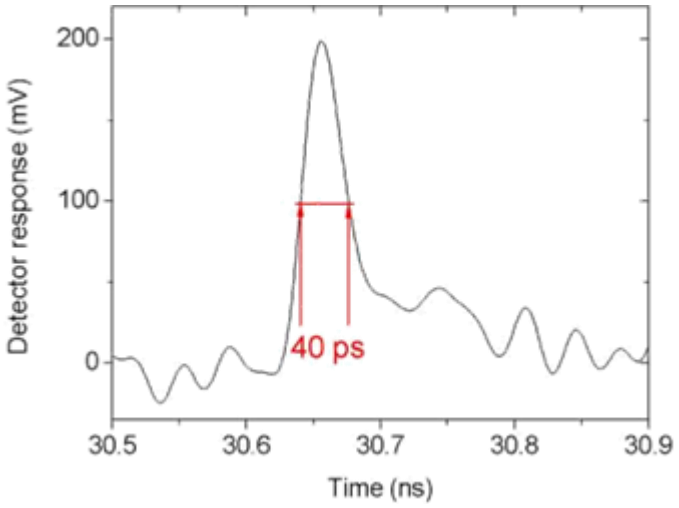
CSR – Readout system and requirements

- *Incoming pulse @ 500MHz (ANKA RF system)*
- Turn-to-turn & bunch-to-bunch CRS measurements (minutes/hours)
- *Wideband DC- 50/60 GHz*





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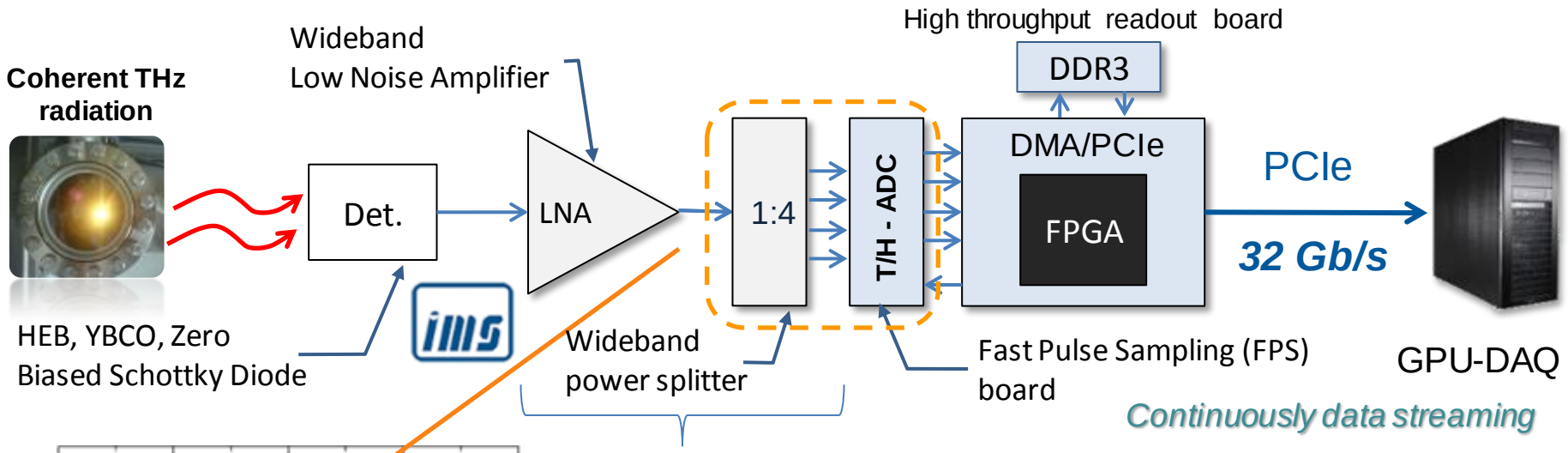

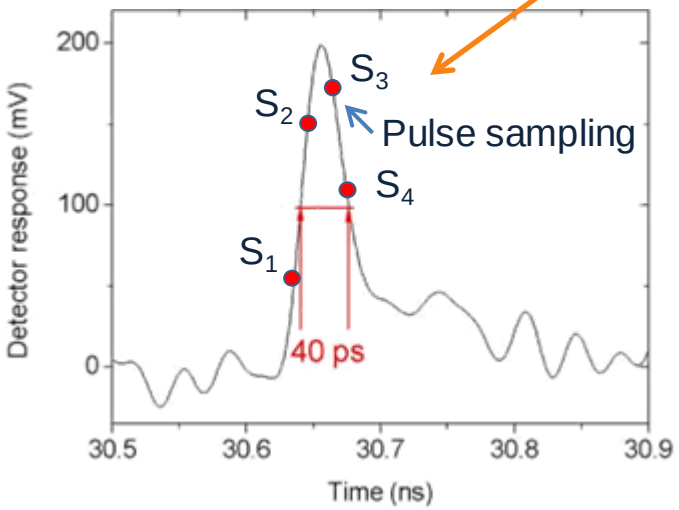

1. **Sampling** each incoming pulse with 4 samples (min. sampling time of 3 psec)
2. **Data transfer** to high-end GPU (Graphics Processing Units)
3. **Pulse reconstruction** and peak amplitude + peak time measurements (GPU)

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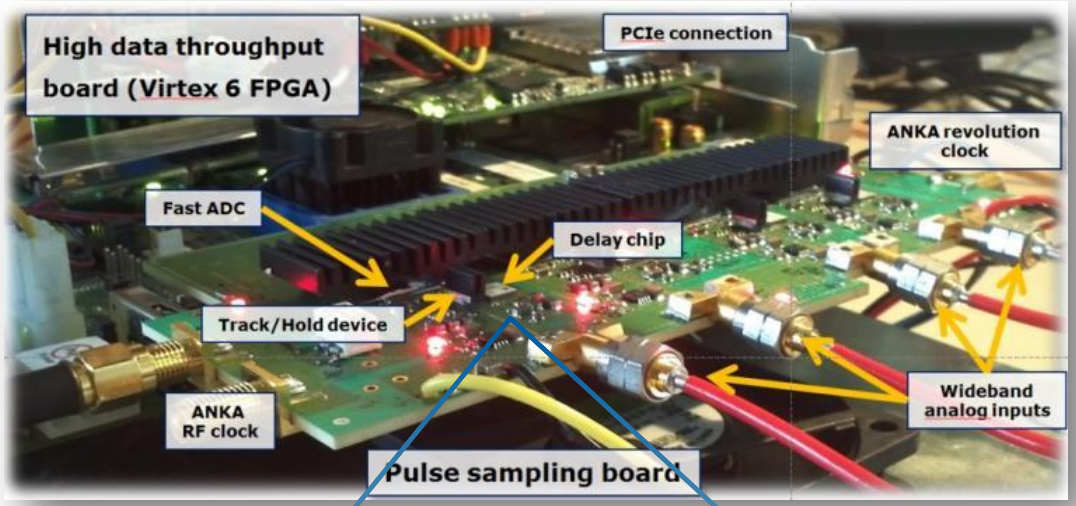
Fast Pulse Sampling board (FPS board)



Performance:

✓ Minimum sampling time: 3 psec → >300GS/s

✓ 12 bit ADC resolution

✓ Configurable for the readout of up to 4 ultra-fast detectors in parallel

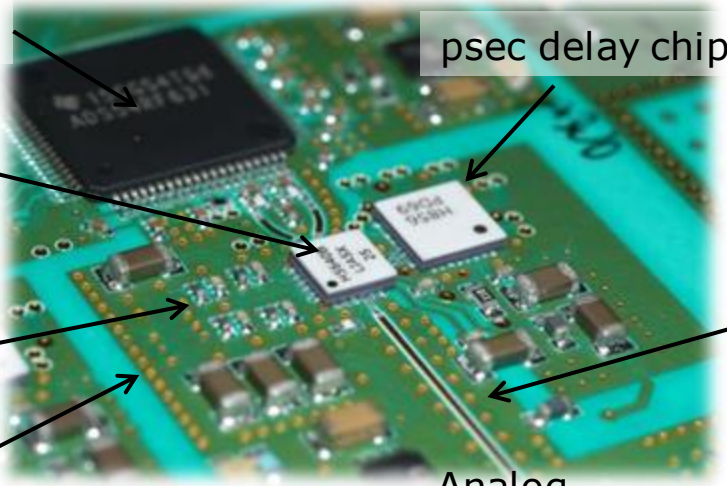
Sampling stage

Fast ADC (500 MS/s)

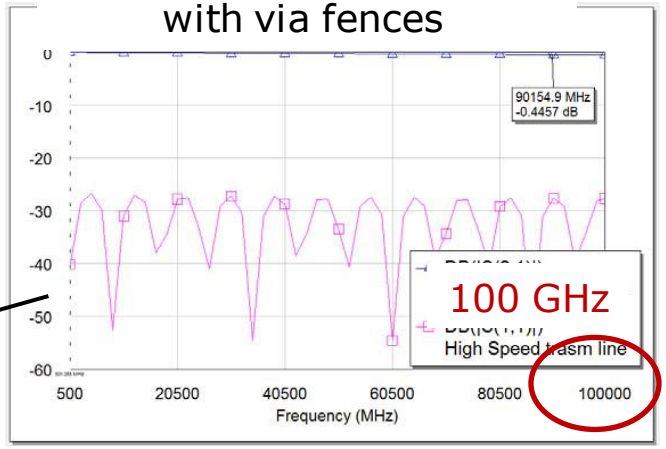
Track-and-hold

RF filters

Shielding via



Wideband CPW trans. line with via fences



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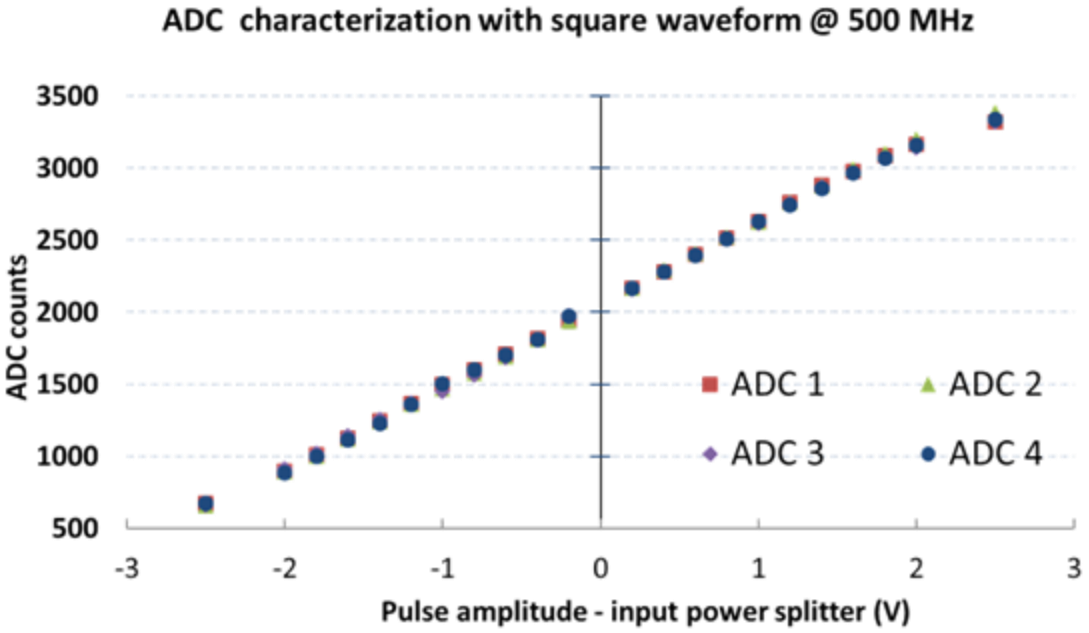
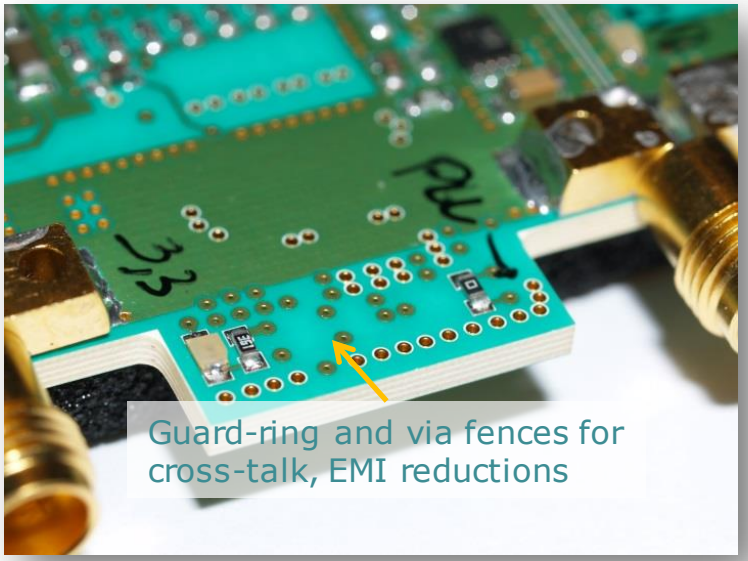
FPS board: characteristic & performance



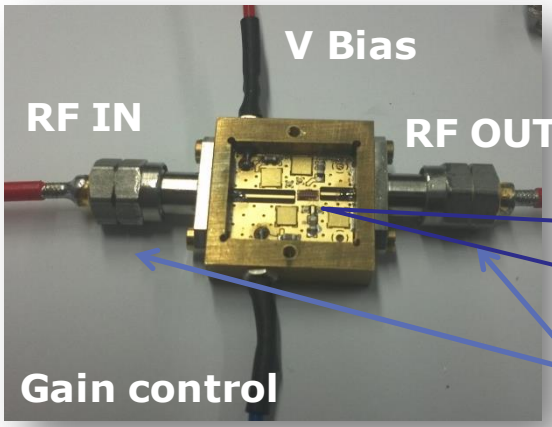
- ✓ Bipolar analog signal,
- ✓ Wide dynamical range
- ✓ High linearity
- ✓ ADC noise < 1mV
- ✓ Total time jitter SrdDev < 1.7 psec

- PCB - 10 layers metal stuck-up (Roger 4003), **analog & digital** layers/circuitries → fully decoupled
- **Fully differential circuitries** (analog and clock distribution) → to reject the noise conditions, thermal & voltage oscillations
- **Layout design for RF/Microwave** applications: via fences, guard ring → to avoid the cross-talk and EMI

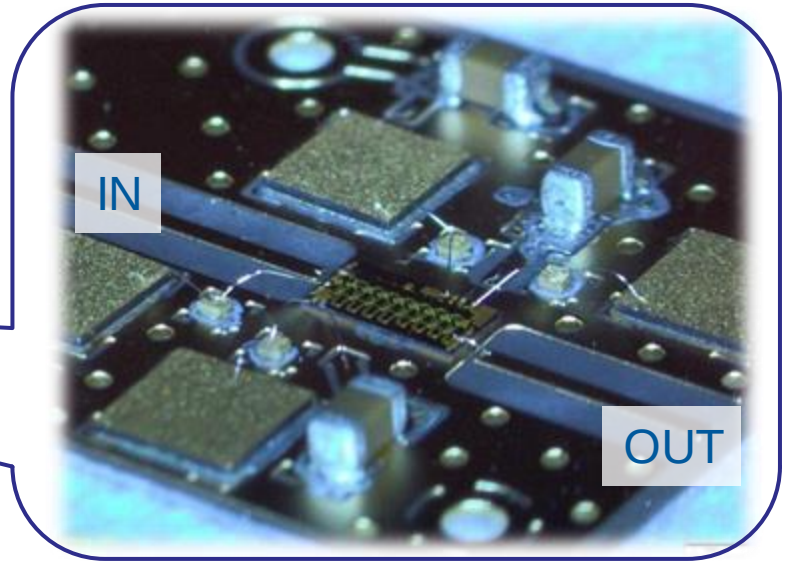


Wideband LNA (Low Noise Amplifier) & power splitter

Wideband LNA

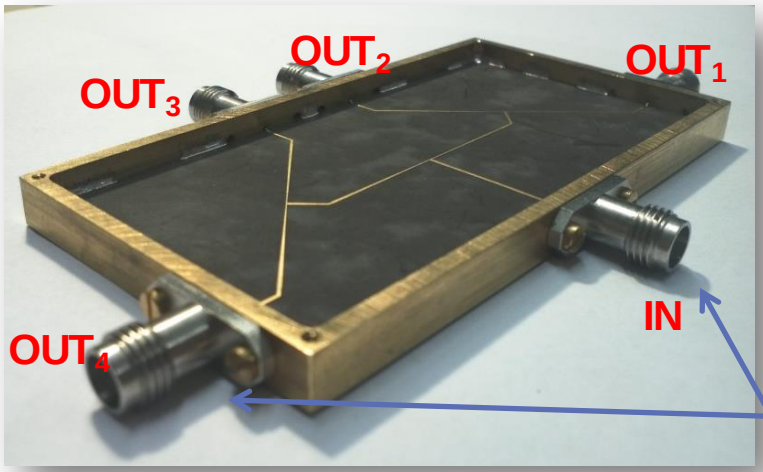


High-freq.
V-connectors



MCM-D technology, new PCB materials for microwave/RF design, MMIC based on GaAs technology. **Flat gain: 12 dB, from DC -48 GHz**

Wideband power splitter



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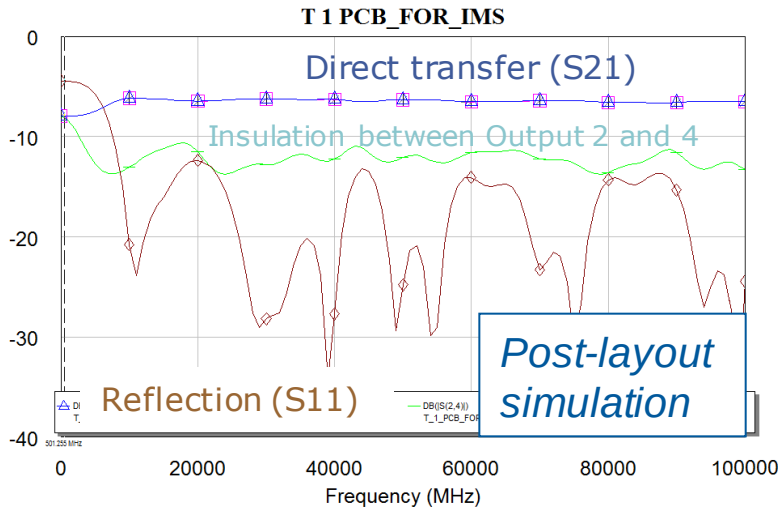
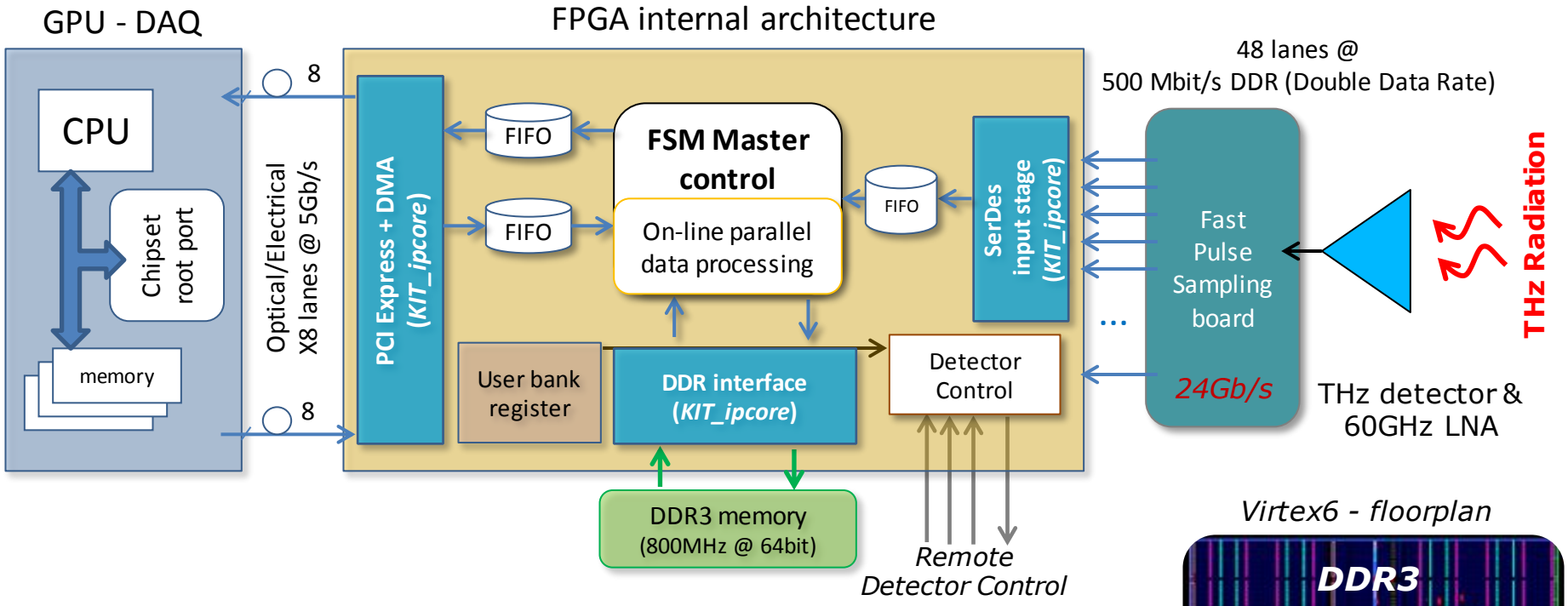
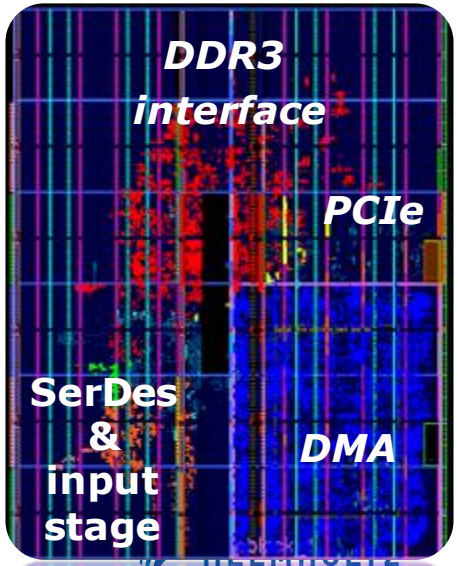


High-throughput FPGA architecture



Virtex6 - floorplan



- ✓ PCIe-Bus Master DMA readout architecture operating @ 32Gb/s [with 8 lanes PCIe @ Gen2] → DMA detals
- ✓ Multi-port high speed DDR3 interface @ 51Gb/s
- ✓ PCI Express/DMA Linux 32-64 bits driver
- ✓ Integration in the parallel GPU computing framework

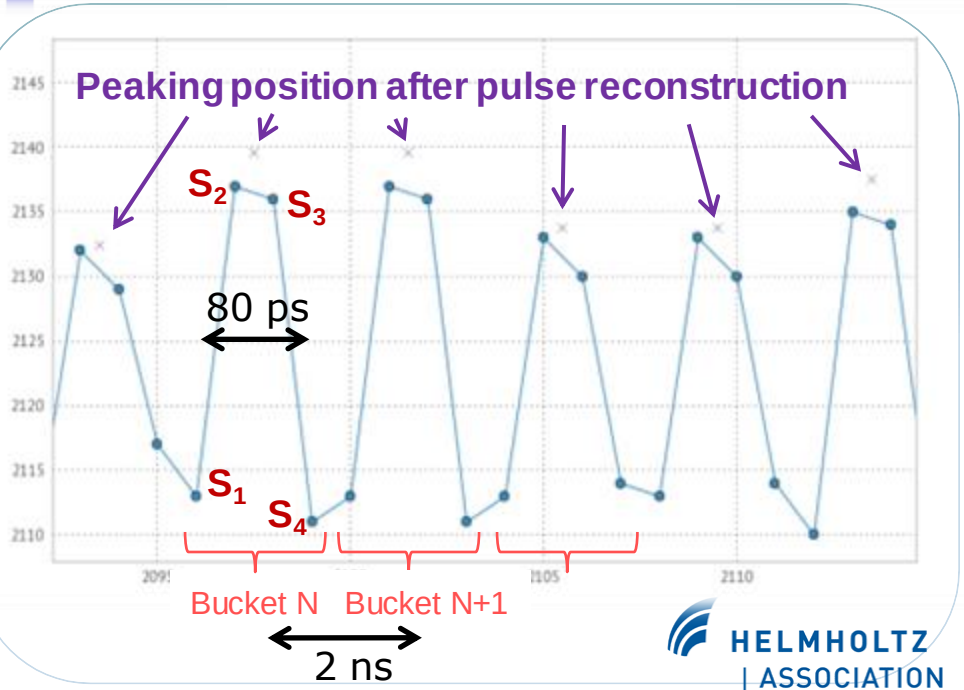
Real-time GPU data analysis

Turn-to-turn & bunch-to-bunch - long observation time.

- Graphic User Interface
- Board control & calibration routines

➡ See M. Brosi's talk "Analysis of CSR multibunch studies"

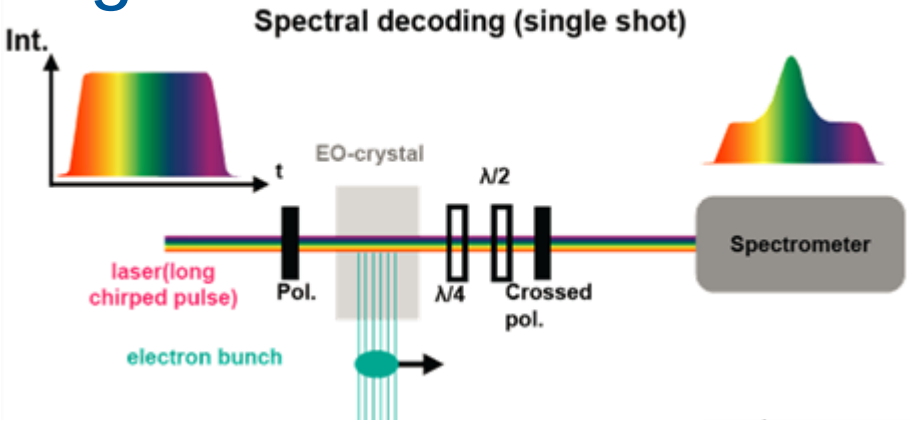
Multi-bunches environments



Real-time GPUs data analysis

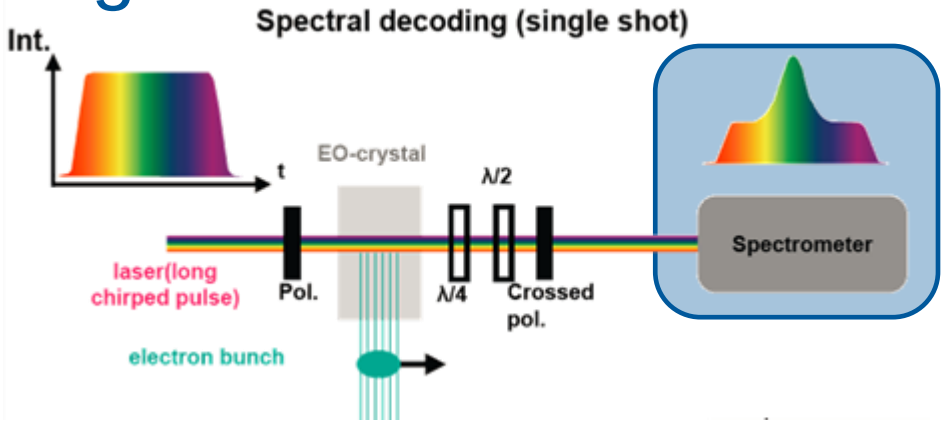
- Fast pulse reconstruction with "Gaussian shape" by GPU
- Fast real-time FFT both amplitude & time oscillations
- Histograms (buckets, turn, etc..)
- ..

A spectrometer for single shot electro-optical bunch length measurements



➡ *See N. Hiller's talk, "Electro-optic sampling for electron bunch diagnostic @ ANKA and FLUTE"*

A spectrometer for single shot electro-optical bunch length measurements

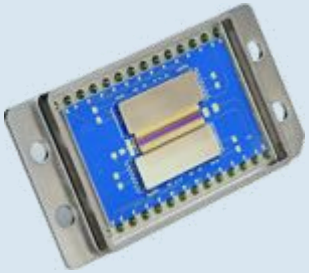


See N. Hiller's talk, "Electro-optic sampling for electron bunch diagnostic @ ANKA and FLUTE"

Spectrometer requirements:

- 256/512 InGaAs pixels linear array
- Frame rate of Mfps (resp. ANKA → 2.7Mfps)

Available sensor & front-end electronics on the market:



Xlin 1.7: 512,	1024 pixels	@ 40kfps
ANDANTA LDA	512 pixels	@ 97Kfps
Hamamatsu G12231	1024 pixels	@ 97Kfps
…		
Goodrich SU1024LE-1.7	1024 pixels	@ 123 kfps

Developing of a 512 (InGaAs) pixel linear array with a continuous turn-to-turn bunch length measurement in the range of Mfps

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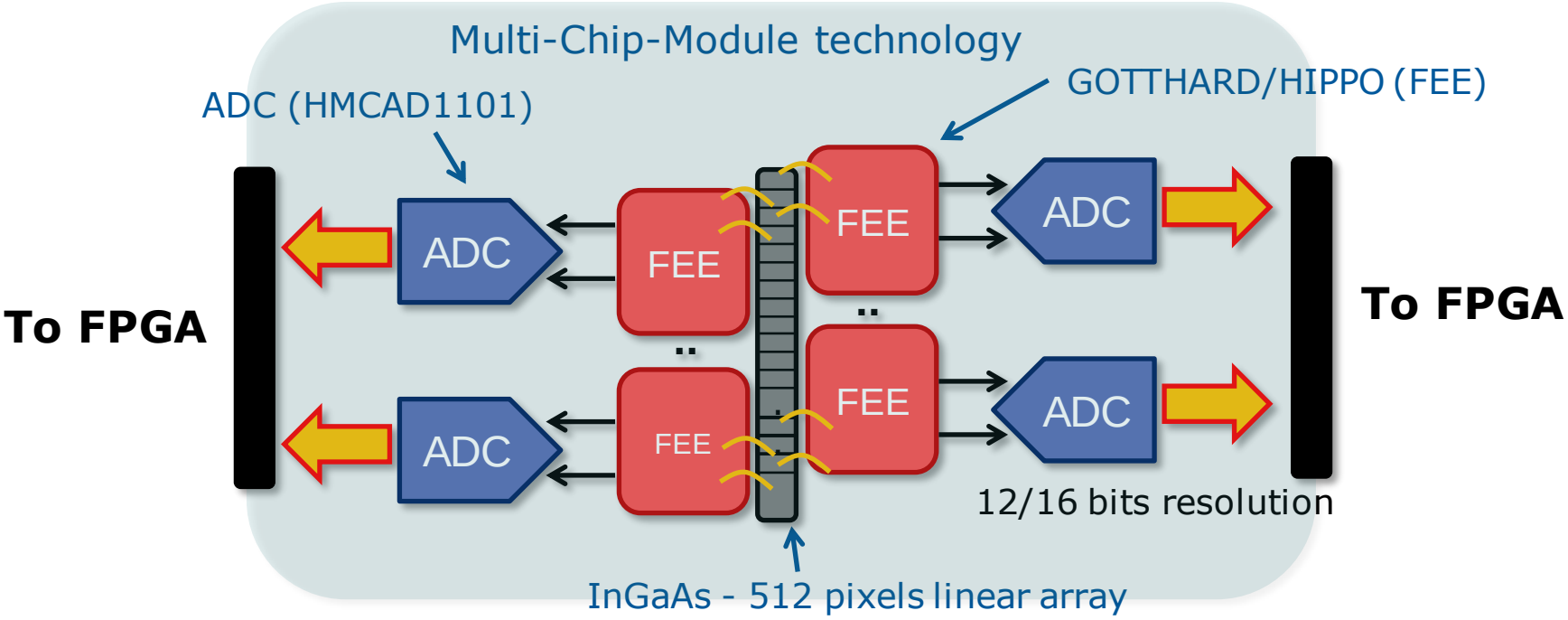
New spectrometer concept



Solution 1: FEE - GOTTHARD - PSI (Gain Optimizing microsTrip sysTem witH Analog ReaDout) → charge integrating readout - IBM 0.13um for XFEL strip-detetctors

→ Calculated frame rate: > 2 Mfps @ 512 pixels

Solution 2: FEE - HIPPO - Lawrence Berkeley National Laboratory (High-Speed Image Preprocessor with Oversampling) → charge sensitive amplifier- 65 nm for Fast X-ray imaging

→ Calculated frame rate: 10 Mfps @ 512 pixels

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Conclusion & what's next

- ✓ **FSP board** → tested and **qualified** with different beam conditions and different detectors *(see also M. Brosi´s talk*)

- ✓ **First system will be delivery to ANKA-Terahertz group**, this include a main readout box + GPU-DAQ with touch screen monitor for a easy user handling

- ✓ **System is configurable to match others synchrotron light sources** → fully programmable PLL clock tree and we benefit of advance/customs data analysis in the FPGA side.

- ✓ **First prototype of InGaAs spectrometer** *for the shot electro-optical bunch length measurements* operating at several Mfps, will be available the next months

Thank you for your attention

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Back up slides

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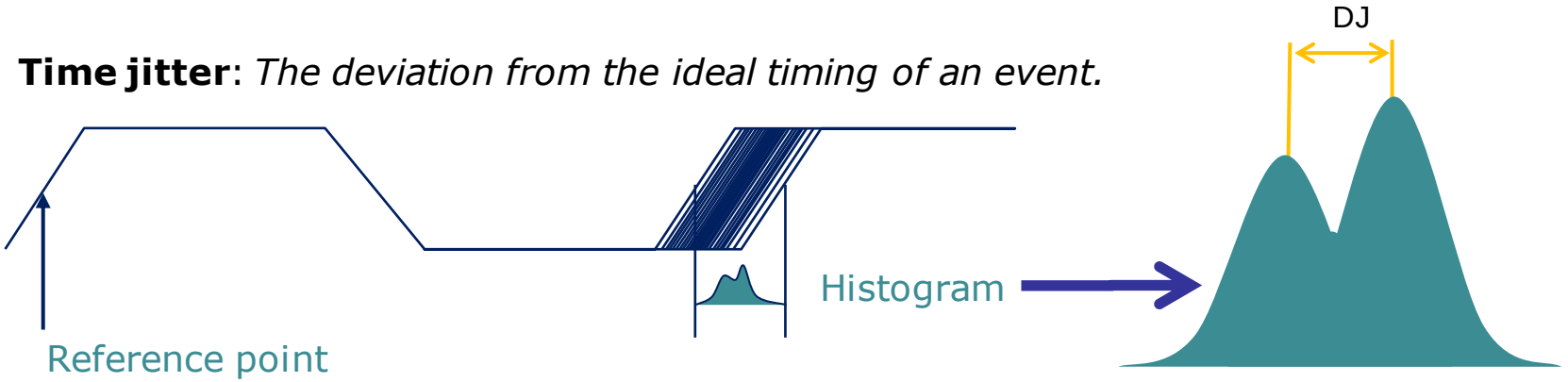
FSP board : Time jitters measurements

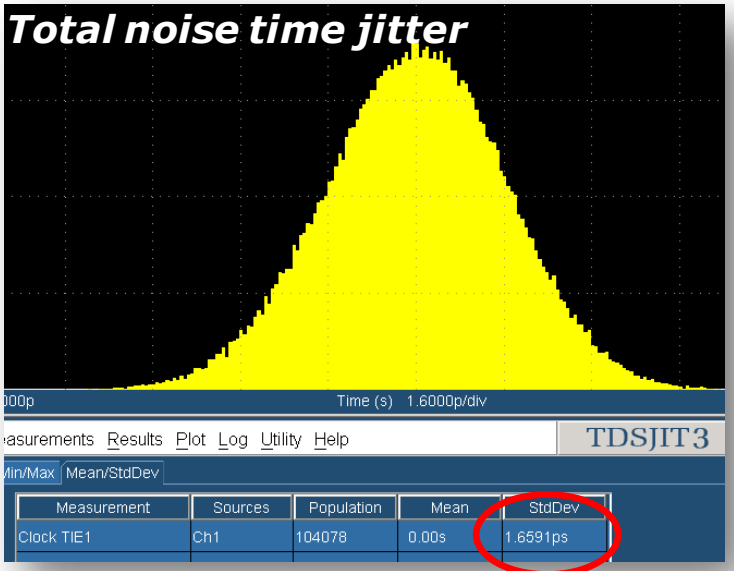
Time jitter: *The deviation from the ideal timing of an event.*



Jitter is composed of: both deterministic (DJ) and Gaussian (random) (RJ) content.

Cross talk, EMI radiation, noisy reference plane, Simultaneous Switching Outputs (SSO), etc.

Thermal and shot noise, etc.

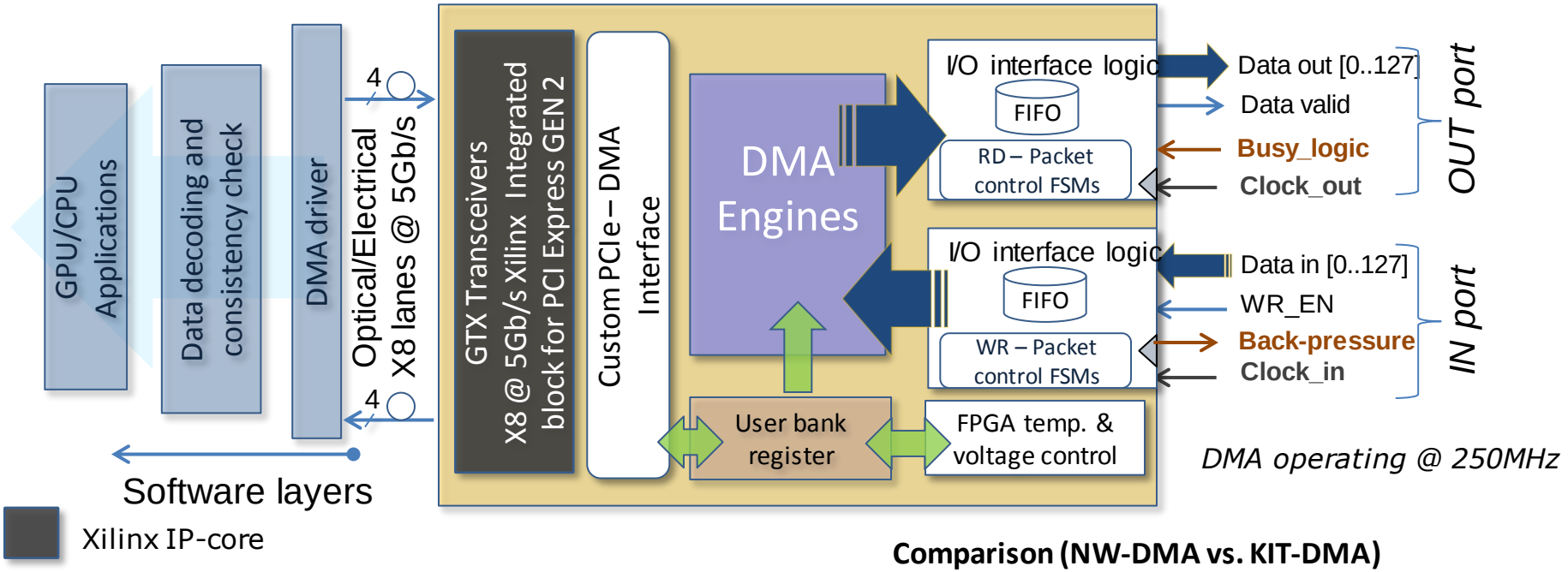


NO deterministic component → NO digital cross-talk in the analog circuitries, EMI or SSO, etc..

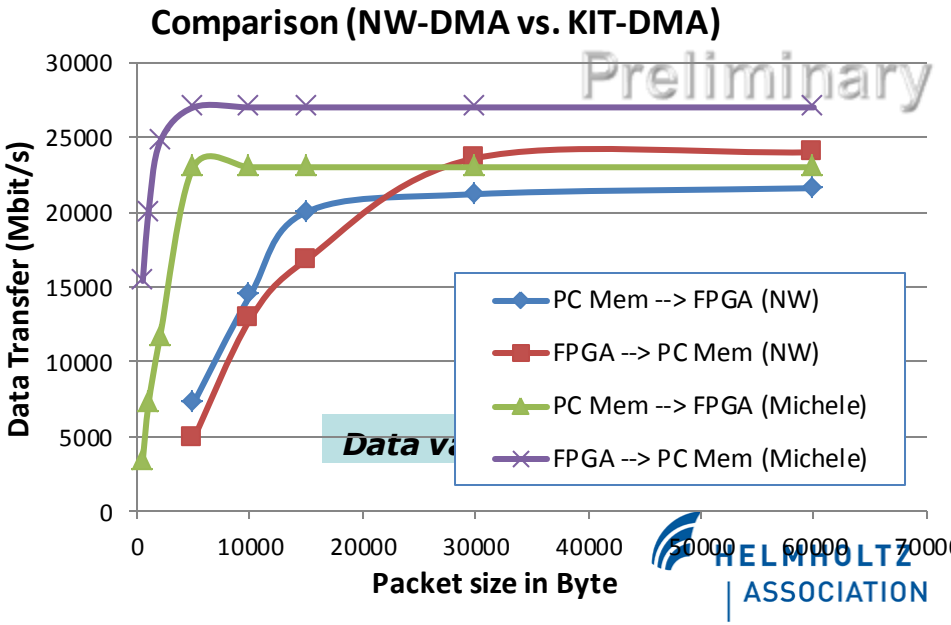
Total noise time jitter StDev < 1.7 psec

N.B. *The time resolution measured on the most advanced ASICs based on CFDs is of the order* ***of 5 ps rms****.*

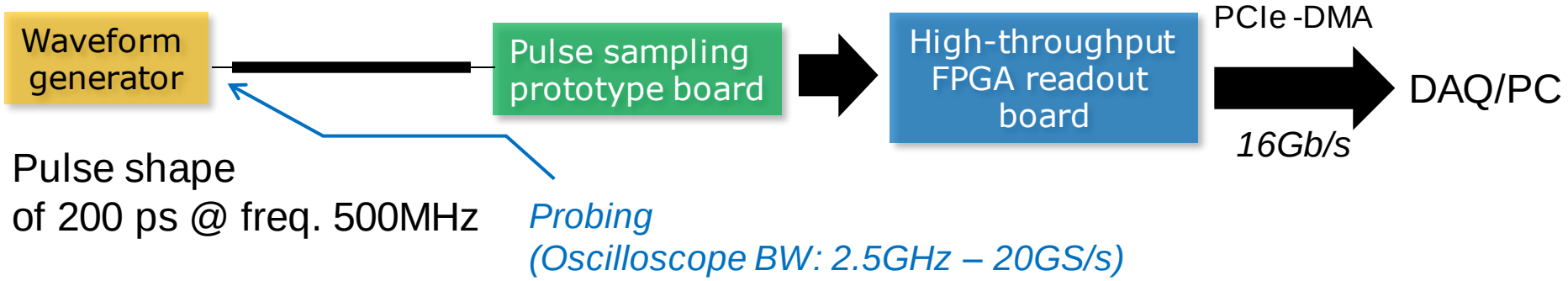
PCIe-Bus Master DMA readout architecture



- ✓Bus Master DMA operating with 8lanes PCIe @ Gen2 (250MHz)
- ✓Two individual engines for write/read from FPGA (User logic) to PC centre memory
- ✓IN and OUT FIFO-like interface (for User logic)
- ✓FIFO used to decouple the time domain between DMA and User custom logic



Fast sampling prototype board – time characterization



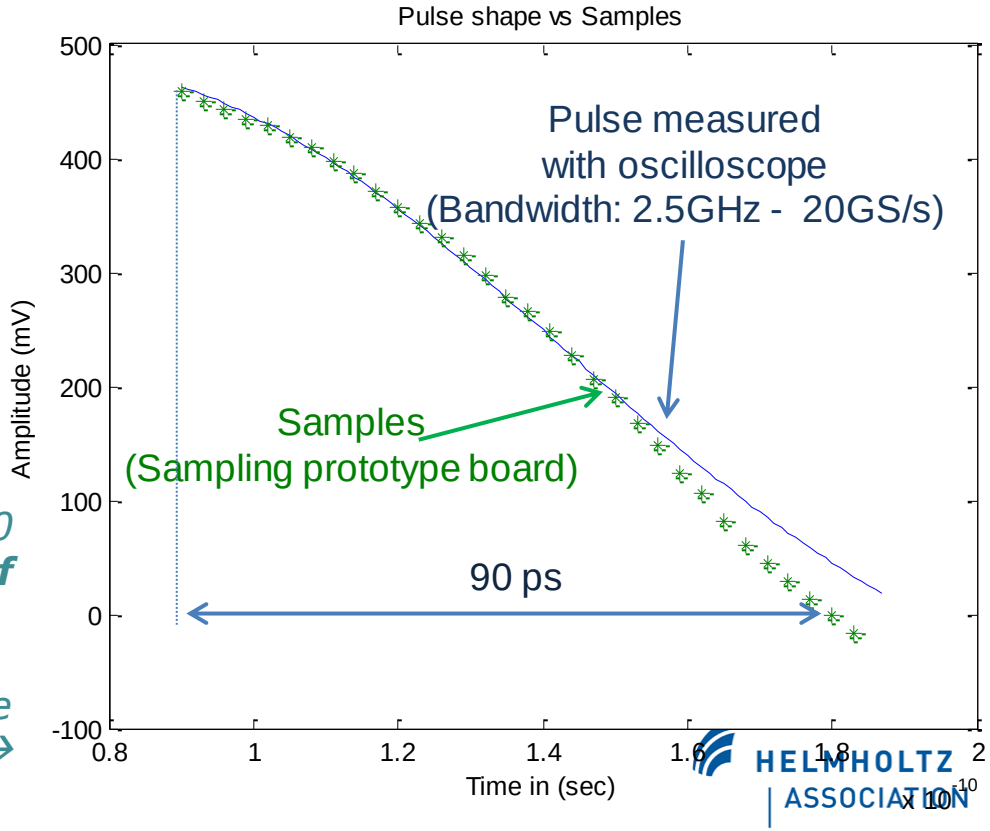
Fall pulse acquired by equivalent time sampling method (both oscilloscope and sampling prototype board)

(When the pulse occurs, a minimum settable sampling time is added by the delay chip in order to move the sampling time with a minimum time step)

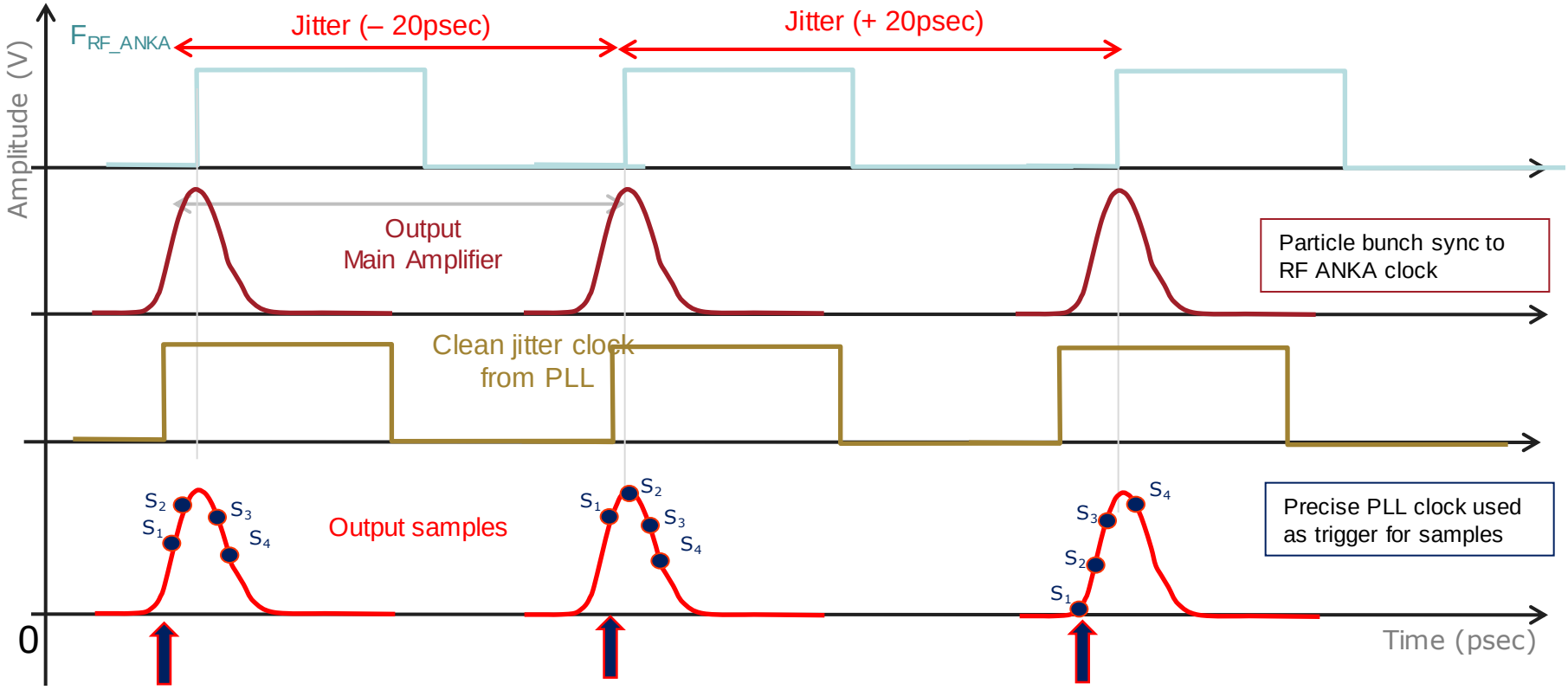
The pulse profile was obtained by 32 samples, one for each delay chip setting.

We recorded the pulse fall time by 30 samples inside 90 ps → a ***time accuracy of ~ 3 ps***

High linearity *between the sampling time (set by FPGA) and the real sampling time → Very low deterministic jitter on the board*



Picosecond time jitter estimation between bunches



Procedure:

Fast reconstruction of the analog pulse by the 4 samples (FPGA or GPU)

→ Measuring of the peak pulse amplitude

→ Measuring of the time jitter between bunches by the position of the samples in the reconstructed pulse

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