Status of the DSSC Project

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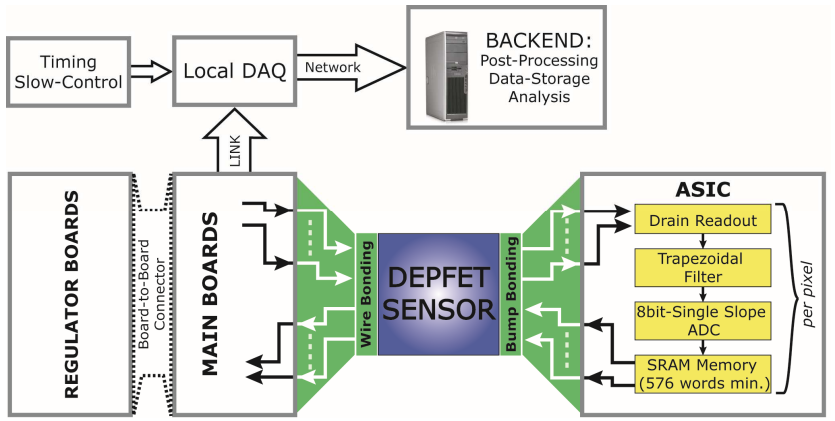
For the DSSC Collaboration

DSSC – Design Parameters

Parameter	
Energy range	optimized for 0.5 … 6 keV
Number of pixels	1024 x 1024
Sensor Pixel Shape	Hexagonal
Sensor Pixel pitch	~ 204 x 236 µm²
Dynamic range / pixel / pulse	~5000 ph @ 0.5 keV > 10000 ph @ E≥1 keV
Resolution	Single photon detection also @ 0.5 keV
Frame rate	0.9-4.5 MHz
Stored frames per Macro bunch	≥ 720 → 800
Operating temperature	-20˚C optimum, RT possible

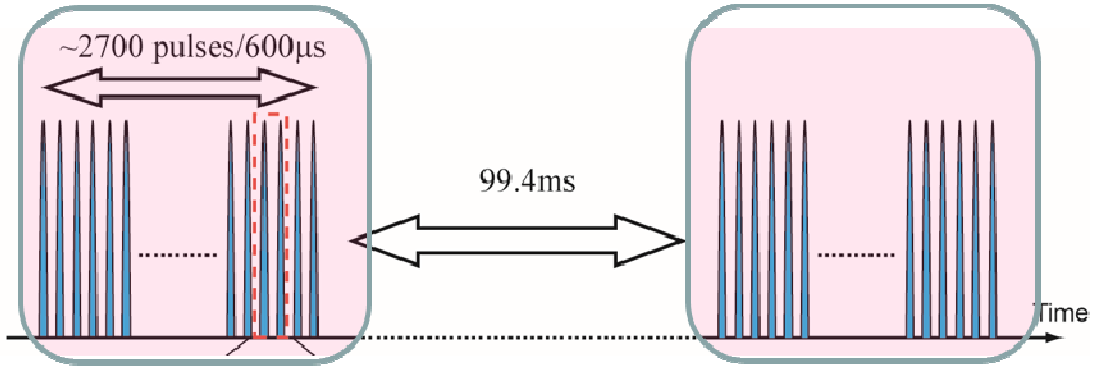
1 Mpixel camera with:

- Single photon sensitivity event at 0.5 keV
- high-dynamic range (>10000 ph/pixel)
- Frame rate up to 4.5 MHz (1 image every 220 ns)

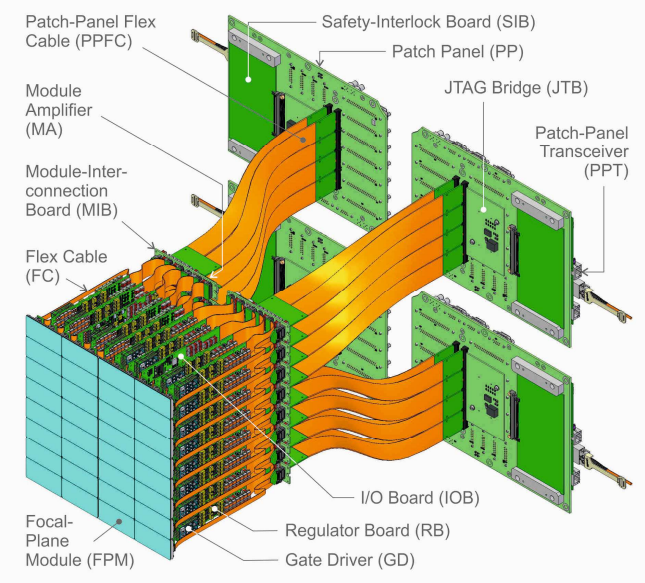


Sensor and focal plane architecture

- Non Linear DEPFET
  - Intrinsic low noise due to small internal gate capacitance
  - Intrinsic signal compression
- Mini SDD array
  - Conventional collecting anode with linear response
  - Simplified technology
  - Same geometry and entrance window of DEPFETs
- Readout concept
  - Full parallel readout
  - Analog shaping
  - 8 bit digitization (9 bit @ f<4.5MHz)
  - In-pixel SRAM
  - Data transmission during the gaps between macro-bunches
- Power cycling
  - 10.7 kW peak power
  - 240 W average power



- Focal Plane composition
  - 1024x 1024 pixels
  - 16 ladders/hybrid boards
  - 32 monolithic sensors 128x256
  - Sensor bump bonded to 8 Readout ASICs (64x64 pixels)
  - 2 sensors wire bonded to a MB
  - Dead area: ~15%



- Original Plan: DEPFET camera to be delivered in 2017
- Mini-SDD camera to be delivered by 2016

Phase II deliverables under present conditions

- We have started Phase II: 01.01.2014 – 31.12.2016

- Even if the DEPFET shows the expect performance, yield problems in large format sensors have been identified in the last semester

- Problems are still under investigation and are not completely understood. Due to the actual long production time of the DEPFET, the consortium in agreement with XFEL has decided to deliver within the next 3 years the following systems:

  - DEPFET sensor ladder camera 128 x 512: April 2015 (if pxd-8 yield is sufficiently high)

  - Mini-SDD ladder camera 128 x 512: March 2015

  - Mini-SDD full camera 1024 x 1024: June 2016

SENSOR

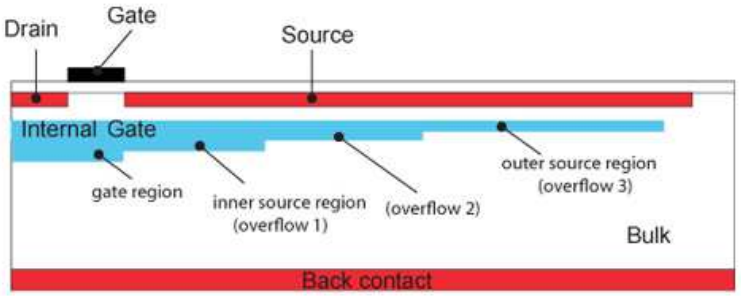
Sensor

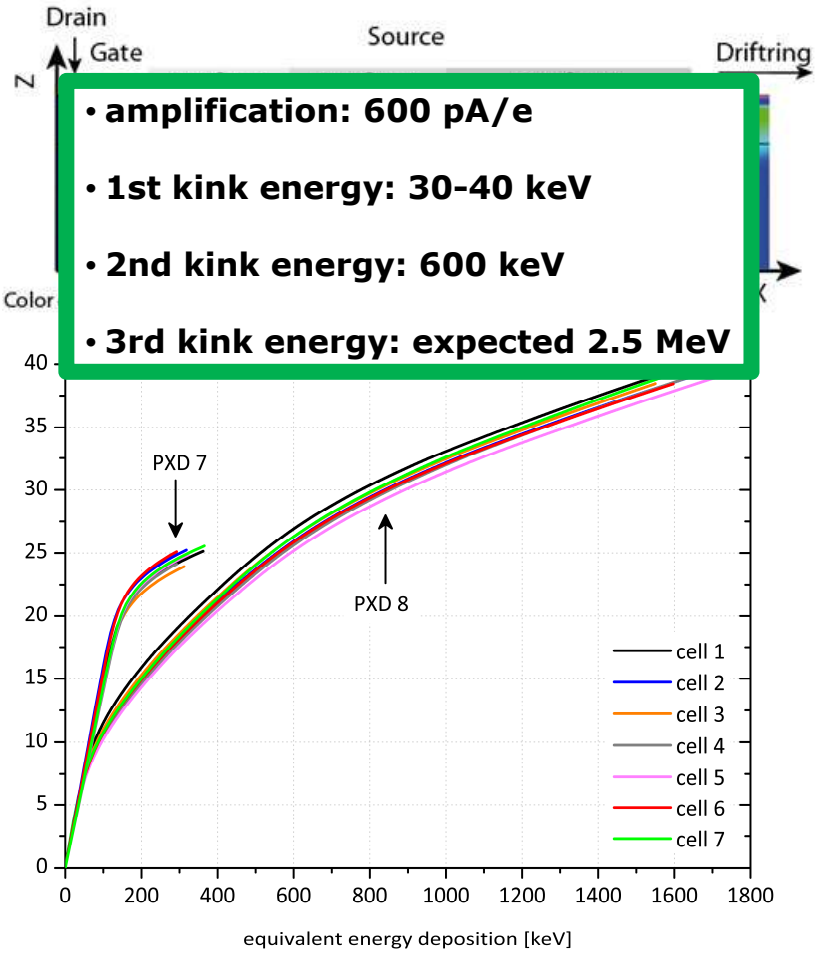
1. Pxd-8 single-pixel level
    - Homogeneity
    - Clear timing
    - Charge collection time
    - New noise measurements

2. mini-SDD sensor concept

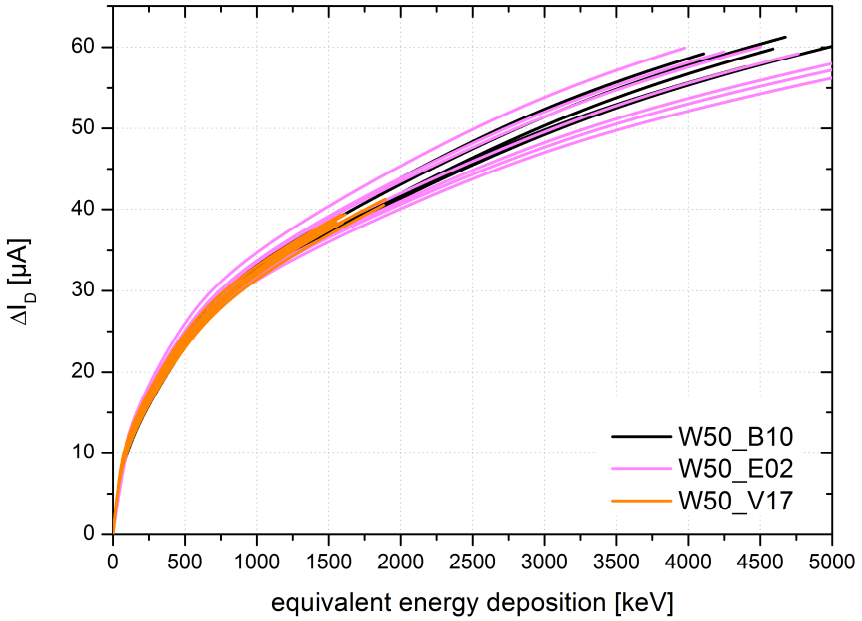
3. Preliminary DEPFET vs mini-SDD performance comparison

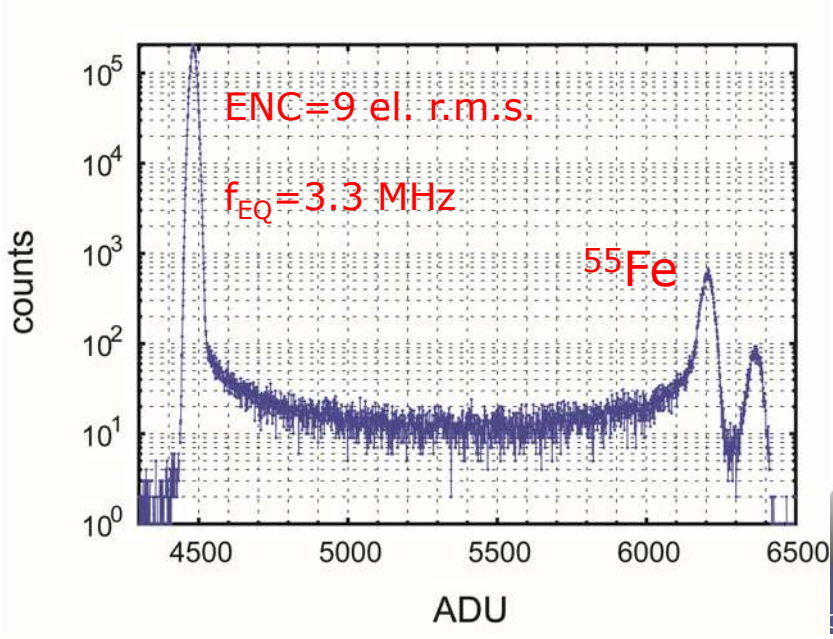
Sensor - Measured Non-linear 7-cell pxd-8 DEPFET Prototype



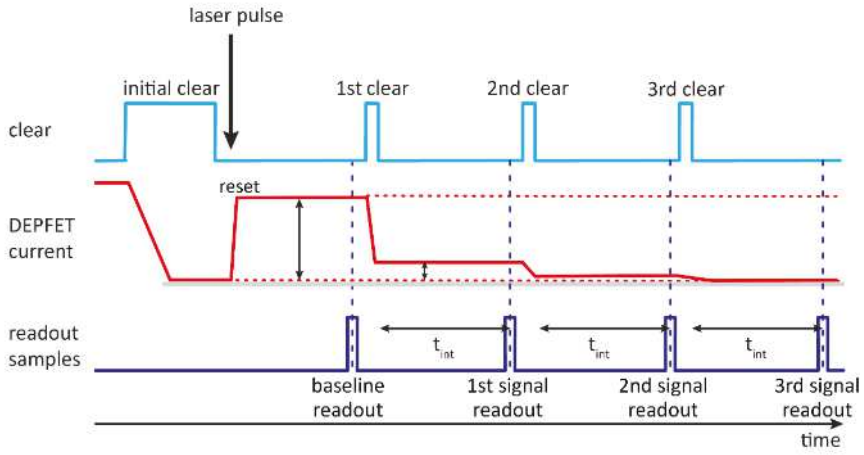


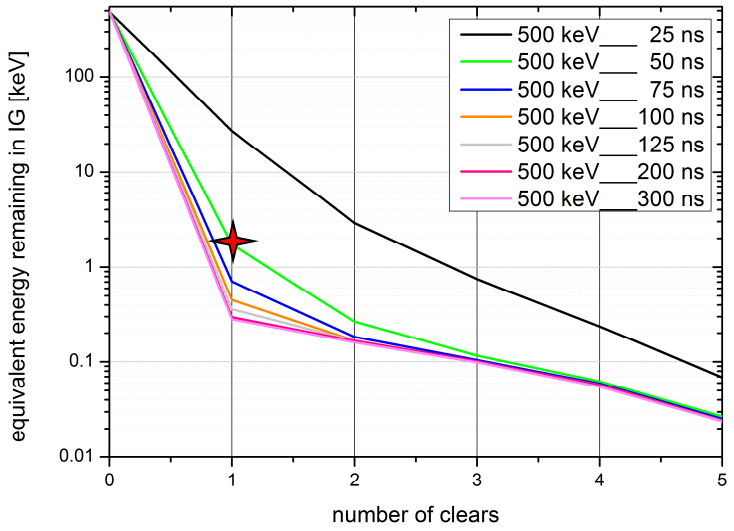
- **amplification: 600 pA/e**
- **1st kink energy: 30-40 keV**
- **2nd kink energy: 600 keV**
- **3rd kink energy: expected 2.5 MeV**

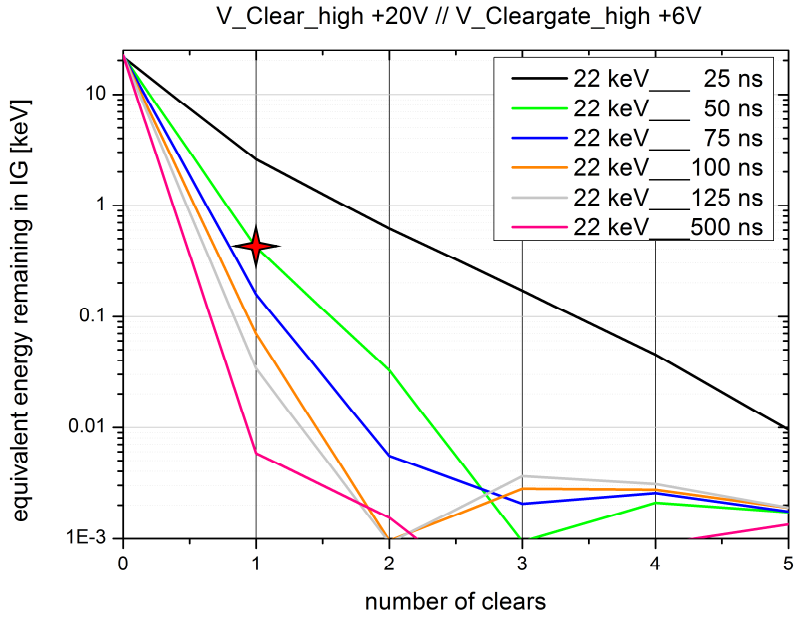


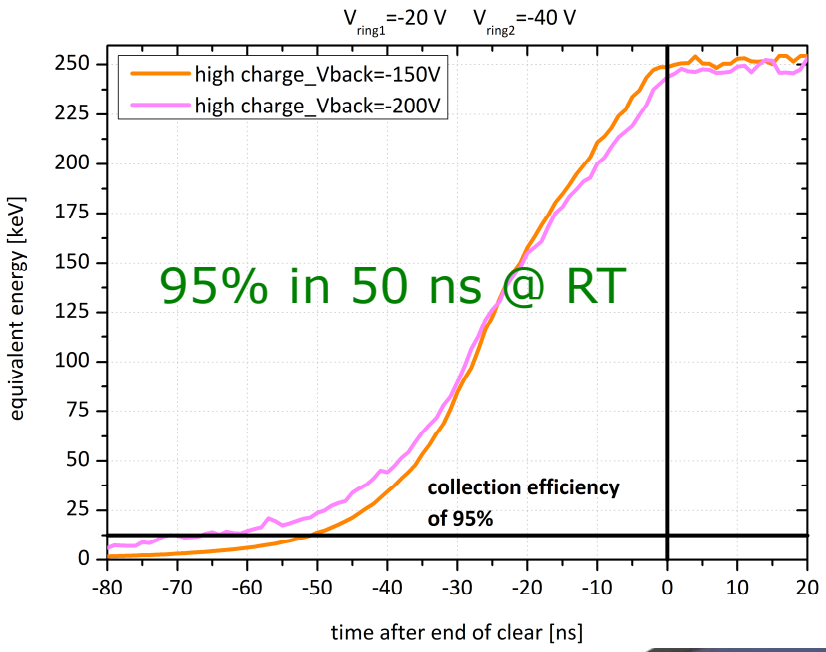


Clear time and charge collection time @ RT

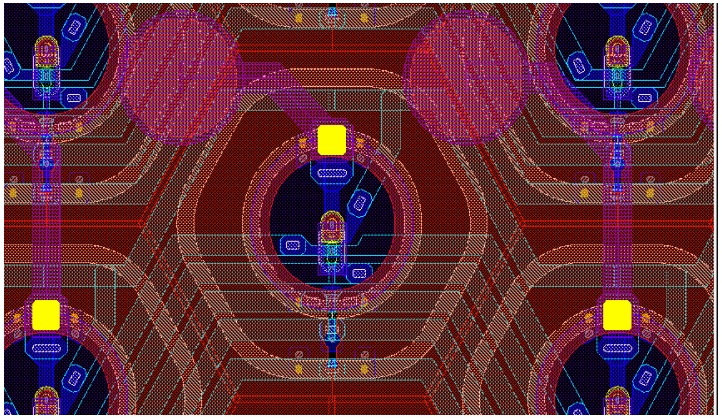




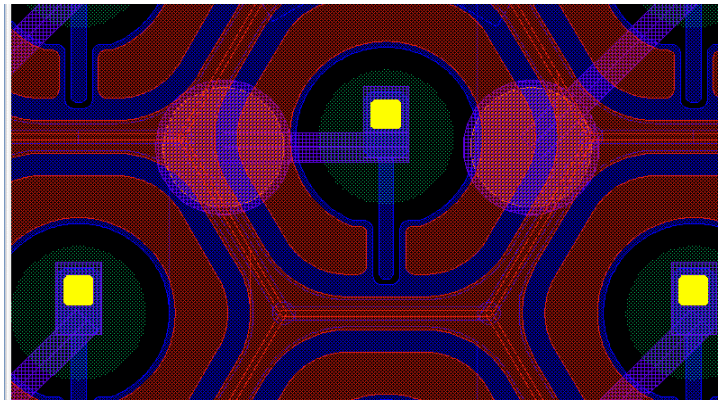




Mini-SDD sensor motivations and main characteristics



DEPFET (G. Lutz, P. Lechner)
- 2x poly, 2x Al, 1x Cu
- 11 implantations

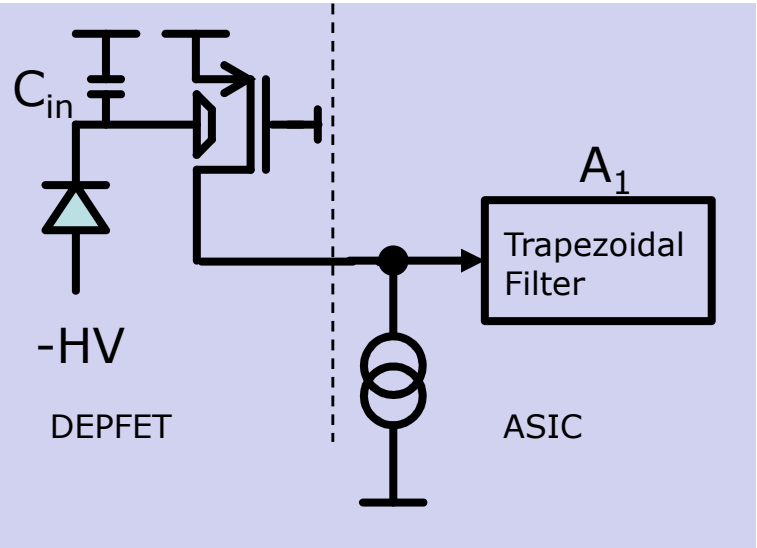


Day-Zero (R. Richter)
- 1x Al, 1x Cu
- 2(3) implantations

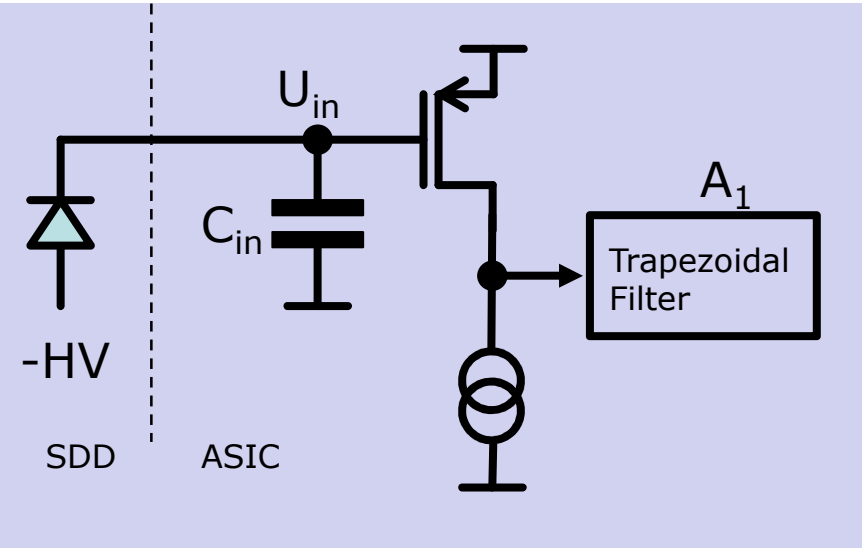
- In agreement with XFEL, the DSSC consortium has decided to design and produce a simplified sensor compatible to great extent with the DSSC system
- This sensor will have the **same geometry, the same entrance window** and the same top metallization **of the final DEPFET** sensor
- The simplified sensor has a **"short" production time** ~ 6 months
- The sensor is based on hexagonal **mini-SDD** pixels without integrated JFET. The pixel response is linear
- **The compression has to be integrated in the front-end of the ASIC**. The ASIC will be able to readout both DEPFETs and mini-SDD sensors
- Even if the mini-SDD sensor has reduced performance with respect to the DEPFET sensor, it will allow one to **perform a large fraction of the foreseen experiments at low energy**

Basic readout node configuration: DEPFET vs mini-SDD

- Charge is collected in the floating int. gate -> very low Cin (60 fF)
- The gm of the DEPFET is quite low (60 – 100 μS)-> high series noise
- The internal gate provides signal compression
- High charge handling capacitance and no voltage swing at the input of the ASIC



- Charge is collected on the anode bump bonded to an external PMOS -> Cin ~300-500 fF
- The gm of the PMOS is higher (> 1 mS)-> low series noise
- In this simple scheme the response is linear -> no signal compression
- Big swing on the ASIC input node

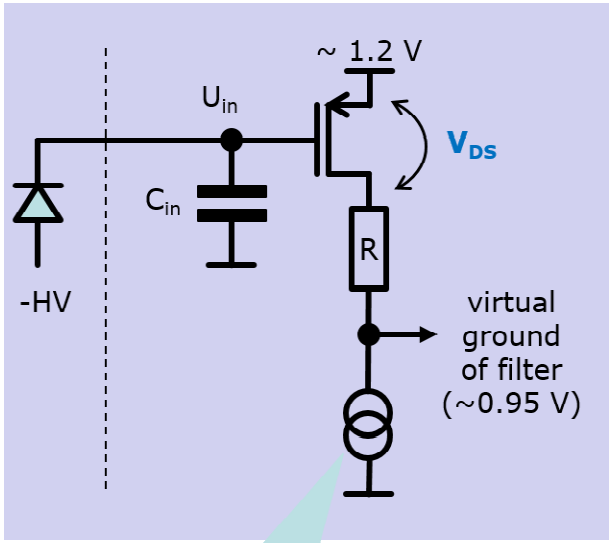


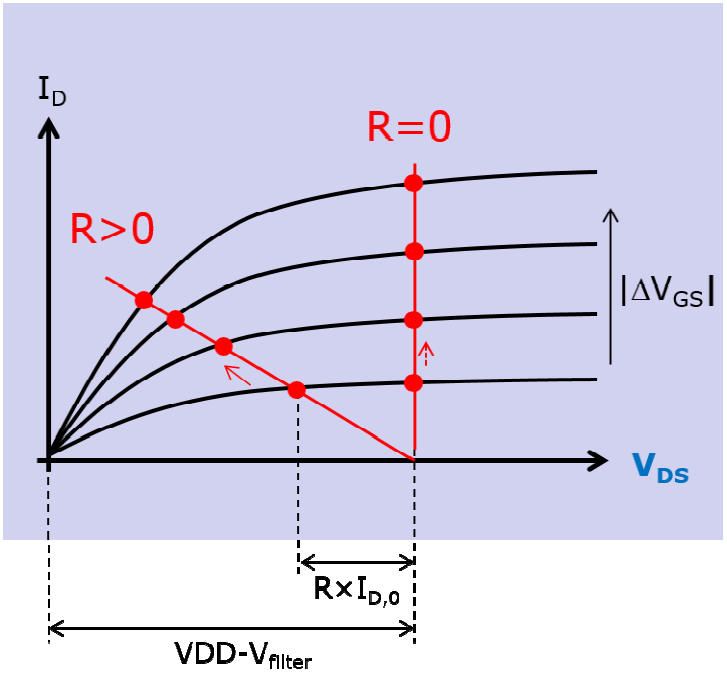
- At the foreseen operating speed the noise of the front end is dominated by the white series noise
- For some operating modes the noise of the front-end is not dominant in DSSC

$$ENC^2 \sim \frac{1}{gm} \cdot A_1 \cdot C_{IN}^2$$

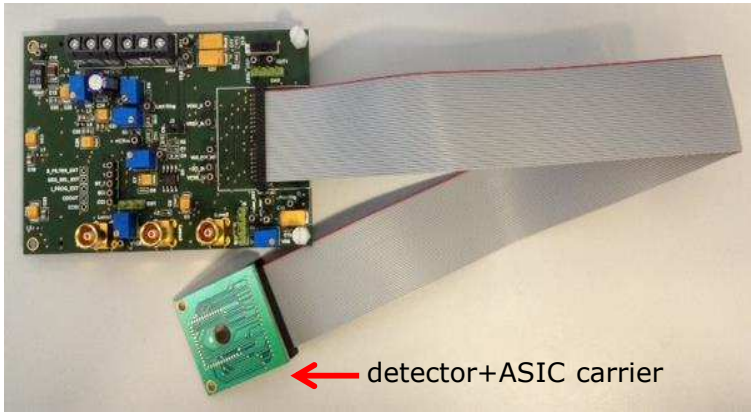
Mini-SDD front-end

- The non linear response can be implemented by the first stage of the front-end
- Two possible solutions have been proposed by Milano and Heidelberg
- A first single channel prototype of the Milano architecture with limited dynamic range has already been tested with a single SDD
- The tested prototype has been introduced in the full-format ASIC F1 in parallel to the DEPFET front-end
- Test Mini-ASIC containing advanced prototypes of both circuits have been designed and are in production





First prototype of mini-SDD front-end

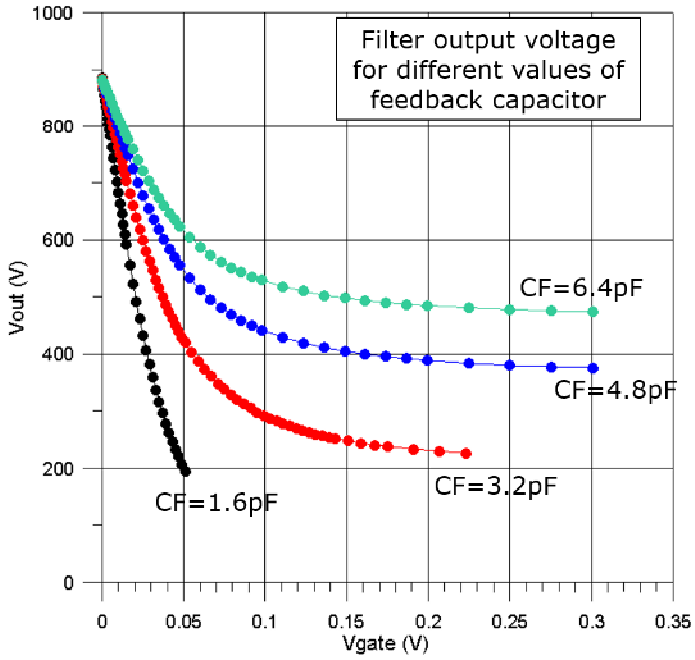


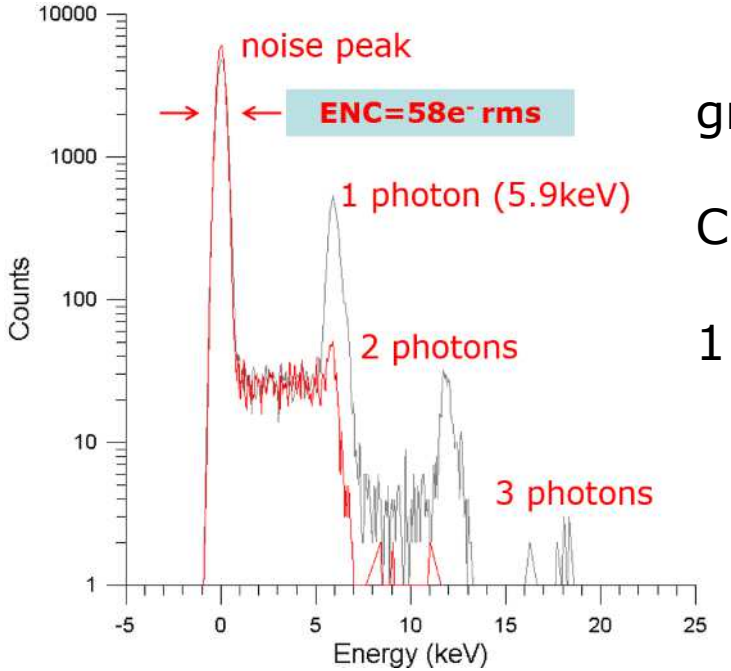
Proof of principle verified

The Cin is dominated by the wire bonding pad

The expect Cin value for the bumped version is ~400-500 fF

An optimized circuit has already been designed and submitted





gm~1.5 mS

C_{in}~1pF

1 MHz

Pxd-8 DEPFET vs mini-SDD: preliminary estimate (1/3)

DEPFET

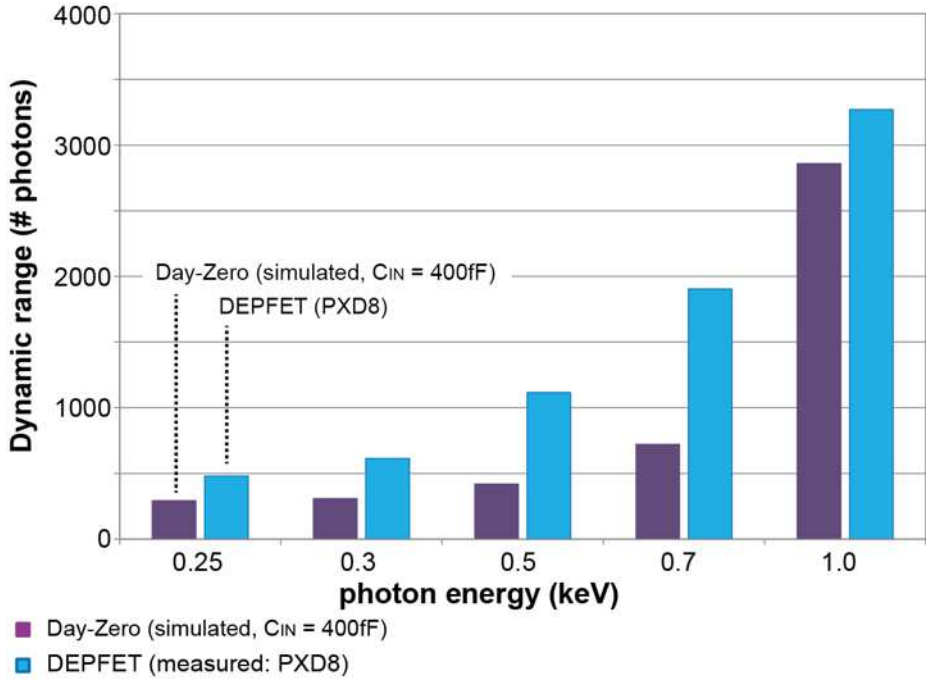
- DEPFET noise measured on pxd-8 pixels with ASTEROID ASIC
- A safety factor of 2 in power has been considered
- 9.8 el. rms @ 3.3 MHz -> 14 el. with safety margin
- Noise scaled with readout speed
- Total noise calculated considering F1 ASIC specs
- Dynamic range calculated on measured pxd-8 curve

Mini-SDD

- Noise measured on single channel prototype (low dynamic range) and a single SDD
- 132.5 el. rms @ 5 MHz with C_{IN}=1 pF
- Noise scaled with readout speed and C_{IN}
- $C_{IN,estimate}$~400-500 fF
- Total noise calculated considering F1 ASIC specs
- Dynamic range calculated with simulations on improved front-end (not on F1)
- Cross talk effects not considered

Pxd-8 DEPFET vs mini-SDD: preliminary estimate (2/3)

Energy [keV]	ADC jitter Noise [el.]	DEPFET pxd-8				mini-SDD			
		dynamic range [ph.]	ENC [el.]			dynamic range [ph.]	ENC [el.]		
			4.5 MHz	2.2 MHz	0.9 MHz		4.5 MHz	2.2 MHz	0.9 MHz
0.25	4.7	480	NA	13	5.7	294	NA	37.2	26
0.3	5.6	615	NA	14.2	6.2	309	NA	40.3	20.1
0.5	9.3	1116	18.4	12.2	8	420	62.6	35.1	24.4
0.7	13.1	1905	21.7	14.4	9.5	722	60.2	41	28.1
1	18.7	3270	26	11.3	11.3	2859	71.6	32.8	32.8
1.5	28	> 4000	21.1	13.9	13.9	2022	58.8	39.4	39.4
2	37.3	> 7000	24.4	16	16	1429	71.6	32.8	32.8
3	56	> 10000	19.5	19.5	19.5	1011	58.8	39.4	39.4



Pxd-8 DEPFET vs mini-SDD: preliminary estimate (3/3)

Energy [keV]	ADC jitter Noise [el.]	DEPFET pxd-8				mini-SDD			
		dynamic range [ph.]	ENC [el.]			dynamic range [ph.]	ENC [el.]		
			4.5 MHz	2.2 MHz	0.9 MHz		4.5 MHz	2.2 MHz	0.9 MHz
0.25	4.7	480	NA	13	5.7	294	NA	37.2	26
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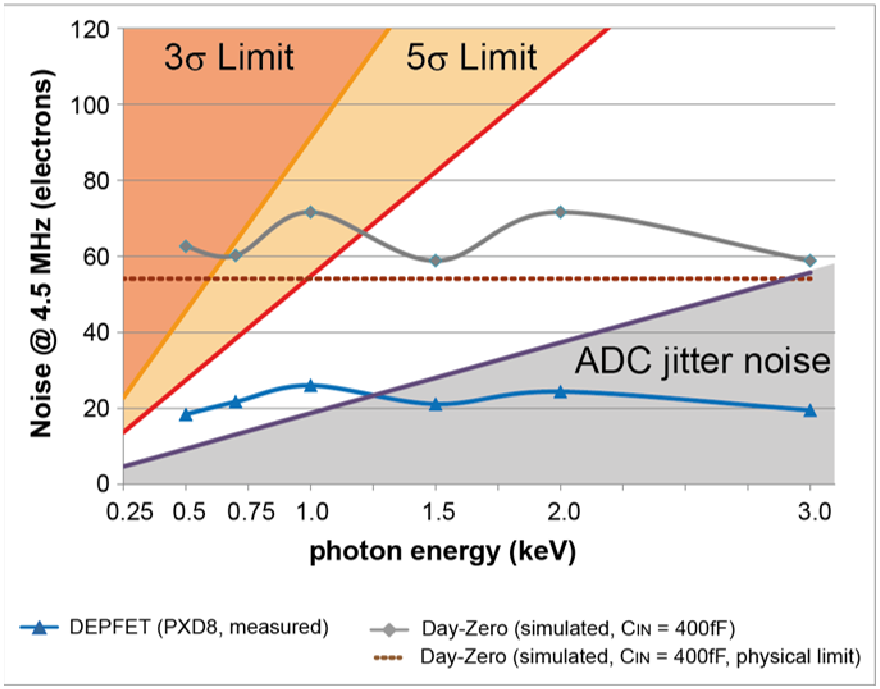
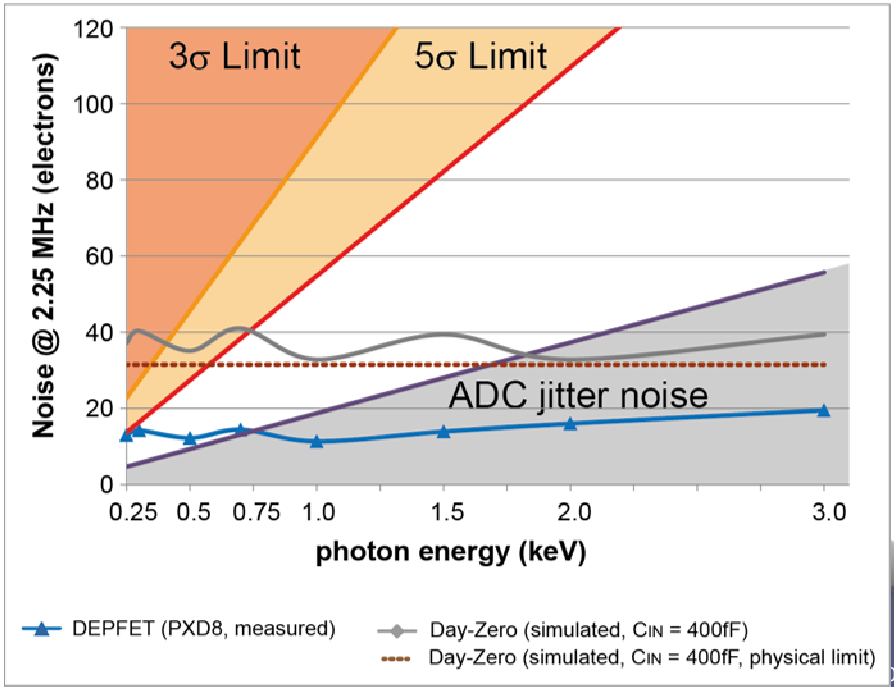




ASIC

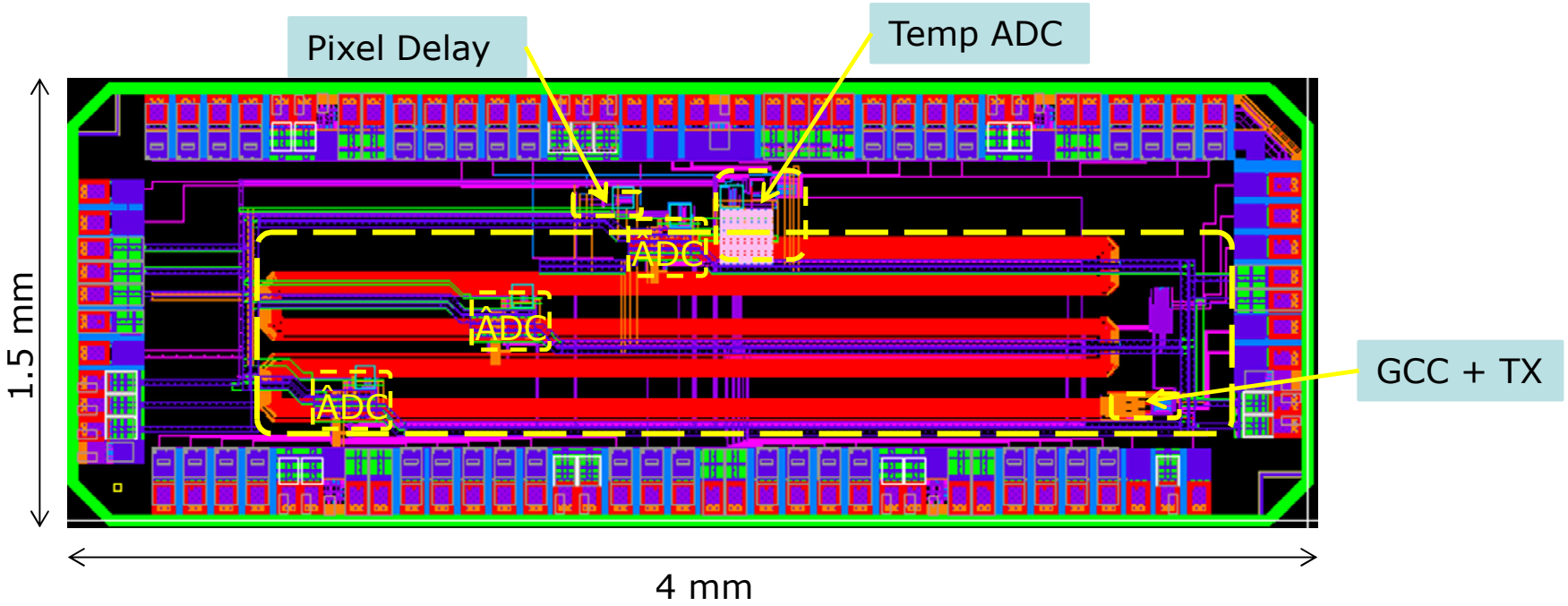
ASIC activity overview

- Chip Characterizations (DESY, HD)
  - Further measurements on MM (8x8) chips
  - Test of ADC test chip @ DESY

- ASIC design
  - Work on Day-0 frontend (HD)
  - Work on Day-0 frontend (Milano)

  - F1 & test chip submission

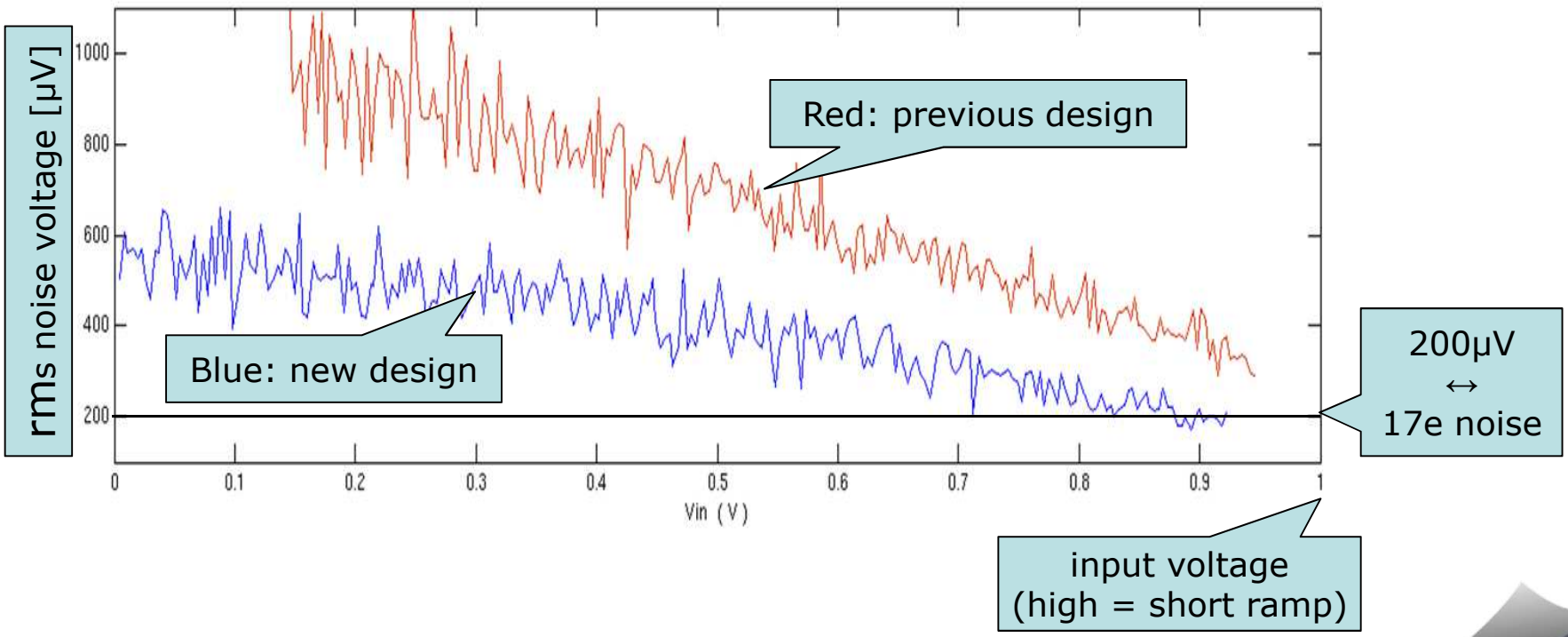
Reminder: ADC4 Test Chip



- ADC Block: - 3 pixel-level ADCs, new comparator design and global bias generation
  - New Counter - TX interface
  - 13mm long transmission line representing 64 pixel column of F1
- Temp ADC with Diode (P^+ in Nwell diode, 180 μm^2)
- Pixel Delay (Single pixel delay block)
- Note: **This ADC version is used in F1**

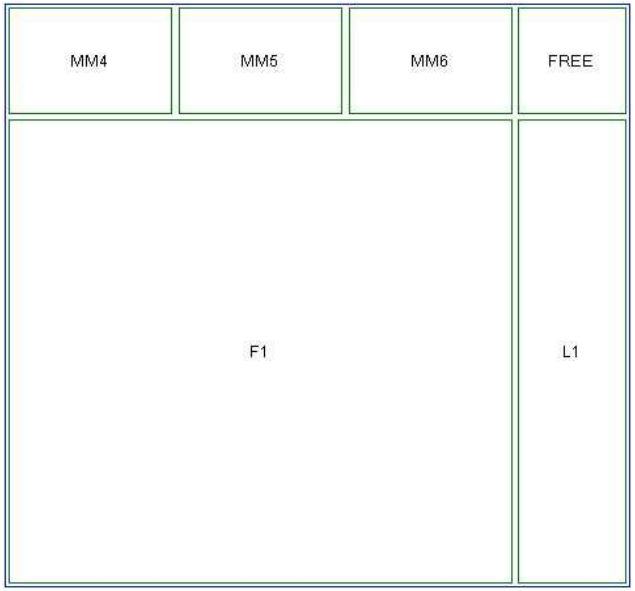
ADC Noise

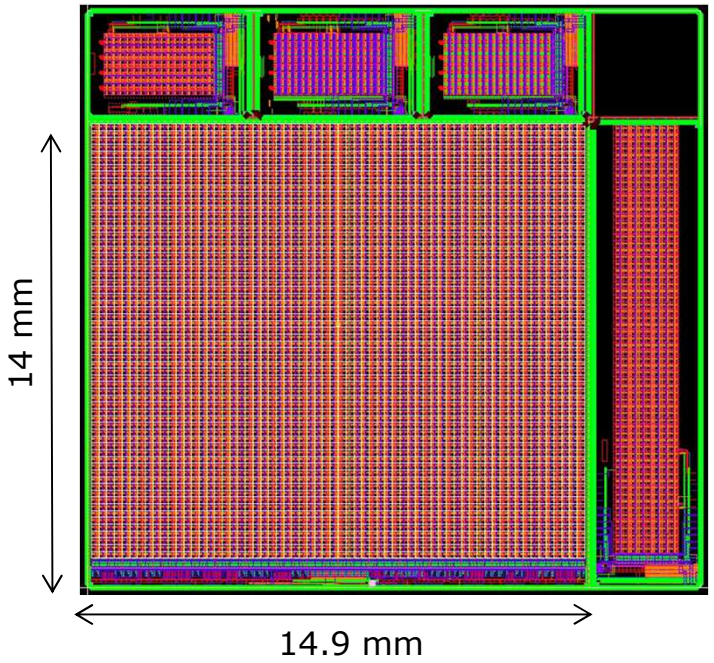
- Has been improved mainly by more current in ADC comparator input stage
- Significant improvement to rms<1/5 LSB (1 LSB = 3.125 mV)
- Noise smaller for high voltages (small # photons) because ramp is short
  - 200µV ~ 1/15 LSB = 1/15 Photon (1keV) ~ 17e noise



Engineering run: Chips submitted

Chip	Pixels	FE	ADC	RAM	Comment
F1	64×64	DEP+D0(MI1)	GCC	800	
L1	8 ×63	DEP+D0(MI1)	Count	800	
MM5	8×16	DEP+D0(MI1)	GCC	400	pixel same as F1
MM6	8×16	D0 (MI2)	GCC	400	Improved D0
MM7	8×16	D0 (HD1)	GCC	400	D0 from HD

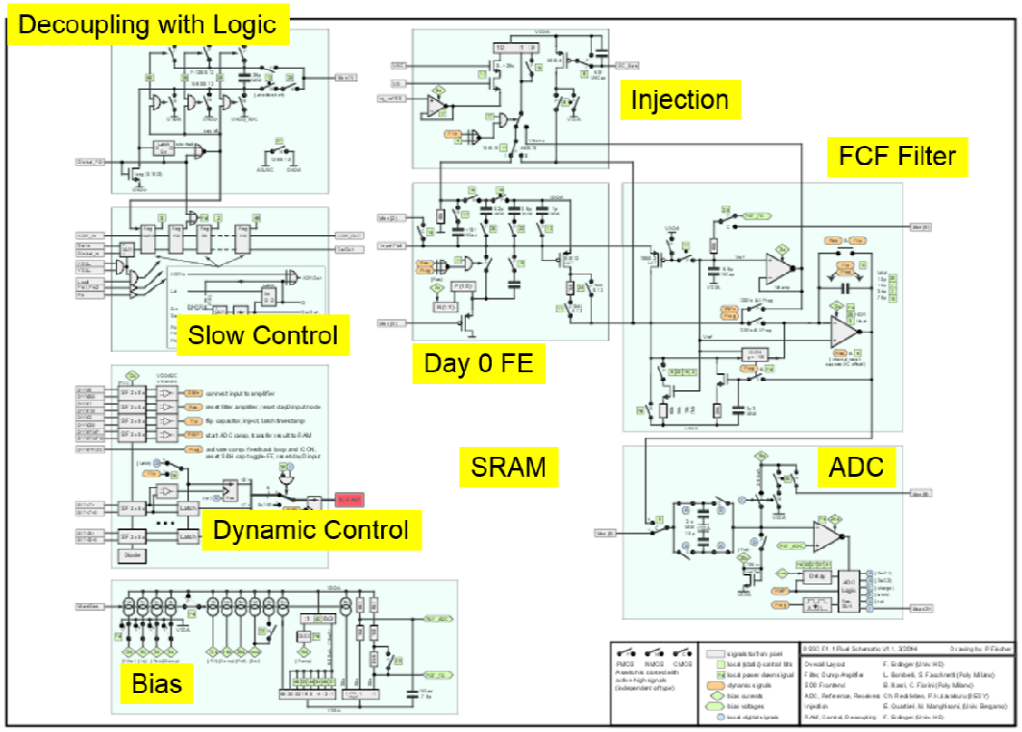


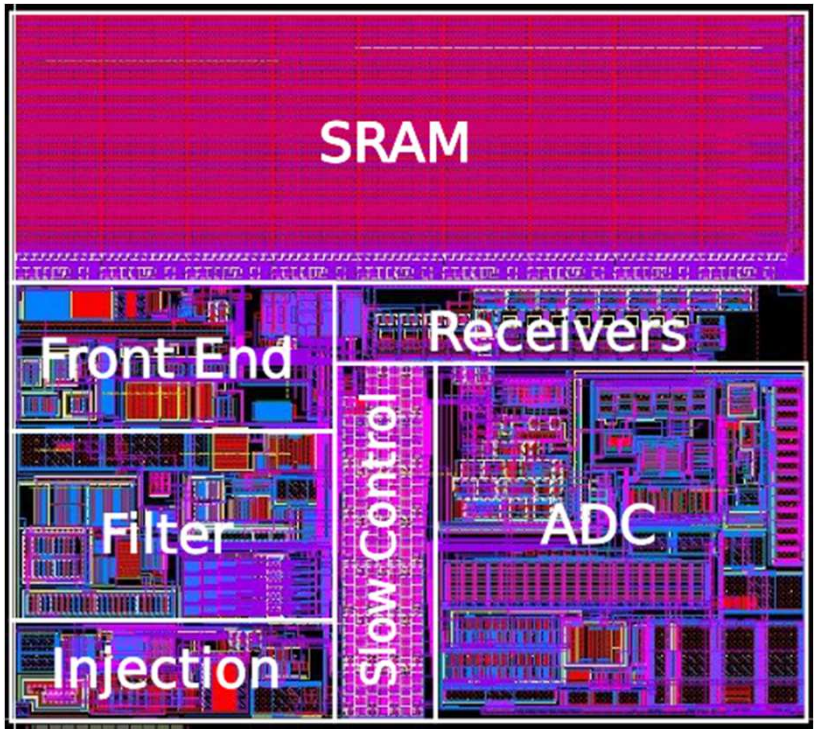


Reticle size ~ 18.5 × 17.6mm^2

- Production is on 8 inch wafers
- Depending on fiducial area, we expect **61 – 69** chips / wafer → **~600 chips**
- **The designed has been submitted to CERN in April. Production can start anytime**

F1 Pixel Schematic & Layout





E1 (M7):

- Power
- MIM Cap Connections
- Fill limited by DRC rule Density to < 70%

MA (M8):

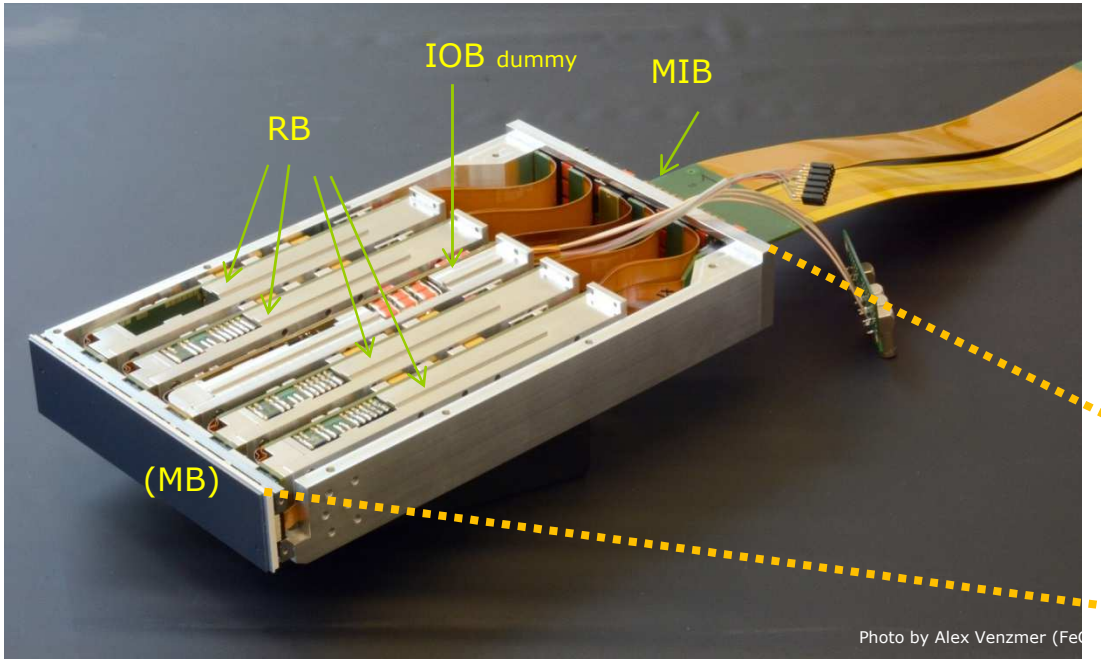
- Bump
- Power (doubles E1 busses)
- Fill limited by spacing. Bump blocks routing

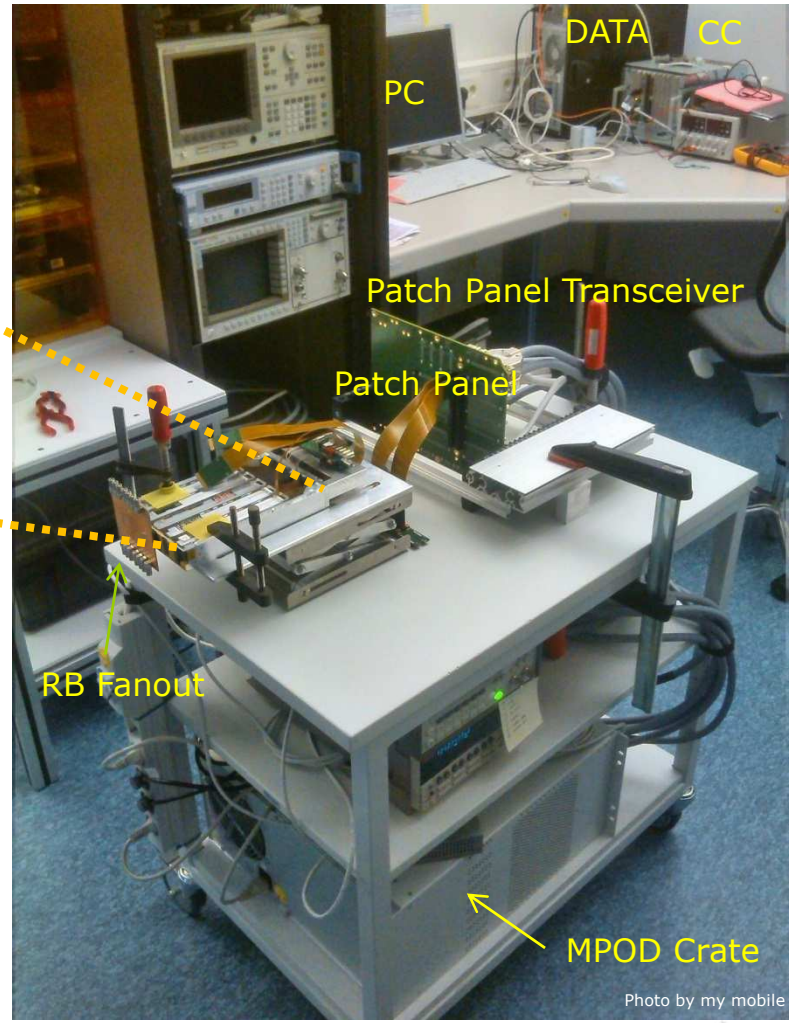
Integration & Ladder Camera

Integration WP and Ladder Camera

- Design modification and start of production of:
  - Camera-Head Components
  - Components of Patch-Panel Electronics
  - Cables & Crates
- finished Tests of Safety-Interlock Breadboard System & started PCB Design
- finalized Setup of PM-5 Test Stand
- Change in strategy:
  - realization of ladder-camera instead of quadrant camera
  - The ladder camera can be equipped with DEPFETs or mini-SDD

Test stand / Ladder Camera Hardware





Top:

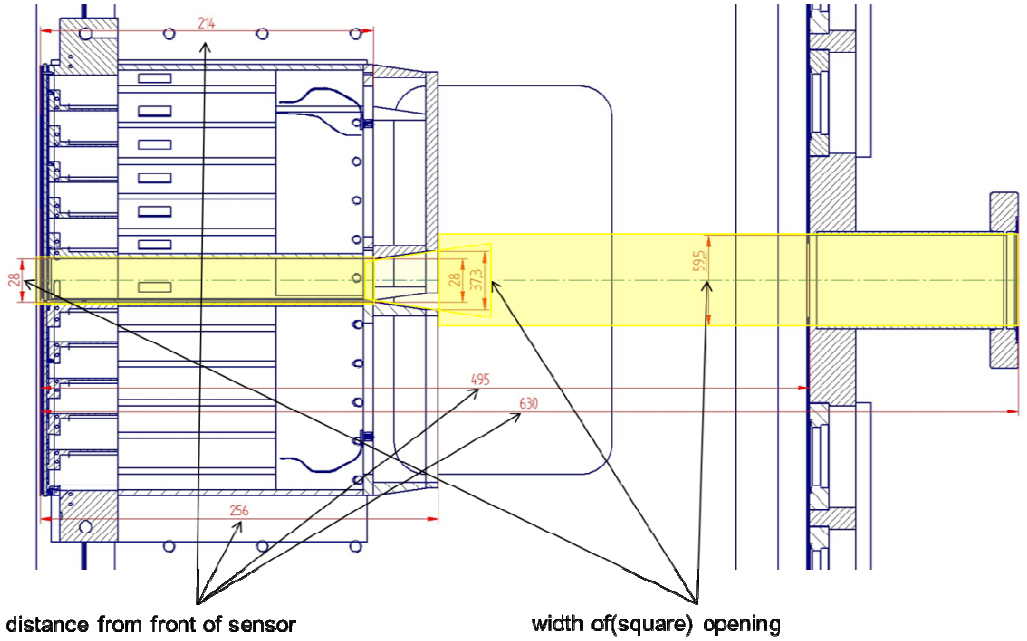
Complete DSSC ladder setup equipped with an IOB dummy board and bare MB.

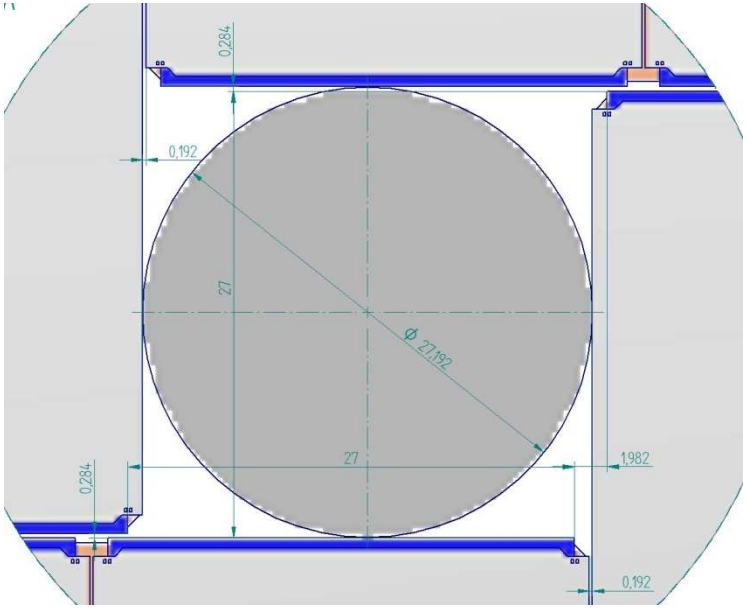
Right:

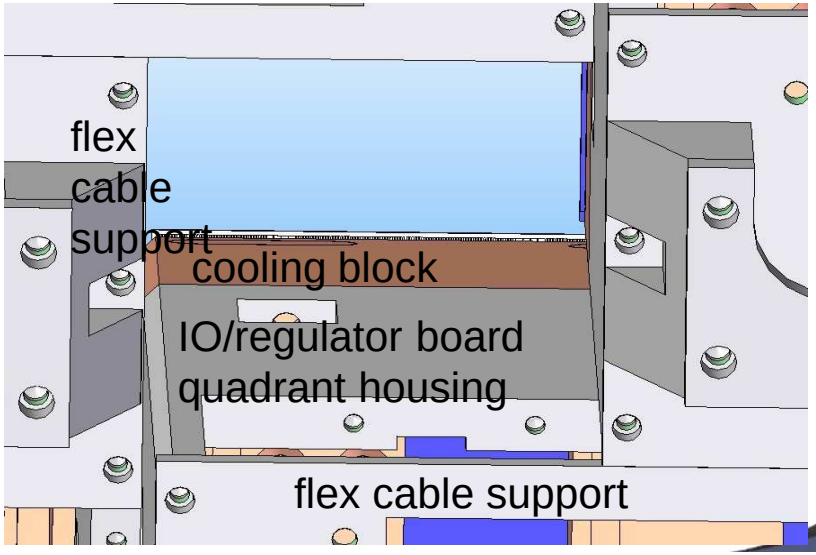
The RBs test setup at DESY FeC Laboratory

1M Module

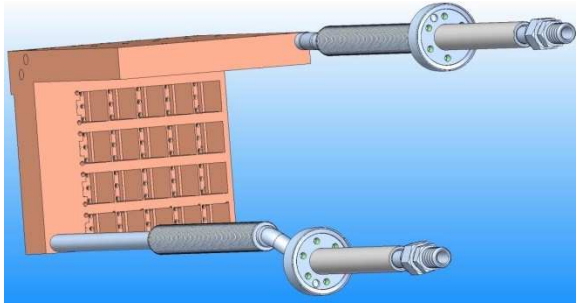
- Beam Path Details discussed with XFEL
- Turned out the “biggest hole” case was the more critical
- XFEL change request incorporated

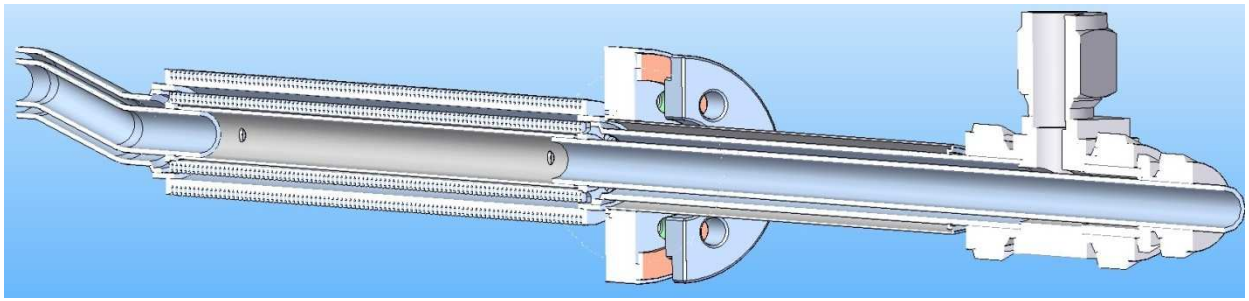




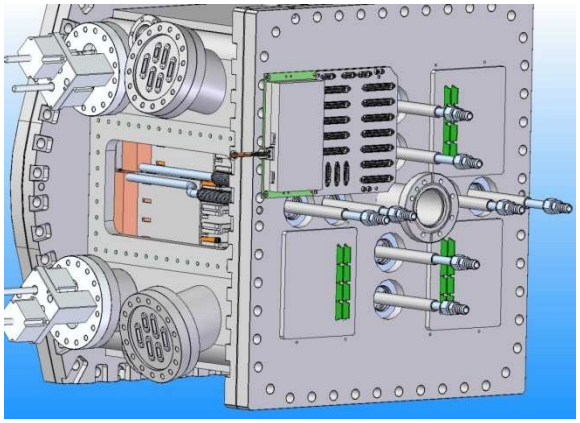


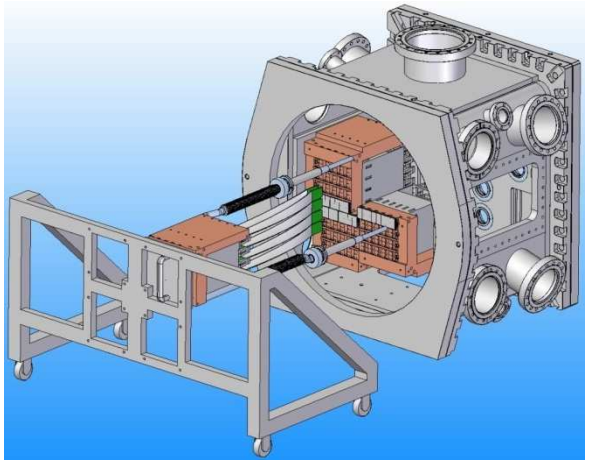
1M Module

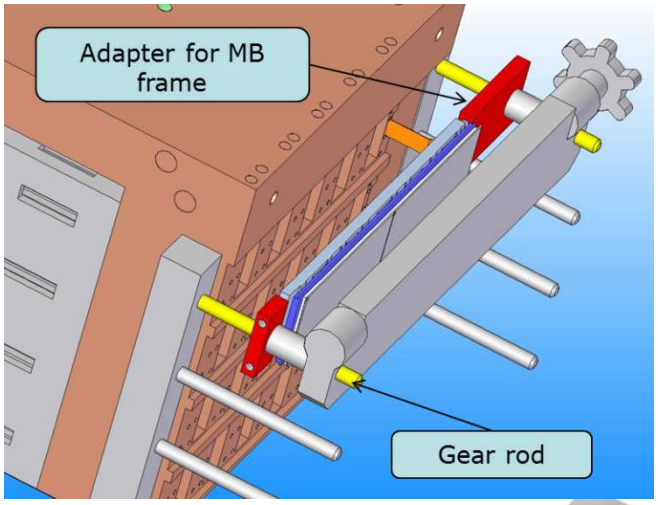




- Working on detailed assembly procedure & tools
- Double-walled coolant pipes to be prototyped
- Integration of sensor assembly into prototype trialed
- Sensor assembly and quadrant handling tools designed







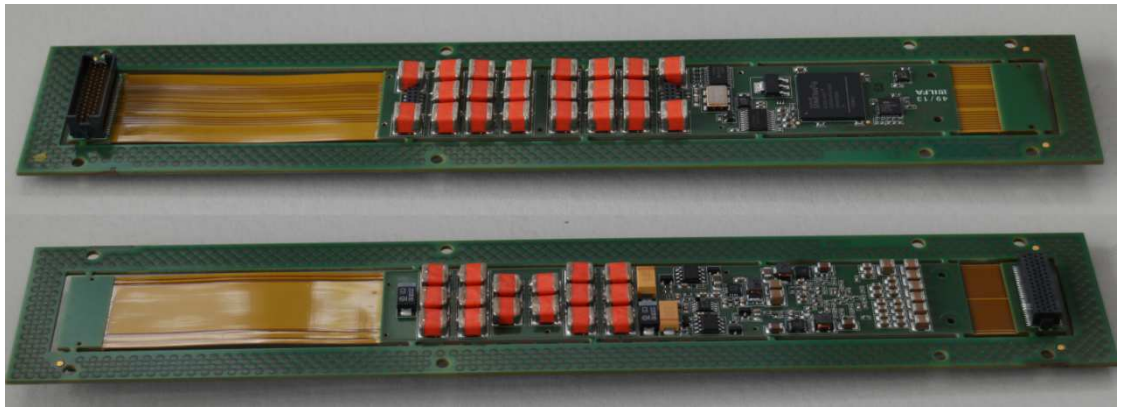
DAQ

DAQ

- 6 I/O pre-series board tested
- Hardware for quadrant-size tests available
- Last modifications towards final production (almost) implemented
- Firmware and Software developmet for PPT has contnued including: full speed data transmission, adevanced remote debug and C&C timing
- Good progress on Karabo SW integration

Test Setup

- Full-chain test setup incl C&C crate and PC data sink (ZITI)
- Equipment also available at DESY



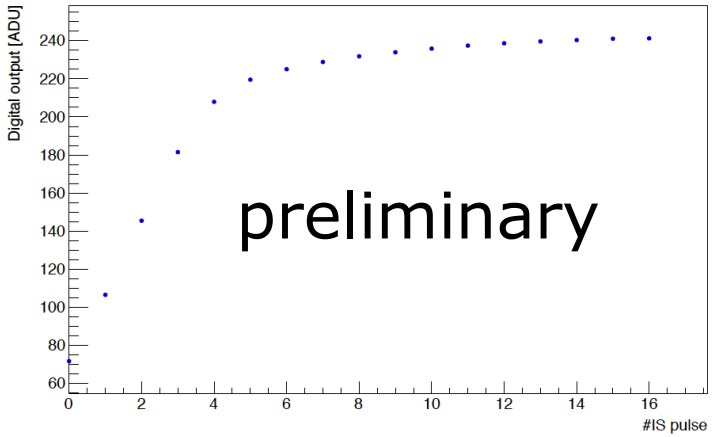
I/O board

- 6 cards delivered and tested
- 2 bugs still to fix (part orientation, bad pin)
- One ASIC unusable
- CAP mezzanine to be ordered

Calibration & Simulation

Calibration & System Simulation

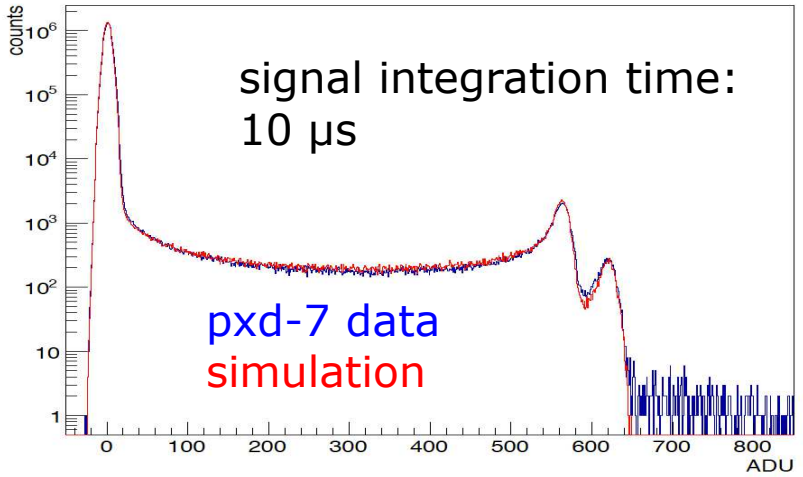
- Experimental calibration of NLSC of DSSC prototype test set-up
  - optimization of test set-up operation
  - elimination / assessment of systematic effects



- NLSC calibration strategy for ladder system and final system
  - X-ray line(s) for offset and gain calibration
  - scan of full dynamic range
    laser pulses: viable for pxd-8 and day-0
    (in progress with XFEL laser group: definition of set-up)

- System simulation
  - charge sharing and charge collection timing effects on spectral response and photon counting probabilities

- Calibration software
  - Upgrade of bin boundary / width determination
  - option to use input signal value, no assumption on linearity



Summary

SENSOR
- Charge collection time and clear time of pxd-8 DEPFET has been measured
- Noise behavior of pxd-8 DEPFET has been measured
- The development of a mini-SDD based sensor has started

ASIC
- Further Characterization of Test Chips ADC_4 and MM4
- F1 full format ASIC has been submitted. Both DEPFET and mini-SDD front end are present
- MM ASICs with optimized mini-SDD front-end have been submitted

CAMERA HEAD Camera-Head & PP Electronics component are in production
- Tests of Safety-Interlock Breadboard System are completed and PCB design has started
- finalized Setup of PM-5 Test Stand

LADDER CAMERA
- Build-up the back-end setup has started
- Preliminary test on PPT has been accomplished

MECHANICS
- Beam Path Details defined
- detailed assembly procedure & tools have been defined

DAQ
- Hardware for quadrant-size tests available
- Last modifications towards final production implemented
- Good progress on Karabo SW integration

CALIBRATION
- Optimization of test setup operation
- Strategy to calibrate the ladder with DPEFET and mini-SDD is under development
- Upgrades in system simulation and calibration software

BACKUP

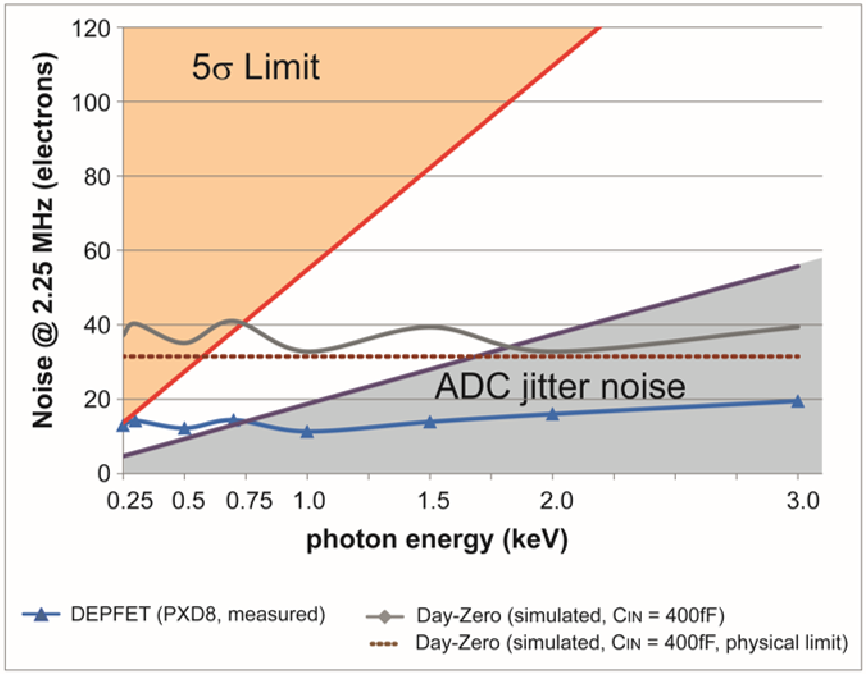
Achievements and Progress Report

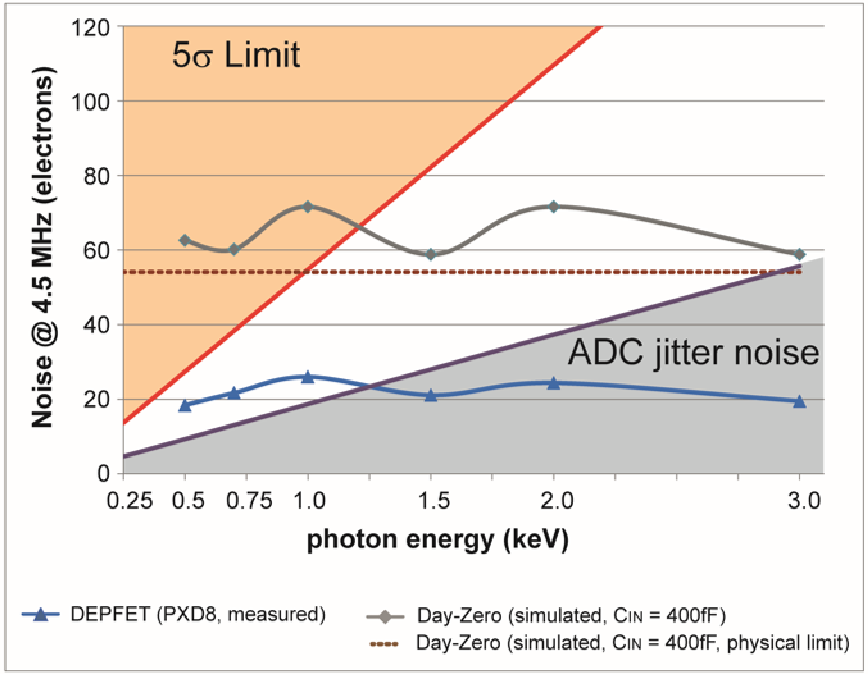
Mini-SDD sensor motivations and main characteristics

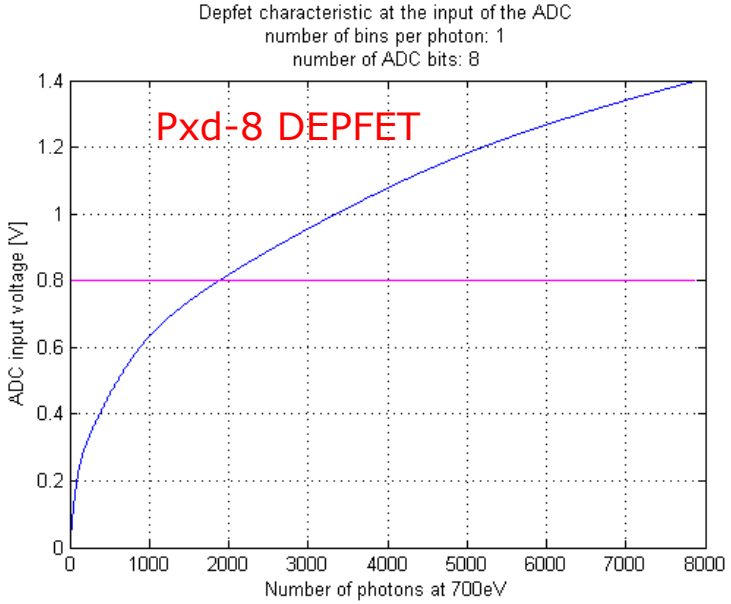
- In agreement with XFEL, the DSSC consortium has decided to design and produce a simplified sensor compatible to great extent with the DSSC system
- This sensor will have the same geometry, the same entrance window and the same top metallization of the final DEPFET sensor
- The simplified sensor has a “short” production time ~ 6 months
- The sensor is based on hexagonal mini-SDD pixels without integrated JFET. The pixel response is linear
- The compression has to be integrated in the front-end of the ASIC. The ASIC will be able to readout both DEPFETs and mini-SDD sensors
- Even if the mini-SDD sensor has reduced performance with respect to the DEPFET sensor, it will allow one to perform a large fraction of the foreseen experiments at low energy

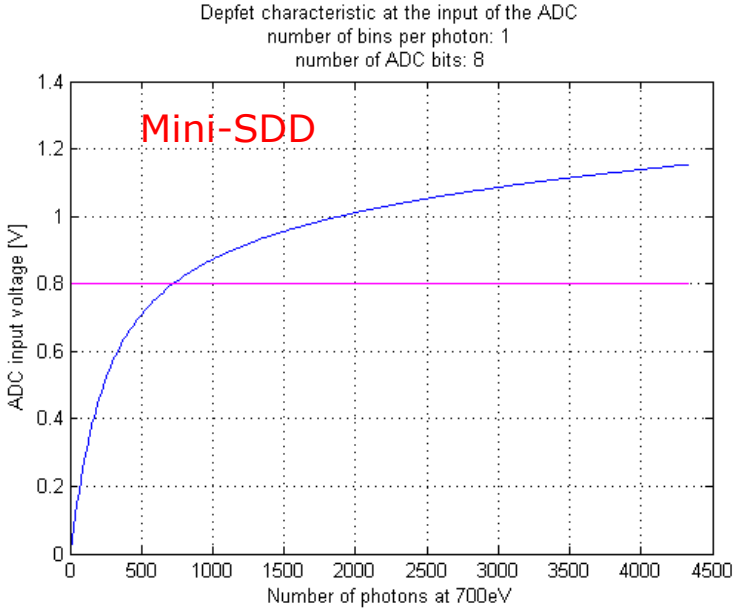
Pxd-8 DEPFET vs mini-SDD: preliminary estimate (3/3)

Energy [keV]	ADC jitter Noise [el.]	DEPFET pxd-8				mini-SDD			
		dynamic range [ph.]	ENC [el.]			dynamic range [ph.]	ENC [el.]		
			4.5 MHz	2.2 MHz	0.9 MHz		4.5 MHz	2.2 MHz	0.9 MHz
0.25	4.7	480	NA	13	5.7	294	NA	37.2	26
0.3	5.6	615	NA	14.2	6.2	309	NA	40.3	20.1
0.5	9.3	1116	18.4	12.2	8	420	62.6	35.1	24.4
0.7	13.1	1905	21.7	14.4	9.5	722	60.2	41	28.1
1	18.7	3270	26	11.3	11.3	2859	71.6	32.8	32.8
1.5	28	3614	21.1	13.9	13.9	2022	58.8	39.4	39.4
2	37.3	7000	24.4	16	16	1429	71.6	32.8	32.8
3	56	10000	19.5	19.5	19.5	1011	58.8	39.4	39.4






Depfet characteristic at the input of the ADC
number of bins per photon: 1
number of ADC bits: 8
Pxd-8 DEPFET
ADC input voltage [V]
Number of photons at 700eV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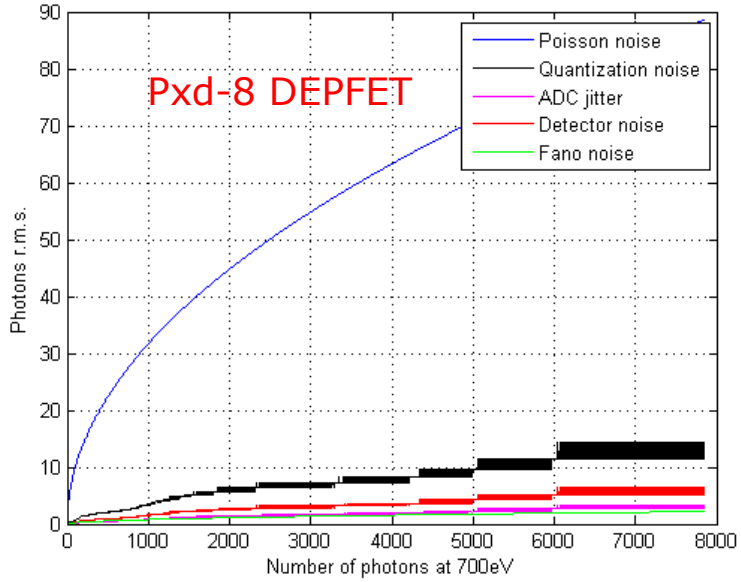
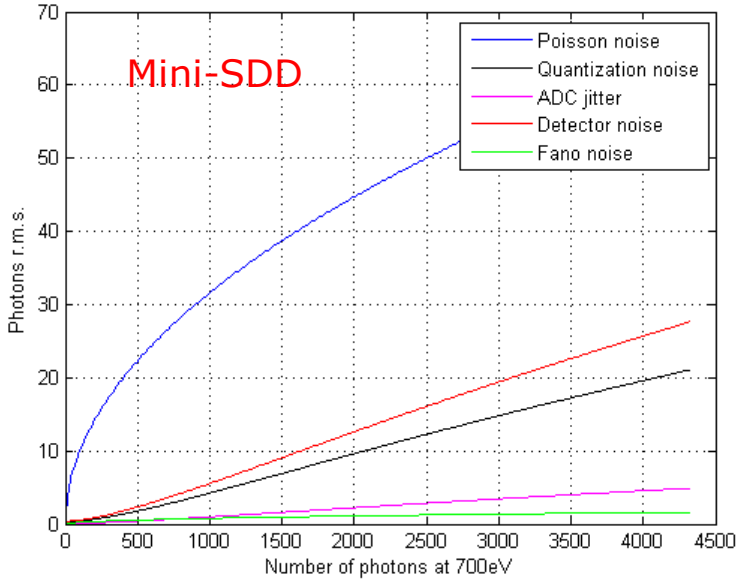
Mini-SDD
ADC input voltage [V]
Number of photons at 700eV


Pxd-8 DEPFET
Poisson noise
Quantization noise
ADC jitter
Detector noise
Fano noise
Photons r.m.s.
Number of photons at 700eV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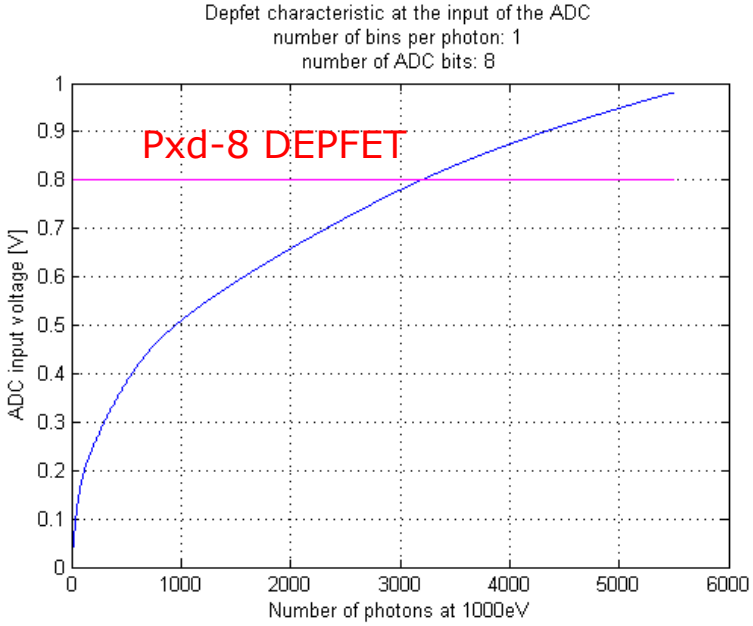
Depfet characteristic at the input of the ADC
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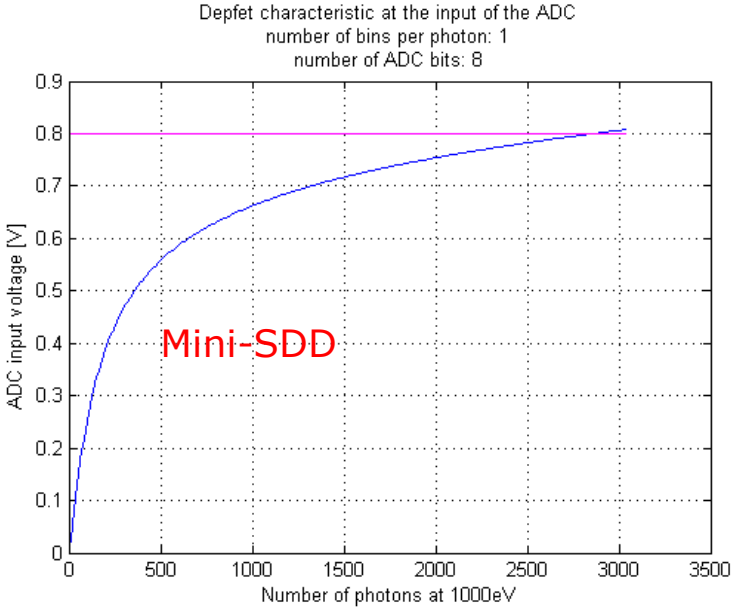
Pxd-8 DEPFET
ADC input voltage [V]
Number of photons at 1000eV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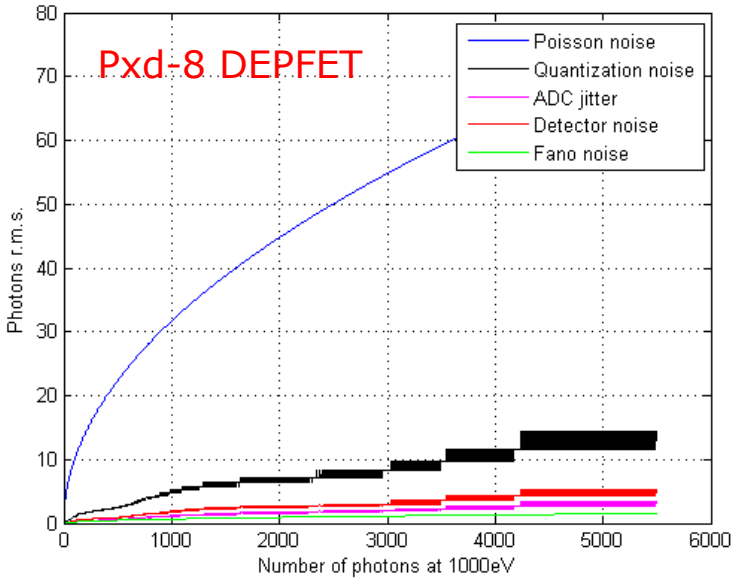
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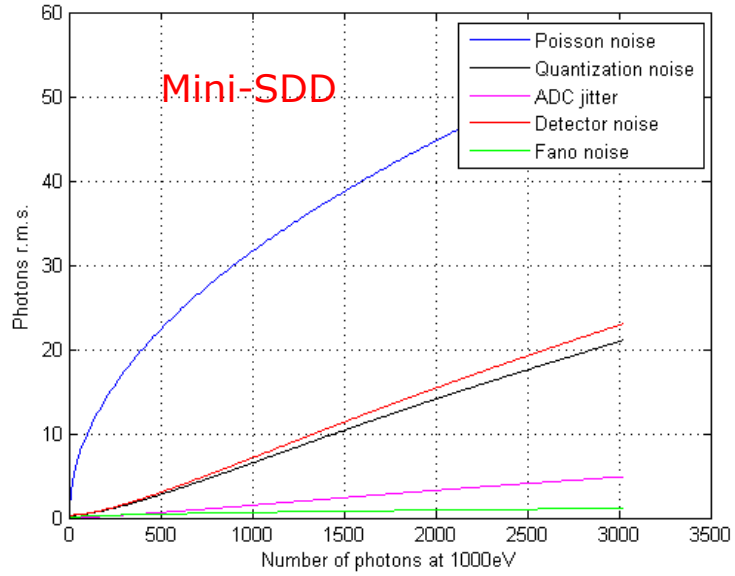
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