TAXI.

Transportable Array for eXtremely large area Instrumentation studies

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HAP Workshop on Advanced Technologies
2–3 June 2014 in Zeuthen

HELMHOLTZ | ASSOCIATION
Alliance for Astroparticle Physics

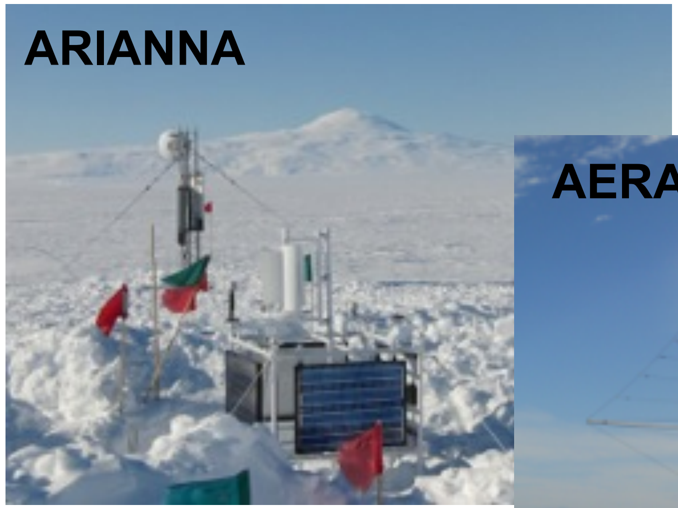
Karlsruhe Institute of Technology

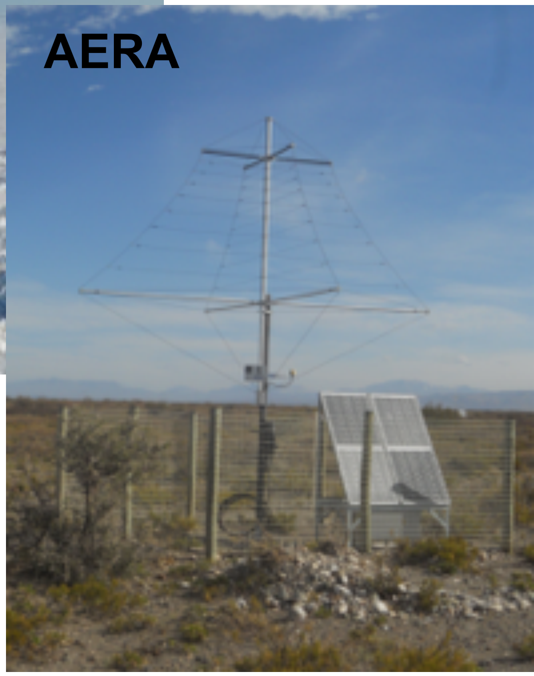
DESY

The Concept

The Idea

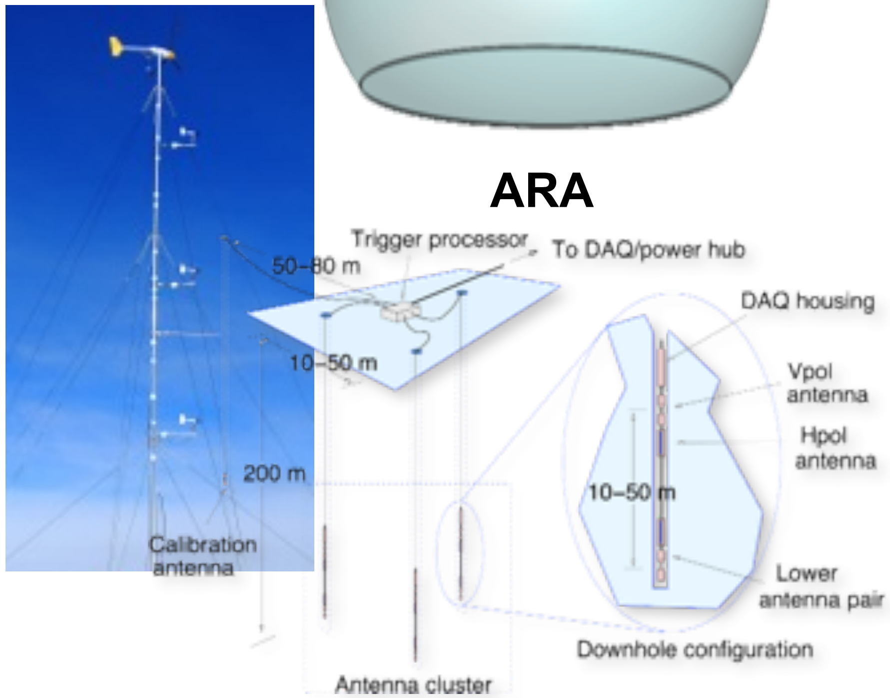
- Common “feature” of many astroparticle projects at the highest energies: (UHECR, neutrinos, (non-imaging) gamma astronomy)
  - Small signal fluxes:
    - Large detection areas required
  - Very similar infrastructure:
    - capture of an analogue signal
    - trigger for distributed stations
    - communications
    - power distribution
    - clock distribution

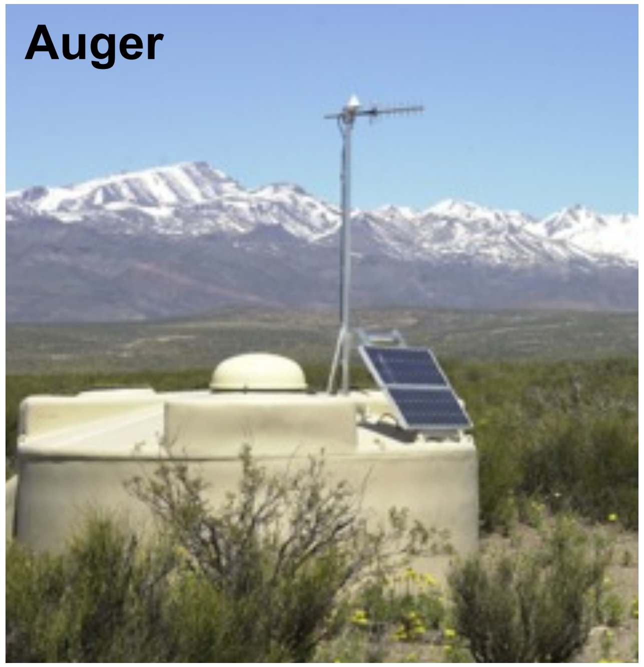




IceCube
Surface Veto

ARA

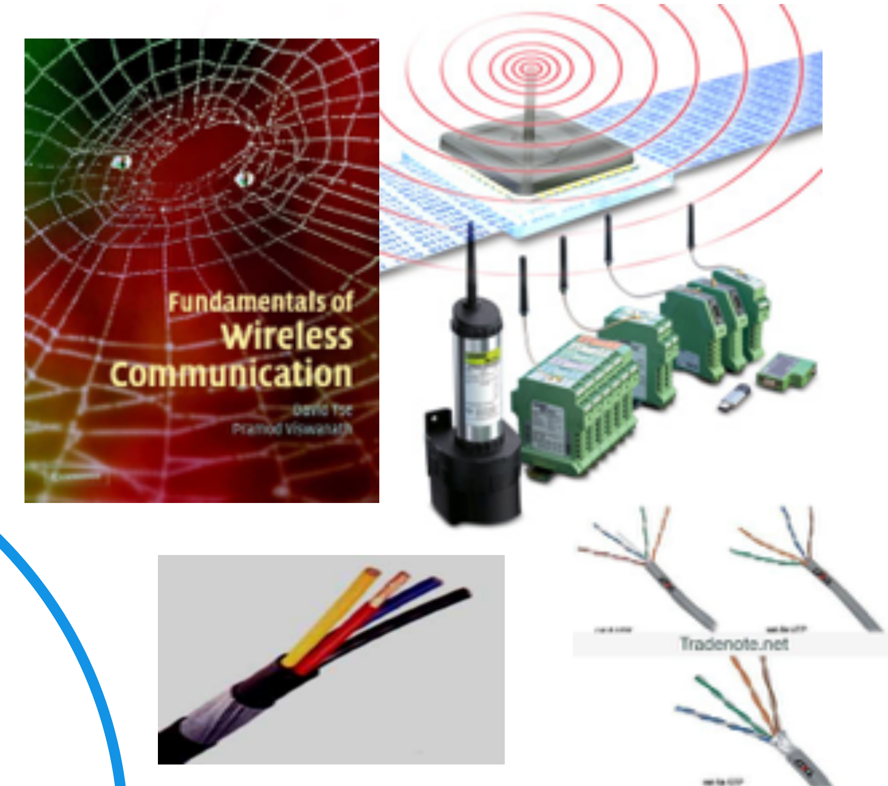




- **Develop a R&D system for testing different aspects of large area detectors**

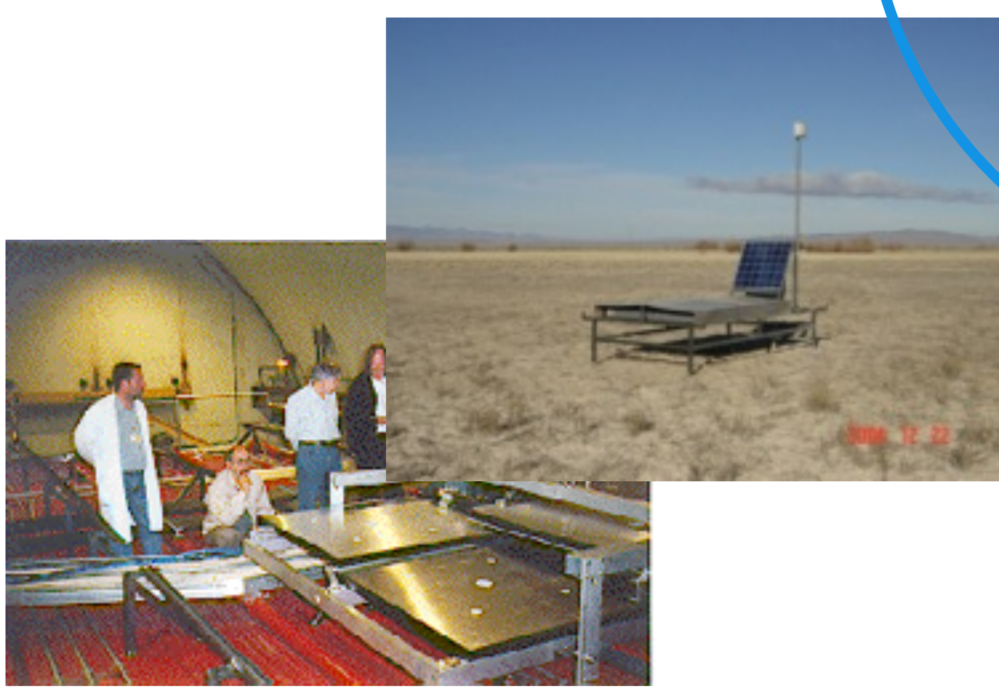
Sensors

Communication



TAXI

Reference Detector

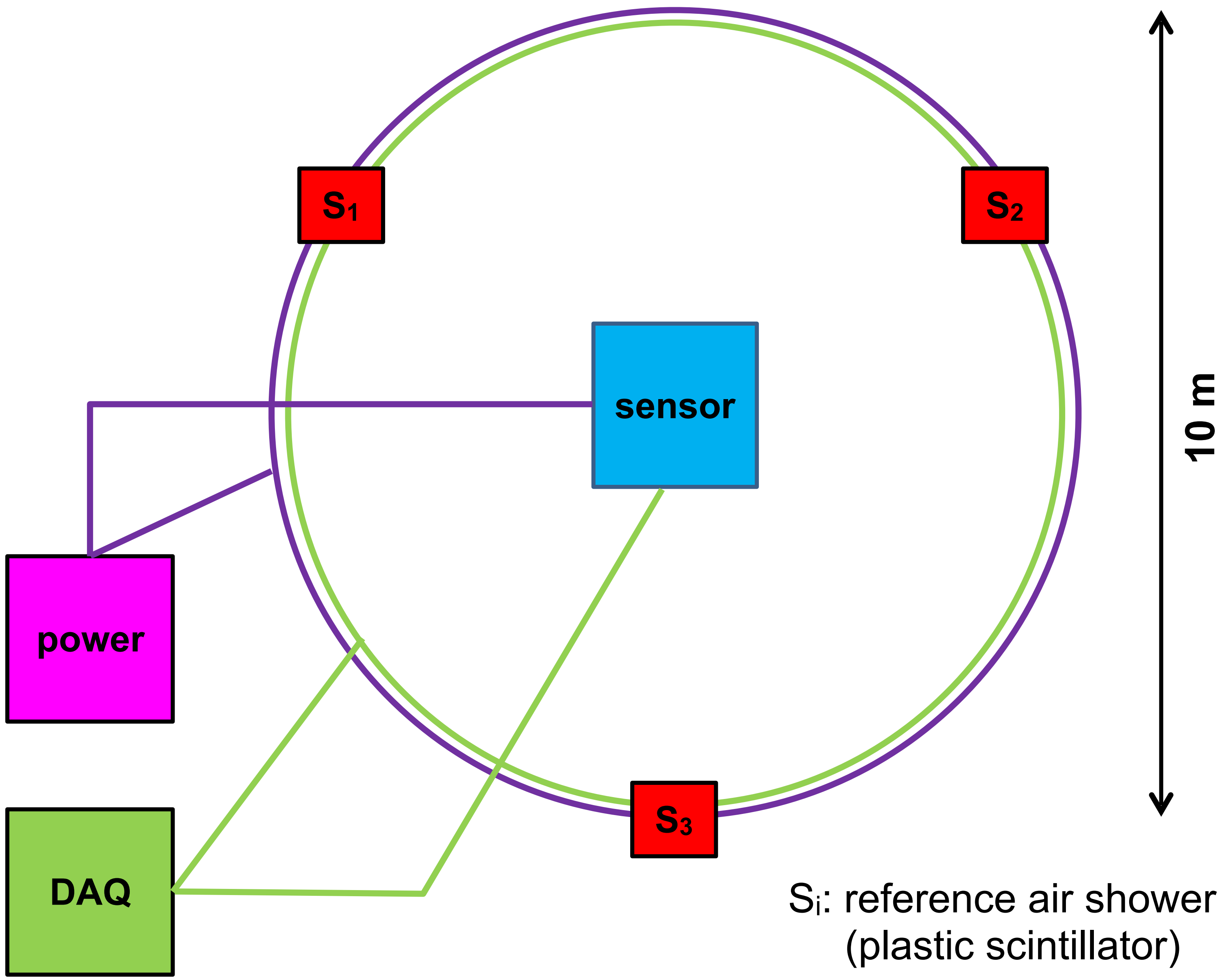


Power Source

First Step: Single Station

Sensor R&D

Idea: Use a simple reference air shower detector for trigger and coarse reconstruction

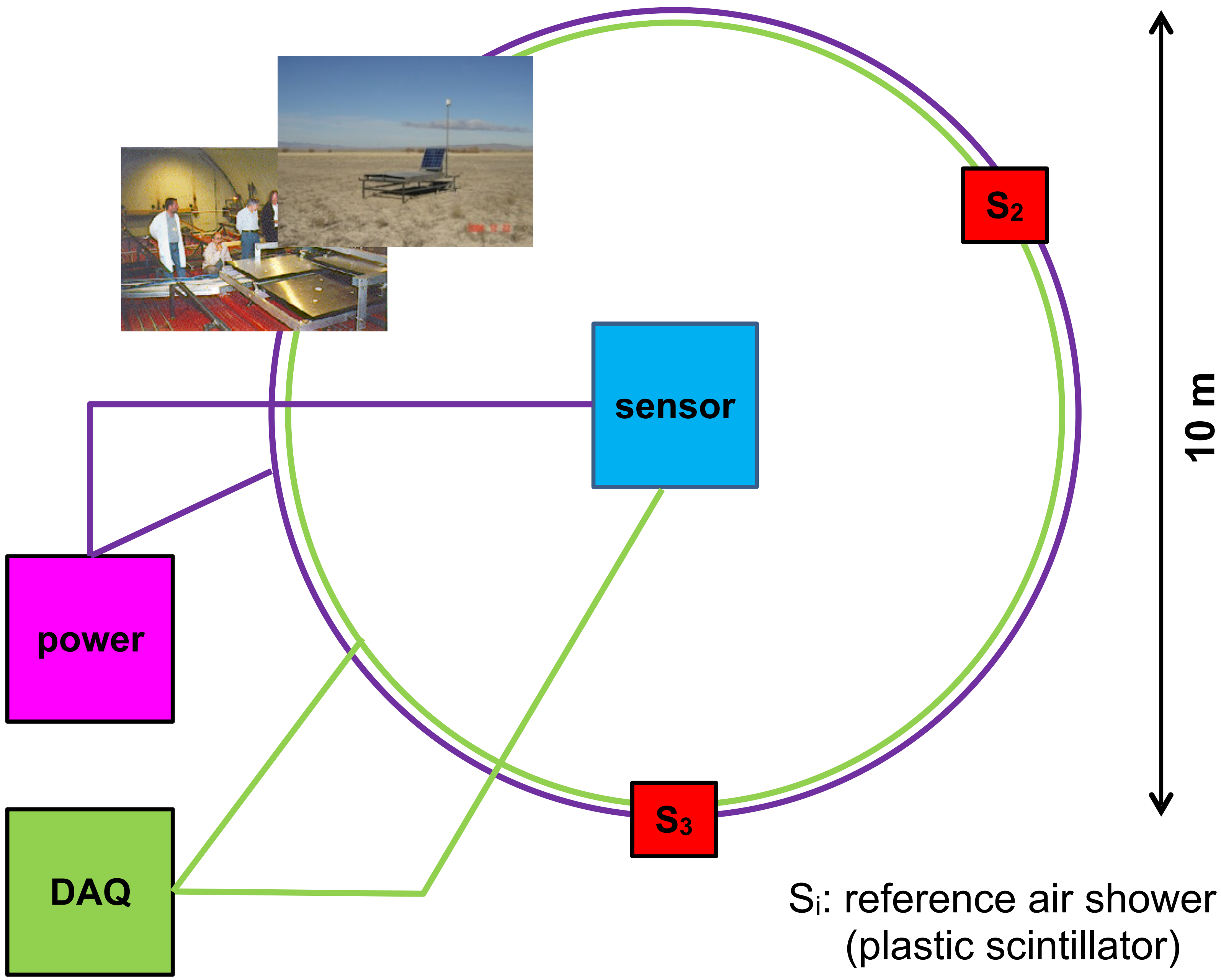


S_i: reference air shower detectors (plastic scintillator)

First Step: Single Station

Sensor
R&D

Idea: Use a simple reference air shower detector for trigger and coarse reconstruction

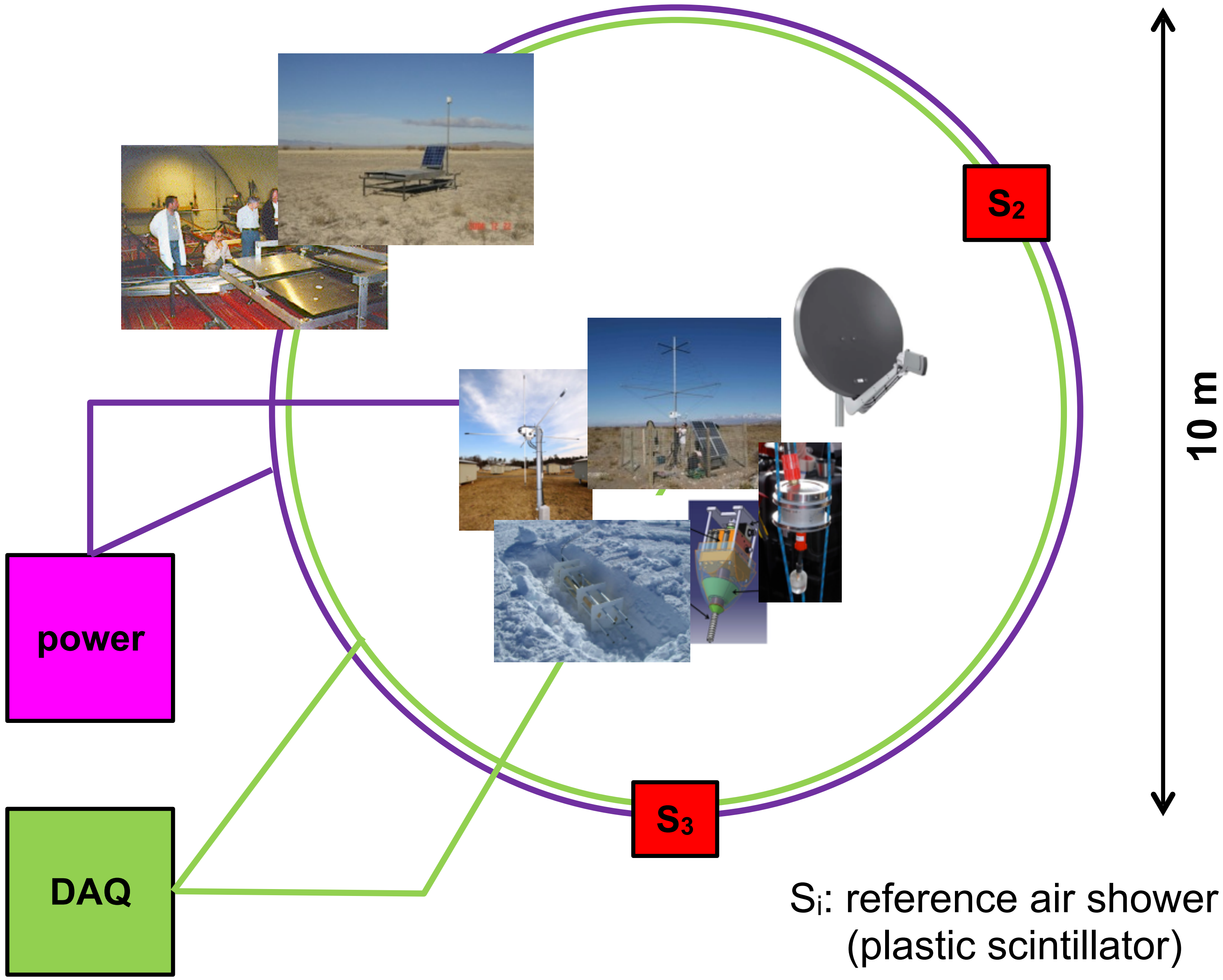


S_i: reference air shower detectors (plastic scintillator)

First Step: Single Station

Sensor R&D

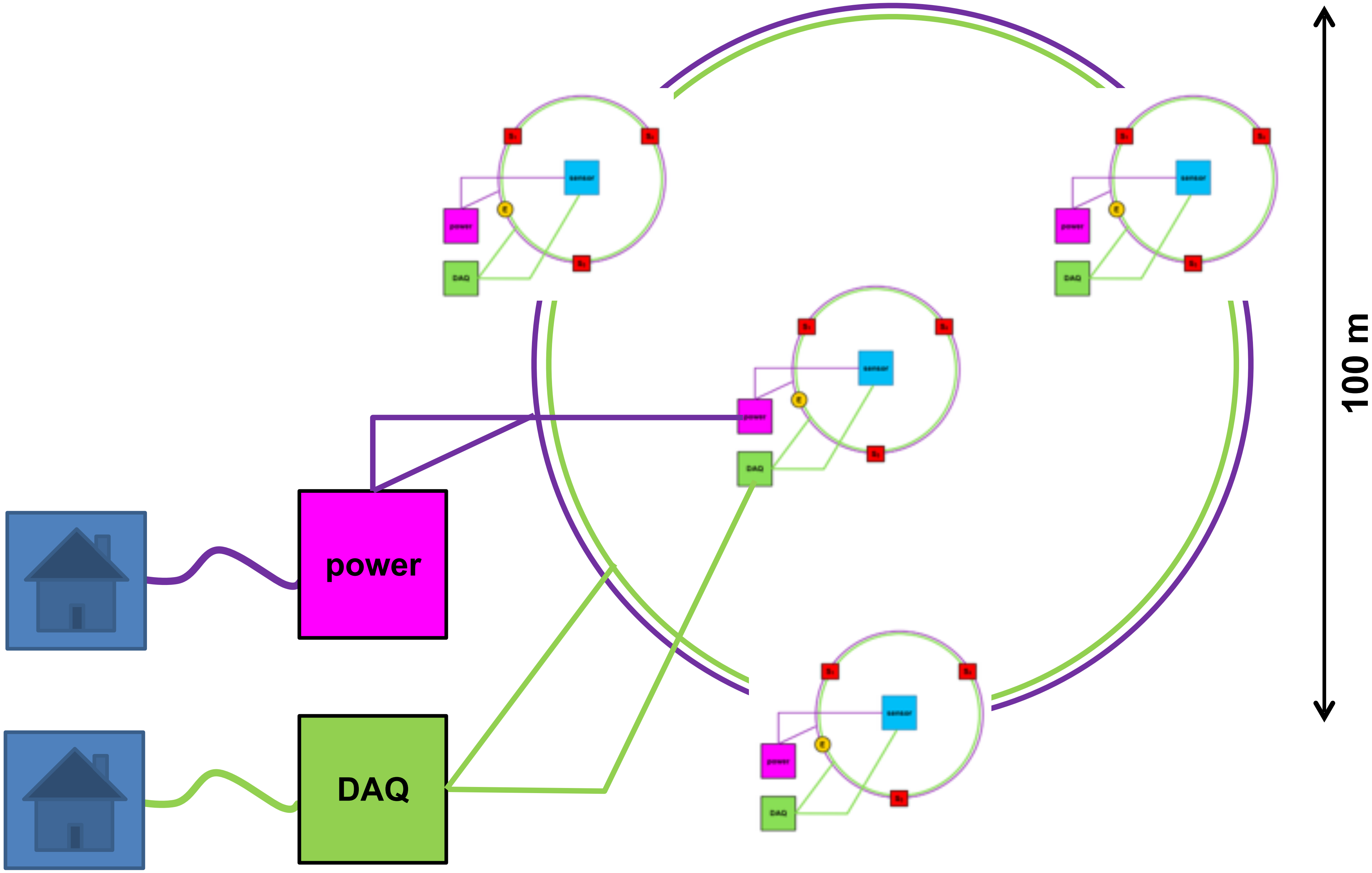
Idea: Use a simple reference air shower detector for trigger and coarse reconstruction



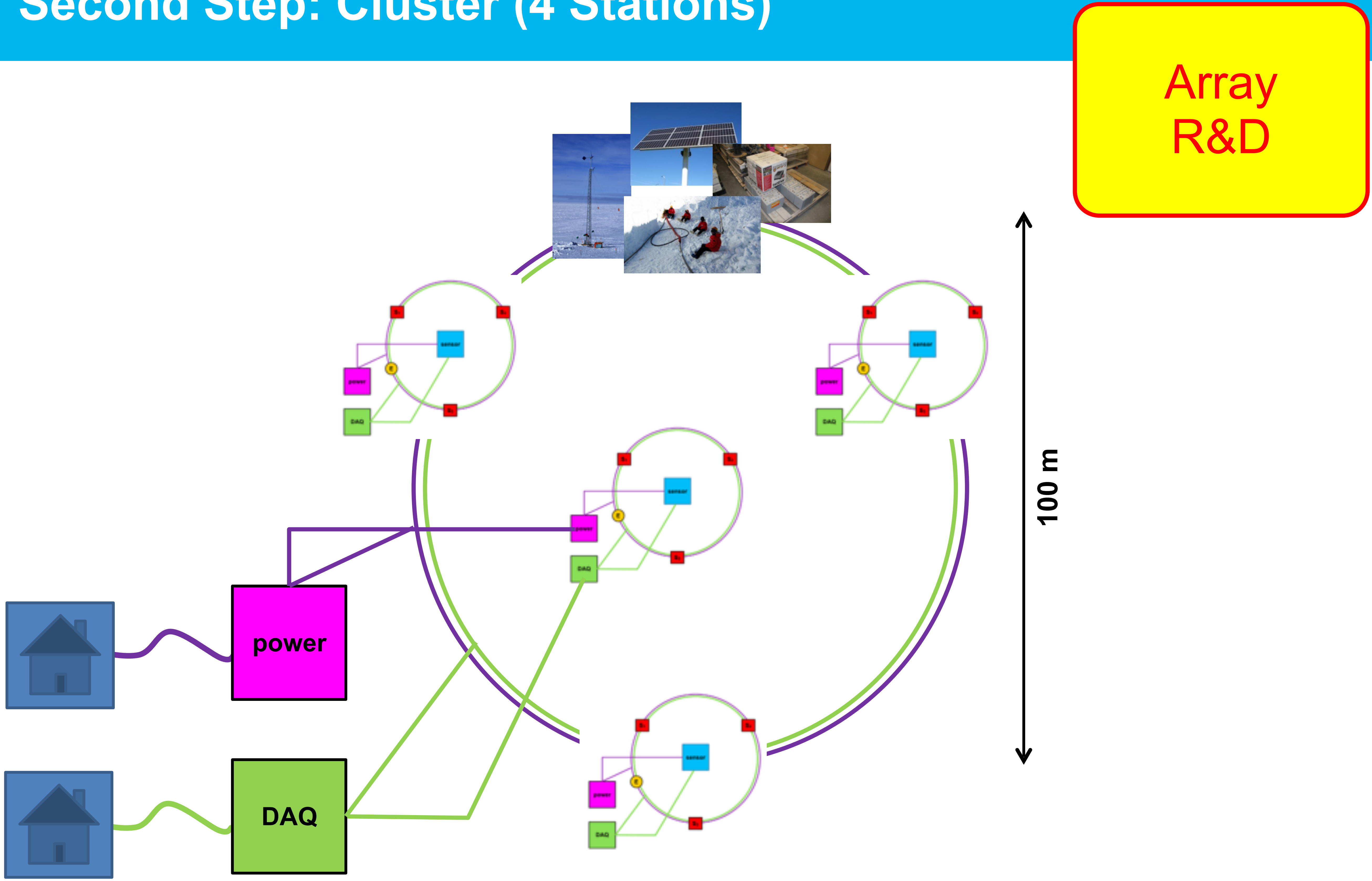
S_i: reference air shower detectors (plastic scintillator)

Second Step: Cluster (4 Stations)

Array R&D



Second Step: Cluster (4 Stations)



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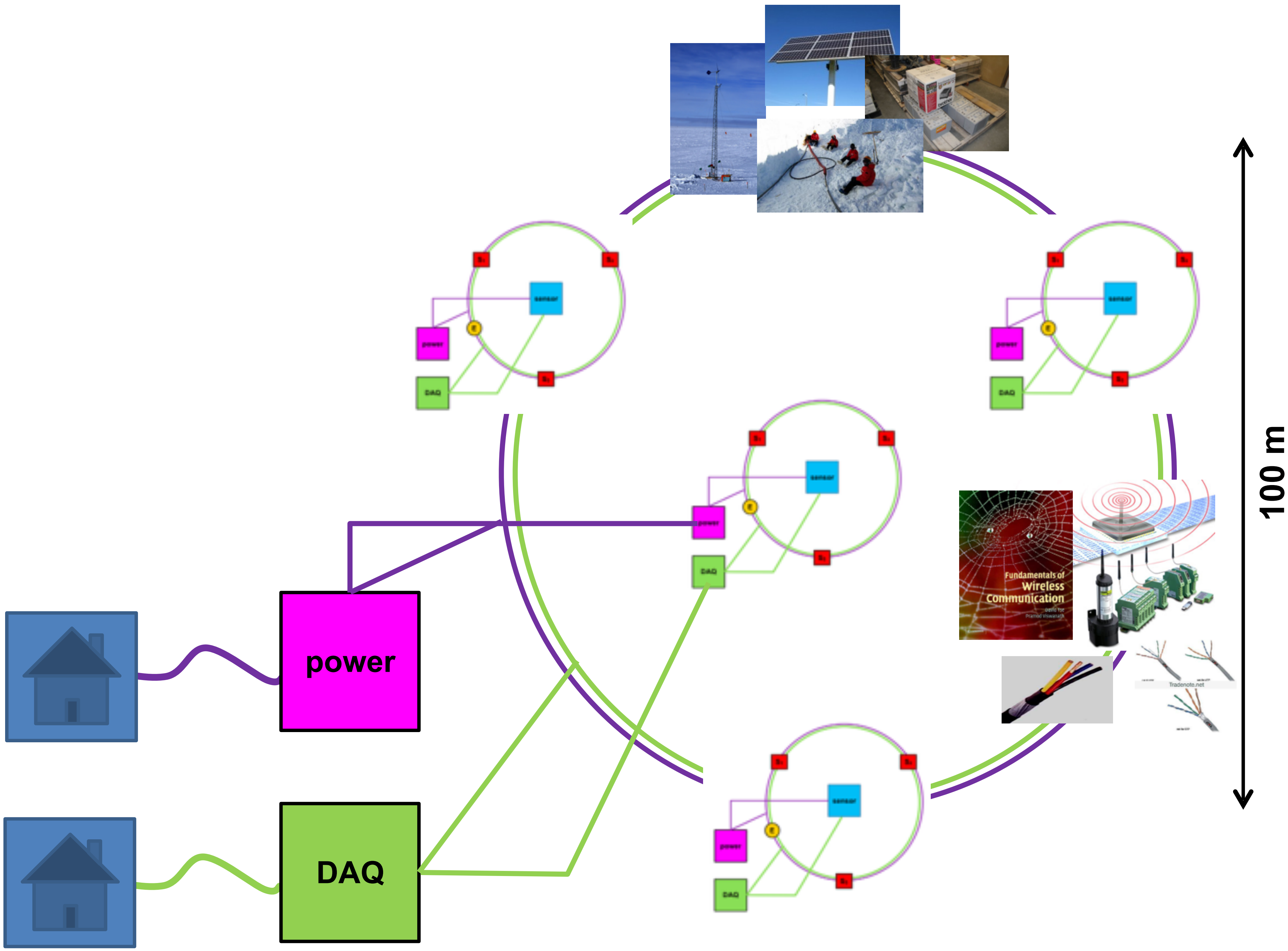
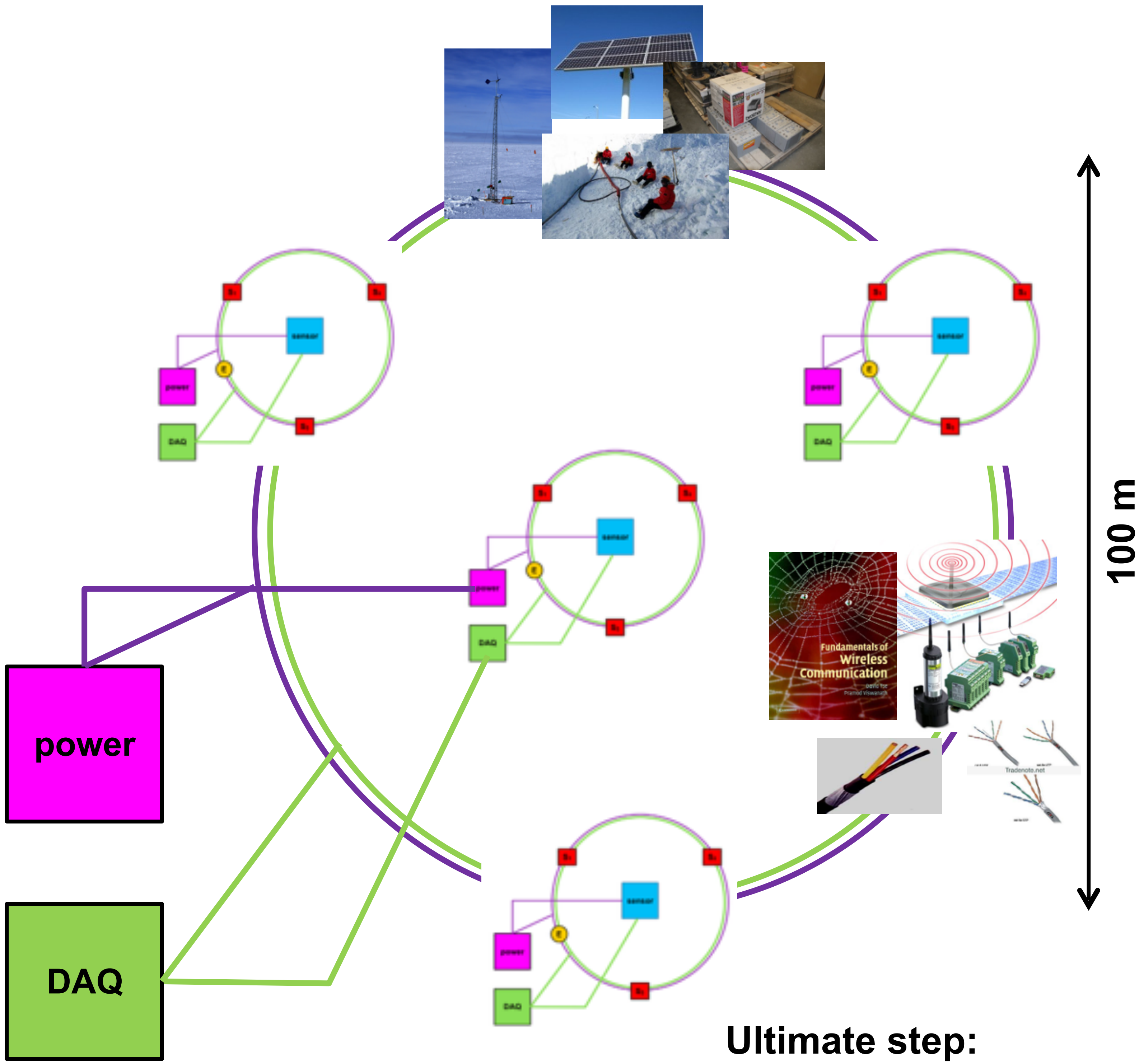


Second Step: Cluster (4 Stations)

Array
R&D



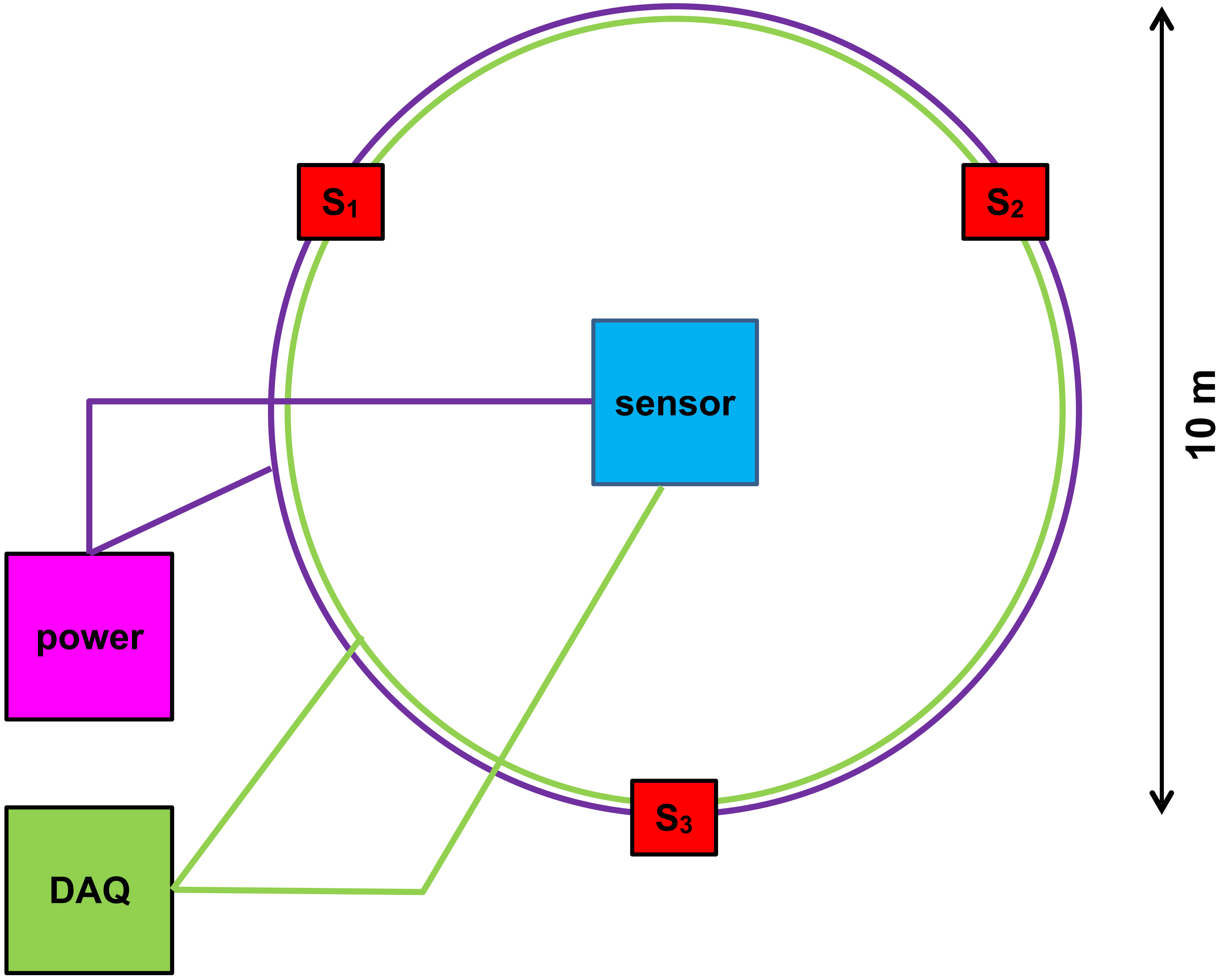
Ultimate step:
self-sustaining power and DAQ

Requirements

- Highly modular system that allows easy interchange of components
  - R&D environment for different system components with well defined interfaces
- Easy transport and setup: site studies for future projects
  - long term background measurement and monitoring
  - signal propagation studies (signal speed, attenuation, refraction, …)
- Operation at isolated sites
  - low power, self-sustained power supply
  - environmental range from Antarctica to hot climate
- Scalability

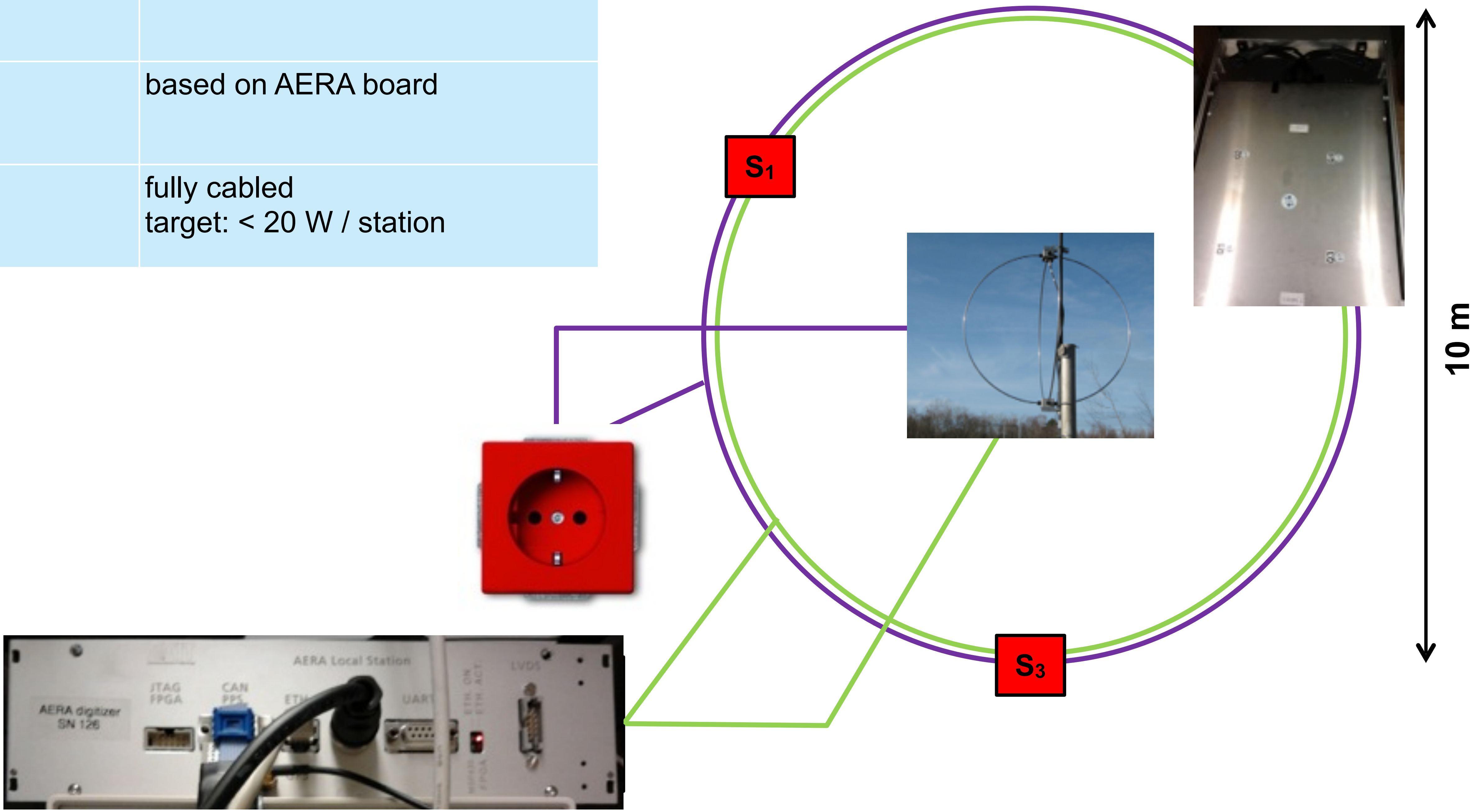
Current Status

Station 1 Operational @ DESY



Station 1 Operational @ DESY

Sensor:	radio antenna (MHz air shower detection)
Ref. Detector:	plastic scintillator
DAQ:	based on AERA board
Power:	fully cabled target: < 20 W / station



Station 1 Operational @ DESY

SALLA antenna
(courtesy of Tunka-Rex)

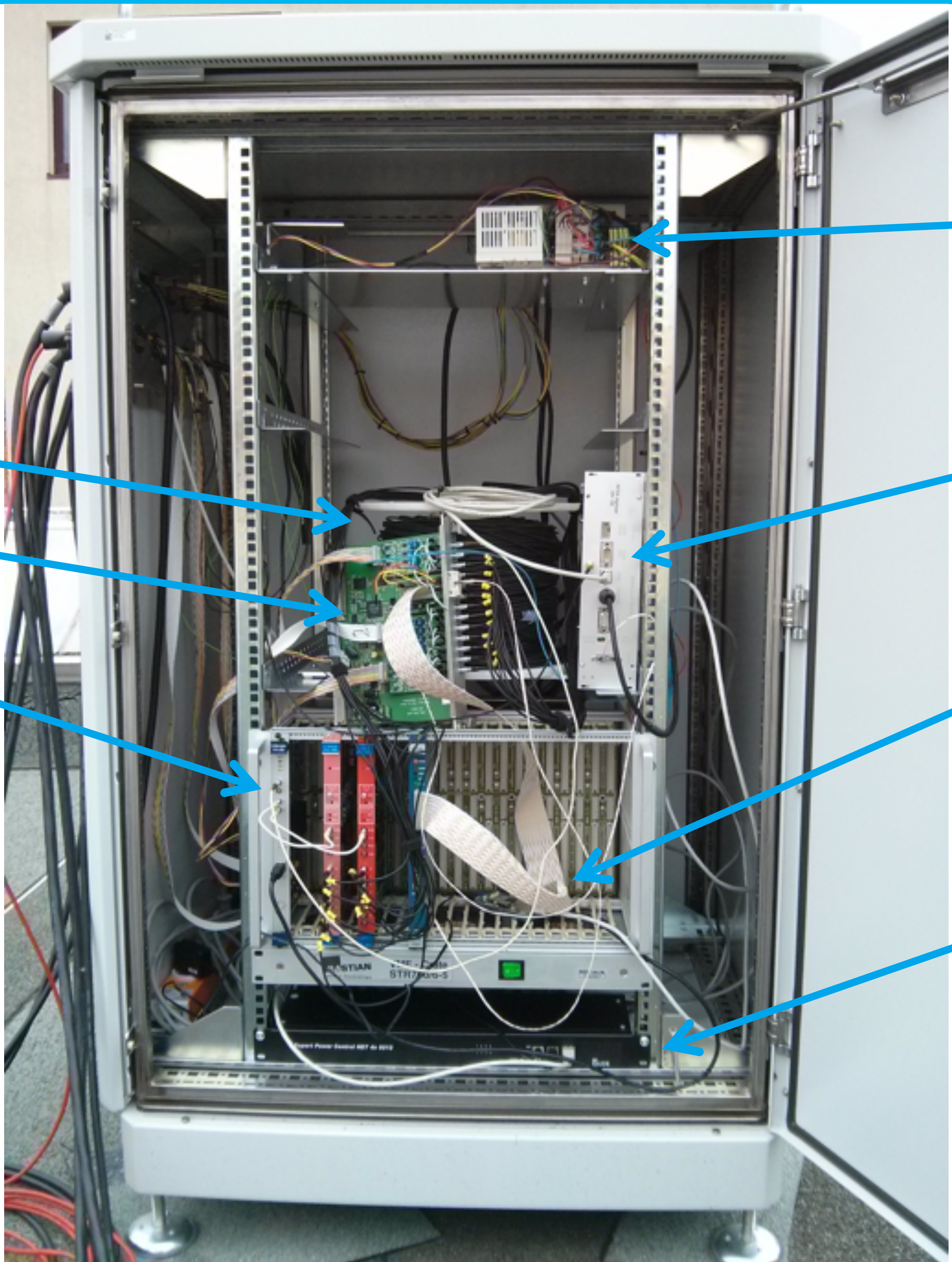
Scintillator 3

Scintillator 2

Scintillator 1

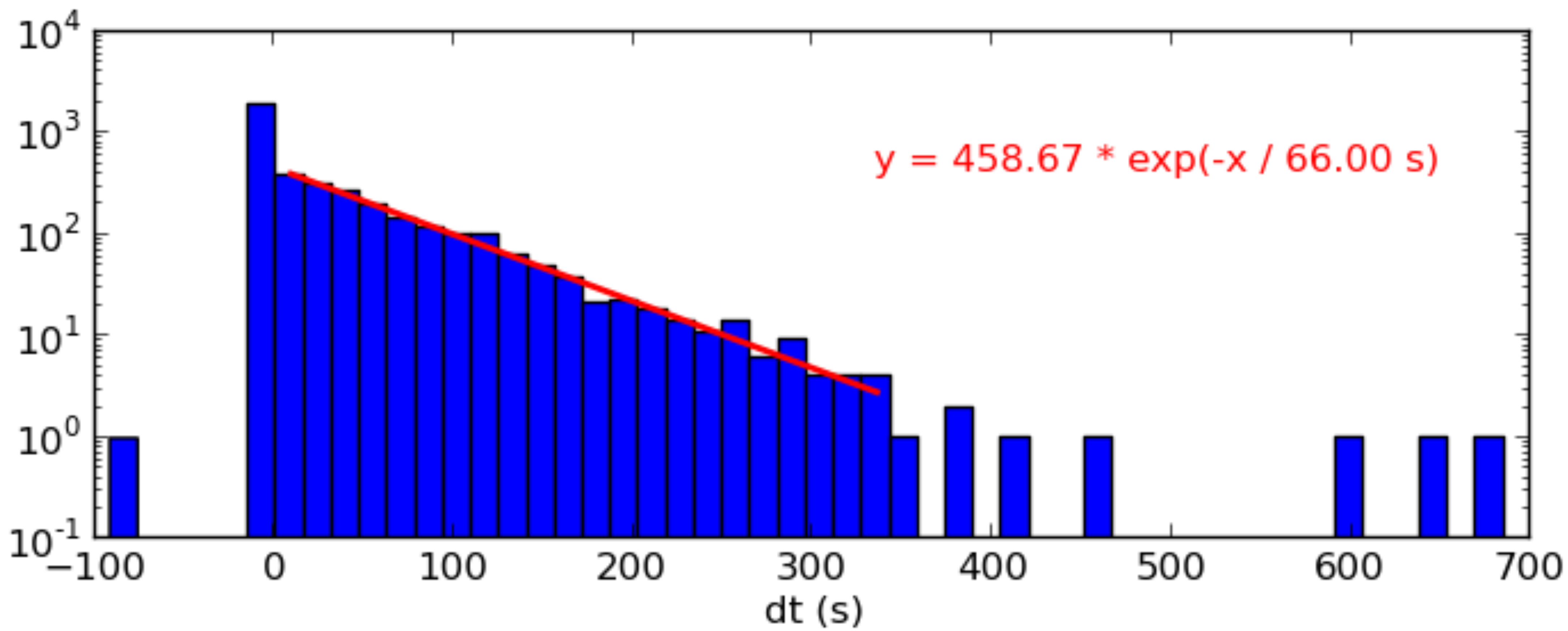
DESY Zeuthen,
Mechanical Workshop

Station 1 DAQ



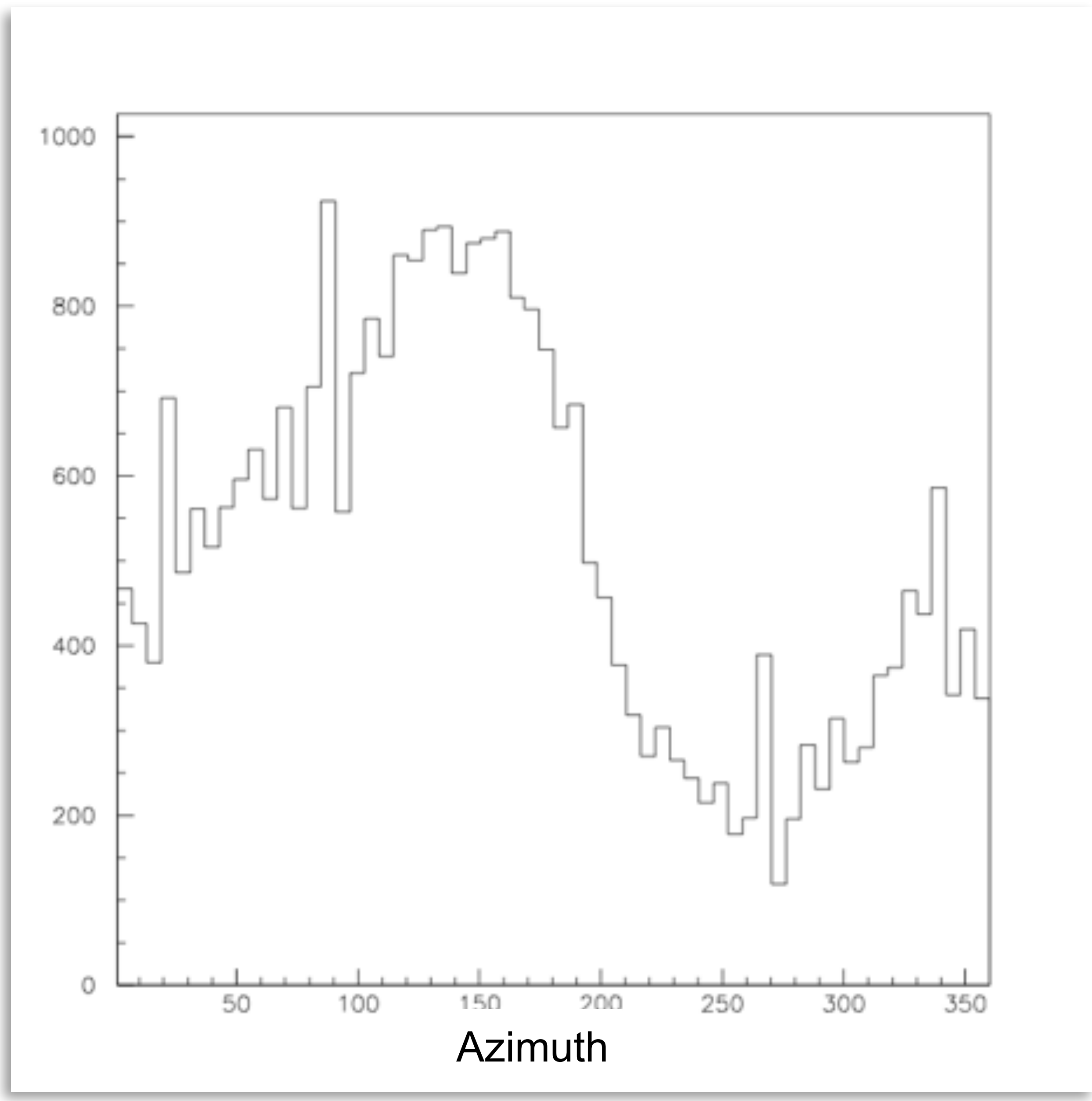
Performance

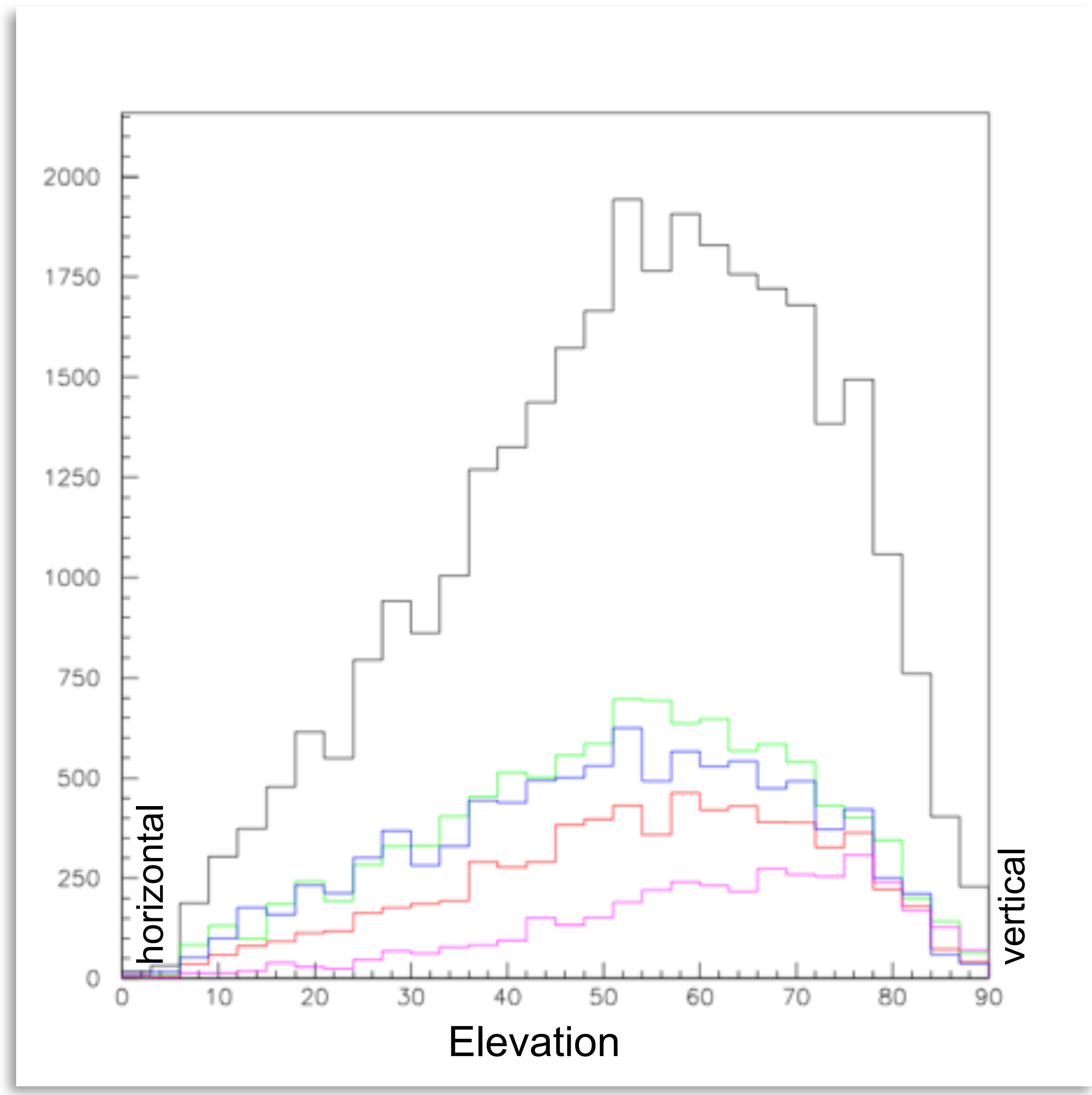
- Air shower trigger from scintillators: 3-out-of-3 condition
  - PMT pulses from scintillators read out by QDC and TDC
    (12 channels: 3 scintillator plates with 4 channels each)
  - Trigger from scintillators used to trigger read out of radio signal
- Rate: ≈ 1 min-1



Reconstructed Directions

Direction of air shower reconstructed from arrival time differences

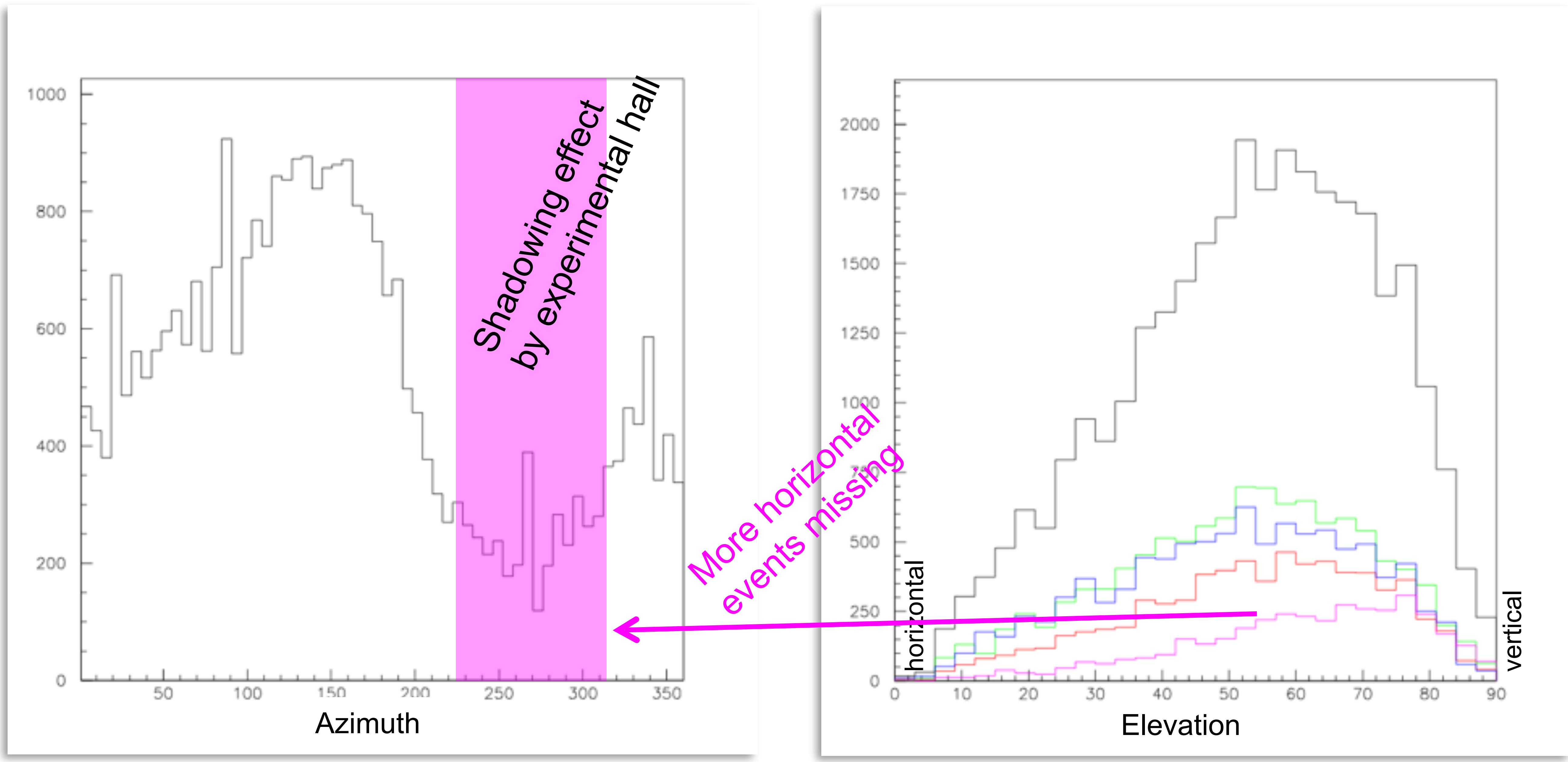




(35 days of data)

Reconstructed Directions

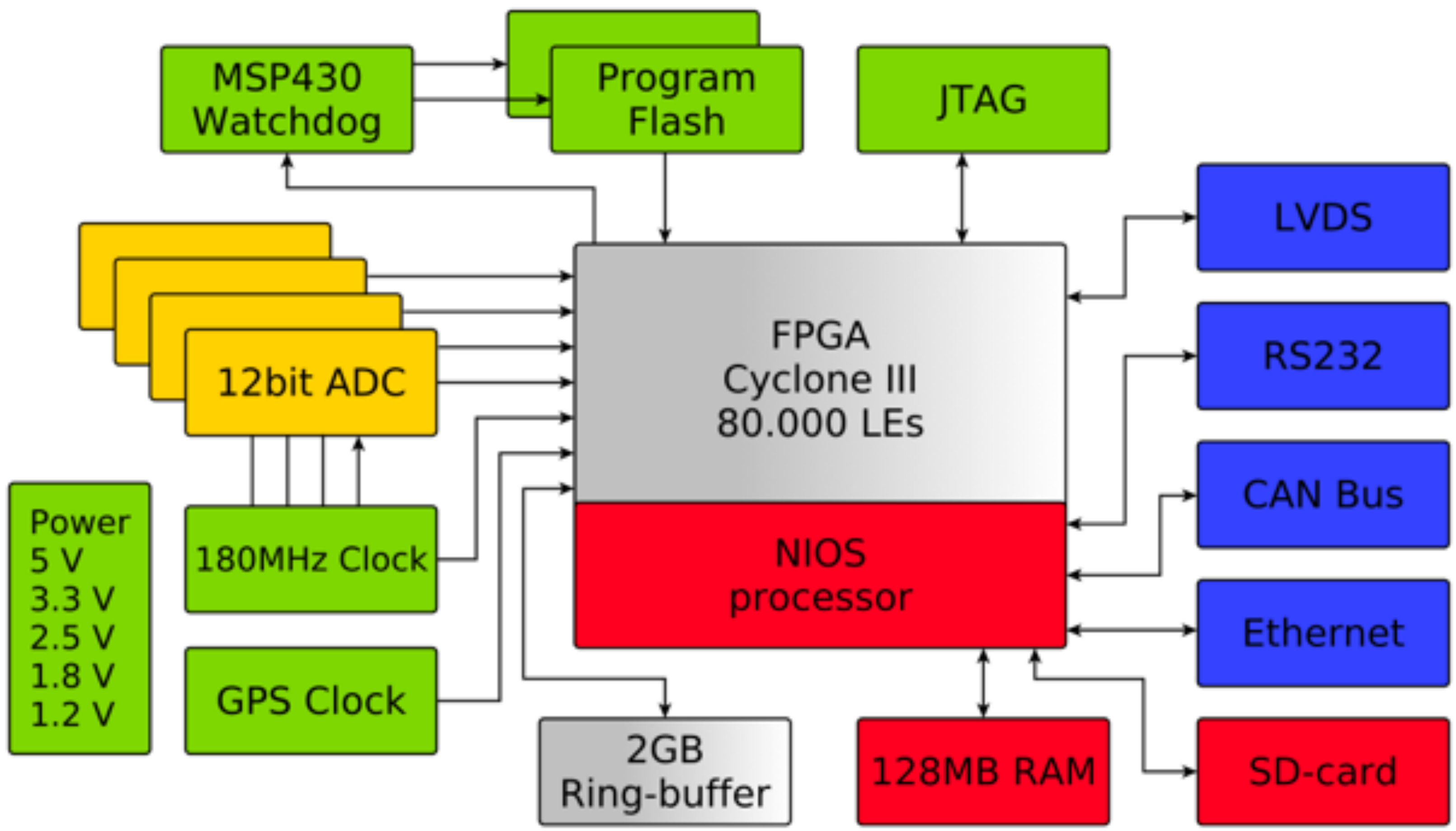
Direction of air shower reconstructed from arrival time differences



(35 days of data)

View in the Direction of 270°

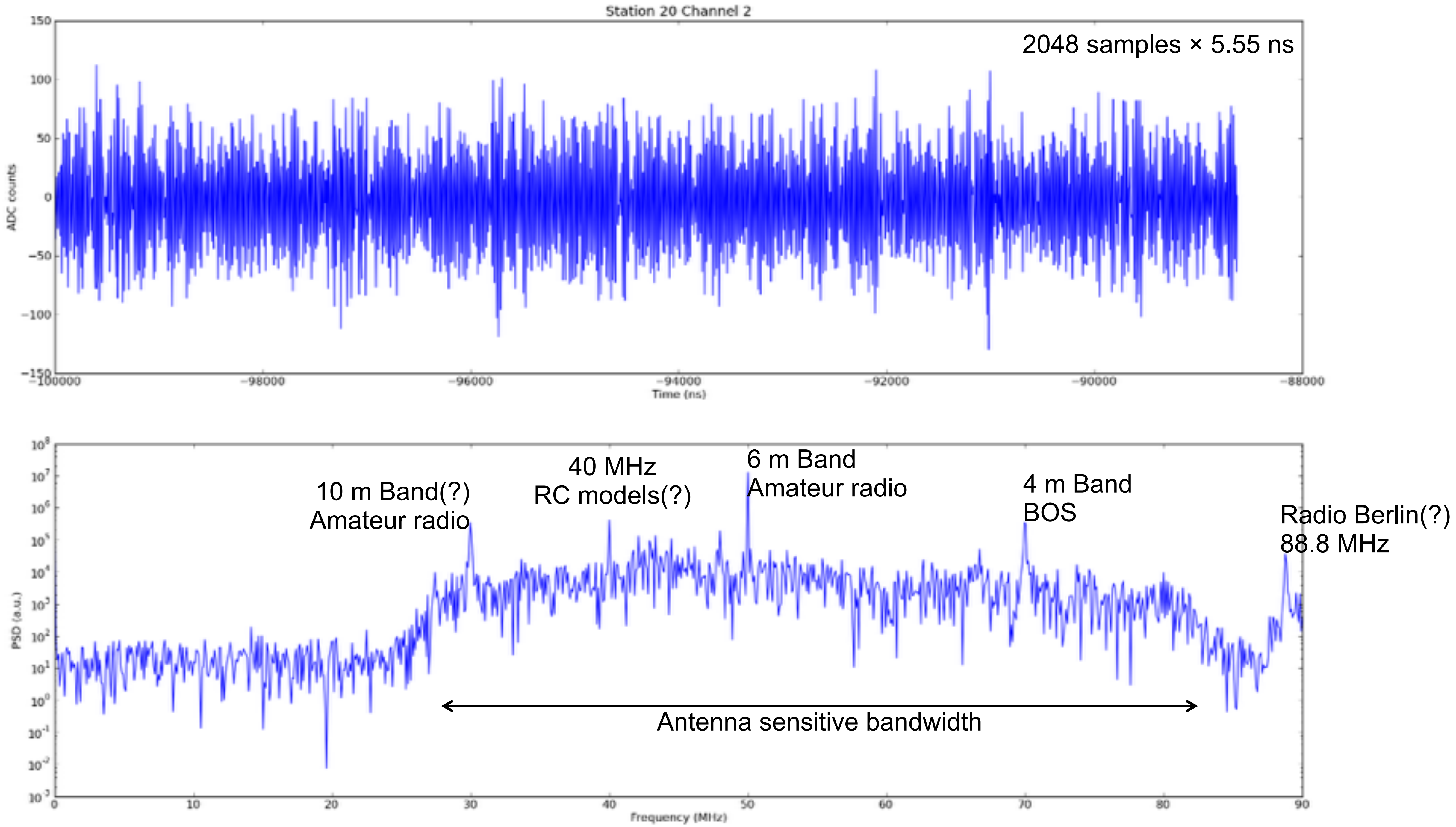
Radio Waveform Readout



Block diagram:
A. Schmidt, PhD Thesis, KIT (2012)

- Developed at KIT (IPE, IKP) for the Auger Engineering Radio Array (AERA)
- Four digitizers (180 MHz, 12 bit; can be interlaced to 2 × 360 MHz)
- Deep ring buffer (7 seconds for 2 channels @ 180 MHz)
- Powerful FPGA for real-time signal processing
- External trigger from scintillation detector
- Power: < 10 W (including LNAs for radio antenna)

Ext. Triggered Event: Radio Background in Zeuthen



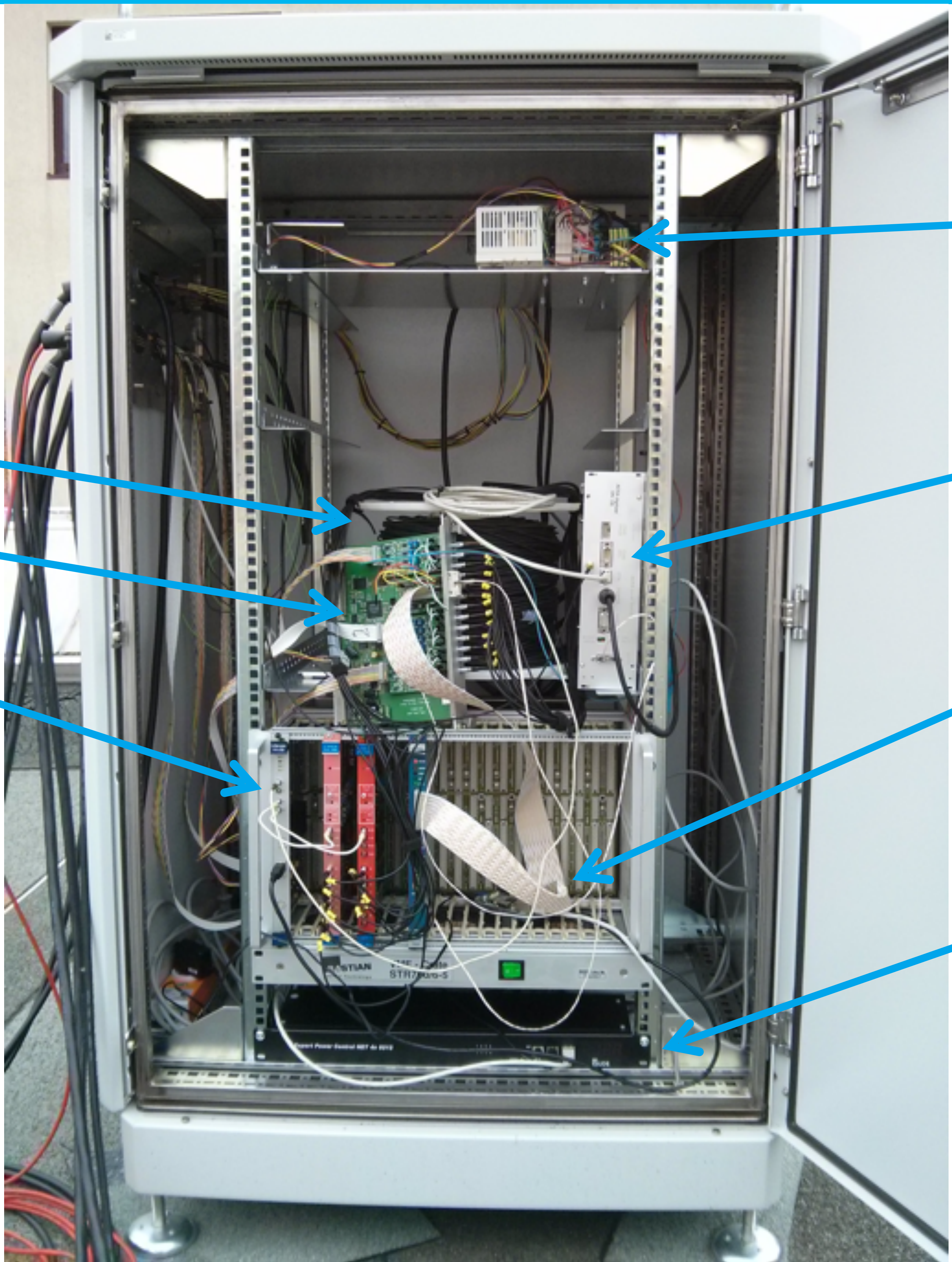
Next Steps and Timeline

Next Step: Replace VME Crate

Cable delay for QDC

Trigger board

VME DAQ f. Scintillators
(QDC + TDC)



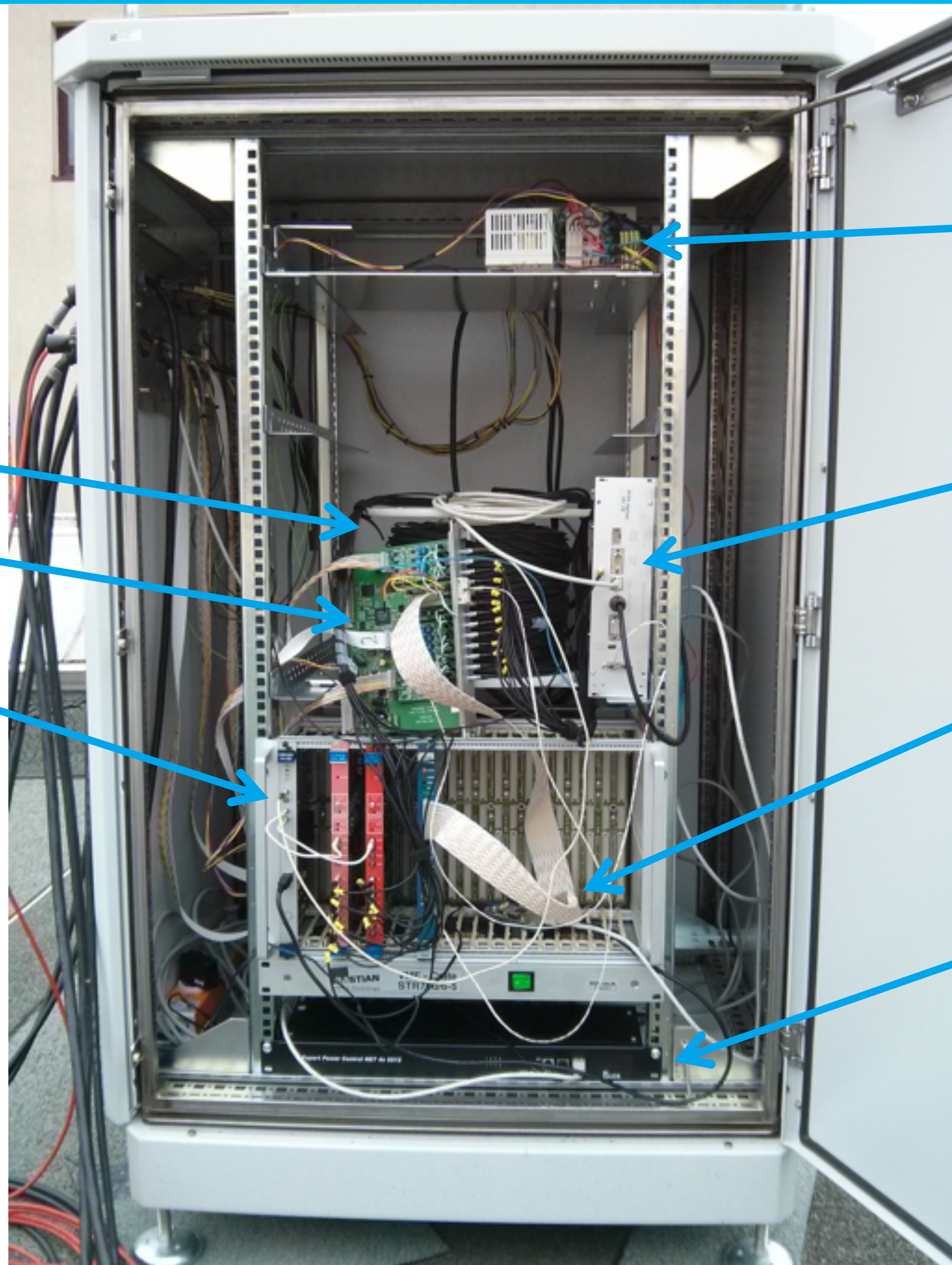
Power supply

AERA board

VME readout:
Raspberry Pi

Power control
via Ethernet

Next Step: Replace VME Crate



Power supply

Cable delay for QDC

AERA board

Trigger board

VME DAQ f. Scintillators (QDC + TDC)

VME readout: Raspberry Pi

Power control via Ethernet

Next Step: Replace VME Crate

~~Power supply~~

24 V input

AERA board

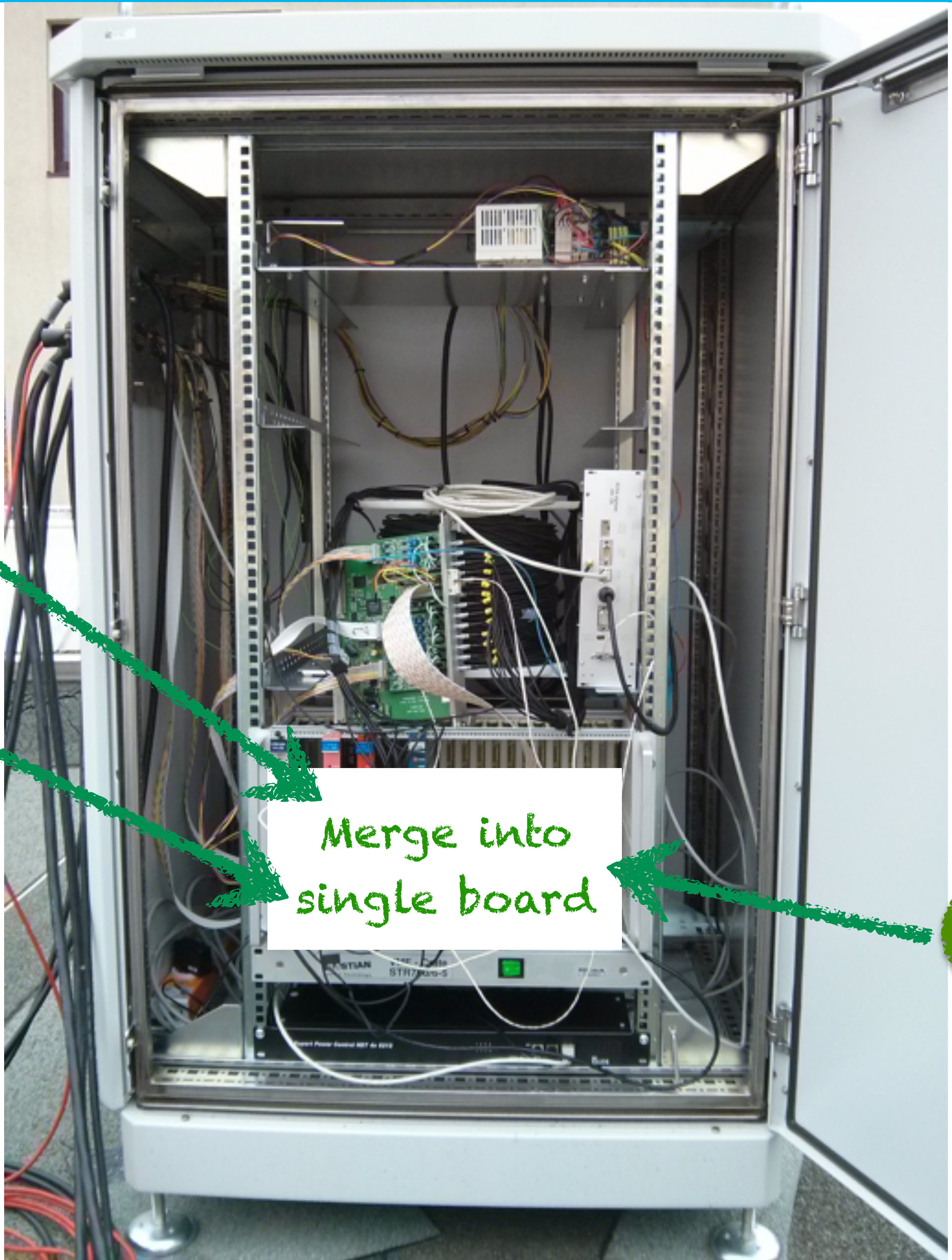
~~VME readout: Raspberry Pi~~

Power control via Ethernet

~~Cable delay for QDC~~

Trigger board

~~VME~~ DAQ f. Scintillators (QDC + TDC)

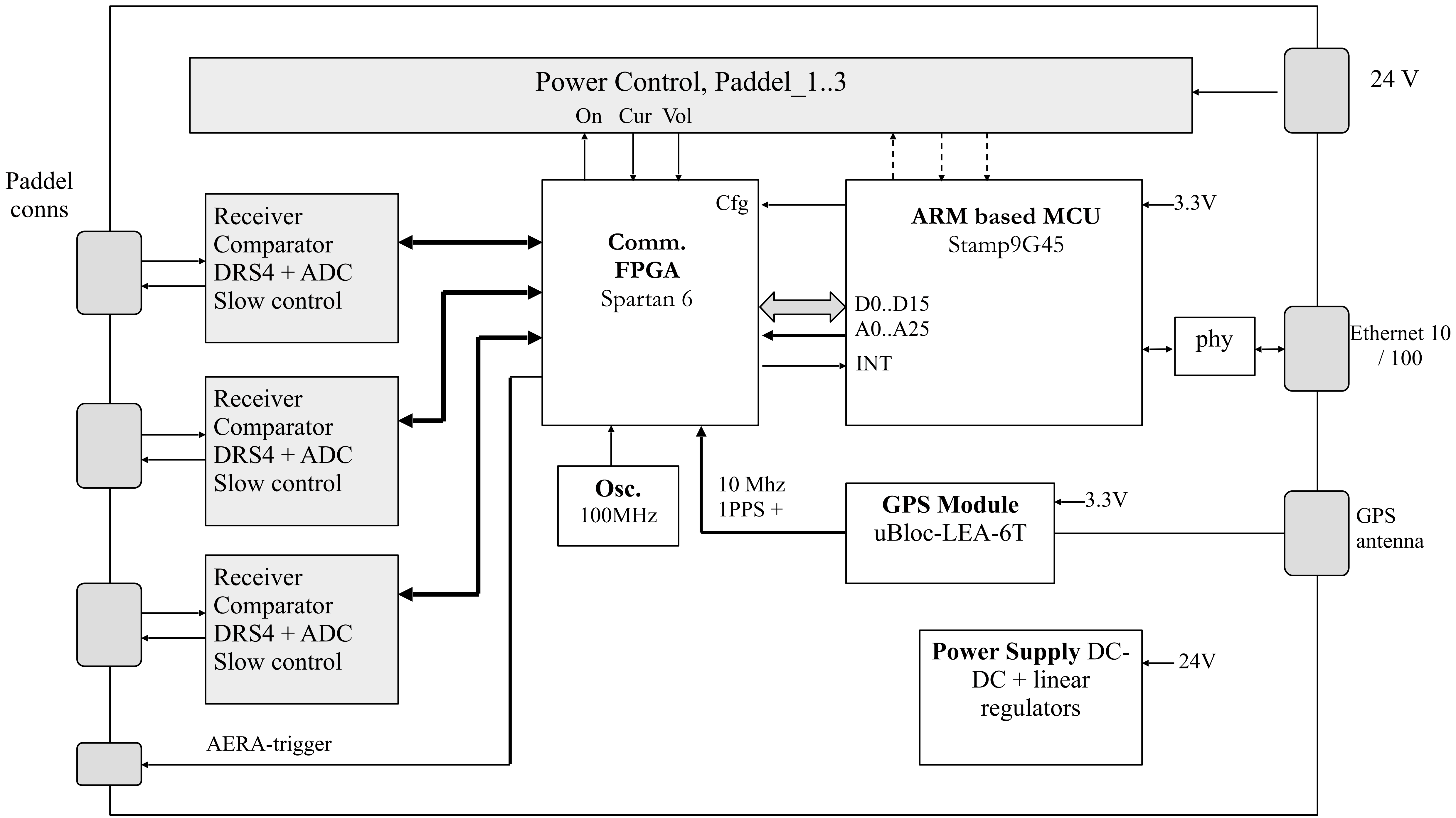


TAXI Station, Design Goal

- Single board design, power consumption < 10 W (w/o ADC)
- Communication via ethernet 10/100
- Single low cost Xilinx FPGA, Spartan 6
- 24 analog channel with differential input
- 24 discriminators with programmable threshold
  - minimum detectable signal: 1mV pk
- TDC functionality, time diff. measurements with 0.5 ns accuracy
- Time stamping
- Optional 24 ADC channel, 1024 samples per channel
  - Sampling rate 200 MSPS … 6 GSPS (DRS4)
  - Dead time: TBD

courtesy K.-H. Sulanke

TAXI Station



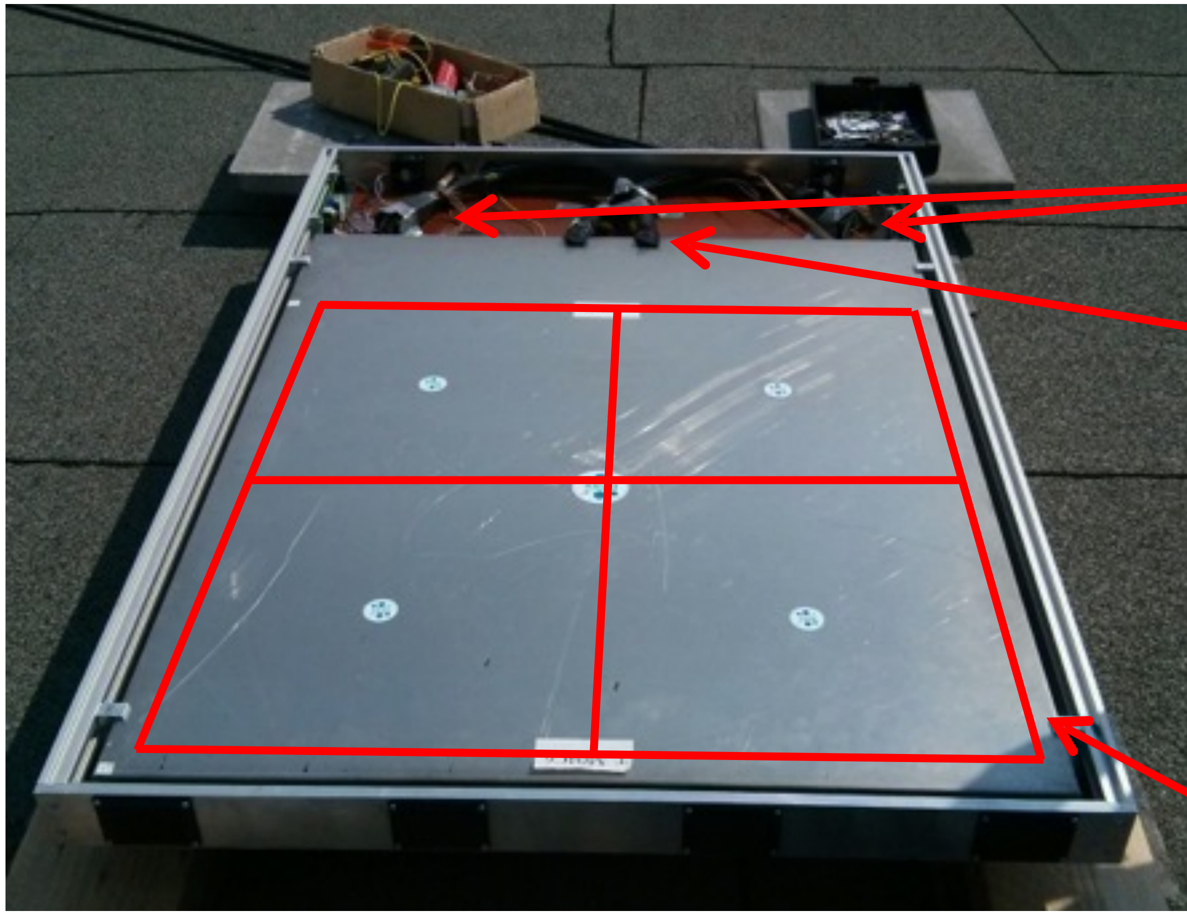
courtesy K.-H. Sulanke

Summary and Outlook

- TAXI is a R&D system for large area instrumentation
  - Modular: Develop and test different components under realistic conditions: Power supply and distribution, communication, triggering, clock synchronization, …
  - Transportable: Perform short- and long-term site studies for prospective experiments
- One prototype station constructed and successfully taking data
- Mid 2014:
  Reach target power budget of < 20 W / station by replacing VME read-out for scintillators
- End 2014:
  Finish four station array in Zeuthen with generic interfaces for power and communications

Backup Slides

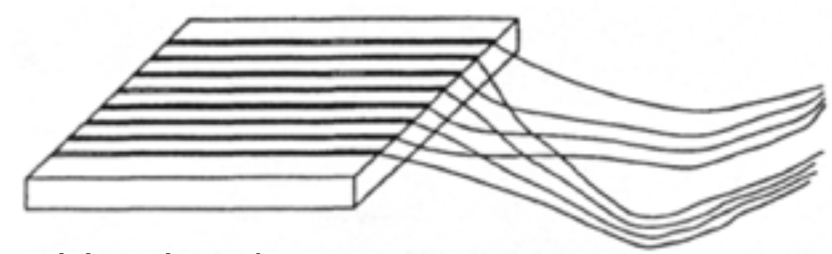
Scintillation Detector



Hamamatsu R 5900-3-M4
2 × 2 multi-anode PMT

optical fibers
each tile read out by 2 sets of fibers

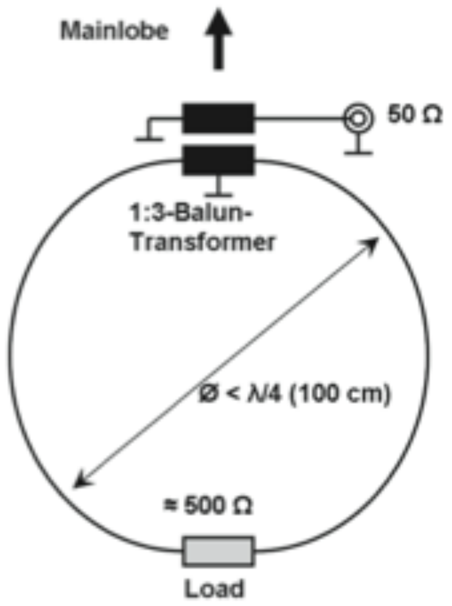
1 m² tiled plastic scintillator
16 tiles, 25 × 25 cm each

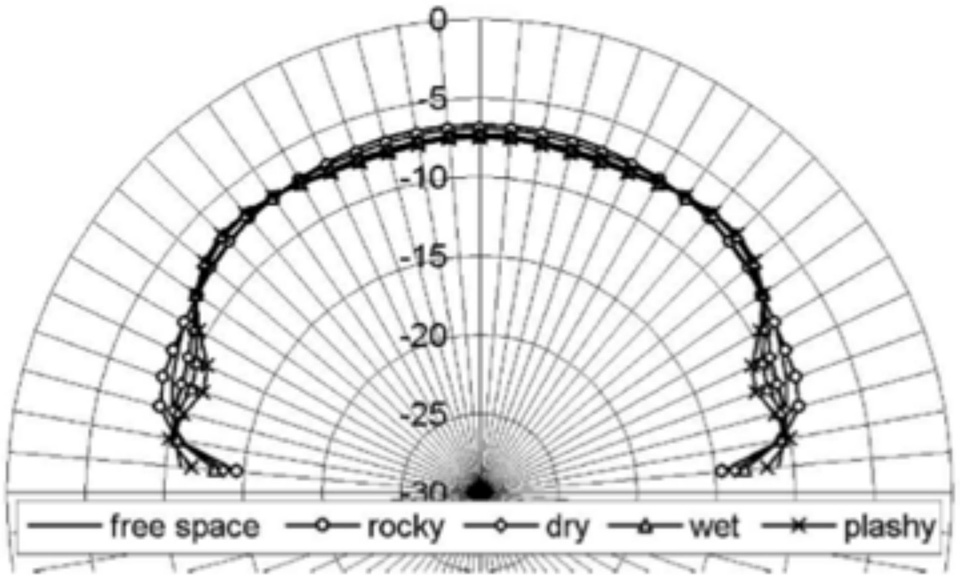


combined to 4 segments
of 50 × 50 cm for readout

- Input: ± 12 V
- Output: differential, analog PMT signal (8 channels)

Radio Antenna

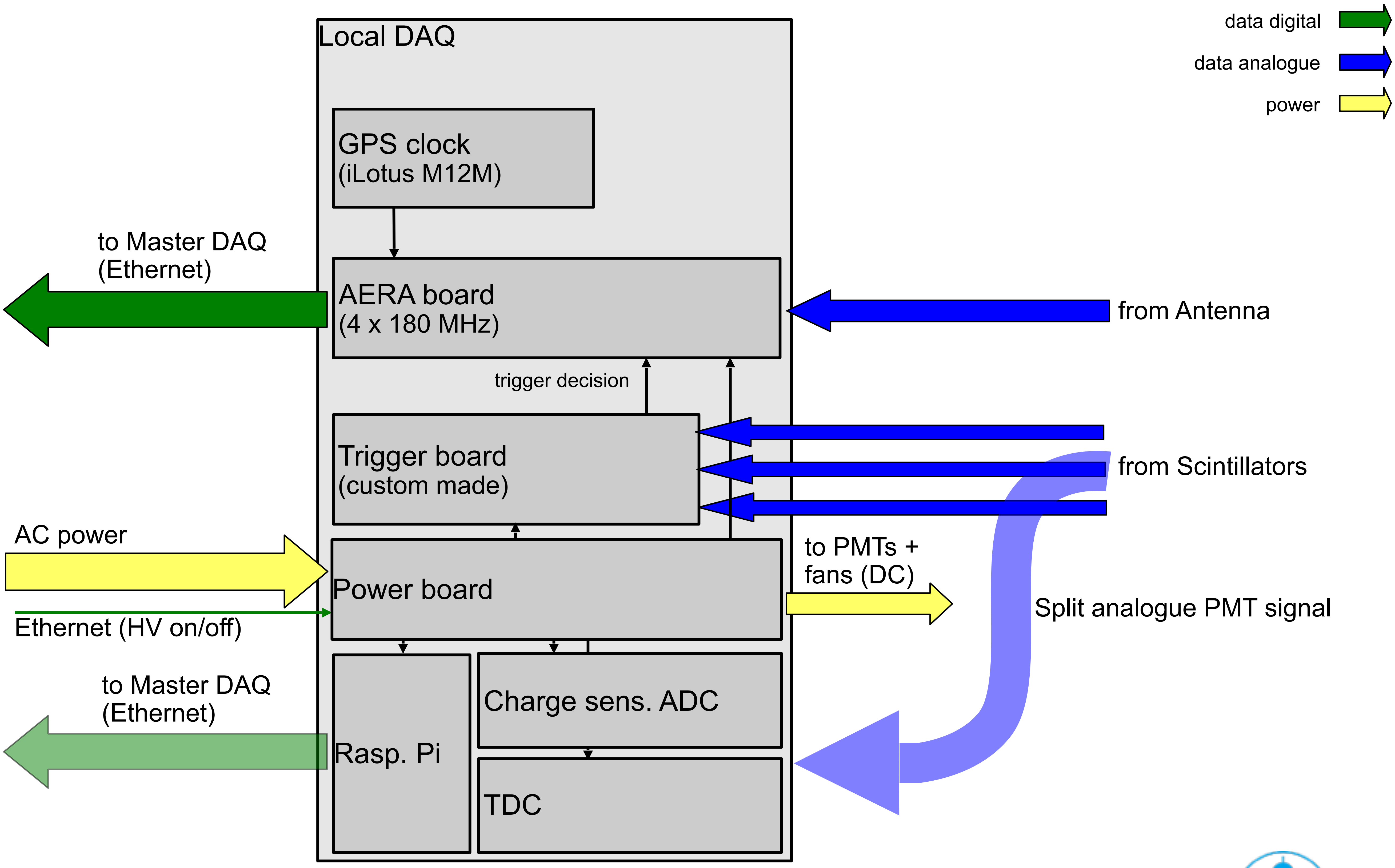




LOPES Collaboration, 31st ICRC, Łódź, 2009

- SALLA: Short Aperiodic Loaded Loop Antenna
- Used in Tunka-Rex
- Flat gain over wide frequency range from ~30 MHz to > 80 MHz
- Very low dispersion (< 5 ns)
- Insensitive to ground properties

Station 1 Data Flow



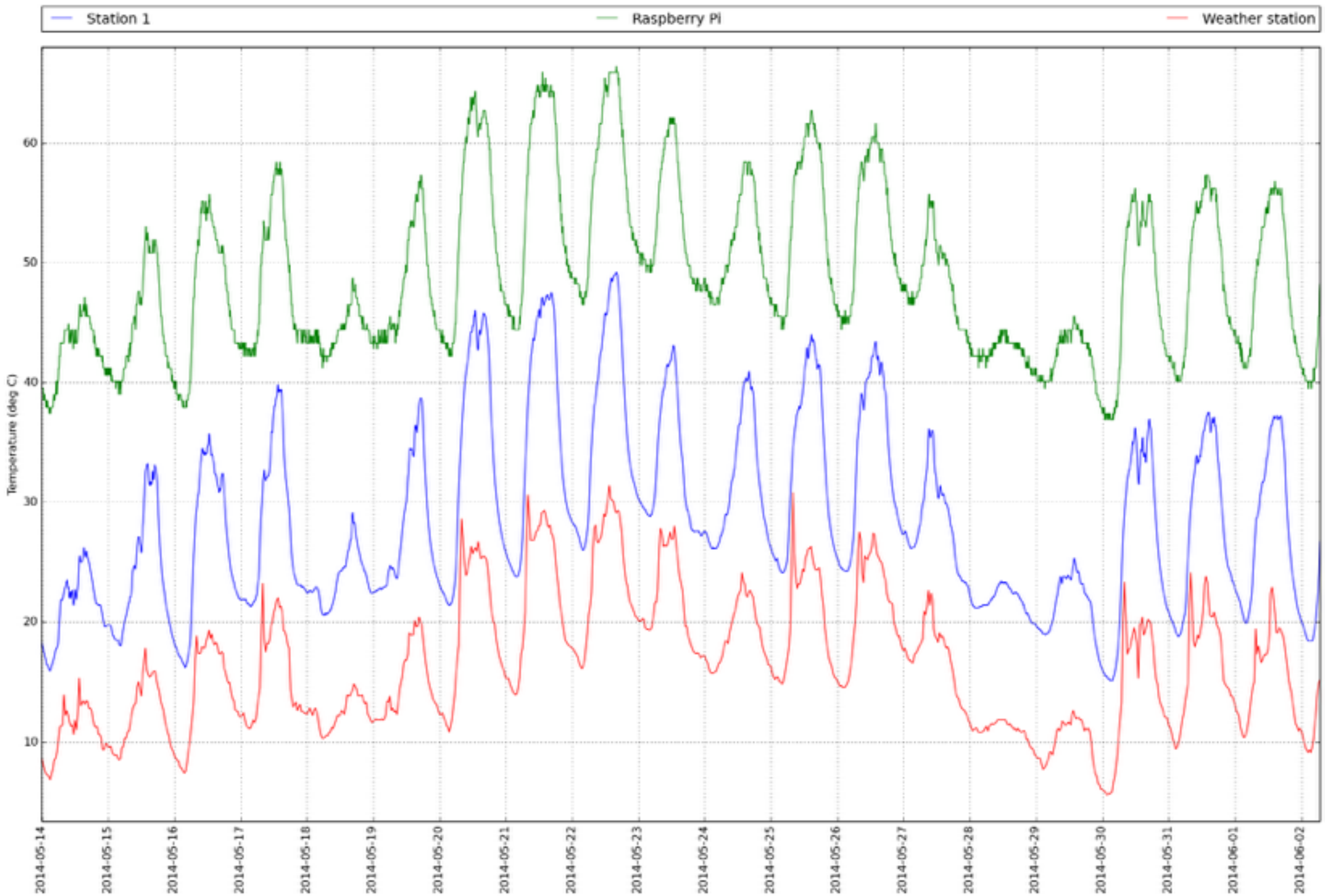
Trigger Board

> Custom made: DESY Zeuthen
> Trigger decision made in FPGA ⇒ flexible trigger logic
> Implemented as stand-alone board
> Inputs:
  - 24 differential, analog signals (3 scintillation detectors × 4 segments × 2 PMTs)
  - Differential receivers and discriminators on three mezzanine boards (1 per scintillation detector)
  - 24 digital signals from discriminators routed into FPGA
> Logic:
  - 1st step: require logical AND between the two signals from one scintillator segment (suppress PMT noise)
  - 2nd step: require at least one segment per scintillation detector in 400 ns
> Outputs:
  - global trigger (to AERA board, VME DAQ, TDC stop)
  - 12× analog signal (analog sum of 2 PMTs / segment)
  - 12× TDC start

Current Mode of Operation

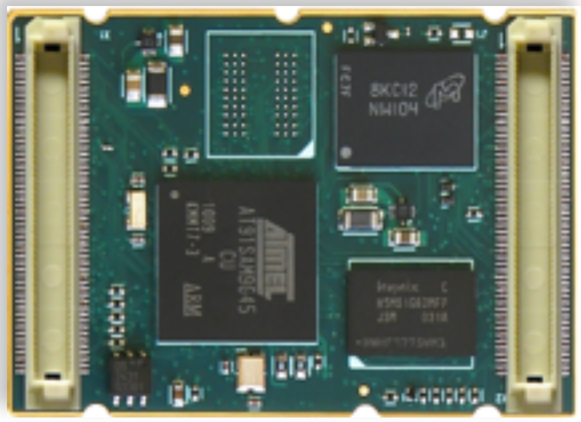
- Unsupervised operation
  - Automatic run transitions every 4 hours
- Readout scheme
  - Scintillation detector triggers AERA board
  - AERA board transmits time stamp to central DAQ PC (in lab)
  - Central DAQ PC requests waveforms from AERA board
  - Can be easily extended to a trigger between several TAXI stations
- Currently, scintillation detector data and AERA board data written to separate streams and merged offline
  - Online data merging in progress
- Trigger rate ≈ 1 min-1

Station 1 Temperature



Ethernet to FPGA Bridge

- ARM based MCU unit (100 €), primarily as ethernet to comm. FPGA bridge
  - Stamp9G45's PCB is only 53.6x38x6.0 mm
  - AT91SAM9G45 runs at 400 MHz with a memory bus frequency of 132 MHz
  - 10/100 Mbit Ethernet, USB, UARTs, …
  - 128 MB NAND flash memory (optional up to 1GB)
  - 128 MB LPDDR-SDRAM (optional up to 512 MB)
  - 16-Bit parallel CPU-Bus (fast FPGA conn.)
  - Memory mapping, DMA, …
  - See also http://www.taskit.de/home.html
  - Comes with real time linux development system
  - Widely used at DESY Zeuthen
  - 400 MHz ARM core can do more than just moving data
  - Might be replaced later
    - e.g by adding the interface part to the Xilinx FPGA



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