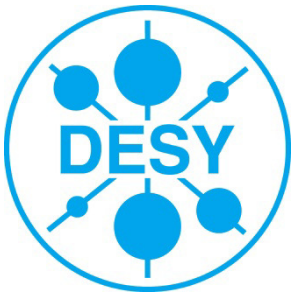
European XFEL

DRAFT Version 0.1 April 2014



Guidelines for DESY Boards

Guide for creation of DESY Schematics and PCBs

by DESY

Michael Fenner

Abstract

This document presents a rule set for getting cleaner designs. All Design rules are taken from design reviews. There is not a single rule that is not based on findings in the designs. Many of them (especially in PCB) are based on errors that managed to get into the produced boards. Following the rules will reduce the number of avoidable mistakes.

DESY MSK

Application Note

© Deutsches Elektronen-Synchrotron
M-Division, MSK – Group
Notkestr. 85, 22607 Hamburg, GERMANY
http://www.desy.de

Notice on Wording throughout this Document
Please carefully distinguish the wording in this guide.
- A “shall”- requirement is a requirement that is mandatory.
- A “should” – requirement is optional but strongly recommended.

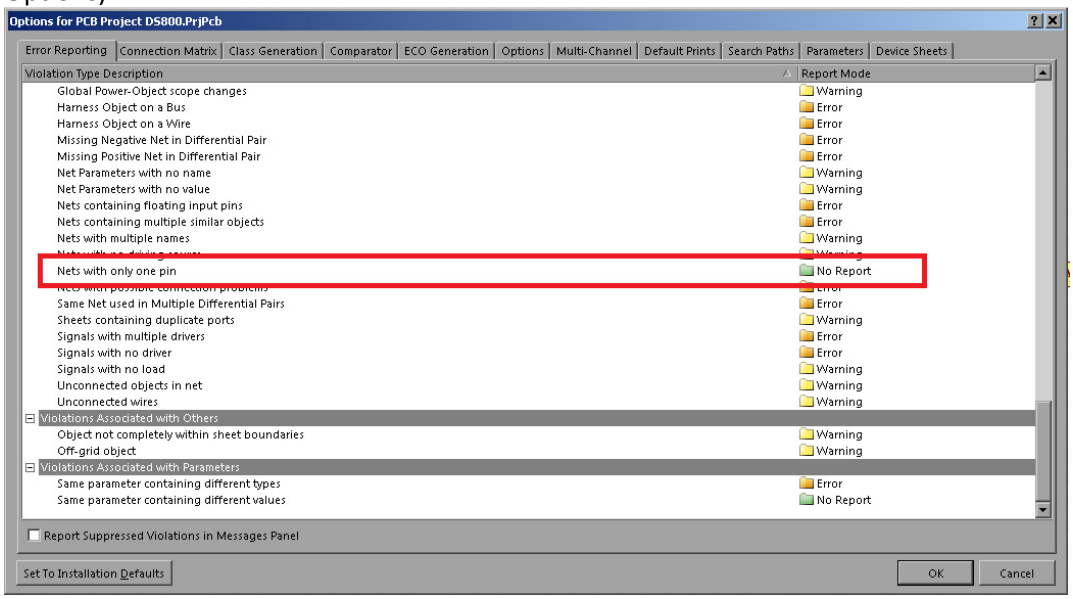
Schematic Rules

Electrical Rule Checks

The Design Rule Check Report (ERC) (Project → Compile Project) shall not contain any valid warnings or errors when project is finished or send to review. It is not possible to avoid all warnings in Altium Designer (especially when you use Harnesses) but it is absolutely necessary that you check the output and remove all valid messages.

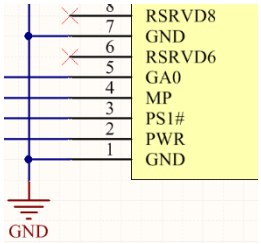
Single Pin Nets

Attention: Alitum Designer does by default not check for single-pin nets. This default setting often leads to open connections because of inconsistent net labels. Always enable this check (Project→Project Options)



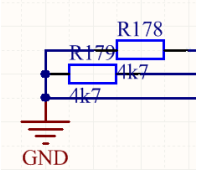
Use NoERC Markers

All intentionally open pins shall get NoERC Markers.



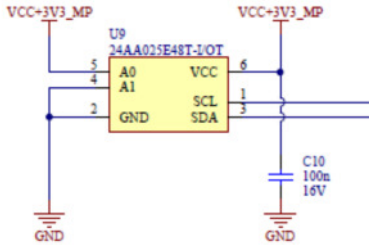
Collisions

Avoid all collisions of texts. Stings and Symbols shall not collide with other objects. Do not draw wires behind schematic symbols



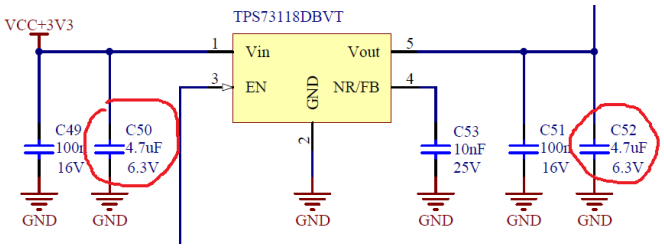
Decoupling of logic ICs

Each logic IC shall have 100nf power supply decoupling (In RF designs there can be some well-defined exceptions). Each Vcc pin should have its own decoupling IC.



Standard Regulator Decoupling

In standard designs, each power regulator shall have decoupling capacitor(s)
The values and types of the capacitors shall match the data sheet requirements (check!) – In RF designs there can be some well-defined exceptions)
Do not omit input capacitor of LDOs.



Commenting

Each I2C IC shall have its address written in schematics as a comment

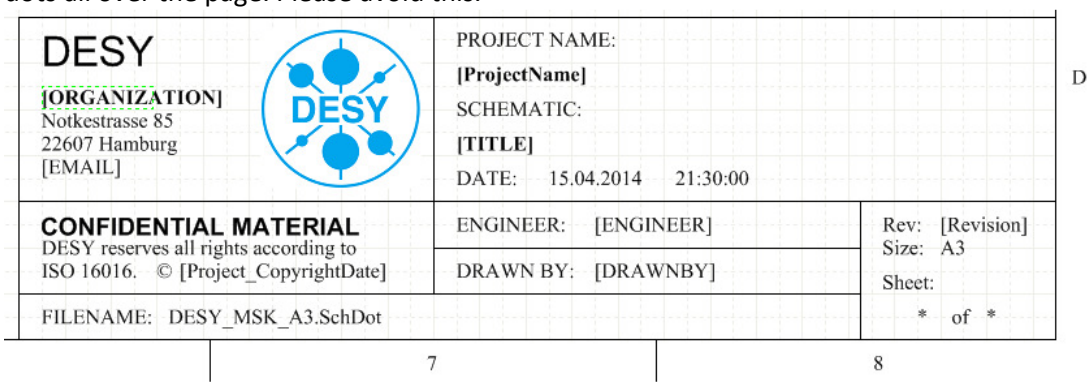
Schematic Templates

All Schematic Pages shall have the standard MSK Template
All Schematic Pages should use the same document size.
Schematic Templates can be found here:
S:\services\Software\Altium\EXTRA\Templates
All parameters shall be assigned. Check “Group” and “Copyright Date”

© Deutsches Elektronen-Synchrotron

M-Division, MSK – Group
Notkestr. 85, 22607 Hamburg, GERMANY
http://www.desy.de

The Background of the document shall be white. By default, Altium Designer has a light gray background (RGB 252, 252, 252) that is not displayed by the screen. In Black and White print out this leads to little dots all over the page. Please avoid this.



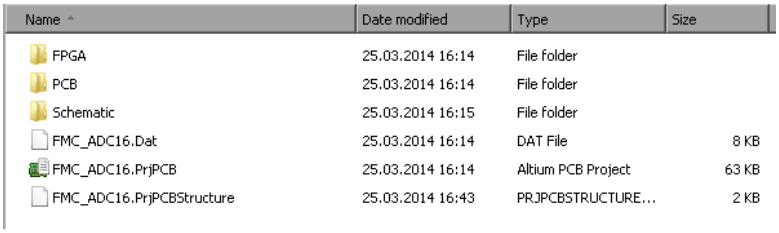
Defaults:

- Organization=MSK Group
- Project_CopyrightDate=Year, e.g. “2015”
- Title=Good name for your page, e.g. “FPGA Power”

File Structure

The project file (.PrjPcb) shall be stored in the project root folder

- The Schematic Files shall be placed in a sub-folder
- The PCB files shall be placed into a sub-folder
- The Output files shall be places in a sub-folder



Name	Date modified	Type	Size
FPGA	25.03.2014 16:14	File folder	
PCB	25.03.2014 16:14	File folder	
Schematic	25.03.2014 16:15	File folder	
FMC_ADC16.Dat	25.03.2014 16:14	DAT File	8 KB
FMC_ADC16.PrjPCB	25.03.2014 16:14	Altium PCB Project	63 KB
FMC_ADC16.PrjPCBStructure	25.03.2014 16:43	PRJPCBSTRUCTURE...	2 KB

Standard Symbols

All Symbols for basic components (resistors, inductors, capacitors) shall look identical throughout the design except that there are good reasons for using different symbols for standard components.
All resistors should use the ISO symbol (rectangle), not the non-standard (American) zigzag symbol.

Unpopulated Components

Unused assembly options (omitted components) shall be commented “DNP” (Not “undefined” or “-“).

Avoid necessity to solder-in Components by Hand

All Component values (e.g. feedback resistors) at shall be shall be calculated and known at design time. If this is not possible, a default or best-guess value shall be used (If necessary, it can be changed later). There shall be no “undefined” values.

When different assembly option exist of which one is mandatory (e.g. Voltage selection via 0 Resistor) one default option shall always be populated. It is not acceptable that components have to be soldered into a new board “by default” to make it operate. (This does not apply if this is necessary for correcting a mistake)

Assembly options

Fixed but configurable chip addresses / chip selects should be made accessible with 0R jumpers or test points for fixing possible address conflict mistakes.

Test Points

Boards that are to be licensed should have test points for every voltage generated by an on-board regulator to allow post-production checking

FPGA Spare Pins to Test Points

Some FPGA pins (for each voltage domain) should be brought to test points (e.g Vias are sufficient as test points) to have later patching options in case of mistakes

Libraries

All parts shall be taken from DESY Altium vault. This means that new parts have to be put to DESY Library before usage (This requires some work on improvement of DESY libraries)
Attention has to be paid to design schematic library symbols reasonably small.

Go to DXP→Preferences→Data Management → Vaults and enter this server:
http://mskaltium-vault:9780

PCB Rules

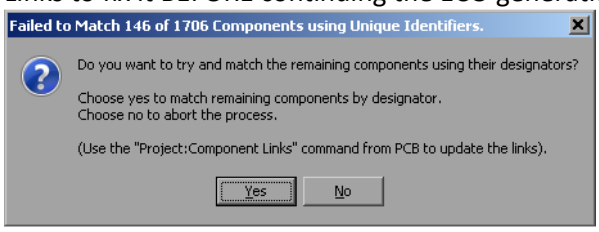
Data Finish

Procedure for finishing Data (Exporting Gerbers) following:

- Import Data from Schematics. Make sure that 0 differences are detected. Check that all components are linked (Project→Component Links)
- Repour all Polygons
- Run Design Rule Check

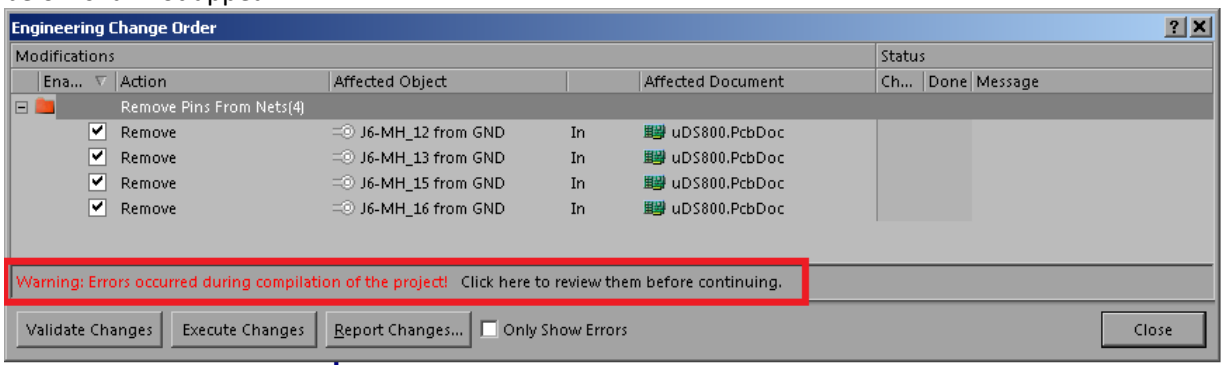
Restoring Component Links

When on Design→Import Changes from PrjPcb following message appears, use Project→Component Links to fix it BEFORE continuing the ECO generation.



No Pending ECO

After Project Finish, the Project shall not contain pending ECOs. Especially the warning ERC warning below shall not appear.



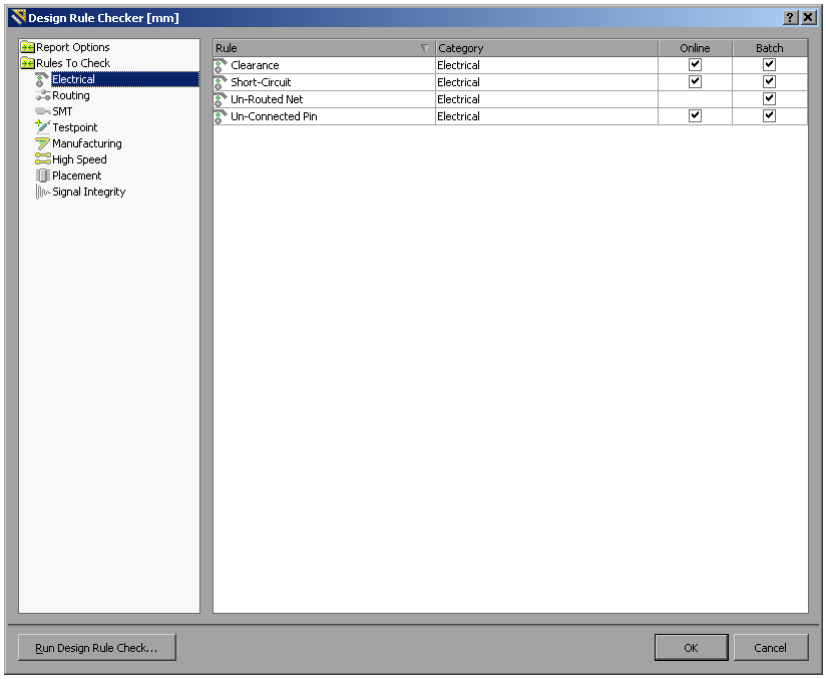
Error Checks

After Project finish, the Rule Check (DRC) shall contain 0 errors.
Especially following checks must be enabled in Batch mode (among others):

© Deutsches Elektronen-Synchrotron

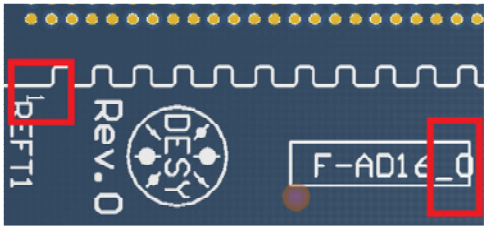
M-Division, MSK – Group
Notkestr. 85, 22607 Hamburg, GERMANY
http://www.desy.de

- Clearance
- Routing Width
- Short-Circuit
- Un-Routed net
- Minimum A. Ring
- Hole Size
- Min. Solder Mask Silver
- Net Antennae



Silk Screen

The Silkscreen should contain the DESY Logo.
The Silk Screen shall contain the Revision Number of the Board. Numbering starts with “A” (preferred) or “1”.
The Board Name shall be printed on the silk screen. Make sure that Silk Screen Name matches the board
Silk Screen Texts shall be checked in 3D view and all text collisions should be avoided
The Board Name shall be printed on the silk screen. Make sure that Silk Screen Name matches the board name (e.g. use “DRTM-VM2LF” instead of “uVM2”)
The Board shall not contain full names of the developers – the initials are sufficient to know DESY-Internally who designed the boards.



Paste Mask

The paste mask shall for standard pins have identical size as the pad except there are good, vendor-independent reasons for changing the shape. Big Pads such as Thermal Pads shall be designed according to data sheet rules.

Solder Mask

If Solder Mask Texts are used, check for Text Collisions in using 3D viewer with switched-off 3D bodies.
Solder Mask should be bigger than pad (non-Solder Mask defined PADs are preferred)

Paste Mask on Vias

Do not put paste mask on vias.

Technology Use

Select a Technology in the beginning of a design and make full use of it.

- Example 1: If you plan to plug vias for better assembly (normally recommended for complex and expensive boards), consequently use via-in pad wherever possible. Do not mix technologies, e.g. Dogbone BGA breakout and Plugged Vias.
- Example 2: If you select 4 mil traces and 4 mil spacing, use 4 mil traces wherever possible. It does not make sense to route some “standard” lines in 6 mil where you have space and in 4 mill where you do not have space. We will pay for 4 mils so using partially 6 mil will only make your life more complex.

Component Correction in the design

Components/ Footprints shall never be corrected in design. Correct it in the library, then import.

3D Models

If possible, Step Models should be used for PCB components in library

PCB Documentation

A finished PCB shall contain following documents when sent to the manufacturer

- Layer Stack up including Report with used Via types (and plugging if necessary)
- …

© Deutsches Elektronen-Synchrotron

M-Division, MSK – Group
Notkestr. 85, 22607 Hamburg, GERMANY
http://www.desy.de

Process Flow Rules

Design Review

Each Project shall have two fundamental reviews

(1) Design Input Review: Specification is checked and Confirmation from all Stakeholders is collected
(2) Design Output Review: Design Data is checked and compared to Requirements

No board shall be sent to production before Design Output Review.

SVN Rules (Applies to project using SVN)

Data shall be committed to SVN every day when design was changed. The Check-In Comment should be a sentence and it should contain a verb (Clear description in SVN before committing)! When a PCB is sent to production and has been accepted by the manufacturer,a TAG shall be created.

RedMine (Applies to projects using RedMine)

Bug Tracking shall be done in RedMine. Everybody who finds a mistake should immediately report it to Redmine. On Final Review of a new revision all Redmine entries shall be closed (fixed or disregarded). Feature Requests should also be reported in RedMine.

Export for Licensing

For license data, the structure shall be as follows:

- TDB

© Deutsches Elektronen-Synchrotron

M-Division, MSK – Group
Notkestr. 85, 22607 Hamburg, GERMANY
http://www.desy.de