The Status and Future of the GDSP Chip

- What is the GDSP ?
- What is the GDSP history ?
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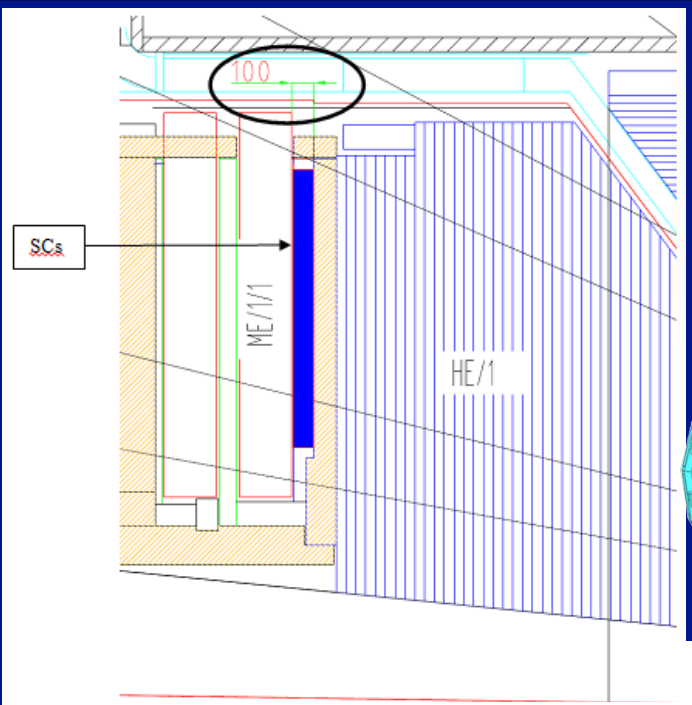
What Is The GDSP Official Project Status ?

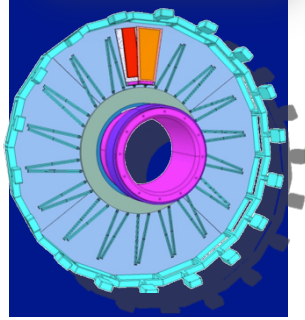
- The GDSP is one of 2 front-end ASIC architectures currently being considered for the CMS high eta up-grade involving GEM detectors.

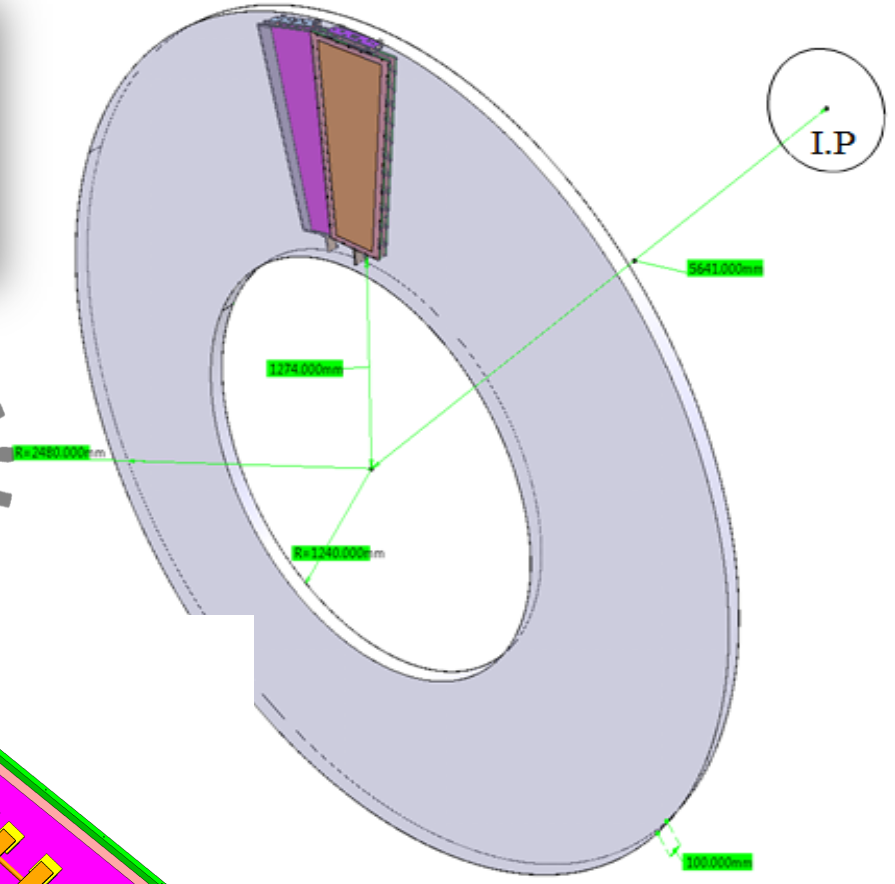
- It is not an independent project with it's own source of funding and manpower resources.

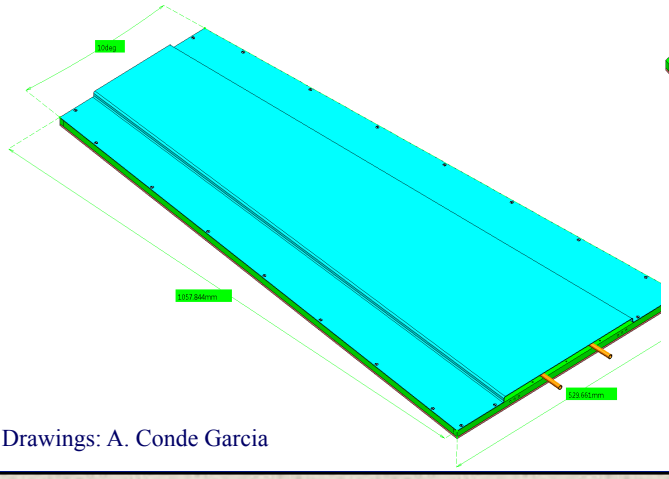
The GEMs for CMS Project

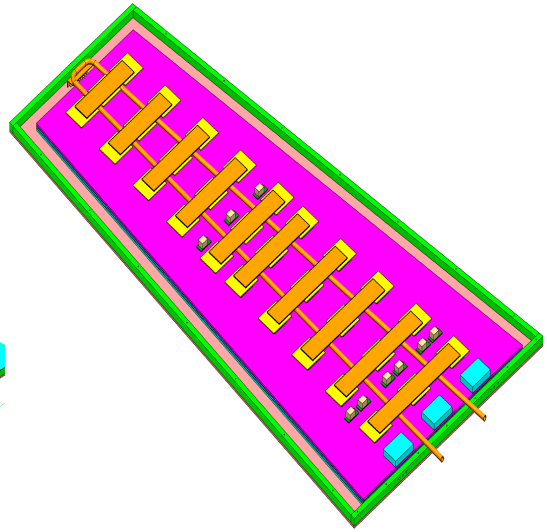
GE Stations : 1.6 > η > 2.1 (2.4)











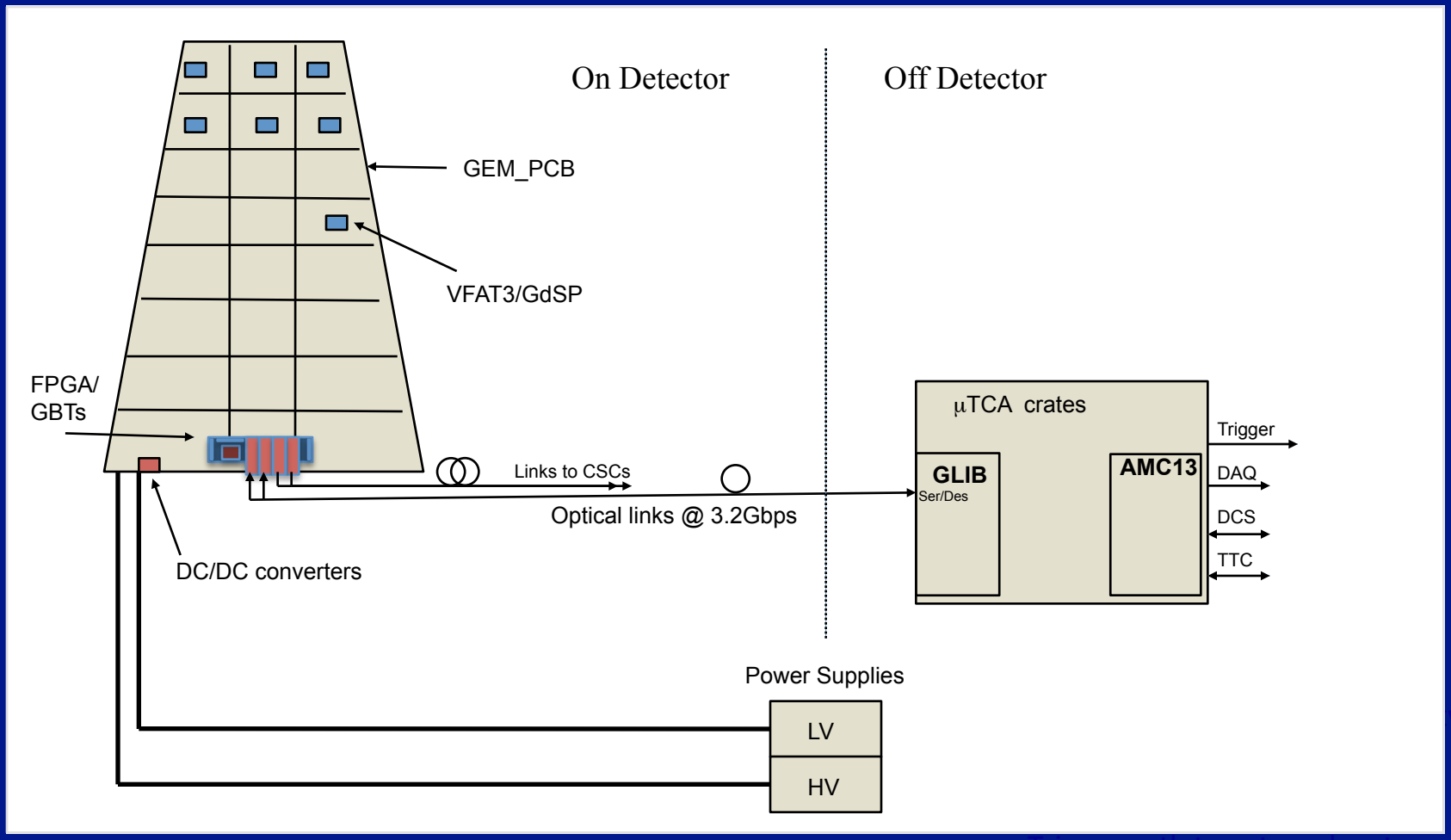
Drawings: A. Conde Garcia

Project to install GEM detectors in the CMS high eta region.

Drawings relate to GE1/1 for LS2

GEM Project Leader : A. Sharma

CMS GEM Electronics System



ween

- Trigger path to external systems at uTCA level.

The CMS GEM project : Global Requirements on Electronics

Provide Trigger & Tracking data from all GE1/1 GEM Chambers

(for the one day workshop Jan 2013)

- GEM detectors
  - Design optimised for gas, and in particular GEM detectors
- Triggering
  - Provide "Fast OR" trigger information with granularity of 2 or 4 channels to send
  - locally to CSC TMB.
  - Timing resolution <8ns.
- Tracking
  - Provide full granularity tracking data on receipt of a LV1A.
  - Be compatible with CMS trigger upgrade possibilities
    - LV1A latency < 20us
    - LV1A rate < 1MHz Poisson

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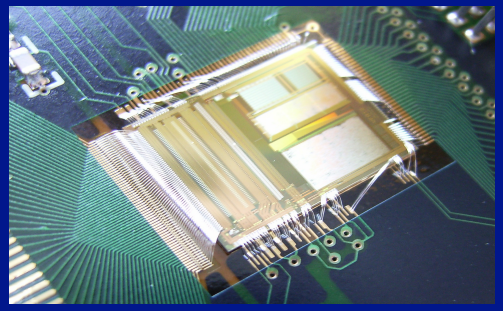
Front-end evolution

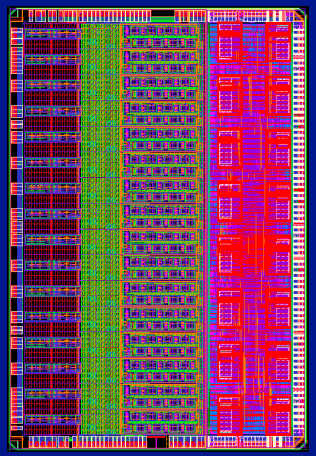
VFAT2



Existing

Used for TOTEM CSCs, GEMs and Silicon. CMS GEM prototypes

SAltro



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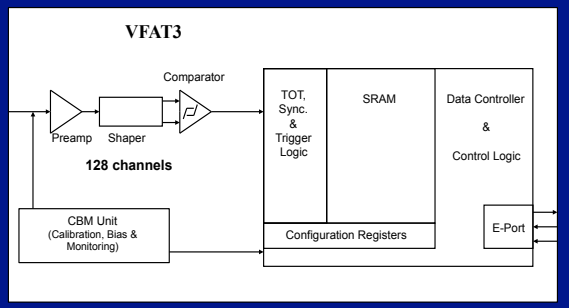
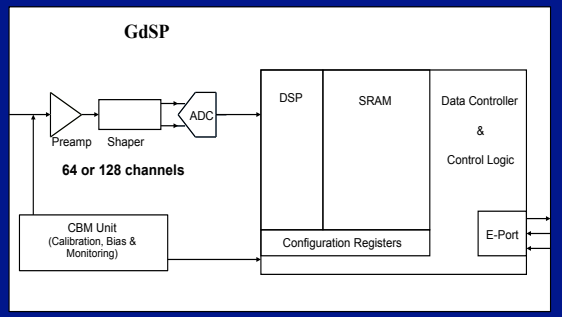
DSP 16 ch demonstrator chip, designed for ILC TPC demonstrator.

VFAT3



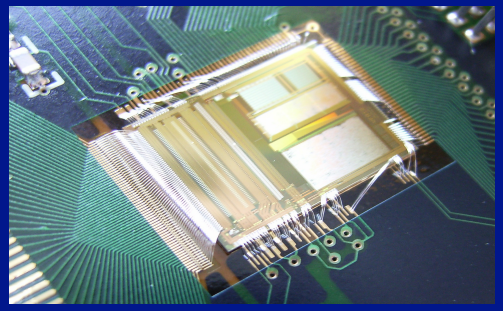
GdSP



Future : design developments

Front-end evolution

VFAT2



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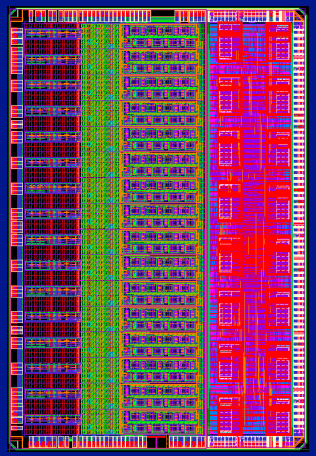

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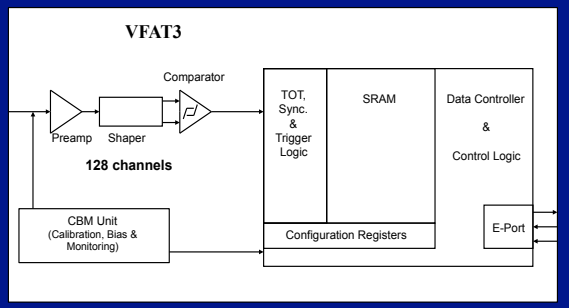

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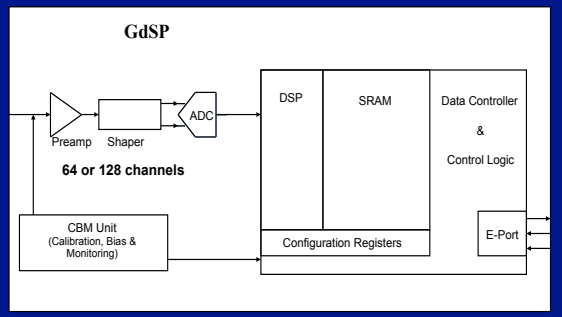
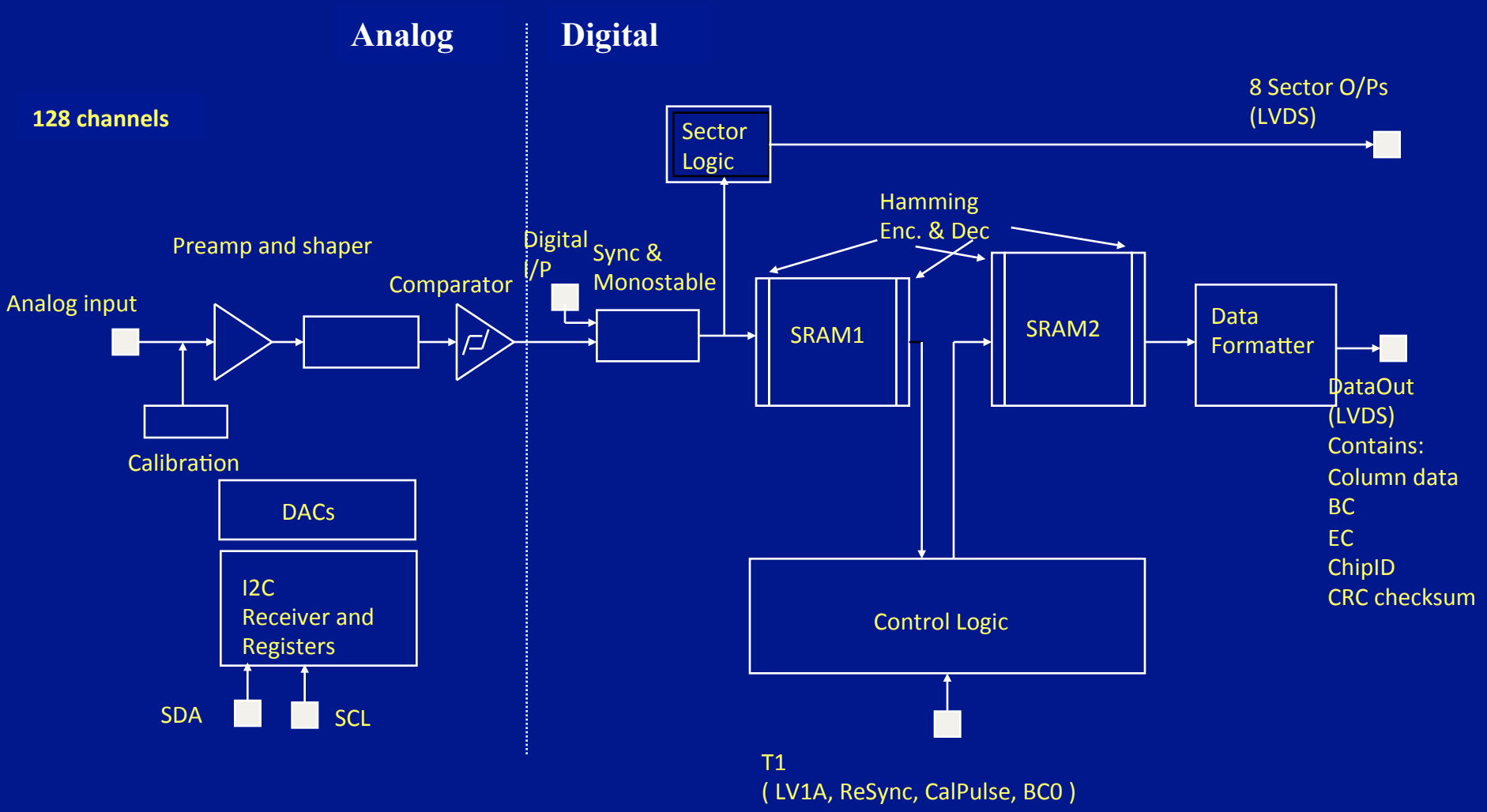
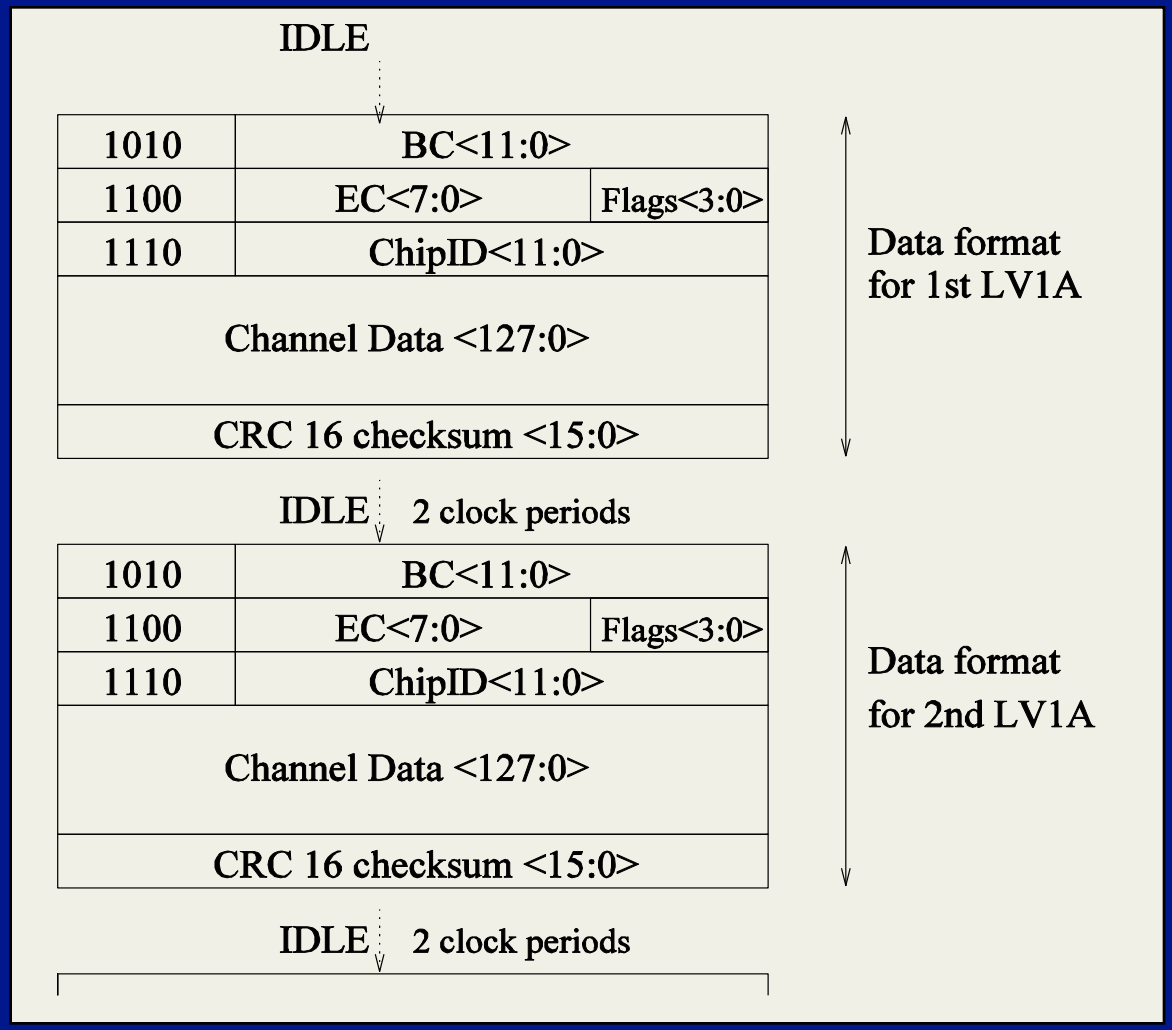


Future : design developments

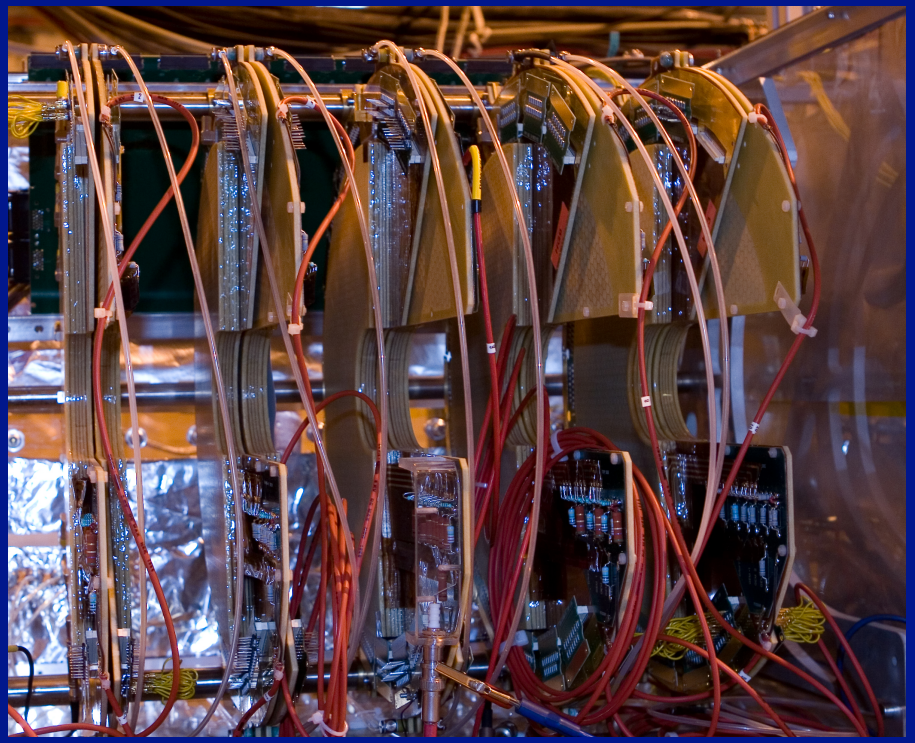
VFAT2


Analog
Digital
128 channels
8 Sector O/Ps
(LVDS)
Sector
Logic
Hamming
Enc. & Dec
Preamp and shaper
Digital
I/P
Sync &
Monostable
Comparator
Analog input
SRAM1
SRAM2
Data
Formatter
DataOut
(LVDS)
Contains:
Column data
BC
EC
ChipID
CRC checksum
Calibration
DACs
I2C
Receiver and
Registers
Control Logic
SDA
SCL
T1
(LV1A, ReSync, CalPulse, BC0)

VFAT2 Data Format



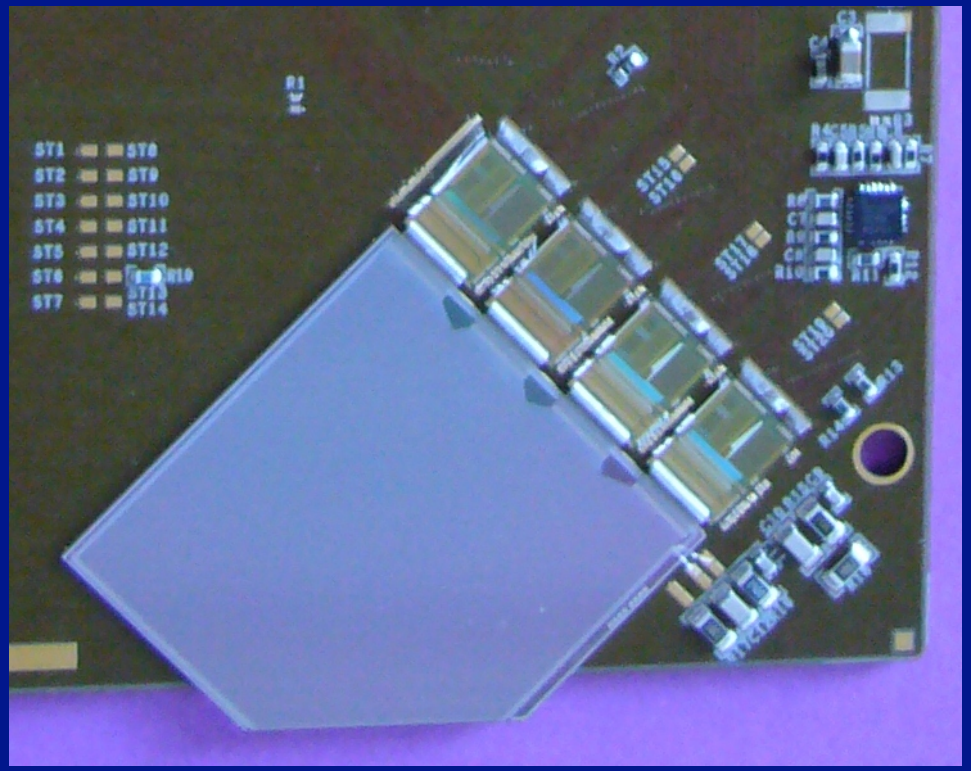
TOTEM's 3 different detector technologies



T2
GEMs

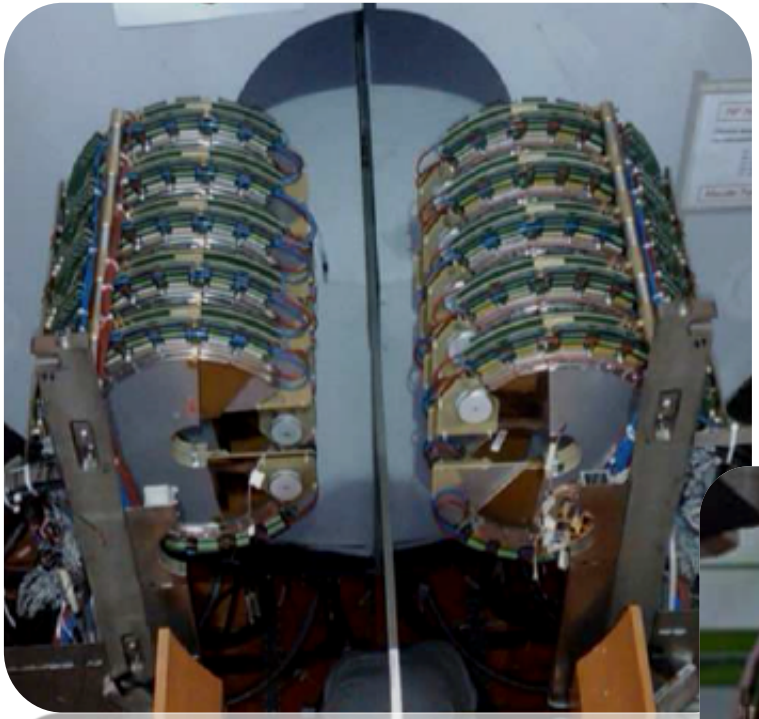
VFAT2 is used with all 3 detector technologies currently operating in LHC.

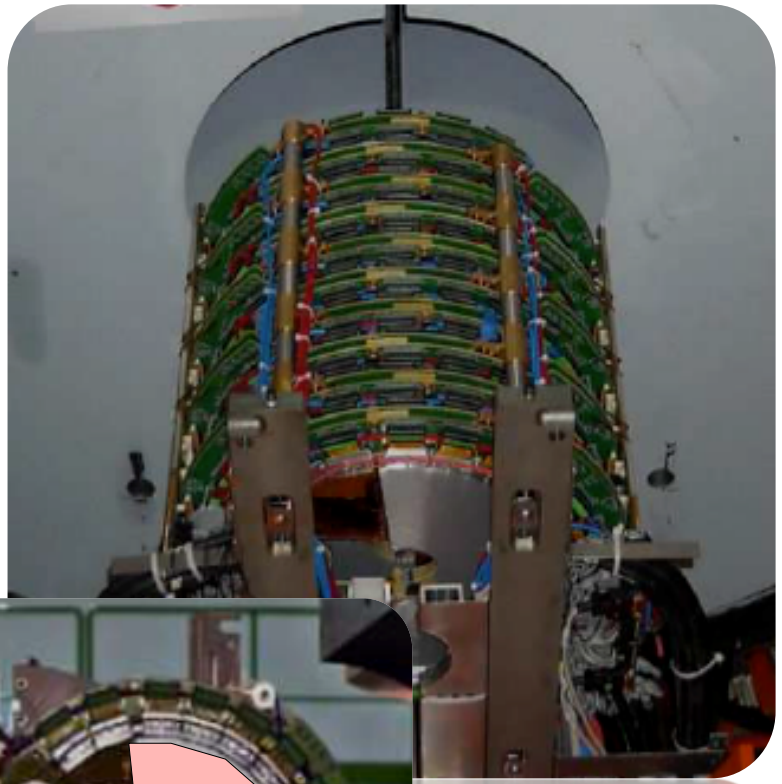
Roman Pot – Silicon strips

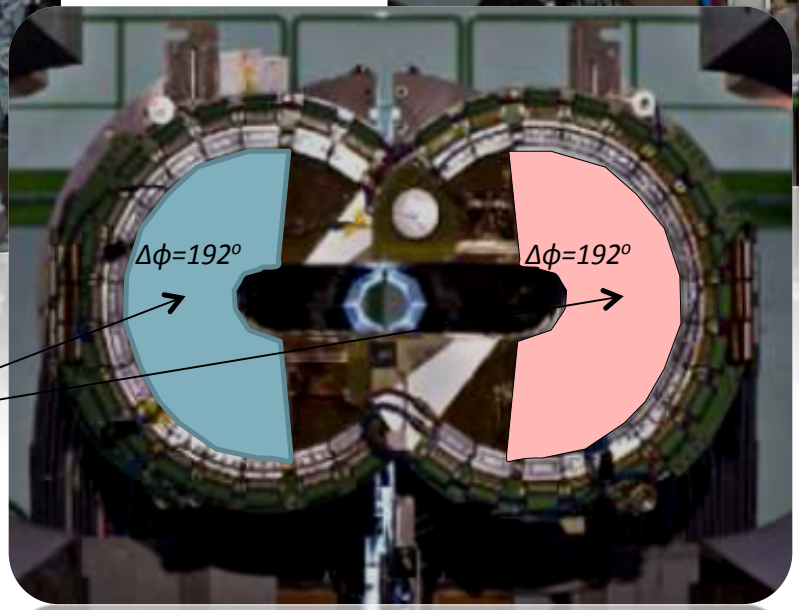


T1
CSCs

TOTEM T2 in open/close position







Sensitive Area

Main reasons to move from VFAT2 to new front-end

- For both Trigger and Tracking we require binary hit data with channel location and time stamp accurate to one clock period.

- VFAT2

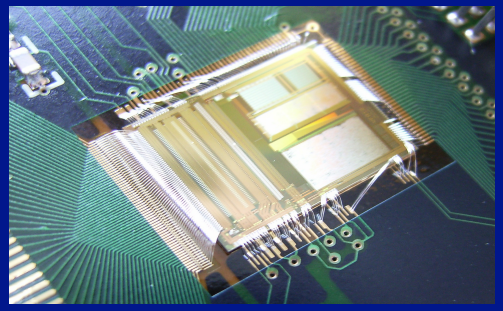
- Maximum trigger granularity = 16 channels
- Fixed shaping time = 25ns
- Data output rate limited to 40MHz.
- Max LV1 latency = 6.4us (LHC=3.2uS)
- Max LV1 rate = 200 kHz (LHC=100kHz)

- Principle additional functionality required by new ASIC

- Increased granularity at trigger level.
- Programmable shaping time, avoid ballistic deficit and improve S/N whilst maintaining timing resolution.
- Reduce effect of background artifacts and baseline shifts
- 320Mbps e-link for data output
- Max LV1 lat > 20us
- Max LV1 rate > 1MHz

Front-end evolution

VFAT2



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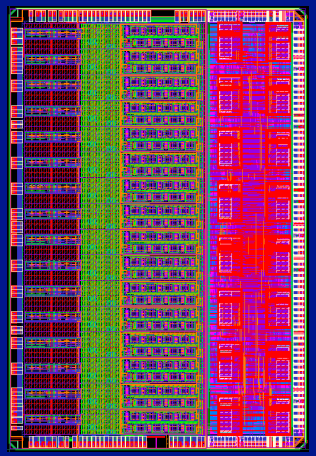

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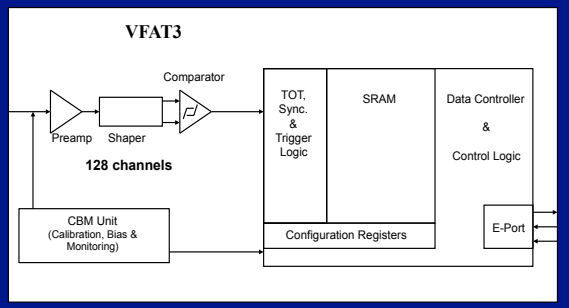
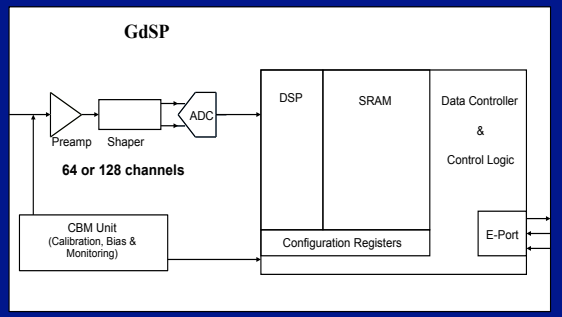
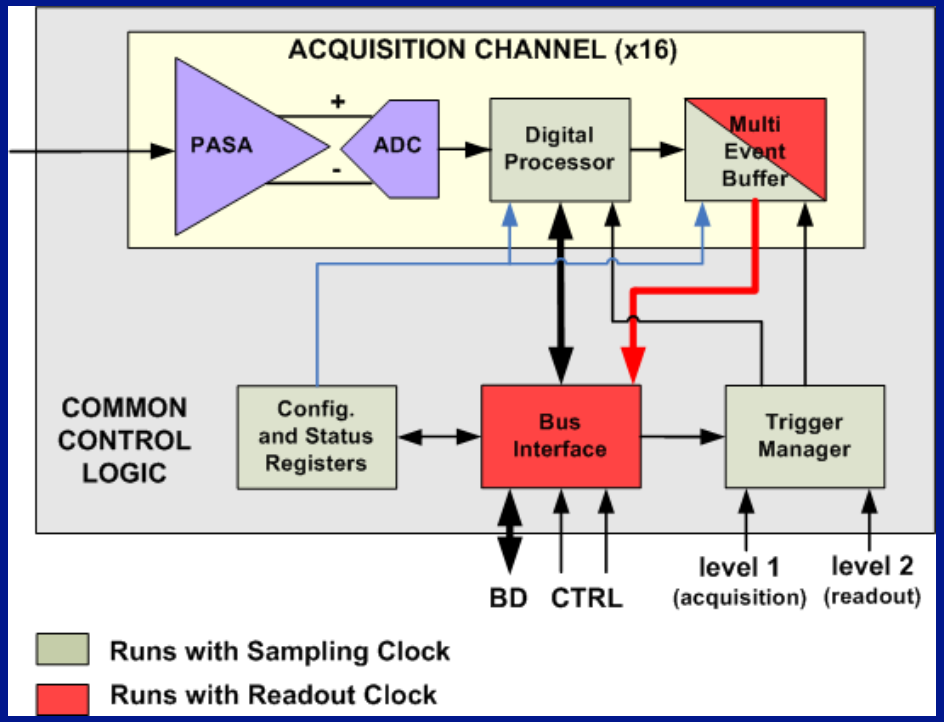


GdSP



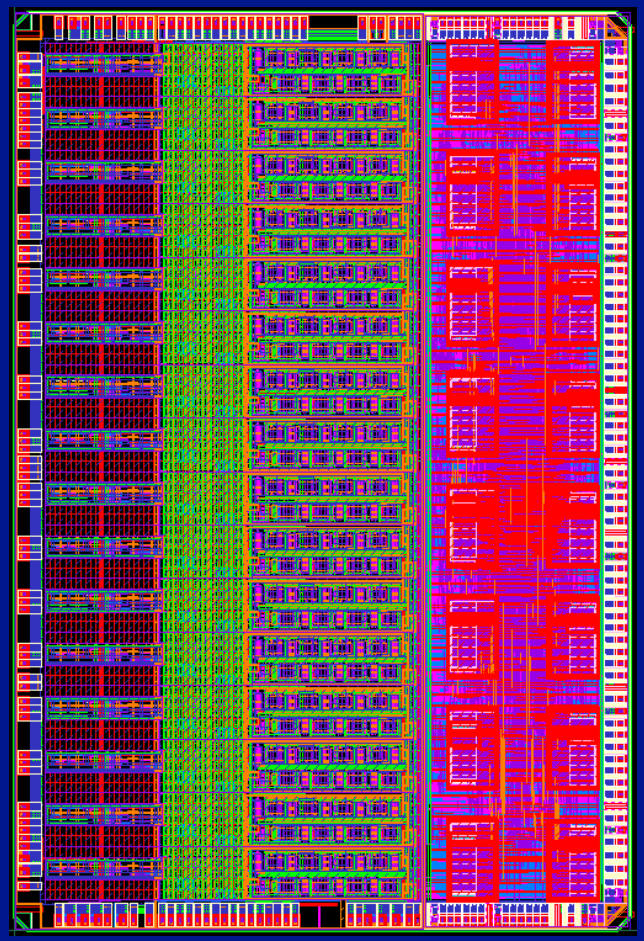
Future : design developments

SAltro16



16 channel demonstrator chip designed in 2009-2010, Tested and working beautifully.

Technology : IBM 130nm CMOS



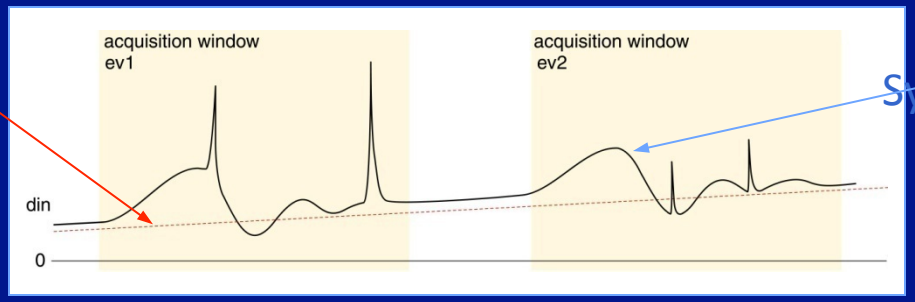
Luciano Musa ..... S-Altro Specs. & Architecture
Paul Aspell ..... Coordinator of design
Designers :
Massimiliano De Gaspari ..... Front-end + ADC
Hugo França-Santos ..... ADC core
Eduardo Garcia ..... Data Processing & Control

Saltro Digital processing

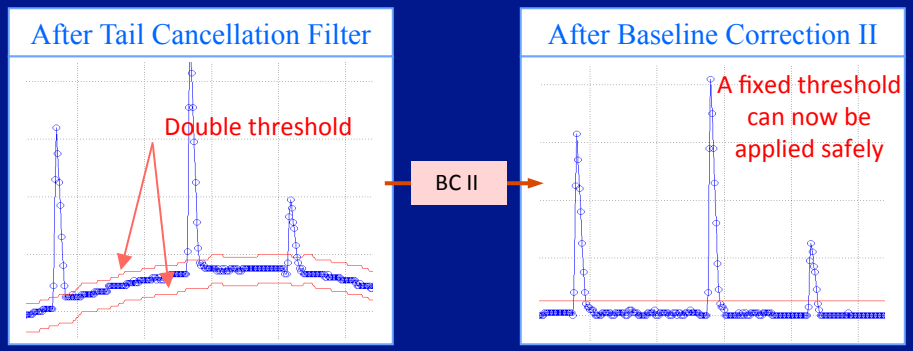
Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to undershoot.
Baseline correction 2	Reduces low frequency baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.

Digital processing

Baseline drift



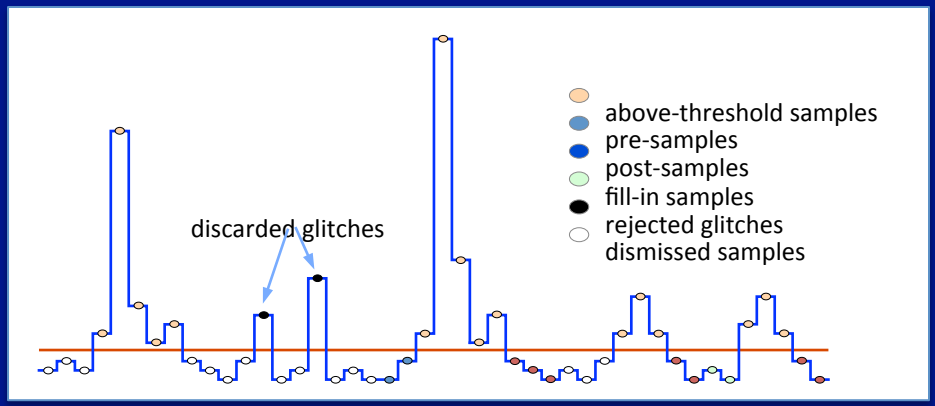
Systematic perturbation



Corrects on-chip for :

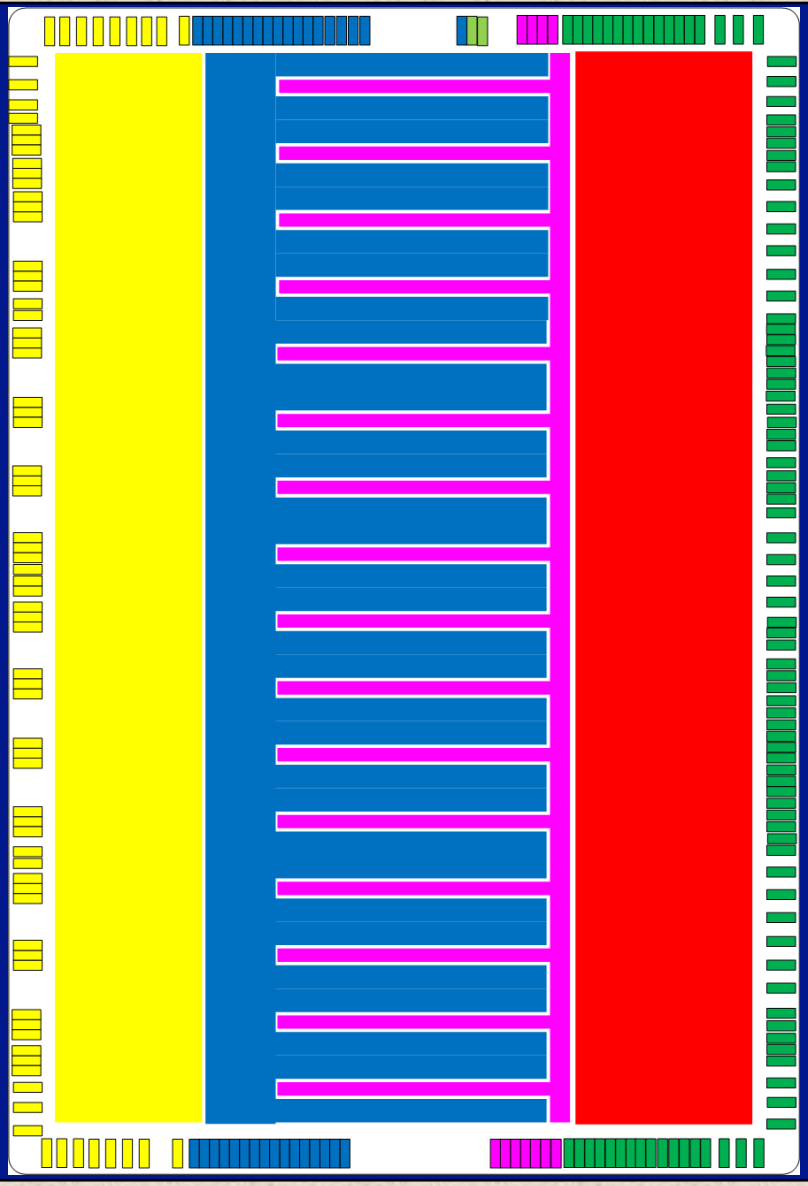
Systematic offsets,
Baseline movements
Ion tails
Removal of glitches

Zero-suppressed output



DP Design and simulations : Eduardo Garcia

SAltro16 Power & Power Domains



Power domains:

PASA analog

ADC analog

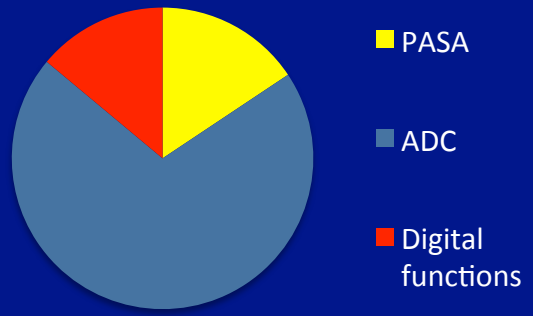
ADC digital

Digital core

Digital Pads

PASA ~8mW/ch,
ADC 36mW/ch @40MHz
Digital functions ~114mW
Total power ~ 750mW

Power Distribution for 16 channels



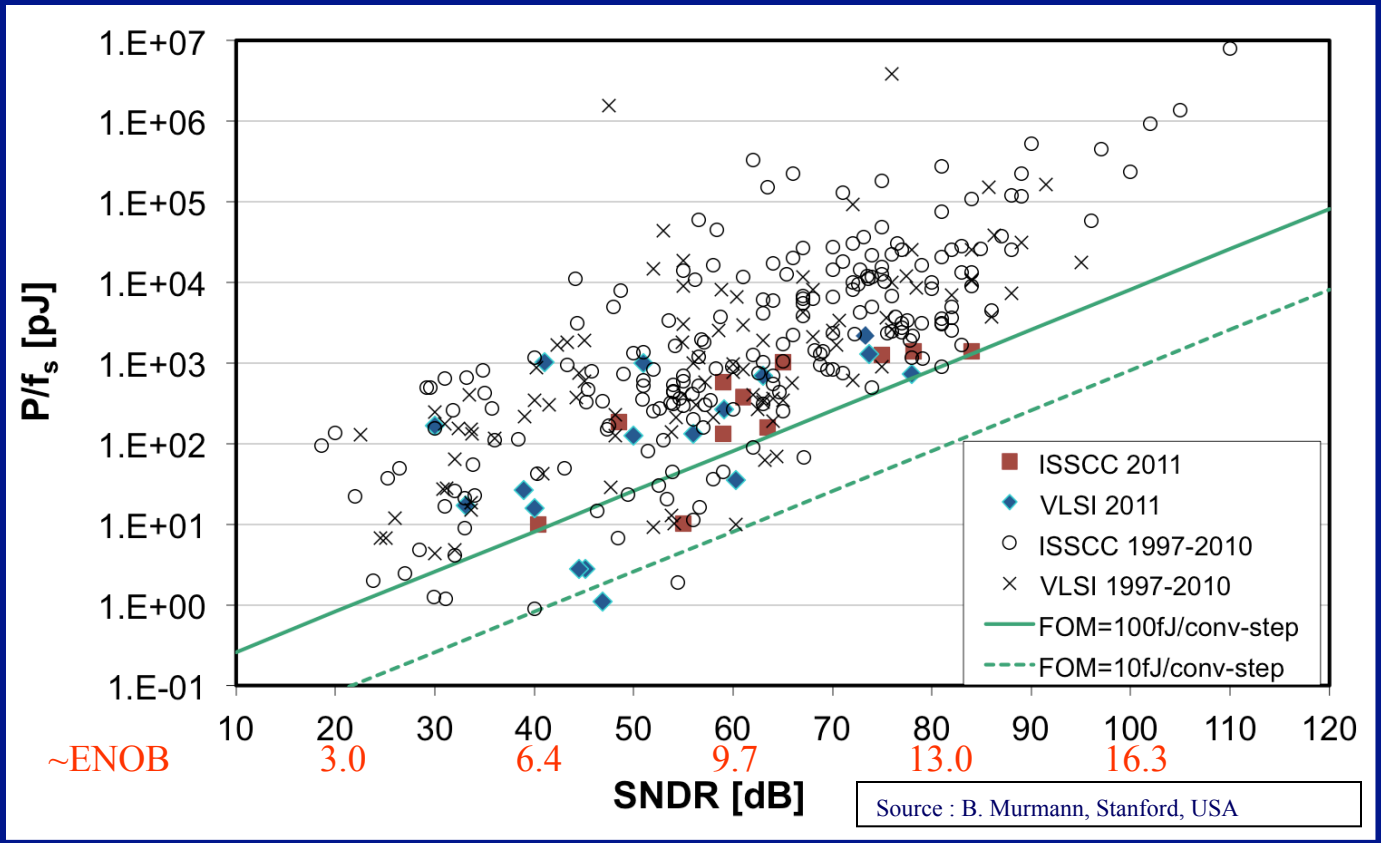
It is clear that the ADC power consumption limits the design to small channels counts.

But times are changing.

ADC Trends

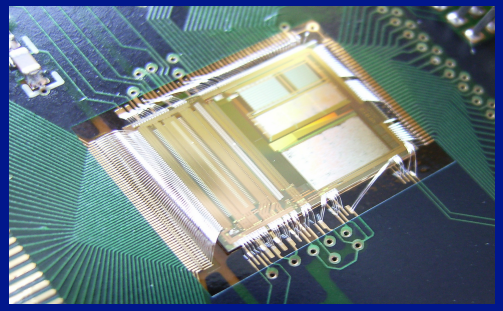
- FOM ~ P / (2^{ENOB}. 2BW)

- 1pJ is high
- (~40mW @ ENOB 9, 40MS/s)
- 100fJ is good
- (~4mW @ ENOB 9, 40MS/s)
- 50fJ excellent
- (~2mW @ ENOB 9, 40MS/s)



Front-end evolution

VFAT2



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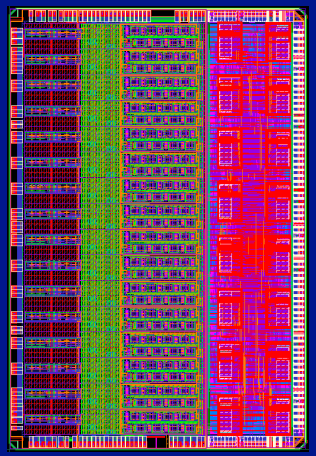

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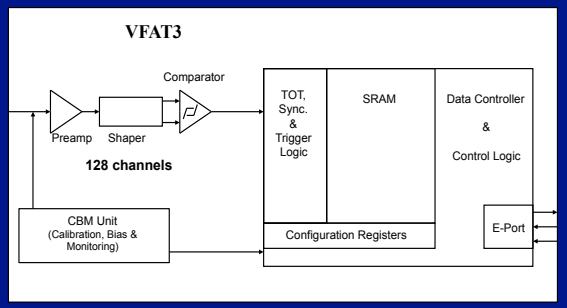

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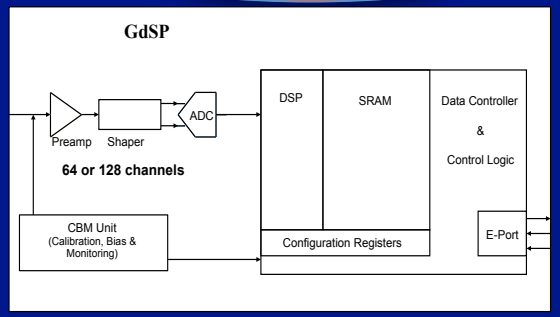
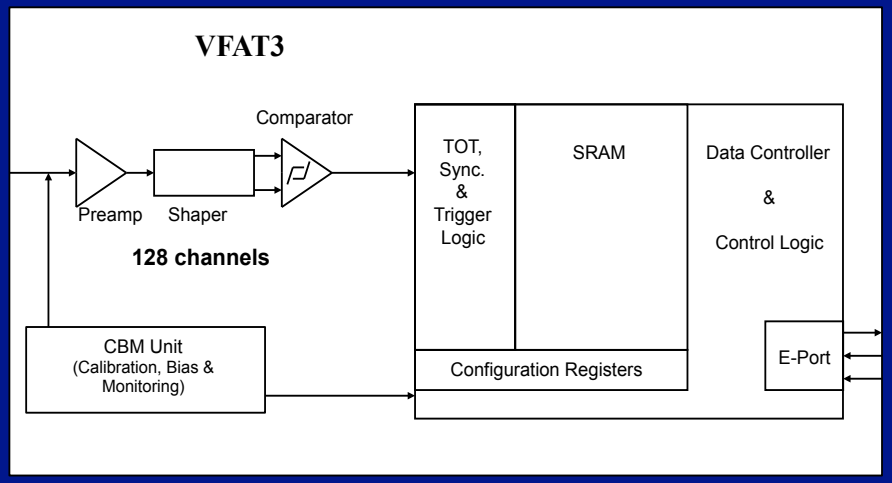


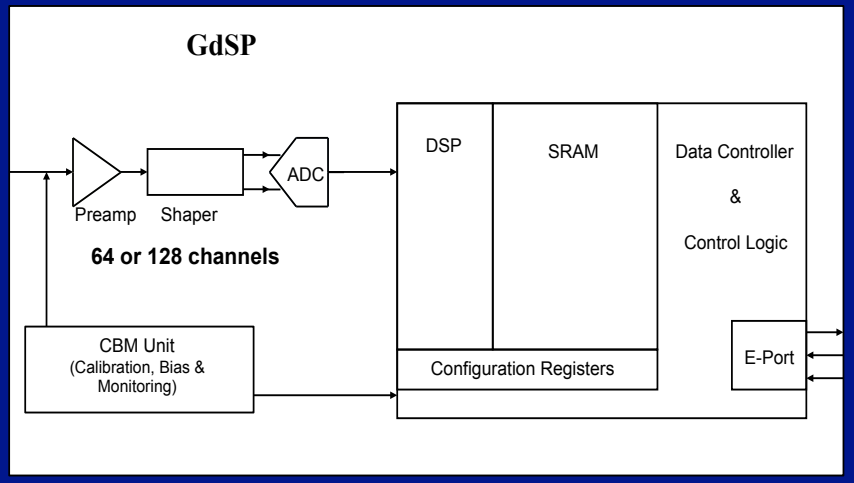
Future : design developments

Front-end Microelectronics Design 2012-2015
VFAT3/GdSP ASIC design

2 Trigger & Tracking Front-end architectures considered.



OR



VFAT3 :

Front-end with programmable shaping time.

Internal calibration.

Binary memory

Interface directly to GBT @ 320Mbps.

Designed for high rate (10kHz/cm^2 depending on segmentation)

Approx. 8-10 man years of design work expected .

GdSP :

Similar to VFAT3 except has an ADC / channel instead of a comparator.

Internal DSP allows subtraction of background artifacts enabling a clean signal discrimination.

Centre of gravity a possibility to achieve a finer pitch resolution (if needed).

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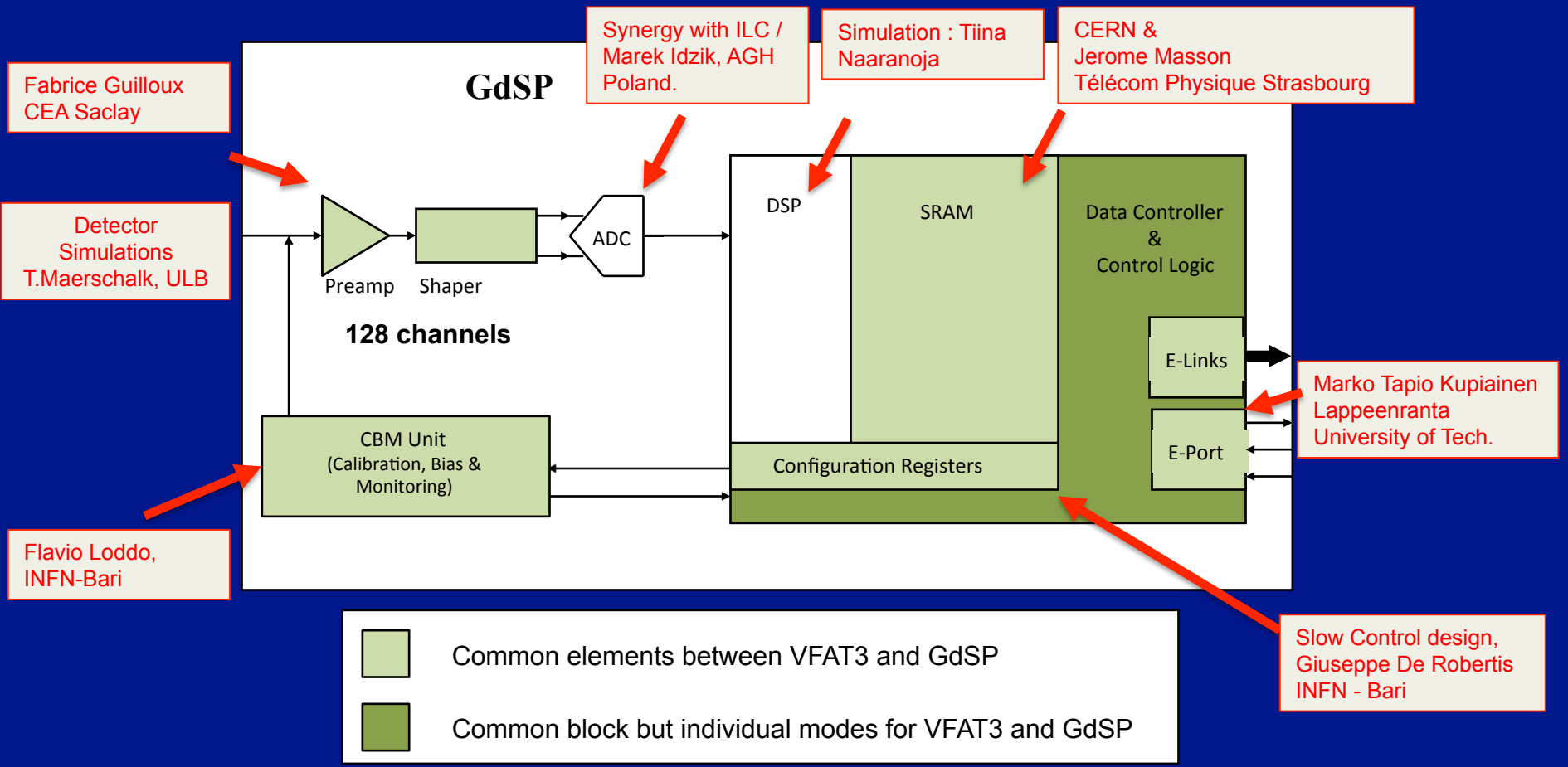
Microelectronics design



2012 : Initial focus on VFAT3/GdSP elements needed for architecture choice and common architecture building blocks.

2013: Front-end prototype + advance design of common modules + define final specific modules & architecture

Aim to complete design by 2015.

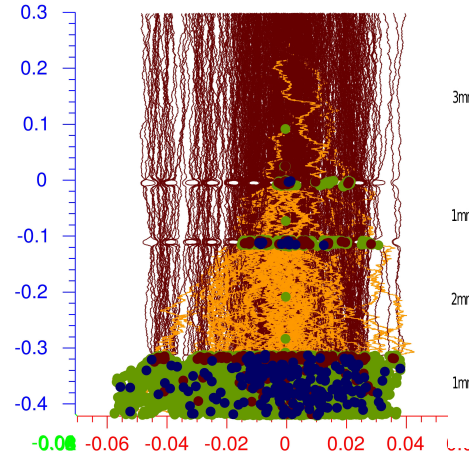
Design team not yet complete : Additional PhD student or Fellow required.

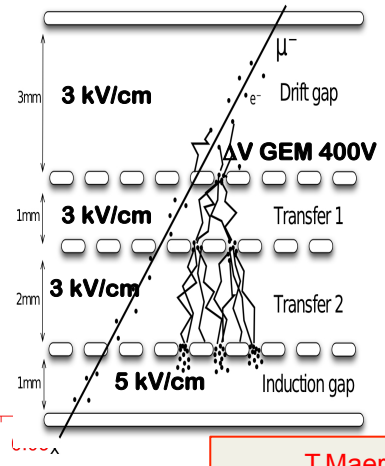
Coordination : Paul Aspell, CERN

Detector Studies & Timing Resolution

Single electrons released in the drift gap

- Single electron avalanches

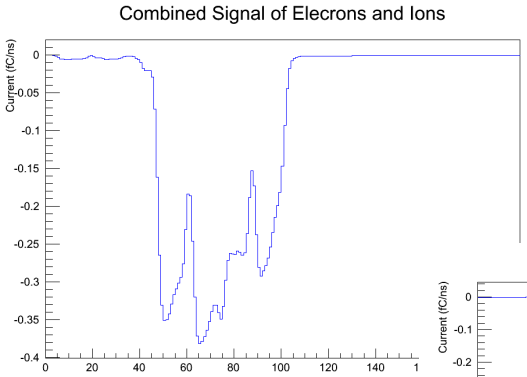




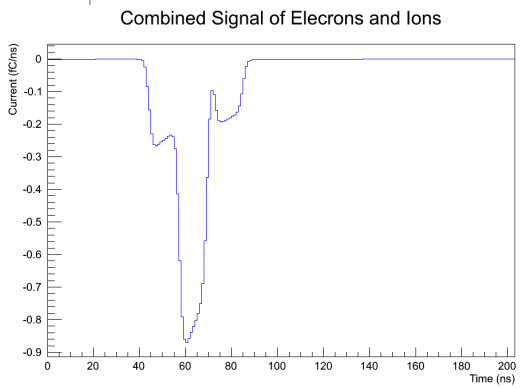
T.Maerschalk, ULB

October 2nd 2012 4

Signal produced by muons



- **Induction gap : 0 - 14 ns**
- **Transfer 2 : 14 - 42 ns**
- **Transfer 1 : 42 - 56 ns**
- **Drift gap : 56 - 98 ns**



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Timing resolution determined by detector.

Fast shaping (as with VFAT2) give good timing resolution (~7ns) but bad signal to noise due to ballistic deficit.

Slower shaping times give better S/N but worse timing resolution due to time walk.

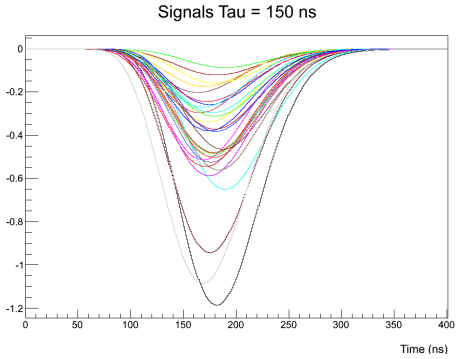
GdSP digital techniques to optimise time resolution with longer shaping times being studied by Tiina.

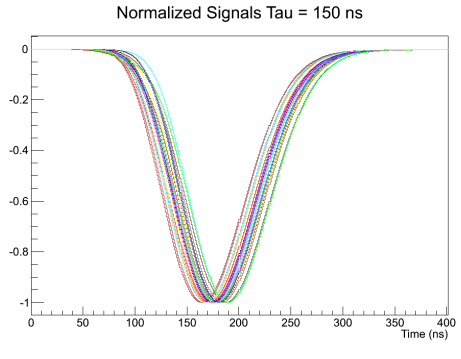
VFAT3 analog discriminator with CFD or time walk correction needs to be designed (next PhD student)

Detector Simulations : Timing Resolution

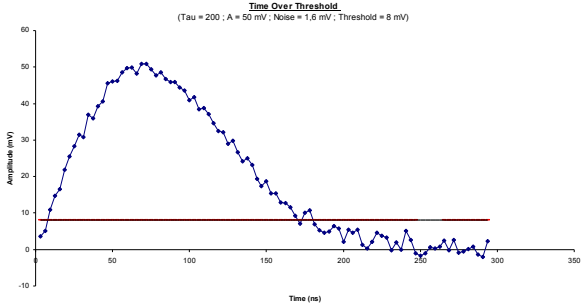
29 simulated signals

- After convolution with PASA electronics transfert function





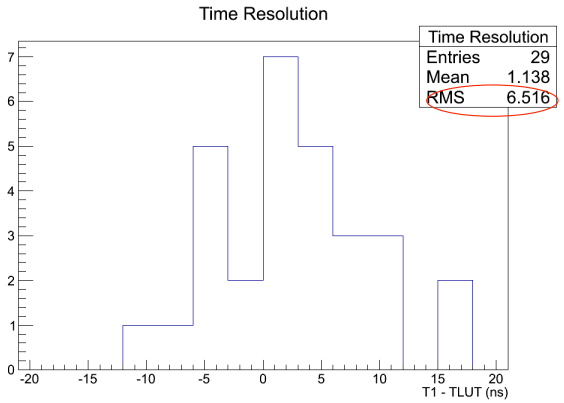
TOT principles



- TOT→# clock cycles → LUT → T1
- Compare $T1_{LUT}$ to real T1 of the signal

TOT Time resolution

- RMS < 7 ns

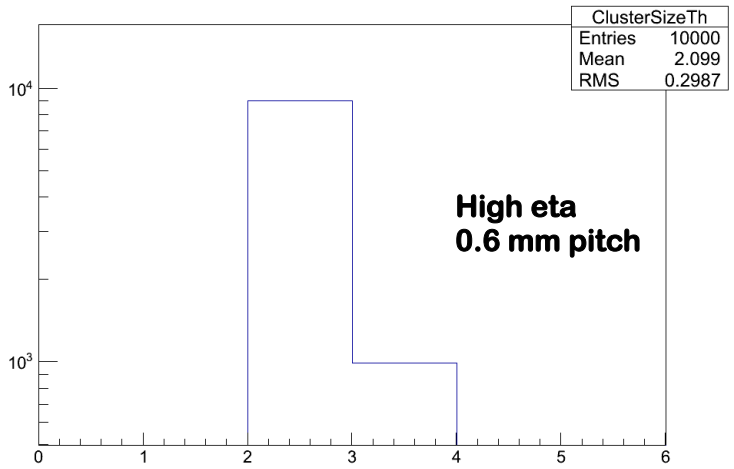


Detector Simulations : Cluster Size

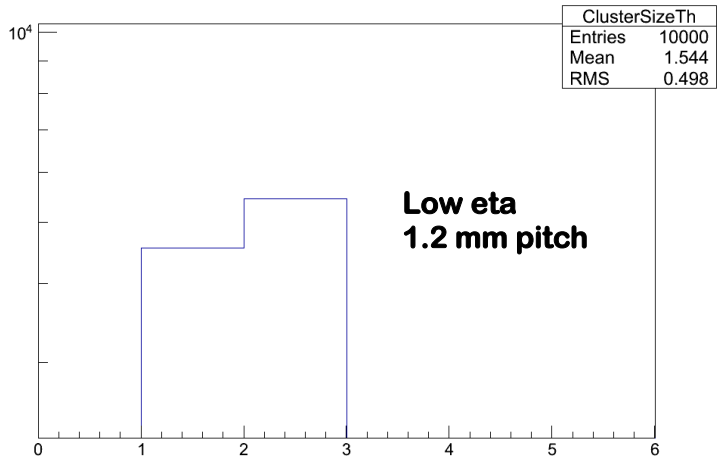
Cluster size

In simulations, threshold applied on strip charge: $Q_{strip} > 5\%\ Q_{cluster}$

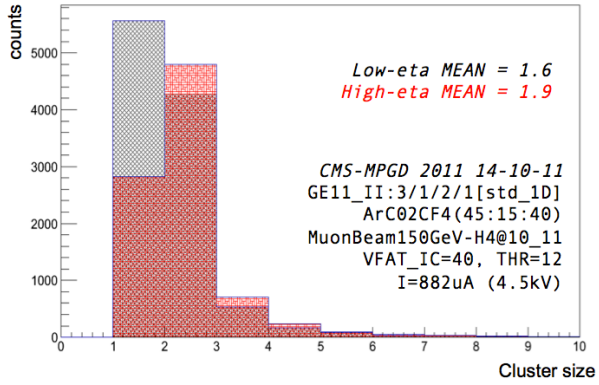
ClusterSize with Threshold



ClusterSize with Threshold



GE11_II cluster size



October 2nd 2012 11

Combining detector charge with front-end

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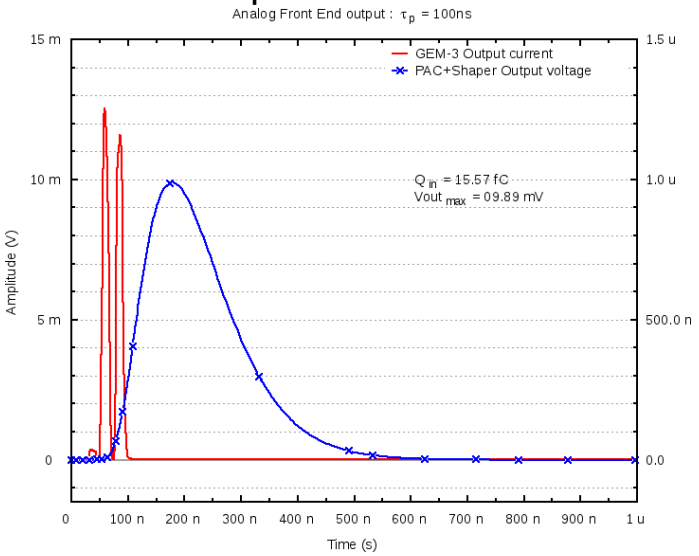
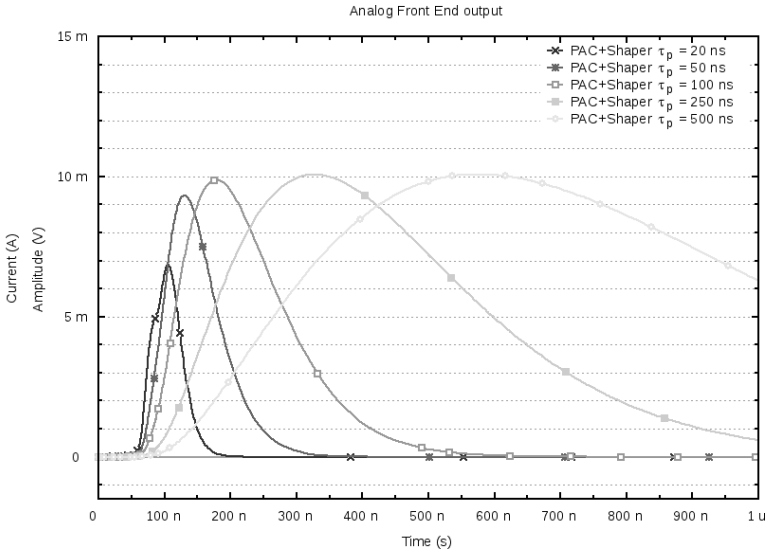
Institut de recherche sur les lois fondamentales de l'Univers

Summary of last results 2 Shaper symmetry

- CSA responses





  - Ballistic deficit @ 20ns + irregular shape
  - Asymmetric shaper is probably better for TOT but increases baseline recovery time
- 2 types of shaper under study:
  - "Symmetric" : complex conjugate poles (Delay Derivative Feedback = DDF)
  - "Assymmetric" : real coincidence poles (Sallen-Key = SK)

CSA and shaper will be tested in a prototype : Common Front End (CFE) Asic

Fabrice Guilloux
CEA Saclay

Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

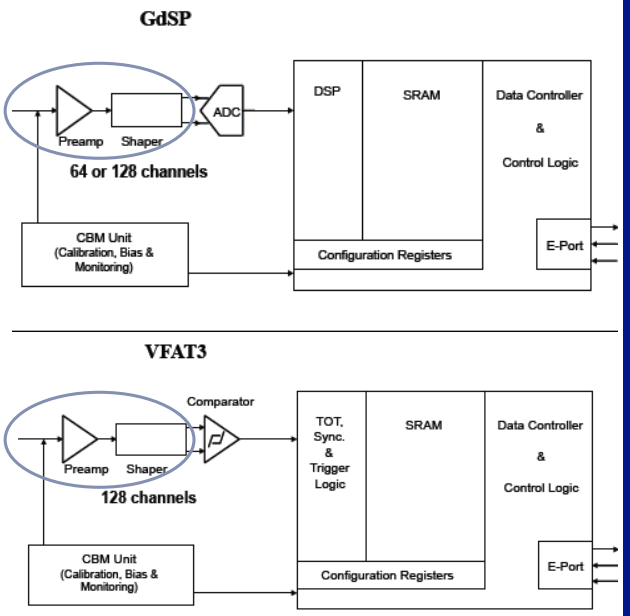
GdSP/VFAT3 ASIC

- Join effort to have one ASIC for 2 projects. Or at least large common parts.
- Common philosophy : Analogue shaper + digital data processing

  - LCTPC (AIDA)
    - specifications derived from SALTRO16 *(slower, low cap)*
    - *Digital filters*
  - Muon CMS upgrade :

Common front end

    - First option : VFAT3 ASIC
    - Second option : GdSP ASIC
    - Specifications derived from previous VFAT2 *(faster, high cap)*
    - *Signal processing :TOT + Trigger logic (+ CoG under study)*



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GdSP Front End : pre-amp study

- Requirements summary

Parameter	VFAT3/GdSP	unit	Remarks
Input capacitance	5 – 10 –30 – 60	pF	Simulation cases
Shaper peaking times	25 – 50 – 100 – 200	ns	programmable
Events input rate			
Gain	12.5 – 25 – 50	mV/fC	programmable
Polarity	dual		
Dynamic range	150	fC	@ 12.5 mV/fC gain
Linearity Error : small charges	<1	%	up to 100 fC
Linearity Error : high charges	<5	%	up to 200 fC
Power consumption	<1	mW/chan.	@ Tpeak = 100 ns
Noise	1100	e-	@ Tpeak = 100 ns @ 1 mW/chan @ Cin = 30pF

- Previous dynamic range : 200fC but 200x12.5e-3 = 2.5V
  (max dynamic range = 2.4V in differential with 1.2V power supply)
  Other solutions
  - Power supply = 1.5V (as SALTRO)
  - Gain <12.5mV/fC

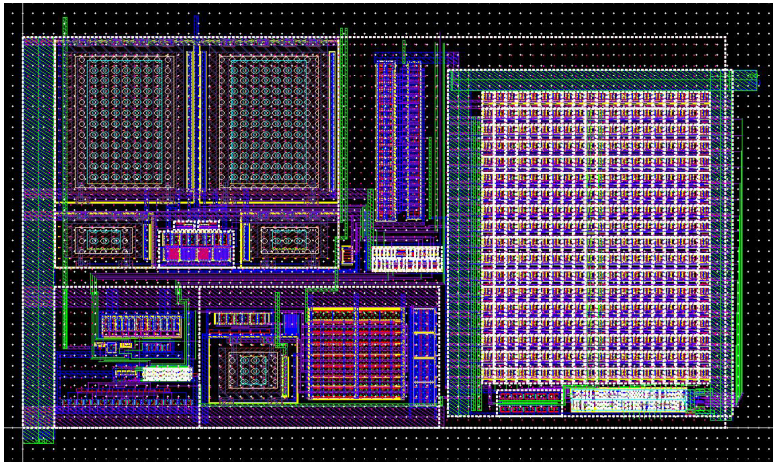
FEATURES

- Bias circuitry for preamp/shaper/discriminator .
- Calibration test pulsing
- Monitoring circuitry [Gain, Temperature (external or internal sensor) .]

BUILDING BLOCKS

- DAC
- ADC
- Bandgap Reference
- ..

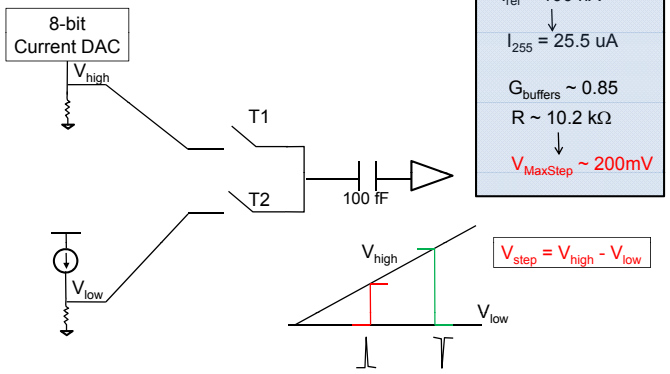
FULL CALIBRATION LOGIC



340 x 190 um^2

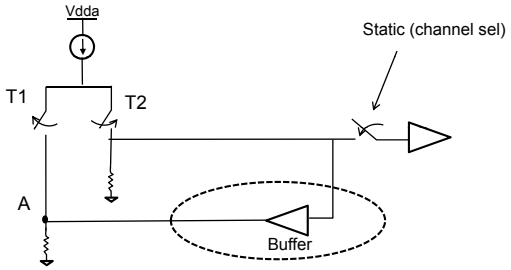
Calibration test pulsing

Step voltage – series capacitor



Calibration DC test pulsing

- A slow buffer gives a reference voltage ~ V_{in} to nodes A to decrease large transients
- Pulse width = 25 ns, 50 ns, 75 ns, 100 ns
- Corresponding Full Scale current = 2 uA, 1 uA, 750 nA, 500 nA



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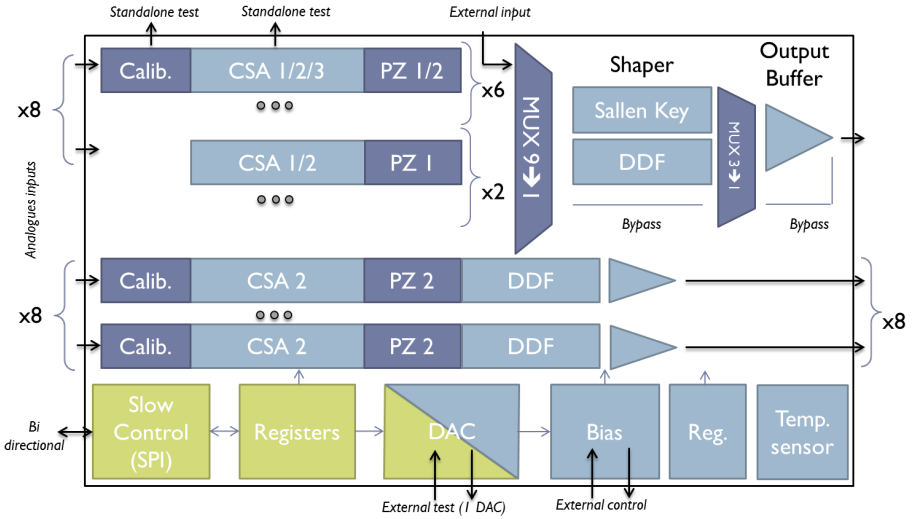
CFE details

- Architecture
  - 16 channels
    - 8 test channels
    - 8 complete channels
  - 8 DACs
    - + DAC in calibration
  - Slow control = SPI
    - More than 110 reg.

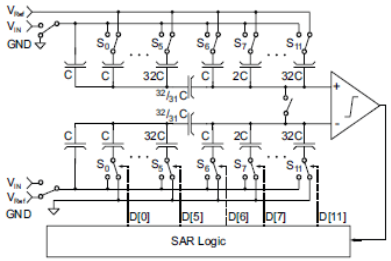


Block	Reference name	type	Typical value	range
BiasCurrent Mirror	IcascPAC	current	30 µA	1 µA → 100 µA
PACBaseBias	IinPAC	current	200 µA	20 µA → 800 µA
RegVddPAC	IbOTAReg	current	200 µA	20 µA → 800 µA
PoleZeroBias	IbnSF	current	100 µA	10 µA → 400 µA
RfeedbackBias	IbLeakCC	current	1 nA	250 pA → 100 nA
AmpOTABias	InbOTA	current	50 µA	1 µA → 500 µA
CSA	VrefOutPAC	voltage	450 mV	100 mV → 1100 mV
Shaper	VrefOutShaper	voltage	750mV	100 mV → 1100 mV

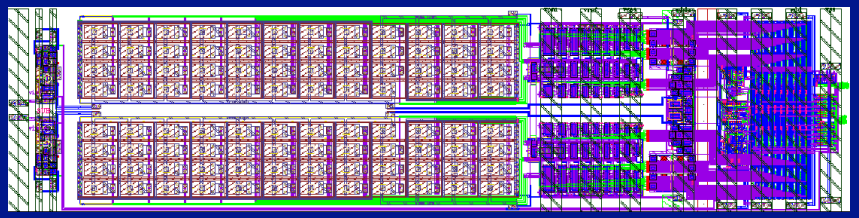
Submission planned for May 2013.

SAR ADC design

Design of 10-bit SAR ADC in IBM 130nm



- Simulated ENOB of the submitted design ~9.4 bits
- We are working on the improved version for the May submission...

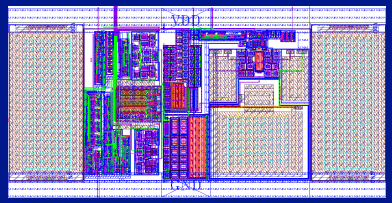


ADC layout 600um x 145um

First prototype in IBM 130nm submitted in February 2012

- Architecture: 10-bit SAR ADC with segmented/splitted DAC
- Fully differential
- Asynchronous SAR logic
- Scalable sampling rate (up to ~50 MS/s)
- Power consumption mostly dynamic, scales with sampling frequency
  - 1-2mW@40MS/s, no static power, also comparator is dynamic
  - Power pulsing for free: No CLK ≈ No power
- ~145um pitch

Synergy with ILC / Marek Idzik, AGH Poland.



PLL layout 310um x 150um

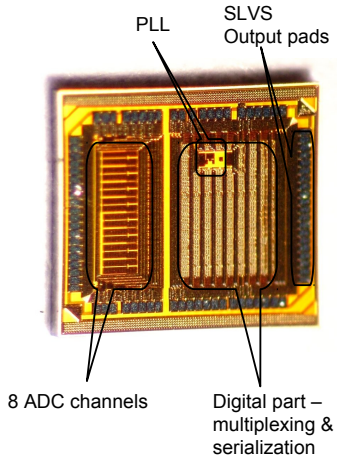
Prototypes under tests... 10-bit ADC, PLL, SLVS

Prototype of 10-bit ADC

- SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch

Prototype of PLL

- Type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO frequency range 8MHz – 3GHz
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- Jitter RMS<5ps

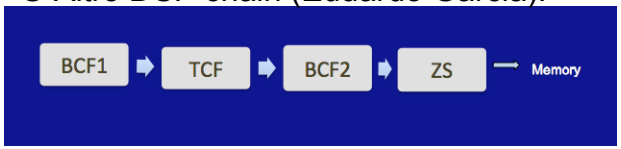


2

DSP

Ideas from ALICE: S-Altro

S-Altro DSP chain (Eduardo Garcia):



Initial idea for GdSP DSP chain (Paul):

- Baseline Correction
- Tail Cancellation Filter = Digital Shaper
- Zero Suppression
- Time Resolution Correction
- Cluster Processing

2nd October 2012 DSP, tiina.naaranoja@cern.ch 3

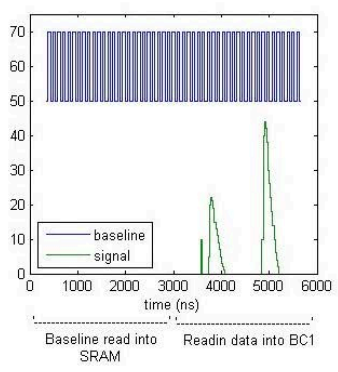
S-ALTRO DSP for GdSP

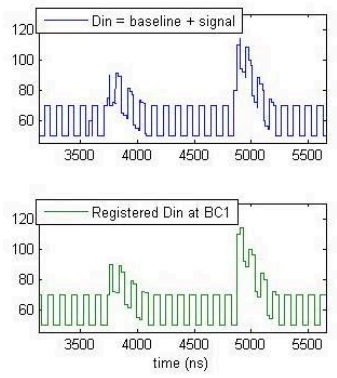
T. Naaranoja

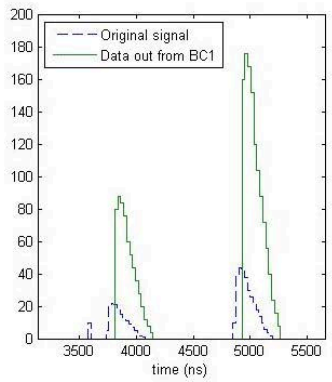
In beginning of the design for digital signal processing (DSP) section of GdSP the DSP in S-Altro is taken as a starting point. The most basic constituents of the digital processor were extracted from the 16 channel demonstrator S-Altro and connected together with an option to bypass individual filters. This construction represents the signal processing for one channel. From the filters in S-Altro digital processor first baseline correction (BC1), digital shaper (DS), second baseline correction (BC2) and zero suppression (ZS) were included. The data formatter, multi-event buffer and SRAMs were excluded since they are anticipated to be sufficiently different in GdSP. A small behavioural SRAM was implemented to be used with BC1.

Table 1: The number of register levels in each DSP block correlates with the delay of the signal in the block. In simplest cases the latency (in clock cycles) equals register levels.

DSP Block	Register levels
BC1	3
DS	1
BC2	3
ZS	11







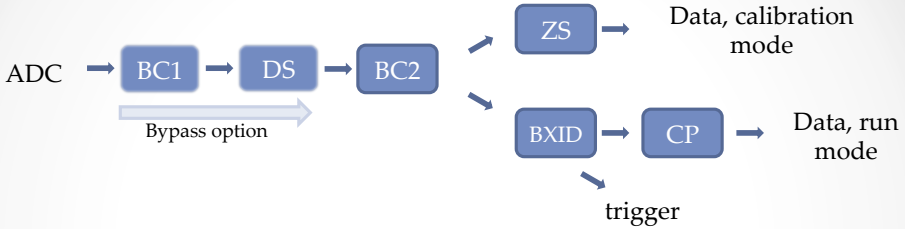
Document summarising S-Altro DSP blocks; operation and programmable options. See Electronics web site.

Tiina Naaranoja

Simulation of systematic noise reduction, BC1

DSP: Possible Techniques To Obtain "Charge" and more importantly "Time"

GdSP digital signal processing



Bunch crossing assignment (BXID)

- Requirements/wish-list:
  - Independent of pulse amplitude
  - Solid performance over 5 shaping times
  - Noise tolerance
  - Pile-up tolerance
- Initially considered methods:
  - Deconvolution method (-> pulse recognition), ToT, Piece-wise linear fitting, Peak finder, Zero-crossing identification, Constant fraction discriminator

BXID: Rounds of simulations

These simulations do not produce final specs!

1st : Verification done

2nd : Performance over shaping times done
- "perfect detector" + random noise (40MHz)

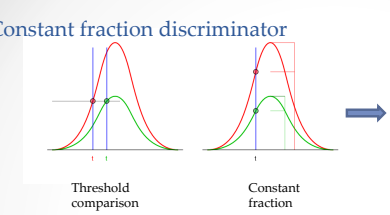
3rd : adding signal enhancement done

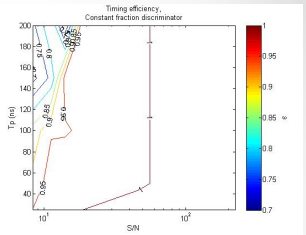
4th : realistic detector + random noise current

5th -7th : pile-up, realistic noise model, from simulink to verilog to do

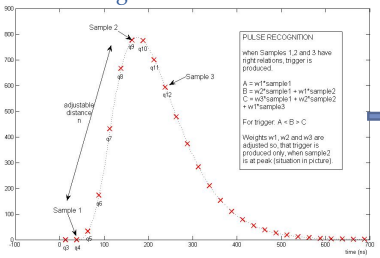
Most promising methods:
Constant fraction discriminator
Pulse recognition (built on deconvolution method)

Constant fraction discriminator

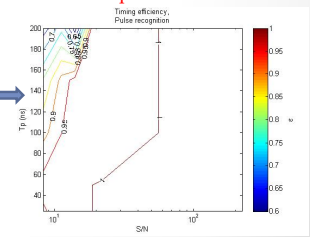




Pulse Recognition



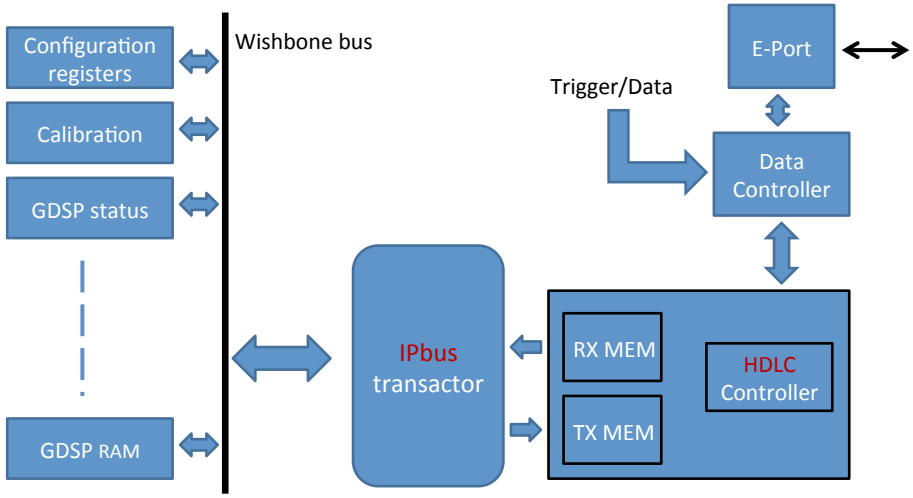
Preliminary, With perfect detector



Tiina Naaranoja

Slow Control Interface

Slow Control Block Diagram



02/10/2012 G. De Robertis - INFN 1

Project Status

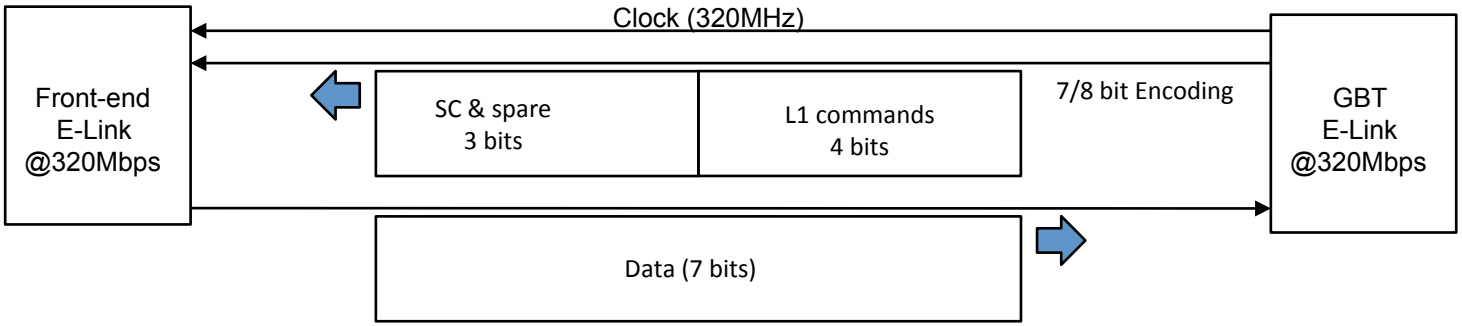
- HDLC Controller
  - RTL verilog code: ready
  - Initial Testbench: ready
- IPbus transactor
  - Implementation is compliant with specification v1.4
  - The RTL code: ready
- We are working on synthesis and PAR for initial area estimation
- Integration with the Data Controller is ongoing
- A new testbench for the whole slow control system is needed for more realistic simulations

02/10/2012 2 G. De Robertis - INFN

Slow Control design,
Giuseppe De Robertis
INFN - Bari

Packet structure for "All hit channels in trigger packet"

RUN MODE

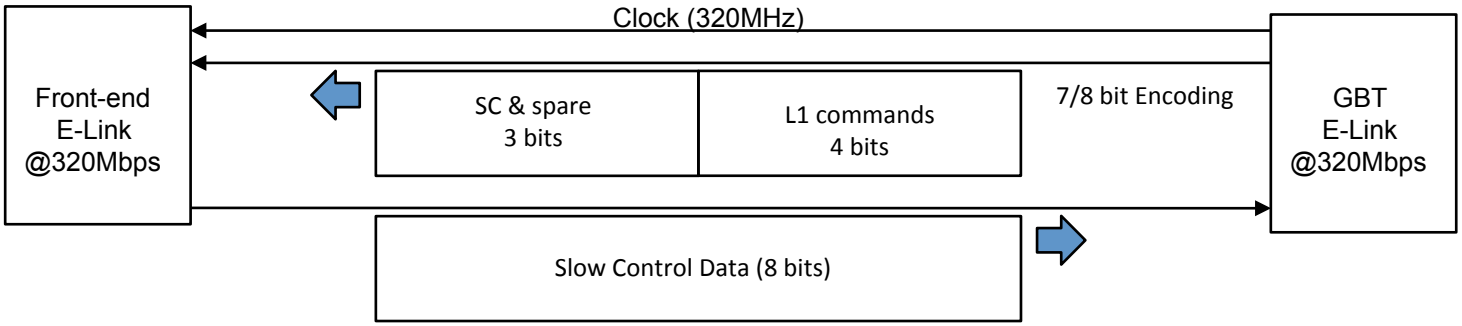


Ideal:
All binary data available for the trigger. Full granularity.

Separation between modes by "control character"
Data to have priority over slow control

L1 Commands :	LV1A, ReSync, BC0, CalPulse @ 40MHz.
Slow Control :	Not during data tacking
Trigger :	Effective bandwidth = 320 Mbps
Tracking :	No tracking data packet

SLOW CONTROL MODE

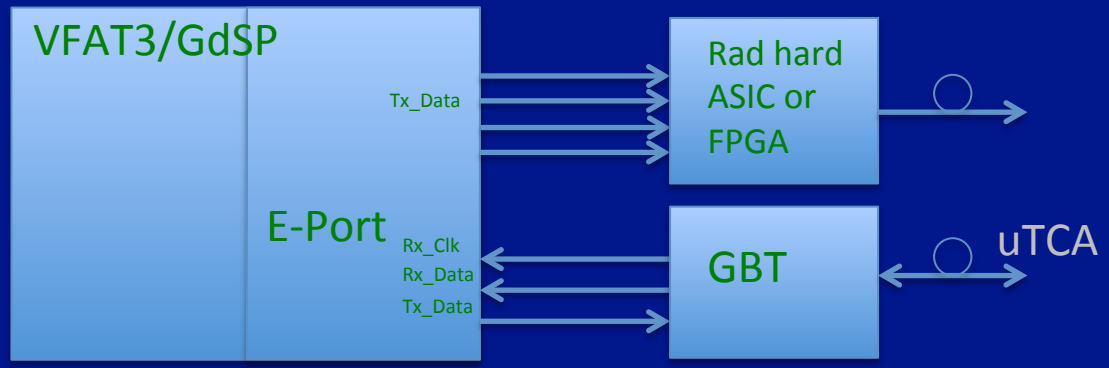


Marko Tapio Kupiainen

E-Links ….

Multiple E-link output ports

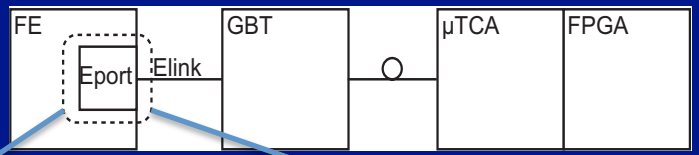
CMS : would carry trigger info

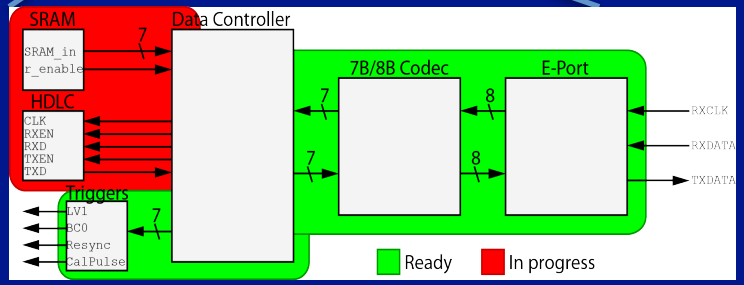


- Data bandwidth is reduced from 320Mbps to 280Mbps in both directions by 7-8 bit encoding.

- Encoding of E-links necessary for :
  - GBT to Front-end …… Allowing “control characters” necessary for synchronisation.
  - Front-end to GBT …… “Control characters” enable alignment of data at the receiver plus identification of SC data and tracking data.

Programmable “max” time interval between Sync “Control Characters”





Verilog design:
Marko Tapio Kupiainen

CMS Project Electronics Timescale & Planning

FE ASIC

Define electronics system for TP, Formation of design teams.

ASIC design starts

2012

FE ASIC design team Approx. 10 man years of design needed.

1st ADC test chip

We are here.

CFE test chip

Choice : VFAT3 OR GDSP ?

2014

Submission of FE ASIC (VFAT3/GdSP)

Possible 2nd Sub. of FE ASIC (VFAT3/GdSP) ?

Readout systems

2011 Starting point :
VFAT2 , Turbo hardware and Labview DAQ software
GEM charaterisation & Test beams

Opto Hybrid & uTCA development

2 super-chamber preliminary prototype (if possible LS1)

2015 Construct & debug VFAT3/GdSP + GBT + uTCA system

2016 Demonstrator prototype of final system

Hybrid & board production

LS2 Installation of GE1/1

The Status and Future of the GDSP Chip

- What is the GDSP ?
- What is the GDSP history ?
- What is the design status ?
- What is remaining ?
- How could the GDSP be adapted to a TPC ?
- What is the future of the GDSP ?
- Summary

Architectural choices

CMS decision for VFAT3 OR GDSP ?

Factors include :

- Time resolution
- ADC design & readiness
- Peak charge calculation ? For centre of mass > spatial resolution
  - Charge processing > say for zig-zag strips
  - Charge readout
- System power requirements
- Baseline subtraction
- Possibility to share development cost and manpower

CMS chip (VFAT3 OR GDSP)

Design for specific memory size

& pay load type

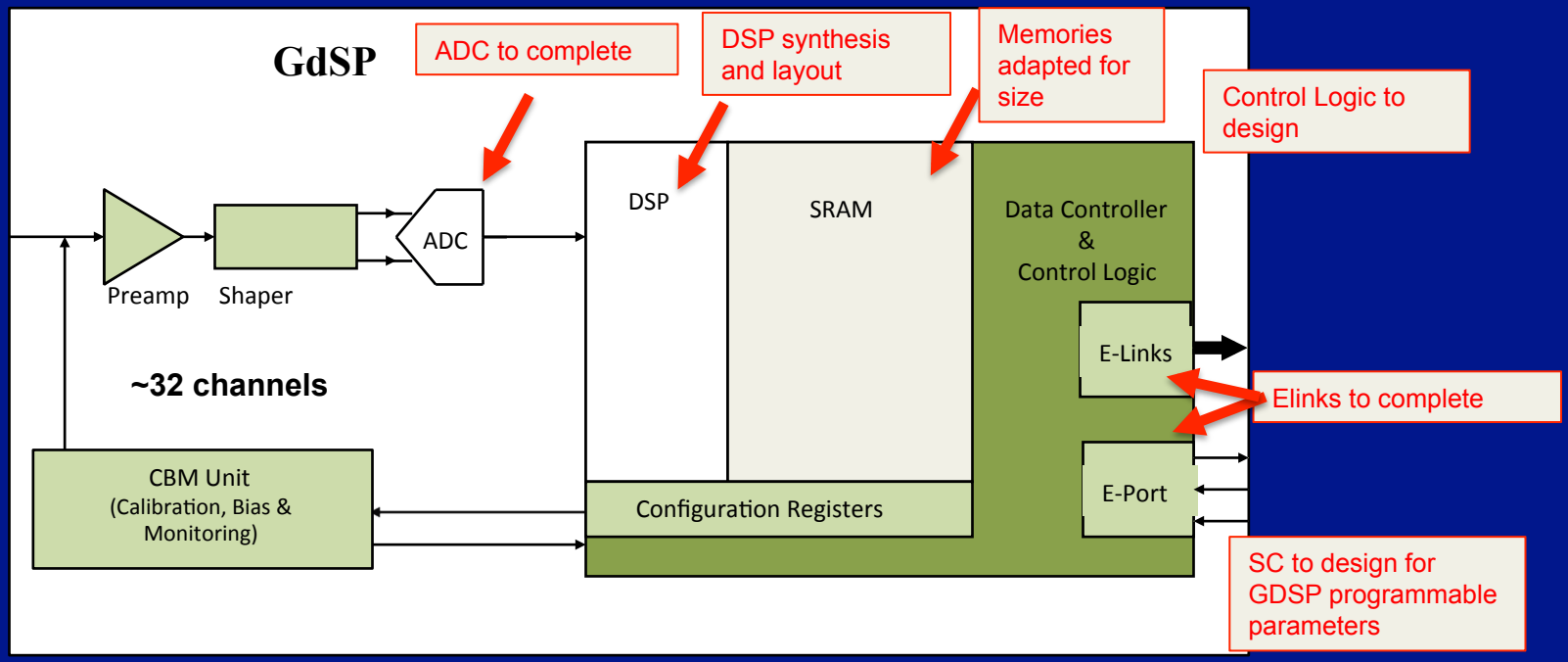
TPC chip (GDSP) ???

TPC likely to need dedicated GDSP version

Design for specific memory size

& pay load type

Remaining work



Final architectural description (GDSP_TPC) [ie. No. of channels, output data type and format]
Completion of individual modules shown
Writing of Verilog and verilogA models for the modules
Definition and design of Slow Control registers (much in common with VFAT3)
Control logic design, synthesis and P&R
Full assembly of the chip
Simulation, verification
Submission
Characterisation

The Status and Future of the GDSP Chip

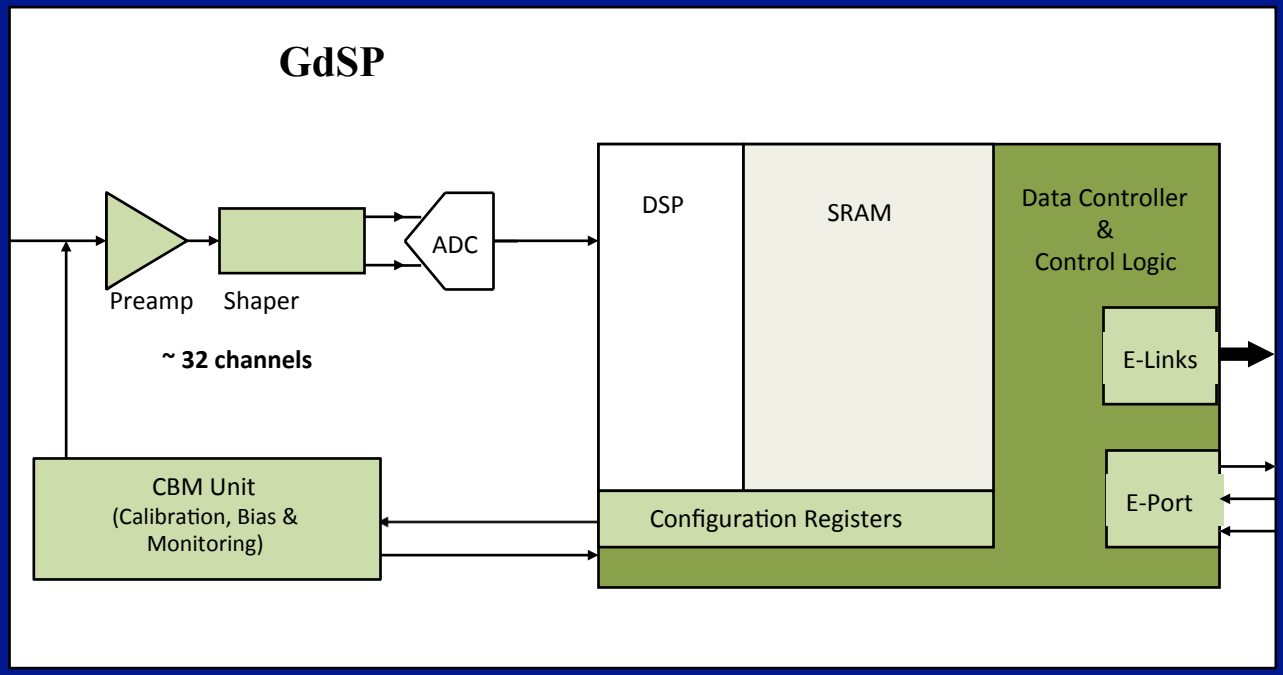
- What is the GDSP ?
- What is the GDSP history ?
- What is the design status ?
- What is remaining ?
- How could the GDSP be adapted to a TPC ?
- What is the future of the GDSP ?
- Summary

How could the GDSP be designed for a TPC ?

- In order for a dedicated TPC version of the GDSP to be designed, the GDSP would need to become an official part of an experimental program together with resources (funding and design manpower)!!

- Front-end and CBM unit identical to VFAT3
- Reduced number of channels , perhaps 32 instead of 128
- SRAM memory structure similar to VFAT ie. SRAM1 operating as a circular buffer and SRAM2 storing selected portions of data from SRAM1 on receipt of a trigger.
- SRAM 1 & 2 enlarged to store 10 bits of ADC data per sample instead of 1 bit as in VFAT.
- Multiple E-link outputs operating at 320 or 640 Mbps.
- Memory depth and pay-load format is application dependent.
- Could be programmable “burst” or “continuous” mode of operation.
- Power management (pulsing) possibilities for ILC TPC application.

Rough power estimate ?



Preamp/shaper < 1mW / channel
ADC < 4mW / channel
Digital power; some hundreds of mW

Power consumption in the region of 0.4 - 0.5W continuous operation

The Status and Future of the GDSP Chip

- What is the GDSP ?
- What is the GDSP history ?
- What is the design status ?
- What is remaining ?
- How could the GDSP be adapted to a TPC ?
- What is the future of the GDSP ?
- Summary

What Is The Future ?

- Under the umbrella of the CMS GEM project many of the modules of the GDSP have been designed or their design is well advanced.

- For TPC application a dedicated GDSP_TPC chip would be needed with it's own memory and readout requirements.

- For this to happen the GDSP would need to become part of an official experimental program with it's own source of funding and manpower resources.

The Status and Future of the GDSP Chip

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Summary

- The GDSP exists at the moment through the CMS GEM upgrade and synergy with collaborators.
- It is not an independent project although collaborating institutes have interest in other projects including the upcoming TPCs.
- TPC application would probably require dedicated GDSP_TPC chip.
- Many of the internal modules are the same as have been developed so far.
- The main differences are the ADC, memory size and data load specification.
- In order for the project to continue to a GDSP_TPC chip then it will need to become an official part of an experiment with financial and manpower resources.