The super ALTRO, S-ALTRO16

CHIP crew:
Luciano Musa … S-Altro Specifications and Architecture
Paul Aspell… Coordinator of Demonstrator ASIC Design
Hugo França-Santos … ADC (PhD Thesis, Lisboa)
Eduardo Garcia… Digital Signal Processing & Control (PhD Thesis, Valencia)
Massimiliano De Gaspari … Front-end, Integration, Tests (PhD Thesis, Heidelberg)

LCTPC:
Main groups working on a readout system based on S-ALTRO16
Brussels, CERN, Lund, KEK, Saga

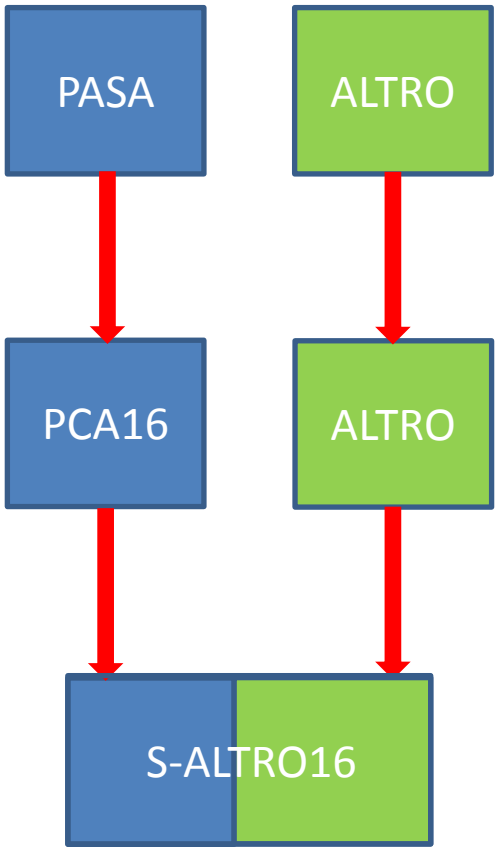
Financing from EUDET – AIDA brings it all together

Development history

ALICE:
+ polarity
12mV/fC
190ns

EUDET:
+/- polarity
12,16,20,27mV/fC
30,60,90,120ns

AIDA:
+/- polarity
12,16,20,27mV/fC
30,60,90,120ns



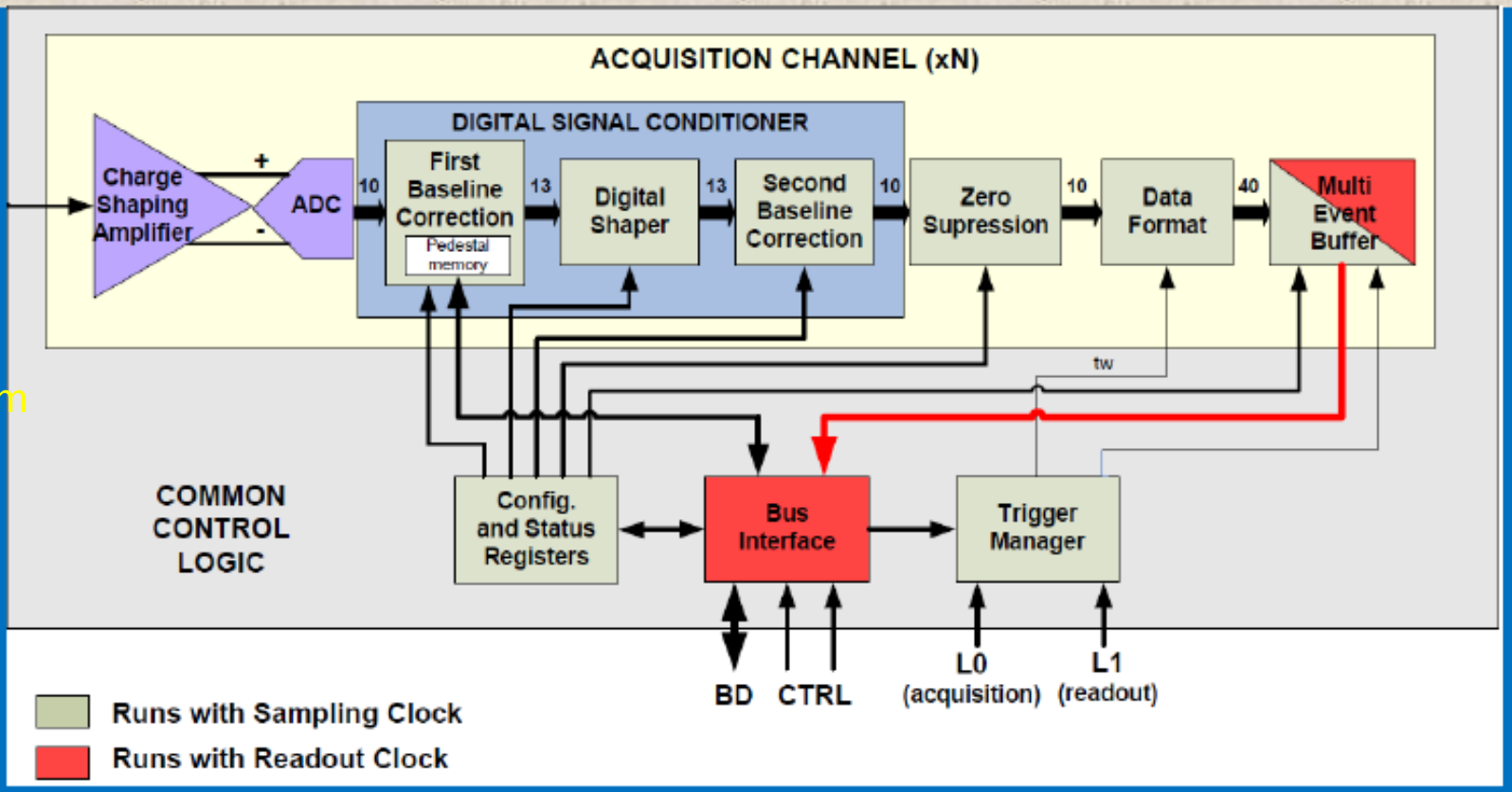
ALTRObus
40 bit wide parallel bus
@40MHz

Many tests on real chamber

Only tested on the bench

System architecture

0.13µm
CMOS
IBM



Level 1: Starts the data acquisition.
Level 2: Validates data from previous L1.
BD : 40 bit bidirectional bus; 20 bits address + 20 bit data.
CTRL : 6 bits.
Sampling clock : max 40MHz. Readout clock : max 80MHz.

Driving forces for LCTPC

High PT physics

Extreme momentum resolution

- Long tracks Large TPC
- High B-field (4-6T)
- low diffusion – narrow pads
- 300-400 coordinates

Don't care so much about dE/dx

Nearby track resolution important

End up with ~5Mchannels

Is it high rate,? No. but want to run untriggered (ungated)

- ion backflow matters for mom. resolution

Readout:

Linear colliders have poor duty factor (ILC, 5 spills of 1ms per second)

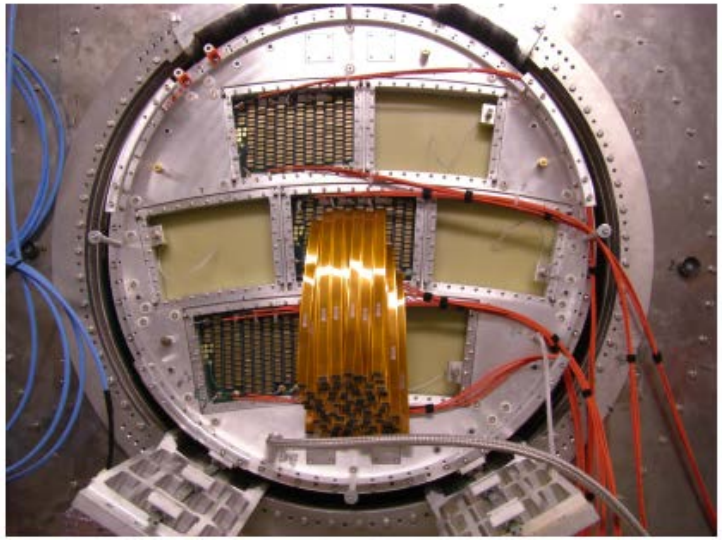
- contiuous untriggered readout but
- storage of full spill (10 times event memory depth)
- readout between spills.
- Power pulsing analog part

The EUDET system:

General purpose readout electronics for ”proof of principle” tests.
Test different TPC-readout concepts.

GEM, Micromegas.....

10000 channels procuced PCA16 + ALTRO



End plate of large prototype TPC

35cm long Kapton cables
1*5.2mm^2 pads

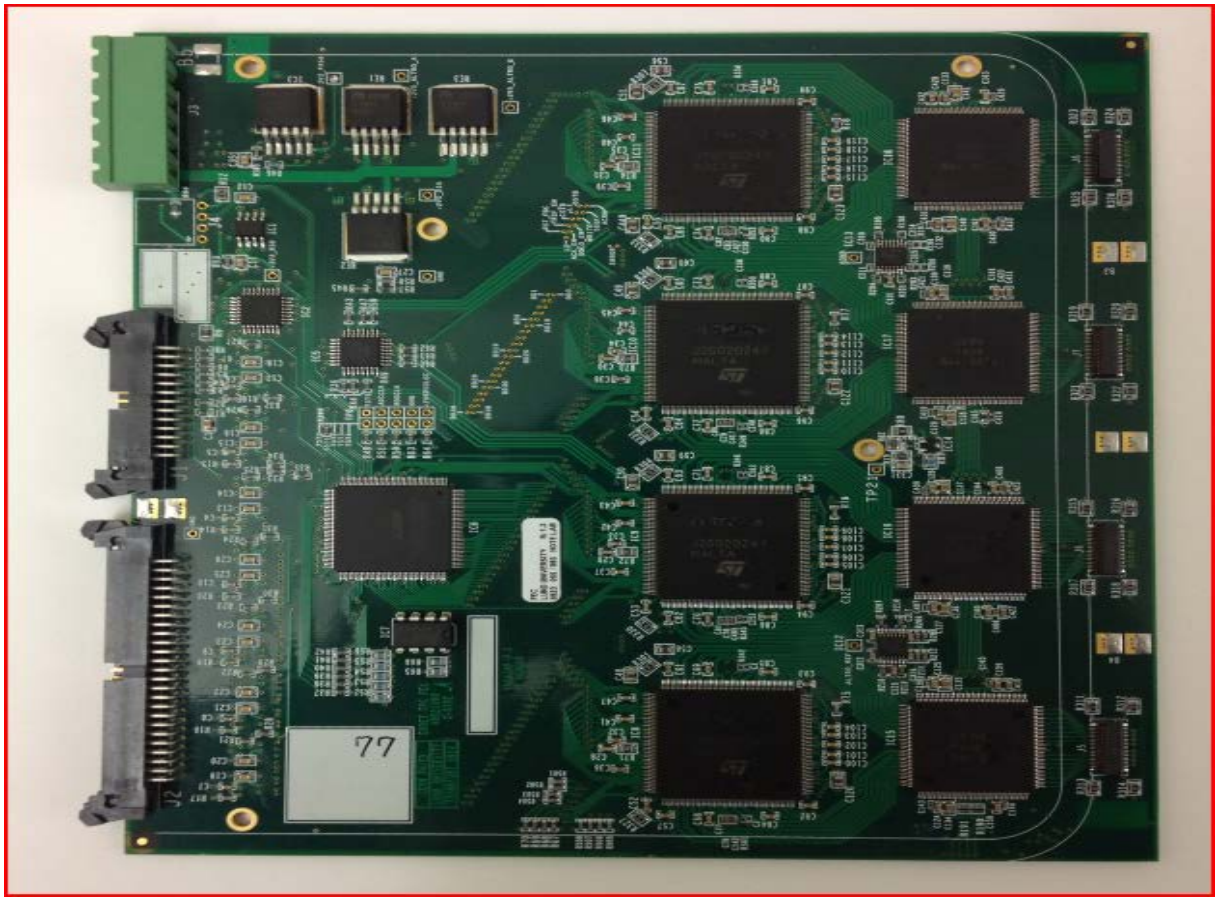
PCMAG+LCTPC prototype

T2k gas

Ar 95%
CF4 3%
Isobutan 2%
Drift 7.5cm/µs

- Constructed by the LCTPC collaboration
- Superconducting solenoid magnet
- B = 1 Tesla
- Drift field 230V/cm
- 5 GeV electron beam at DESY

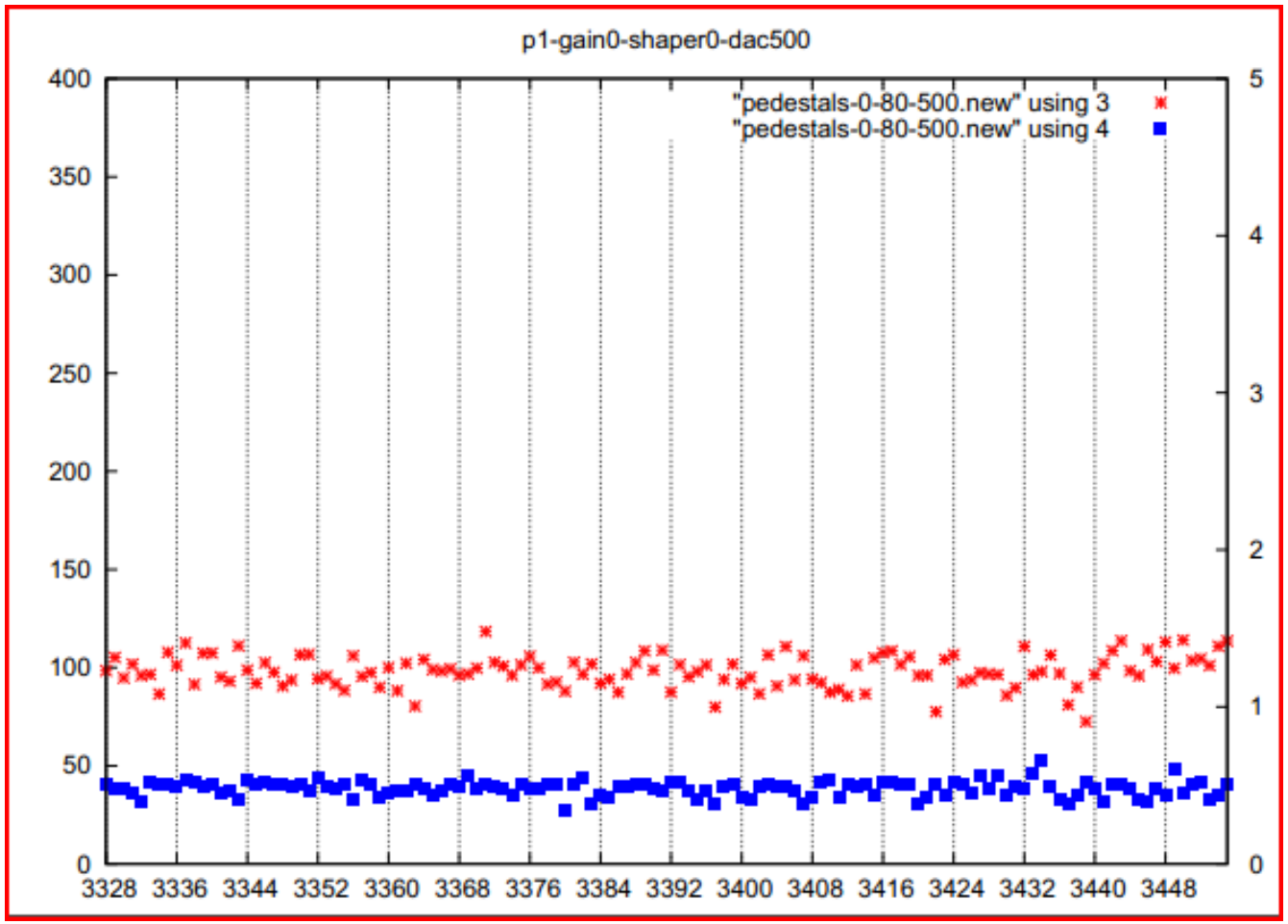
128 ch FEC, PCA16 + ALTRO



20MHz sampling rate

EUDET front end electronics, 128ch FEC

Noise PCA16 + ALTRO FEC



Pedestal ADC channels

120ns
12mV/fC

RMS ADC channels

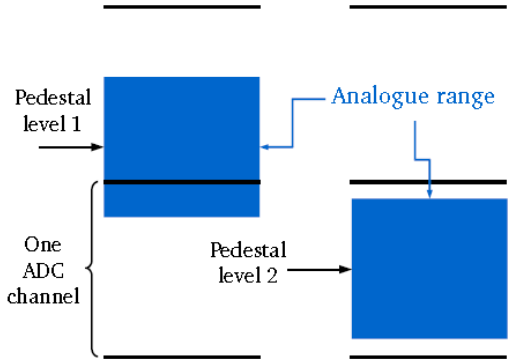
Channel number

Mean 0.485

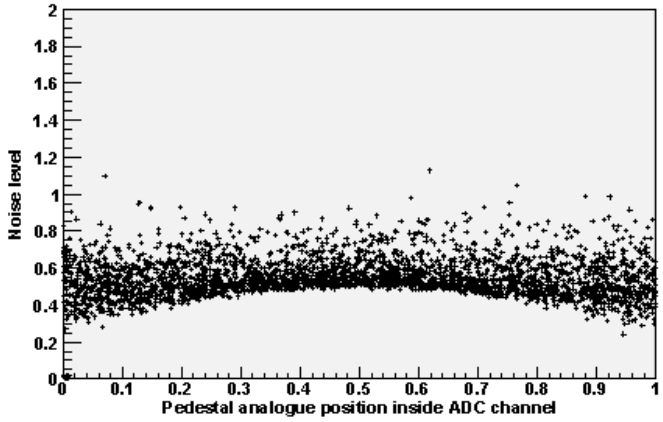
ADC resolution limits the sensitivity

1/sqrt(12) effect on RMS
of rectangular distribution

RMS_{ADC} = 0.29 ch
RMS_{analog}=sqrt($0.49^2 - 0.29^2$)=0.39 ch

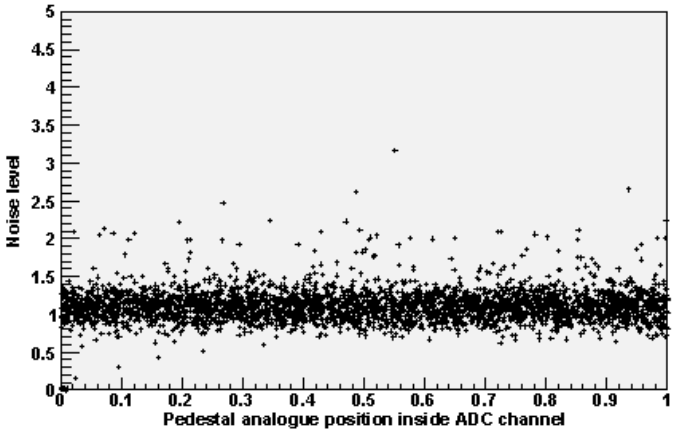


RMS



(a) Low gain

12mV/fC

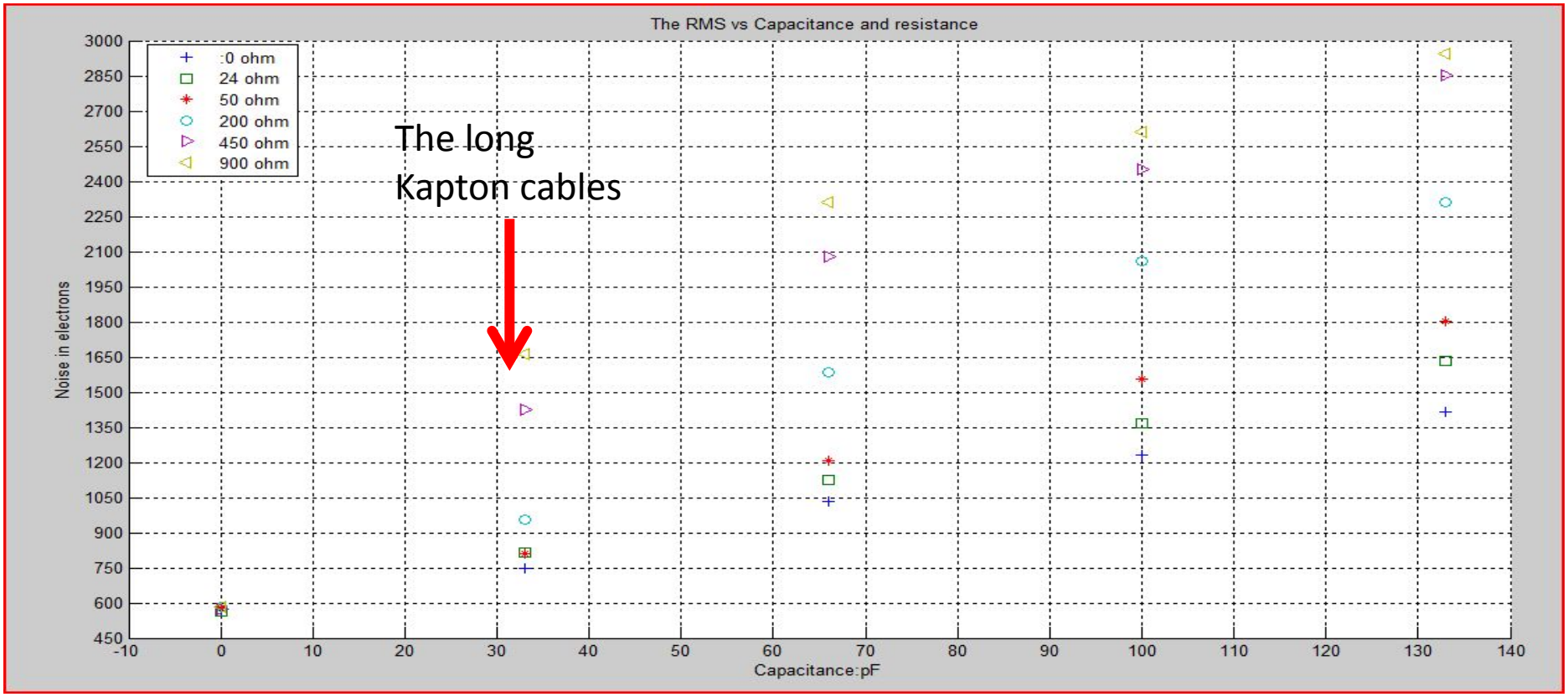


27Mv/fC

ENC Noise PCA16 + ALTRO FEC

Series resitors

12mV/fC, 120 ns risetime



Additional input capacitance

Resolution in bend plane

residuals

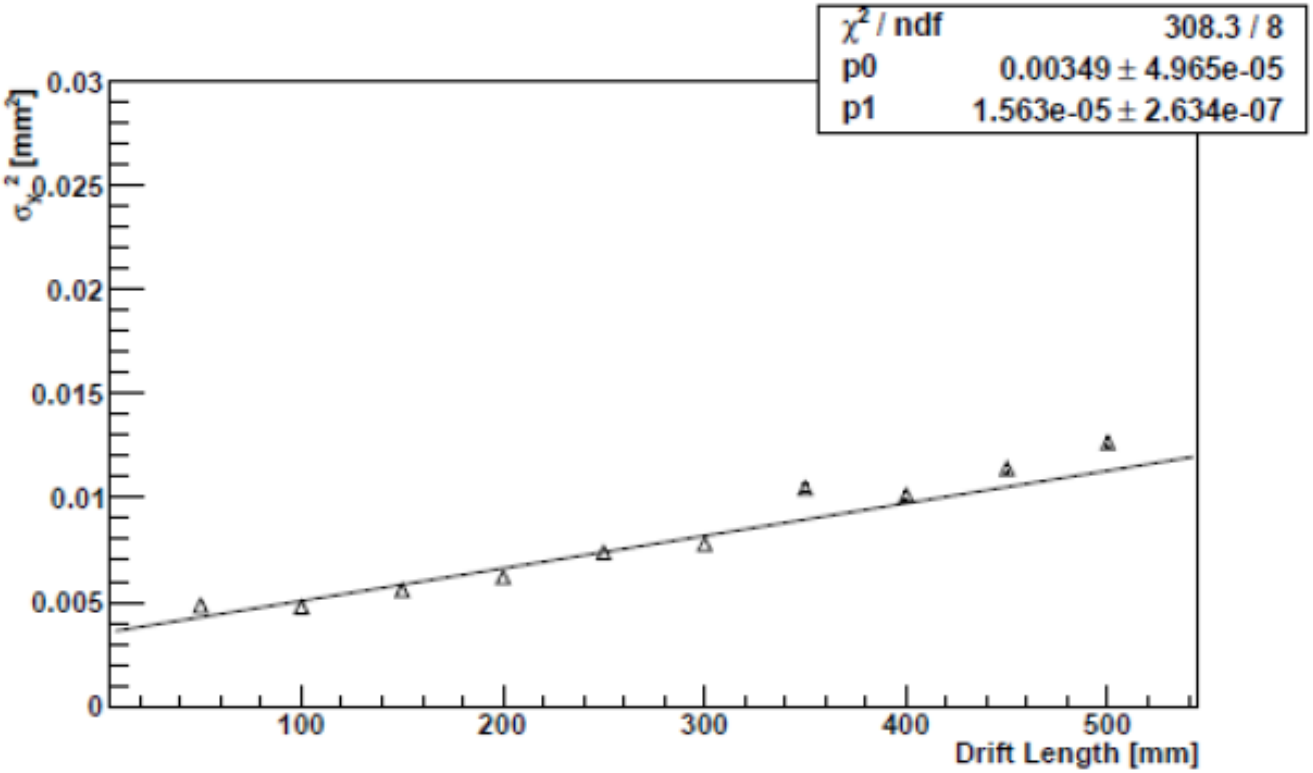
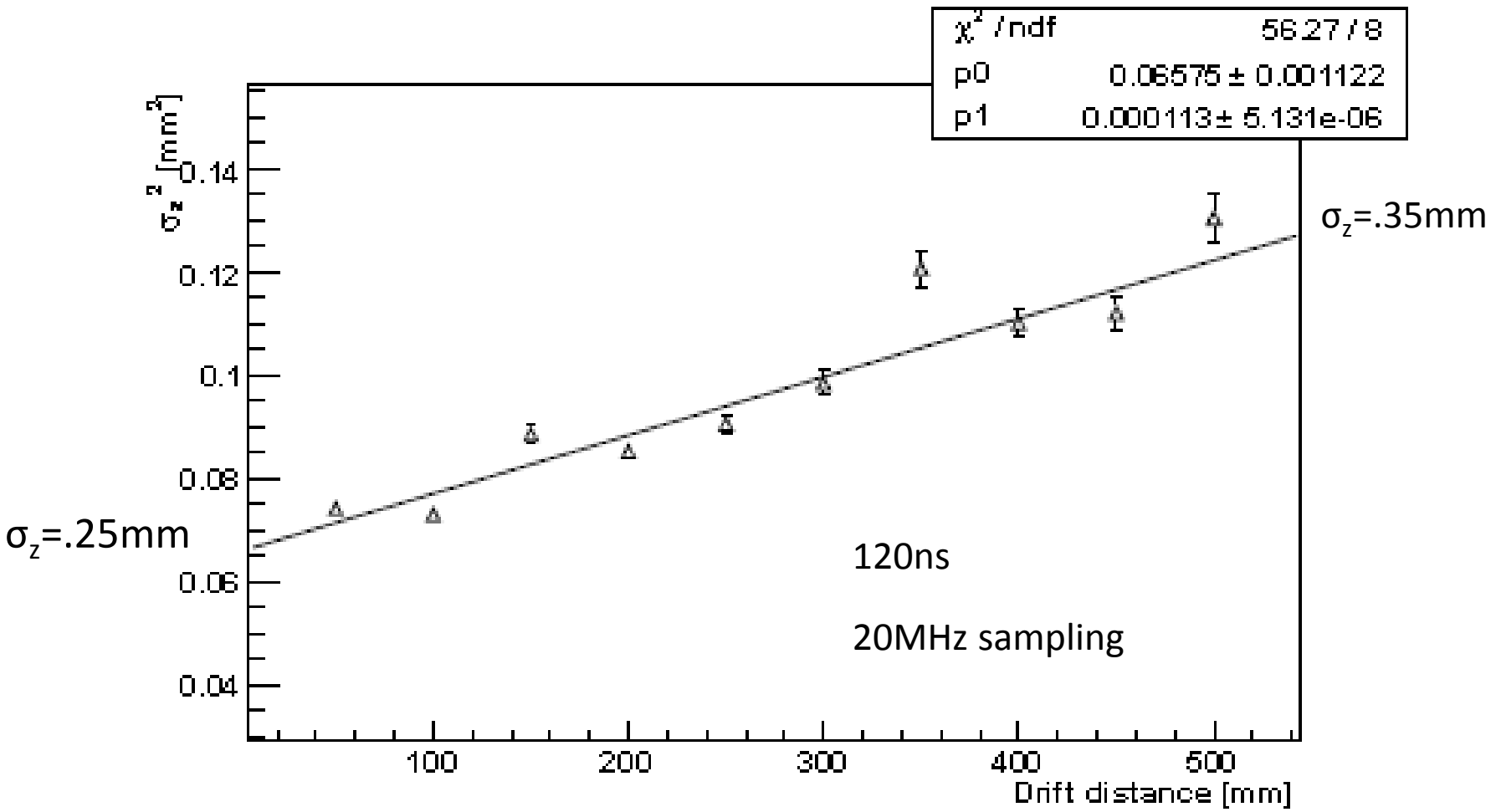


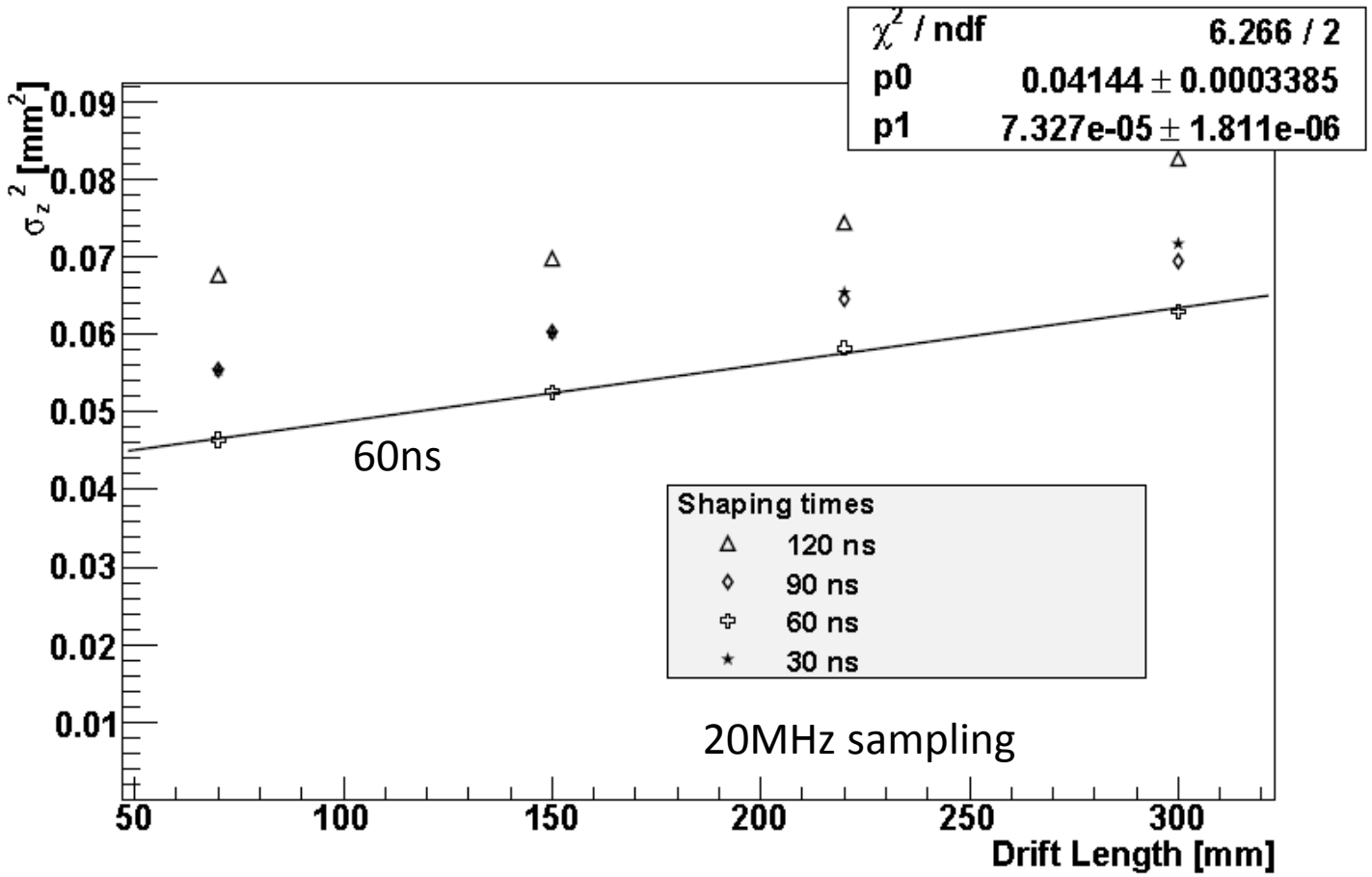
Figure: Measured resolution for different drift lengths. The line crosses the y-axis at 0.00349 mm^2 which corresponds to an intrinsic resolution of $\sigma_y(0) = 59.1 \pm 0.4\mu$m.

Slightly better now after field distortions fixed

Residuals in drift direction

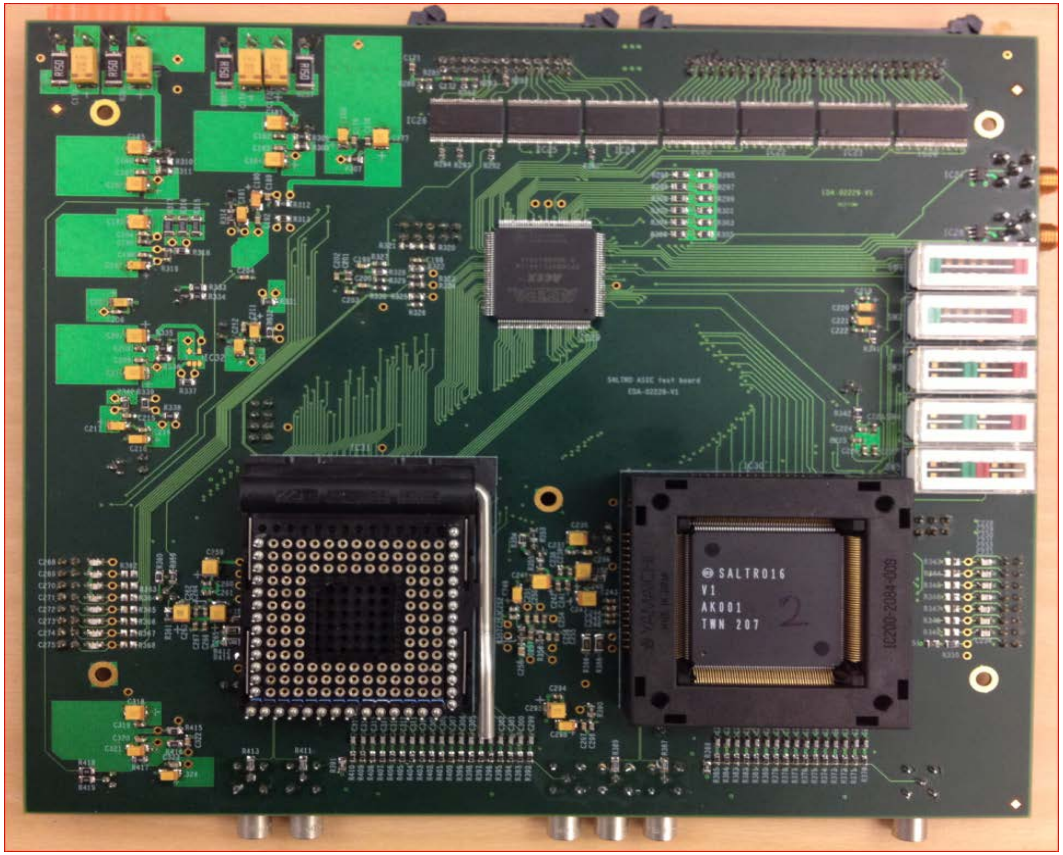


Residuals in drift direction



S-ALTRO test board

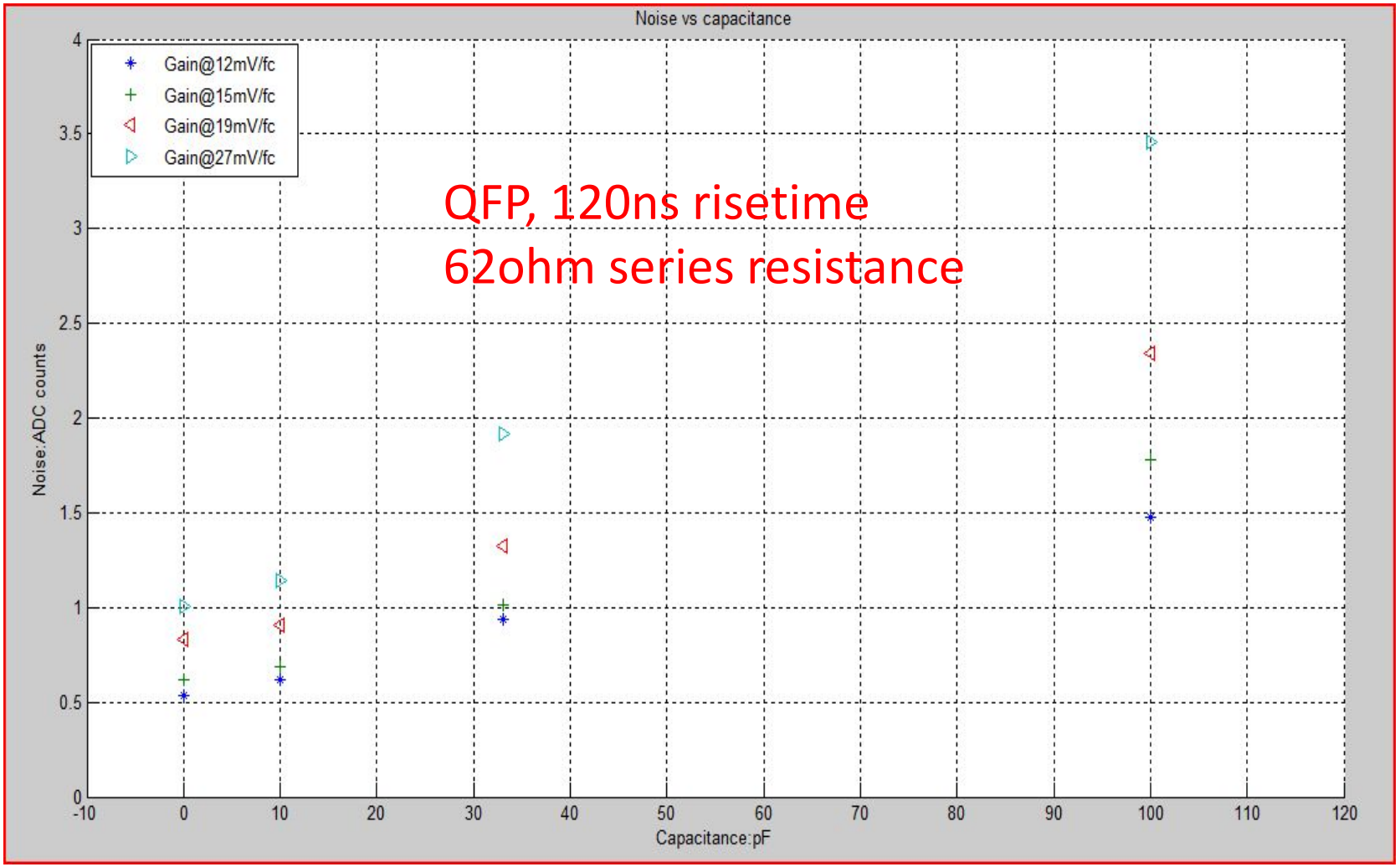
Reads through ALTRObus backplane



PGA versions tested by Massimiliano
Ideal version inputs not bonded
Bonded inputs more noise. PGA bad

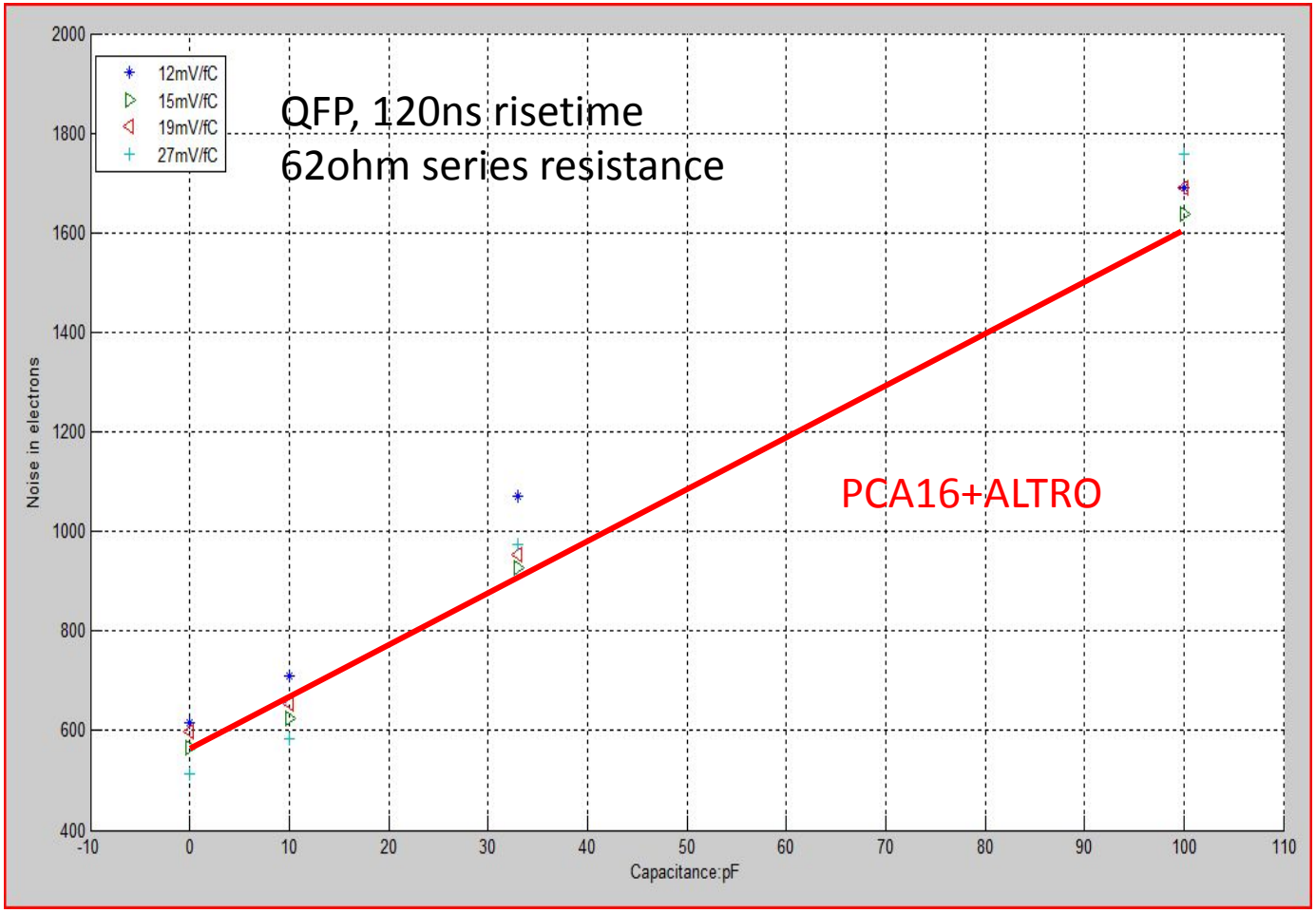
QFP version, Liangliang Shi
master thesis Lund

SALTRO16 noise in ADC channels



Additional capacitance

SALTRO16 noise in electrons



Additional capacitance

Noise summary

	Config	120ns L 12	120ns L 27	30ns L 12	30ns L 27	120ns H 12	30ns H 12
PGA3 Inp nc	Noise LSB	0.480	0.655	0.526	0.683	0.498	0.504
	Noise fC	0.088	0.051	0.103	0.059	0.092	0.100
	Noise e-	547	316	641	370	574	625
PGA4	Noise LSB	0.709	1.346	1.475	3.263	0.668	1.279
	Noise fC	0.129	0.104	0.287	0.283	0.123	0.254
	Noise e-	809	649	1796	1768	770	1587

Measured noise averaged over 16 channels

S-ALTRO16 prototype in LCTPC

Demonstrator that proves that this can be built when ILC or CLIC gets go ahead.

Shall adress all difficulties

large enough to be realistic

dense enough to be realisitc, electronics fit behind pad.

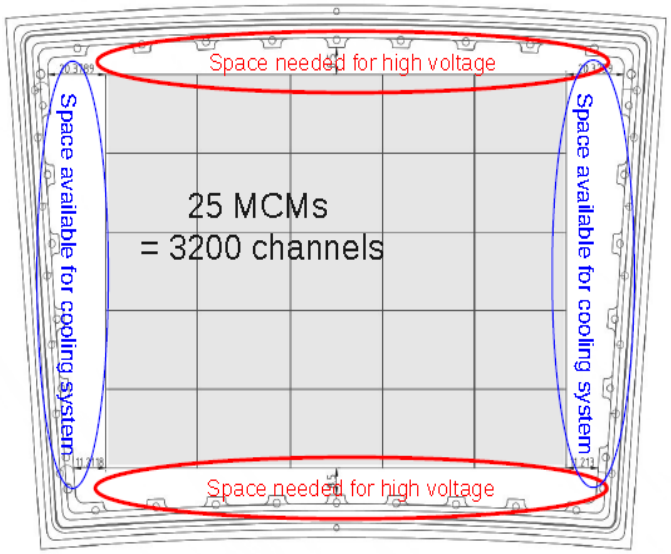
solve cooling, CO2

power pulsing at very low duty factor (ILC 1ms beam on at 5Hz)

May add to ”proof of principle” with very low input capacitance (minimal noise)

A full scale prototype requires final chips and serious money

25 Multichip modules (MCM) on a panel

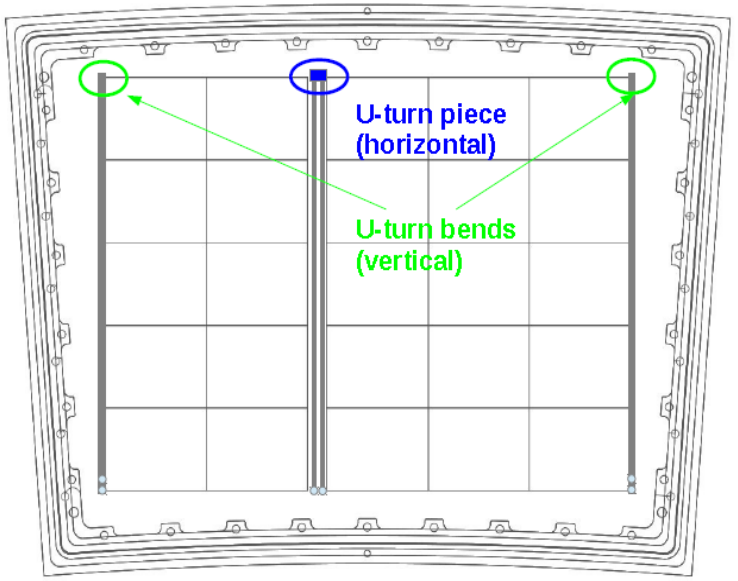


Per Panel
25*8 S-ALTRO16
3200 channels.

One MCM, 128 channels, 23*33 mm^2

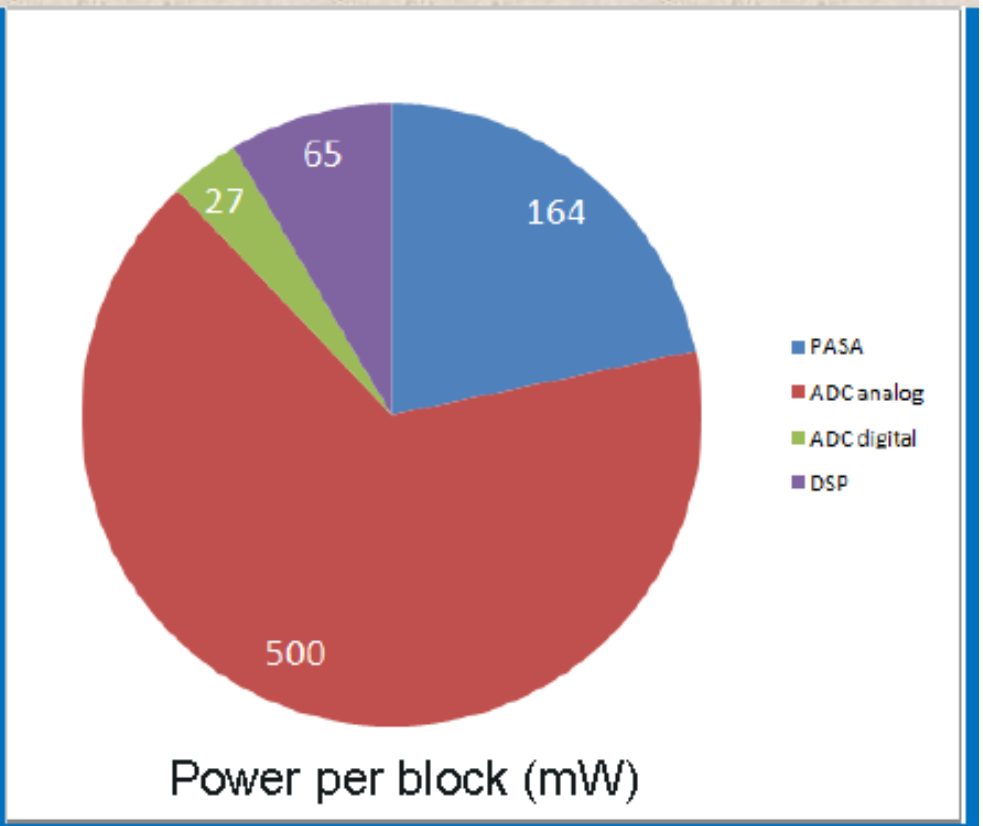
Pad size ca 1*8mm^2

Chips available for 2.5 panels



Power consumption

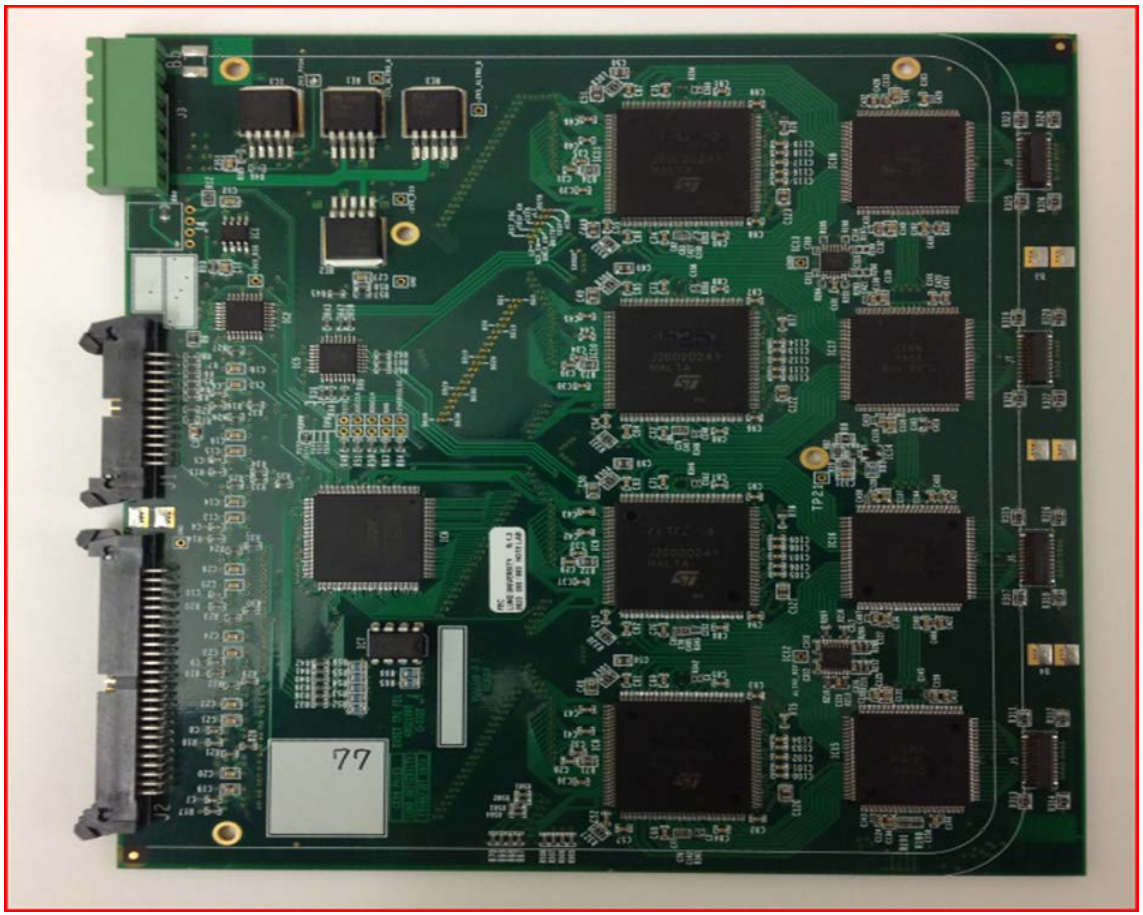
	40MHz operation	Smart shutdown
PASA	10.26mW/ch	235uW/ch
ADC analog	31.28mW/ch	394uW/ch
ADC digital	1.71mW/ch	≈0
DSP	4.04mW/ch	10.8uW/ch

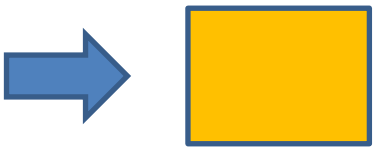


Smart shutdown: shutdown control lines for PASA and ADC, clock removal for the DSP.

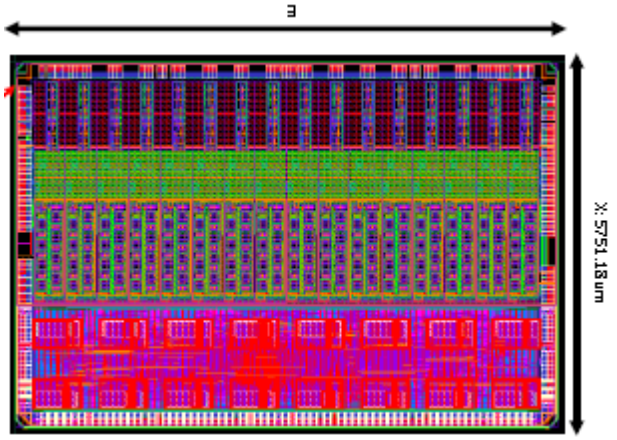
Total power consumption: 757mW.

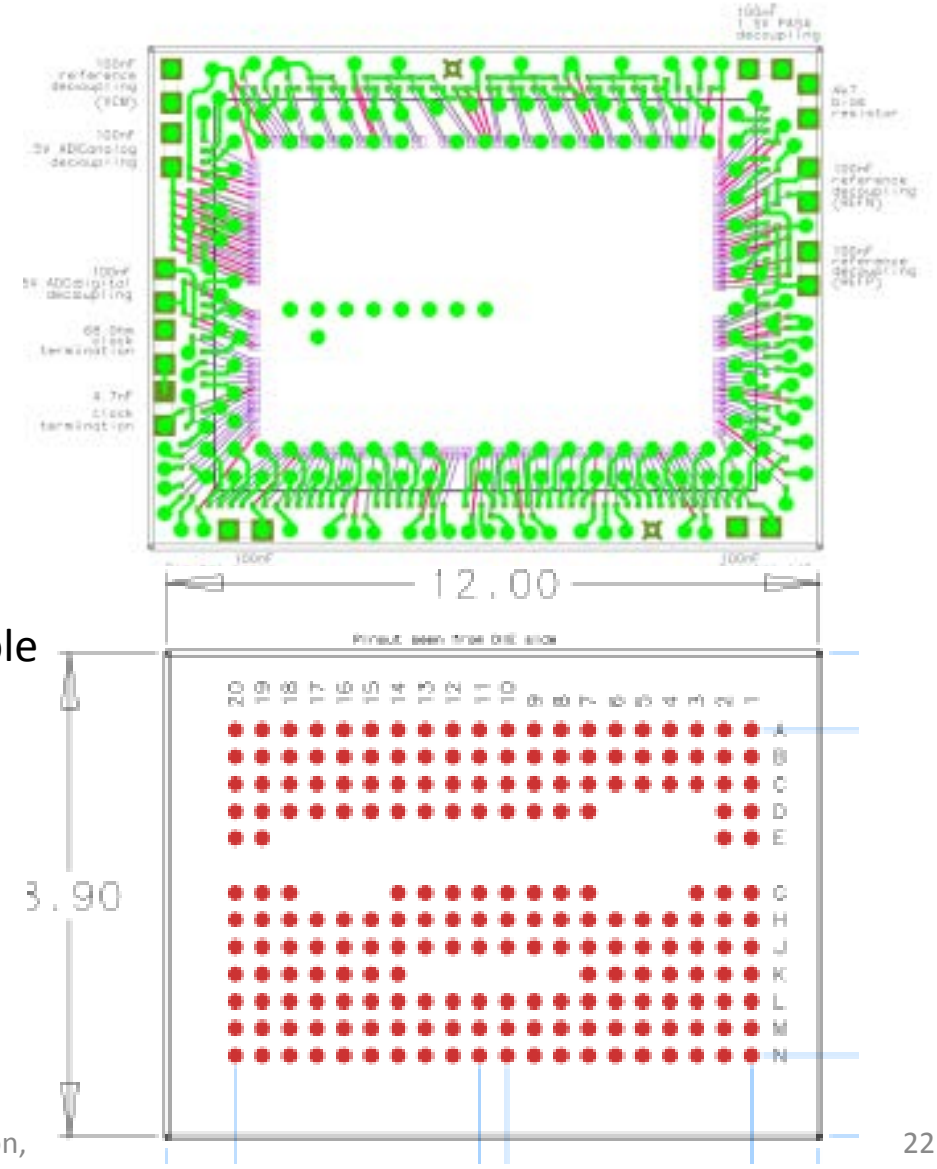
Massive Miniaturisation needed





Wirebond naked die to carrier board



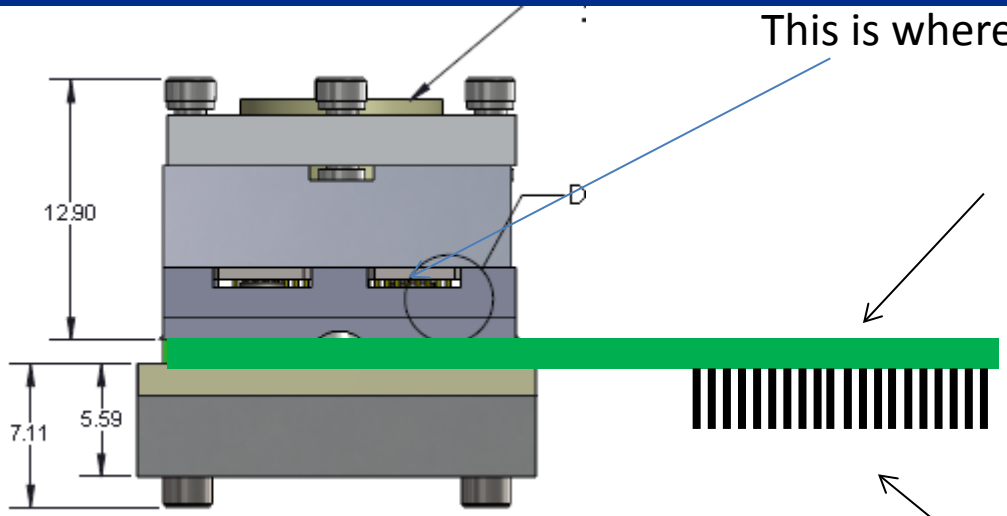


Die not prepared for bump bonding

- Unstested chips, only 600 available
- Minimize losses

BGA footprint on below side
0.5mm grid
8 layer board

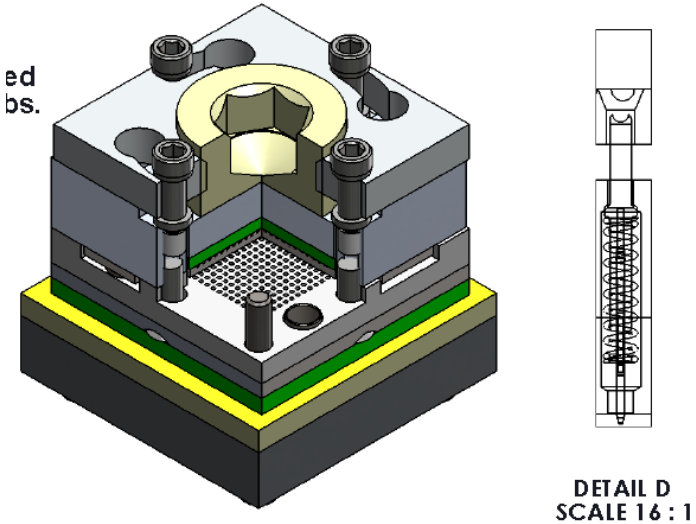
Test carrier board in BGA socket



This is where the carrier card is

Our receiver board has BGA-GRID corresponding to chip carrier. The springloaded probe-pins press on both carriercard and receiver board

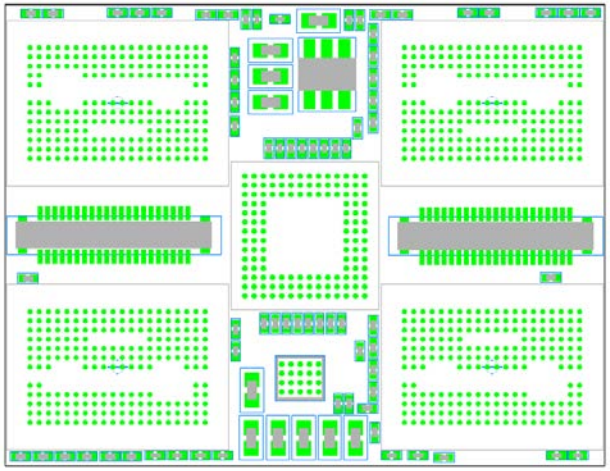
Pins fitting PGA socket on testcard



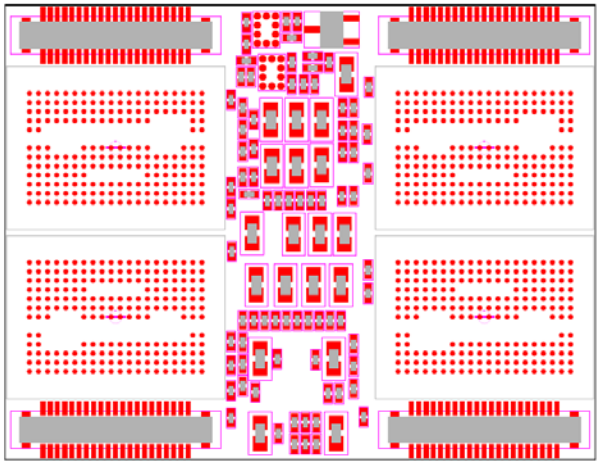
Spring loaded micro pins in 0.5mm pitch BGA grid array

Assemble MCM with 8 Carrier boards

Top side



Below side



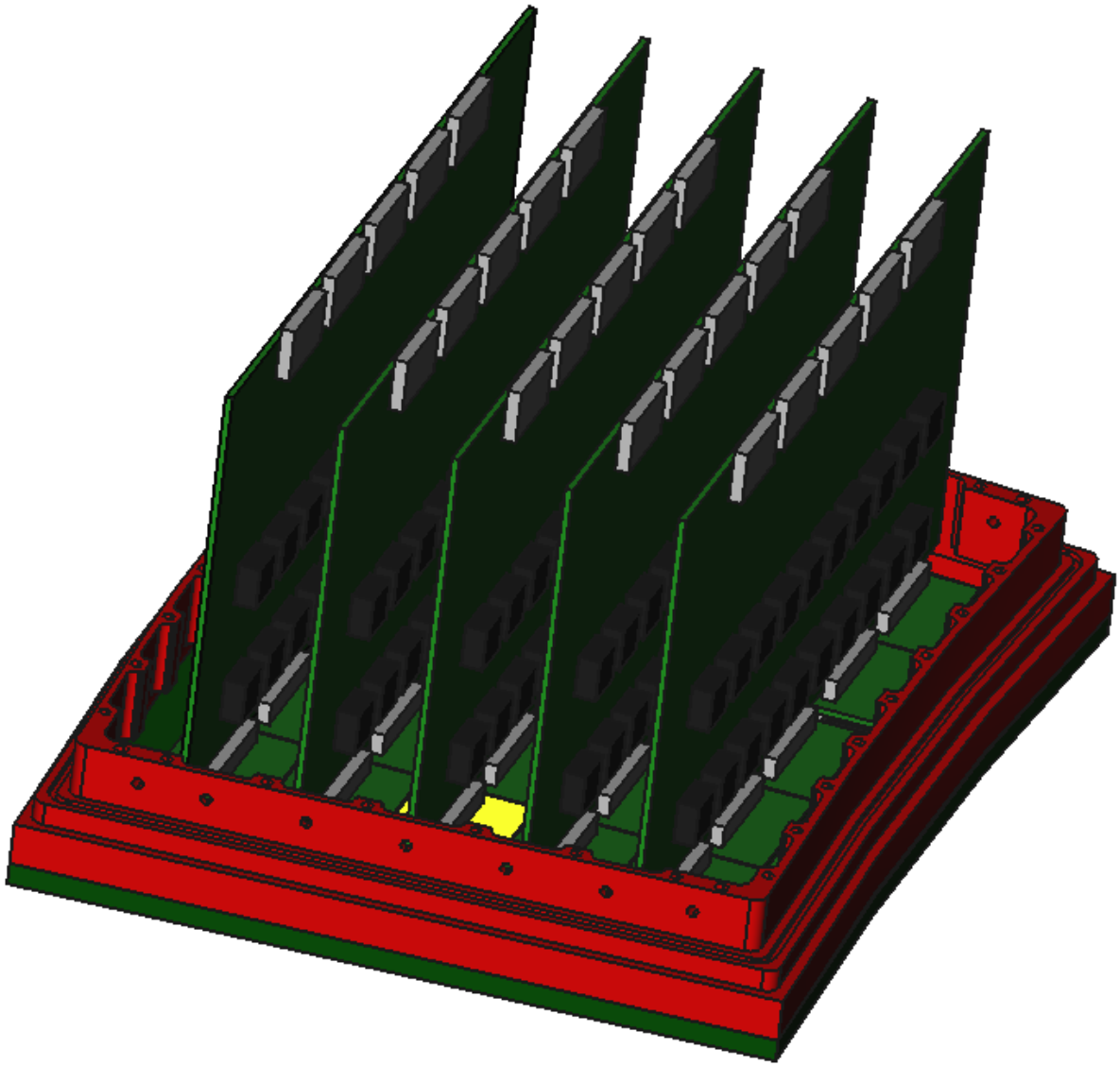
Can not use ALTRObus for readout. Do parallel-serial-parallel by CPLD on MCM

No place for voltage regulators. Place on vertical board where Serial connection to SRU connects.

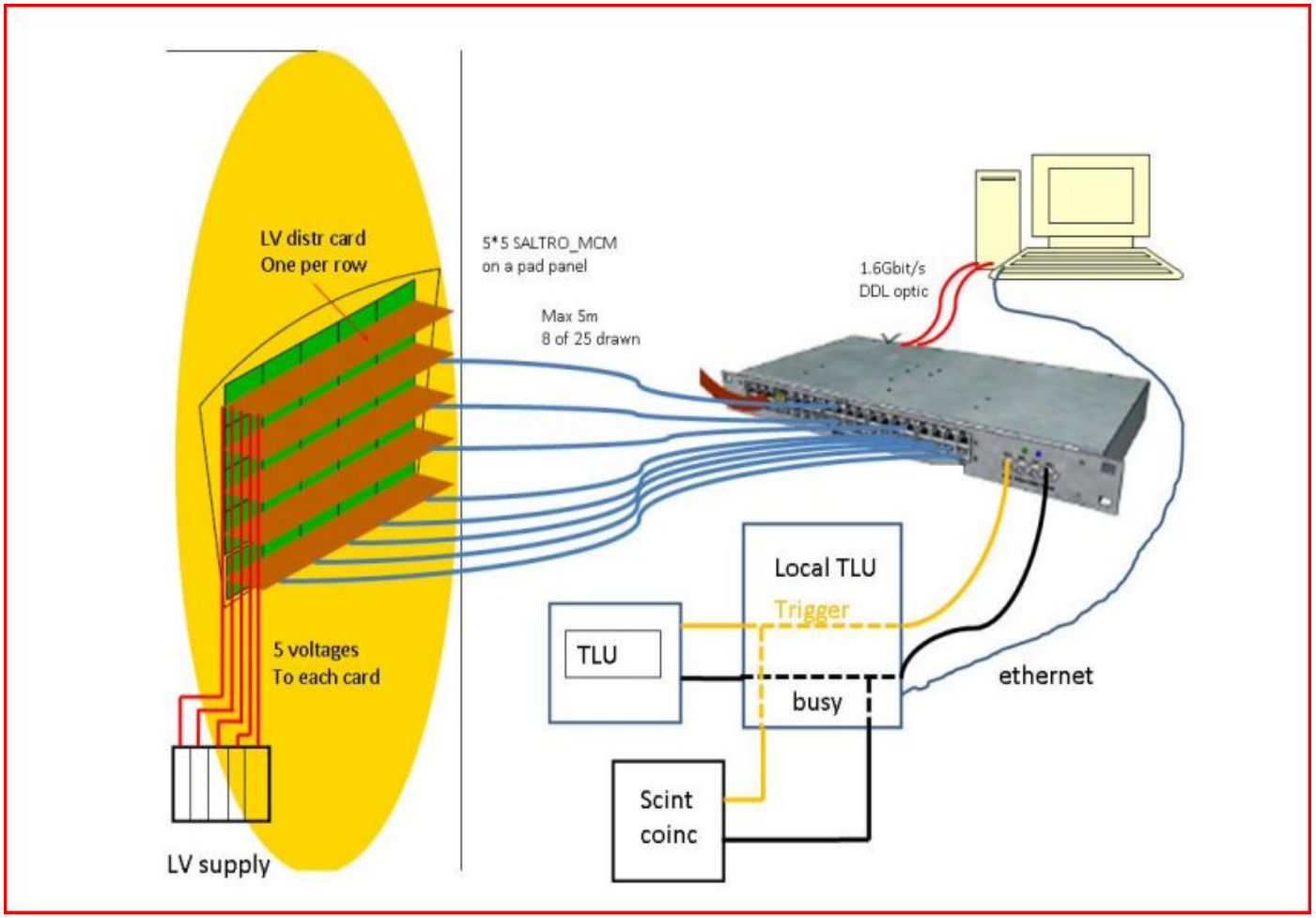
How small it has to be

4 MCM on a VISA card

A module with LV-distribution cards



Read it out with serial link to SRU



Hear about RD51 Scalable readout system in Hans Mullers talk

Some lessons for continuous readout

Reduce avalanche gain pays in ion backflow and trip risk

Increase sensitivity by trimming:

- Fine ADC scale in pedestal region. Zero supp acts on digitized data (non linear ADC)
- Take many samples on pulse (tail and wing samples shall not define threshold)
- None or very short cables to reduce inp capacitance
- Input protection without noise addition (series resistor)
- If integration of digital and analog adds noise, skip it (at least ALICE)