SPADIC – Self-triggered charge pulse processing ASIC

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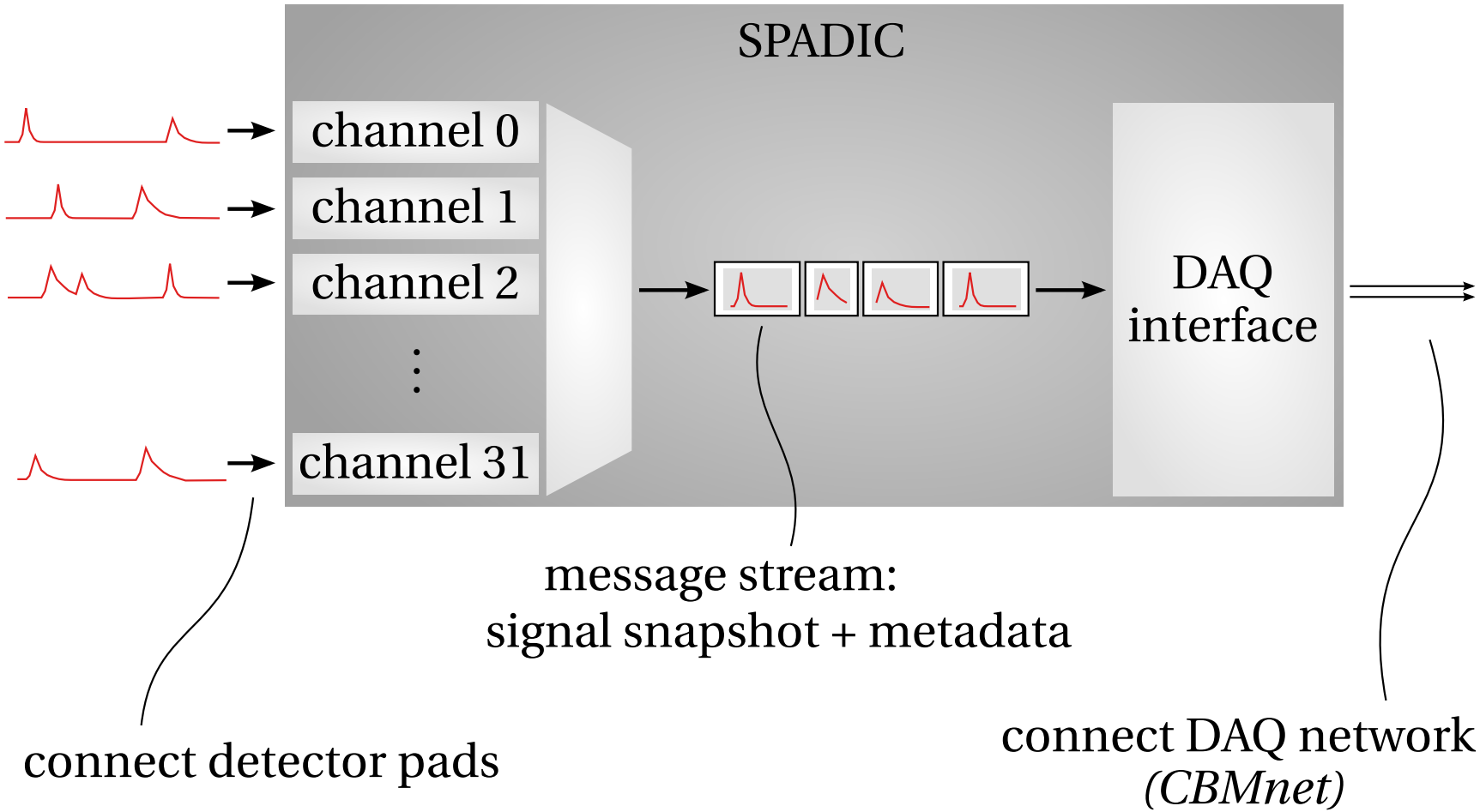
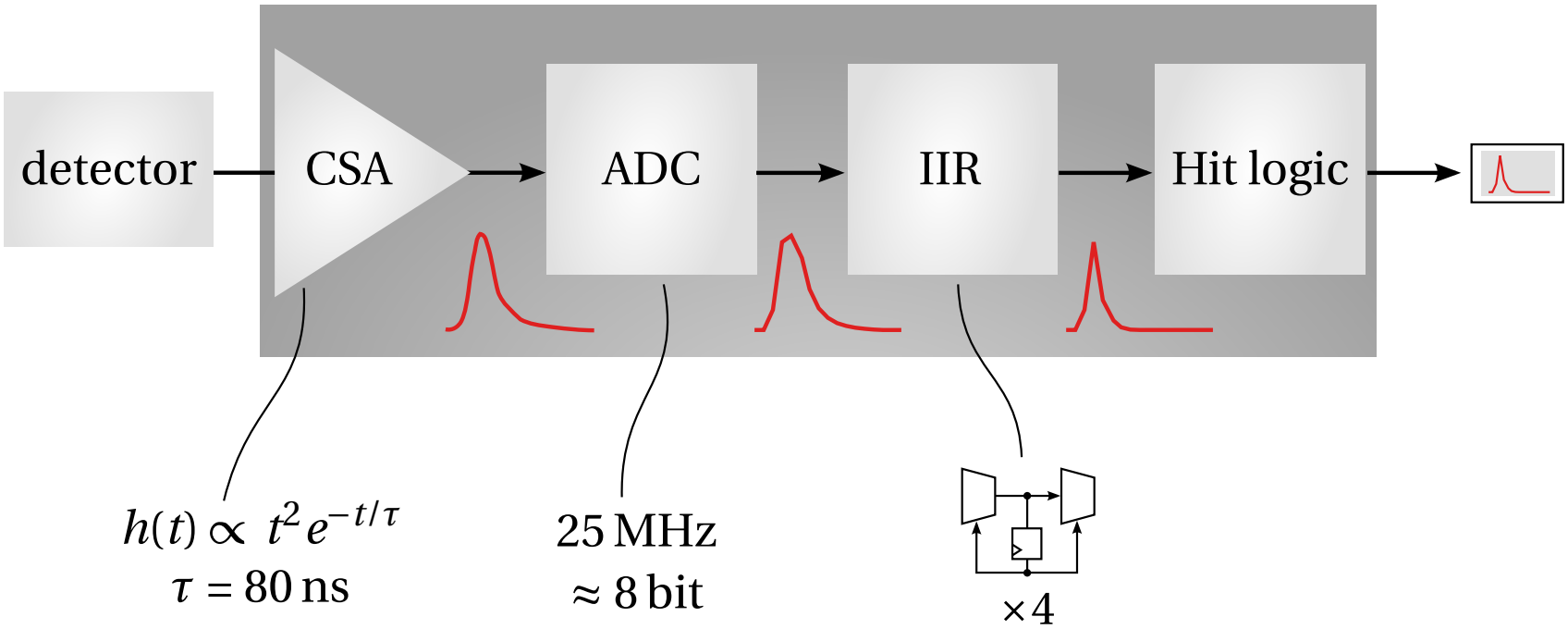
Introduction

- Self-triggered Pulse Amplification and Digitization ASIC
- main application: TRD subsystem of CBM (FAIR/GSI)

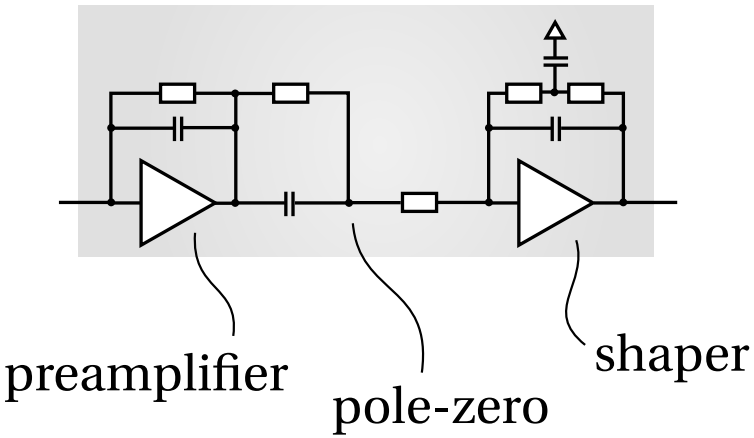
Concept

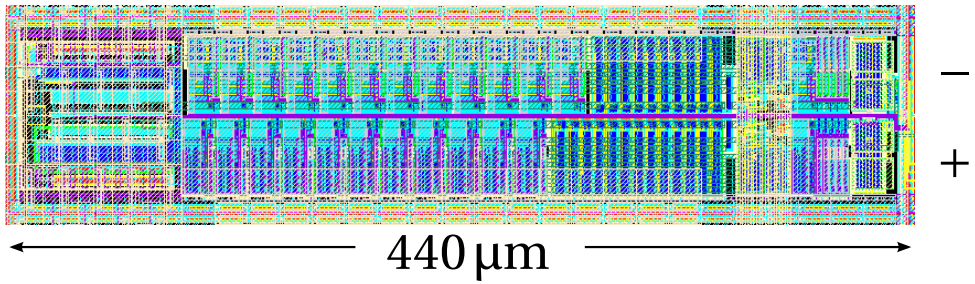

SPADIC
channel 0
channel 1
channel 2
channel 31
DAQ
interface
message stream:
signal snapshot + metadata
connect detector pads
connect DAQ network
(CBMnet)

Channel overview



Charge amplifier





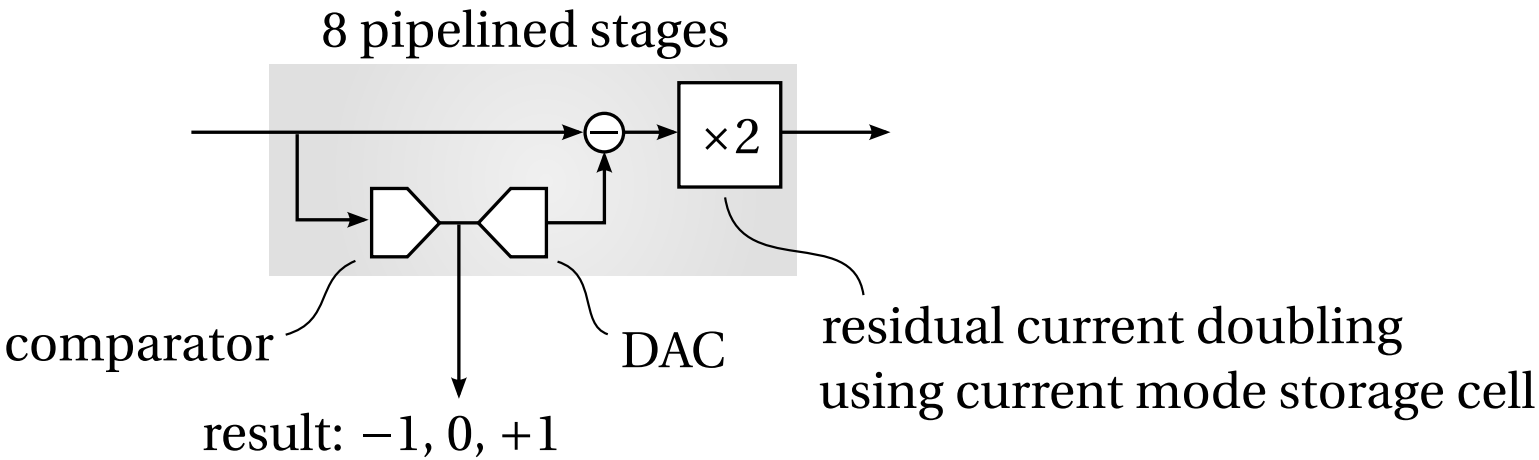
- input range: 75 fC
- shaping time: 80 ns
- noise: 800 e^- @ 30 pF

two amplifiers per channel selectable:

- positive polarity (4 mW)
- negative polarity (10 mW, not optimized)

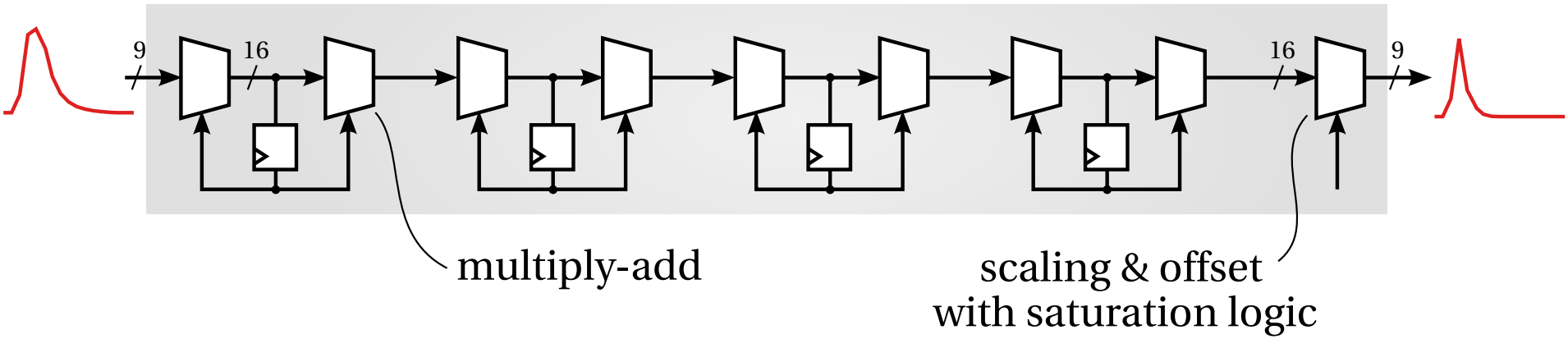
layout & schematics: modular, scalable

ADC

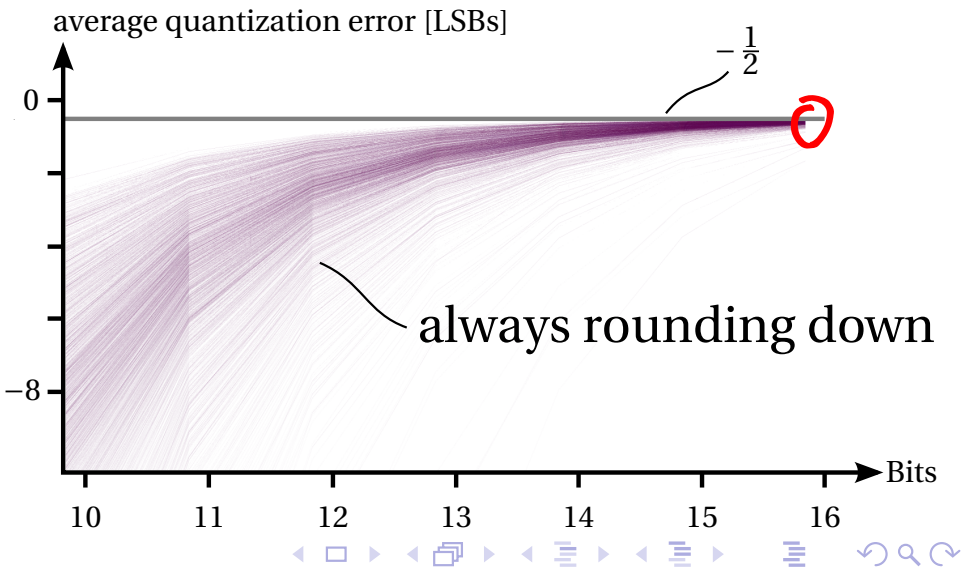


- current mode pipelined design
- 25 MHz sample rate, continuously running
- 9 bit nominal output
- resolution ≈ 8 bits
- 4.8 mW, rad-hard layout, $400 \times 300\,\mu m^2$

IIR Filter



- 16 bit internal resolution
- 6 bit coefficients
- freely programmable ($\frac{-32,\ldots,31}{32}$)
- instability excluded

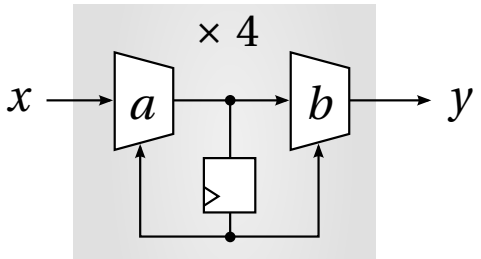


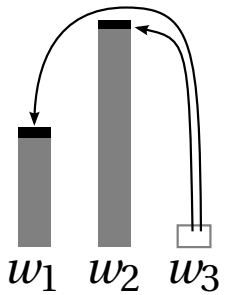
IIR Filter

purpose: “tail cancellation”

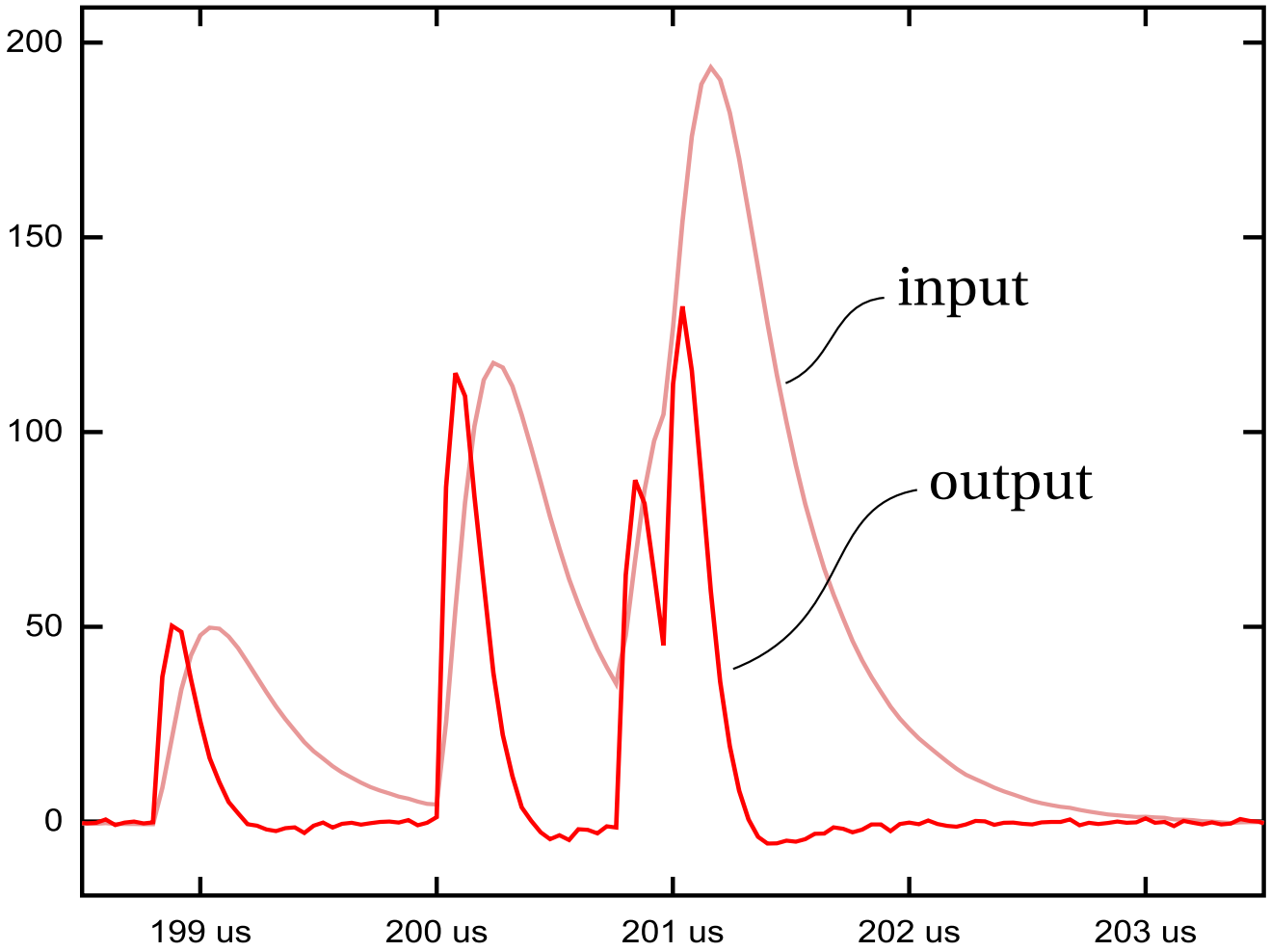
shorten pulses → reduce pileup/help hit logic

- model signal as sum of exponential terms:
  $x_n \propto \sum w_i q_i^n$
- recursion: $y_n = x_n + b x_{n-1} + a y_{n-1}$
- each filter stage shifts relative weights:
  $w_i' = \frac{q_i + b}{q_i - a} w_i$

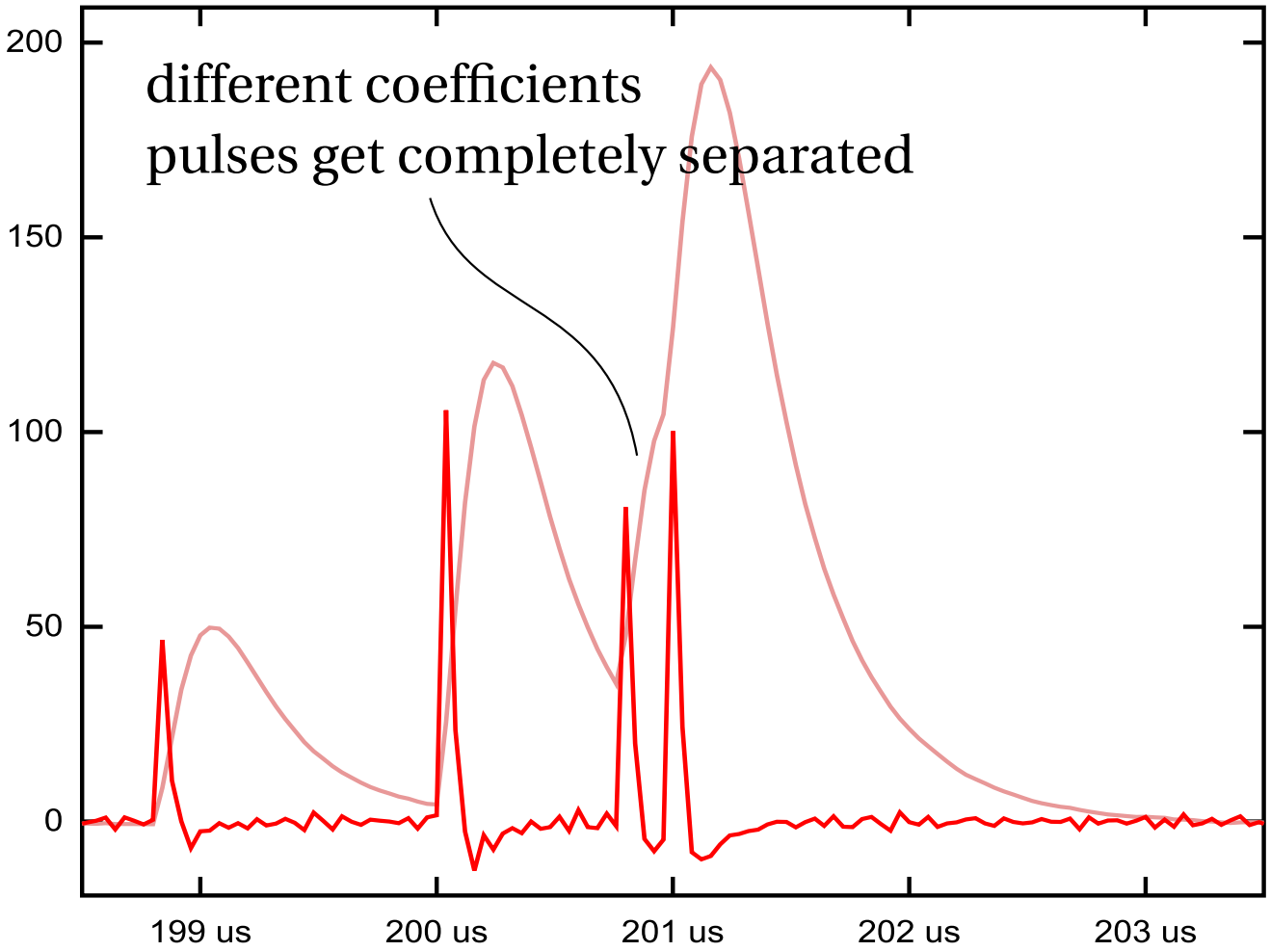




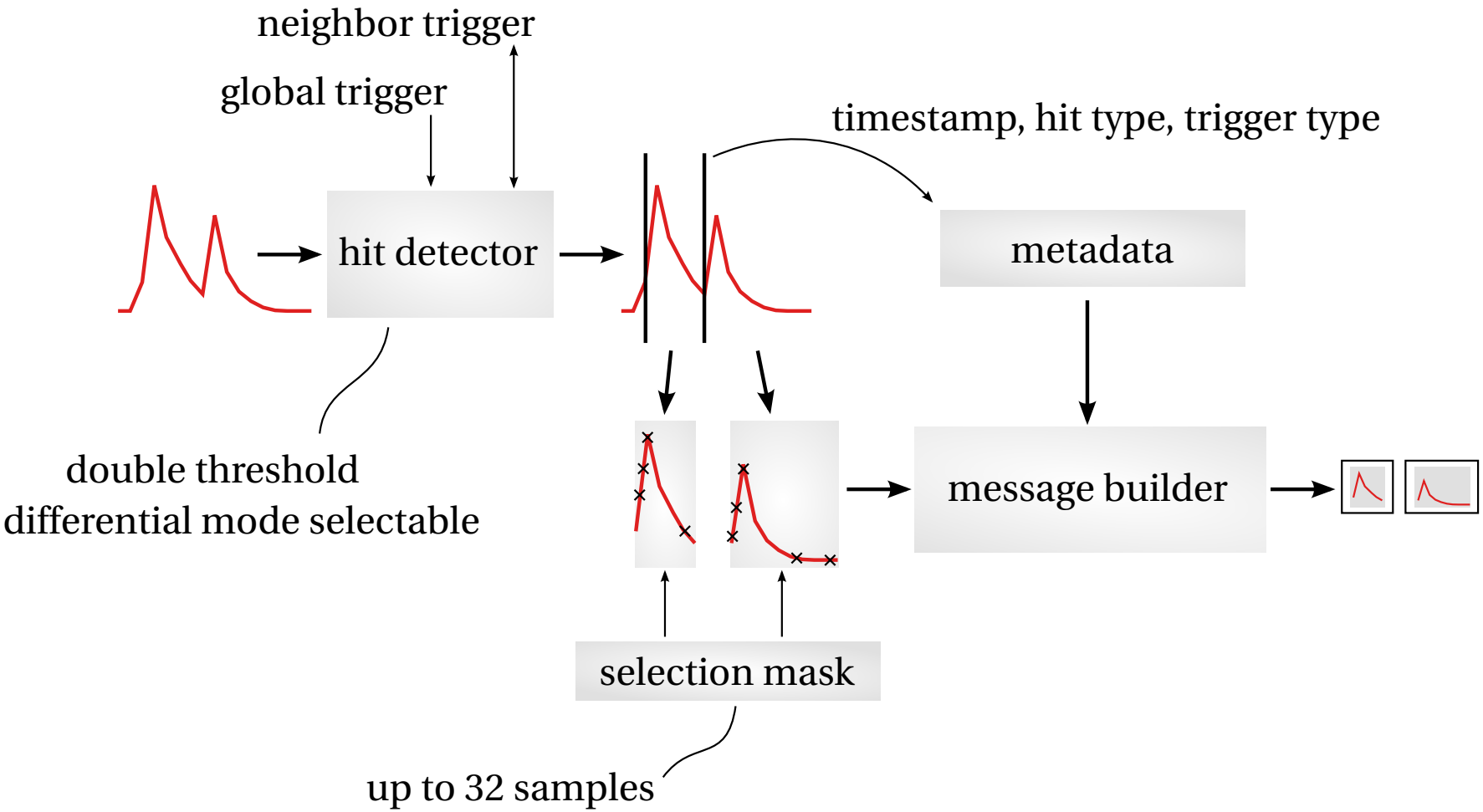
IIR filter: examples (simulation)



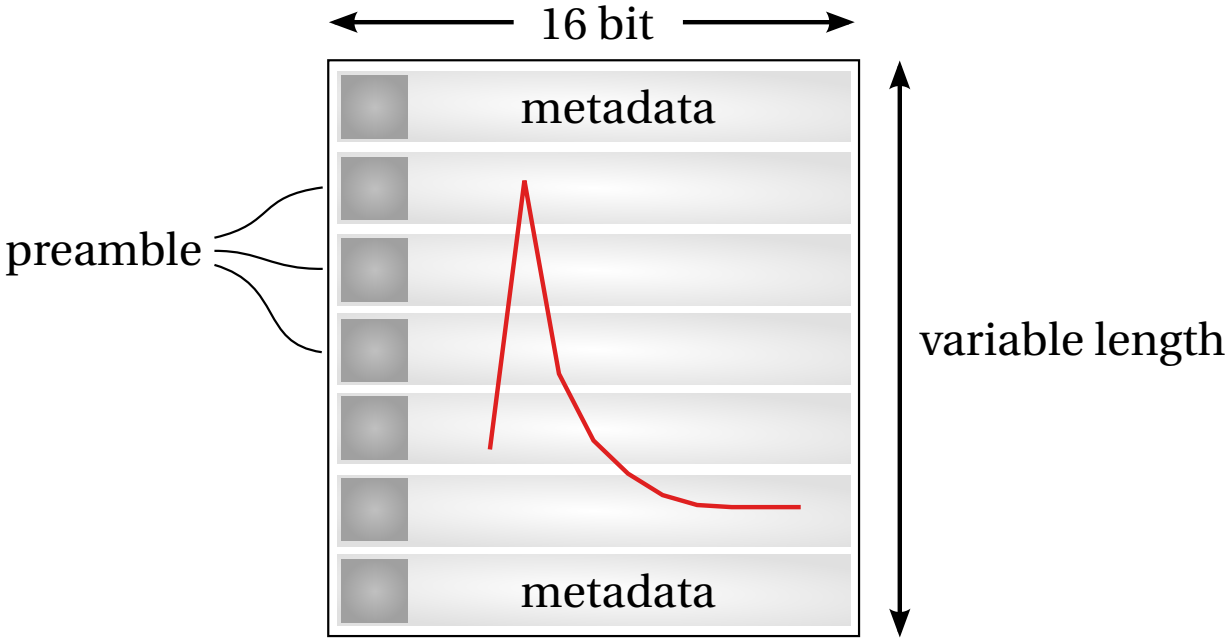
IIR filter: examples (simulation)



Hit logic

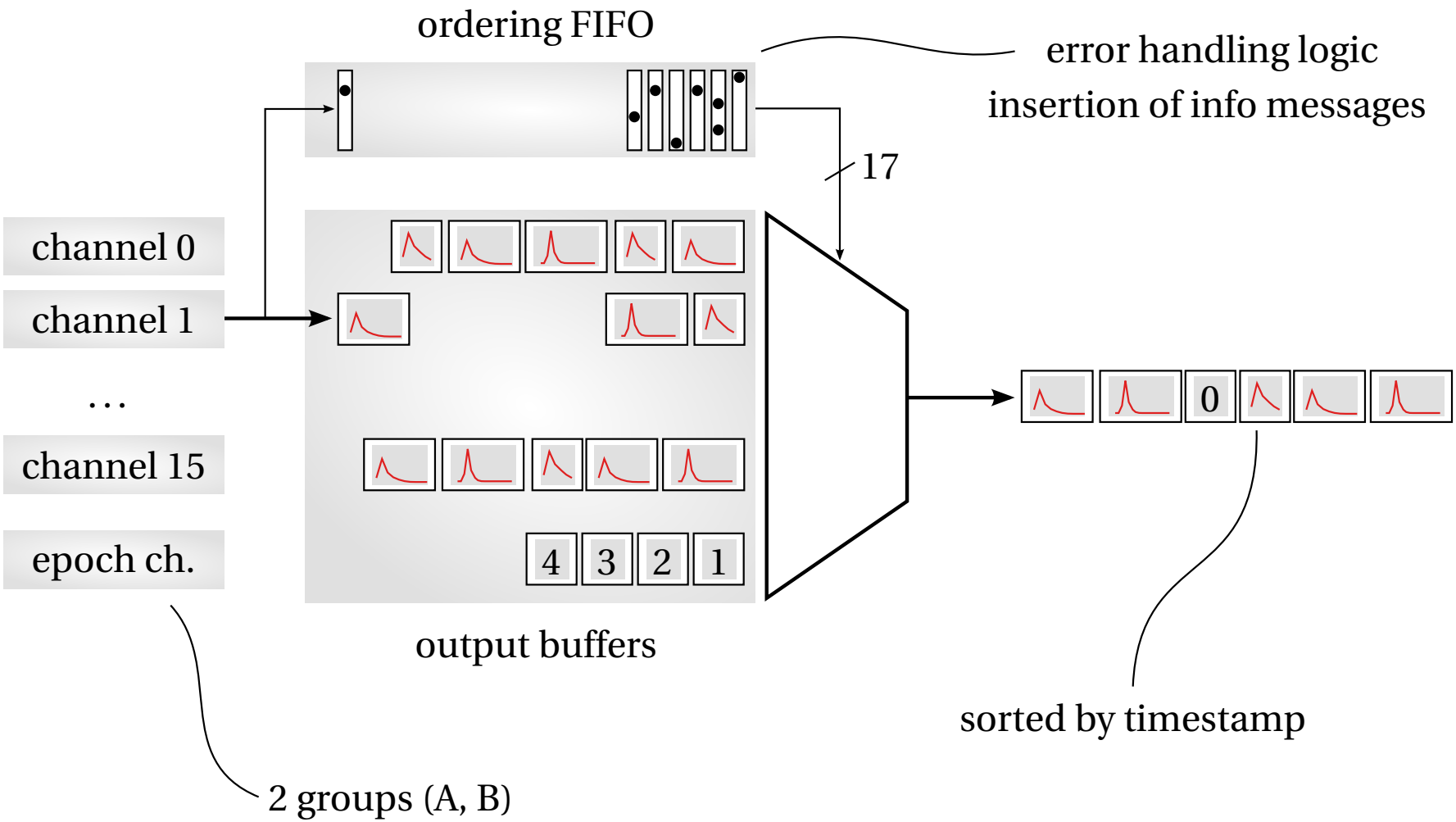

neighbor trigger
global trigger
timestamp, hit type, trigger type
hit detector
metadata
double threshold
differential mode selectable
message builder
selection mask
up to 32 samples

Message format

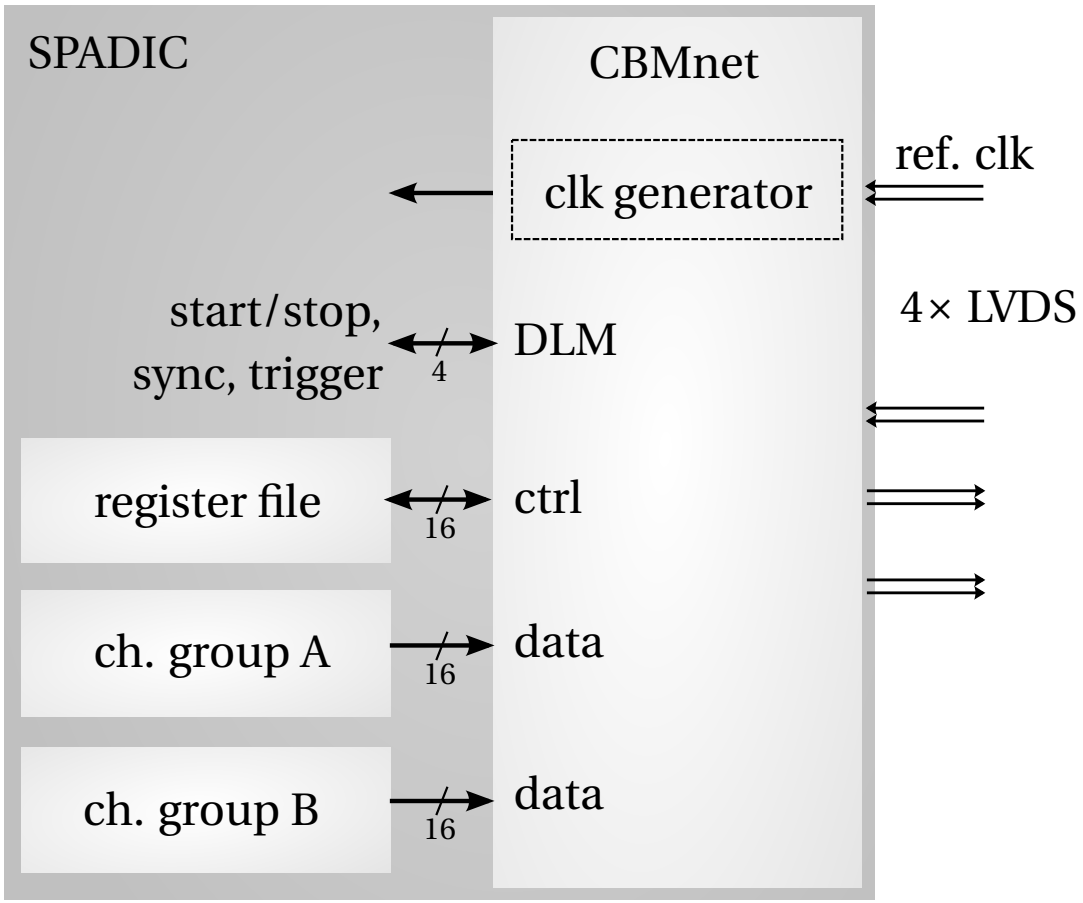


- every word has a preamble (4 or 1 bit)
- easy recovery of message stream

Message output multiplexing

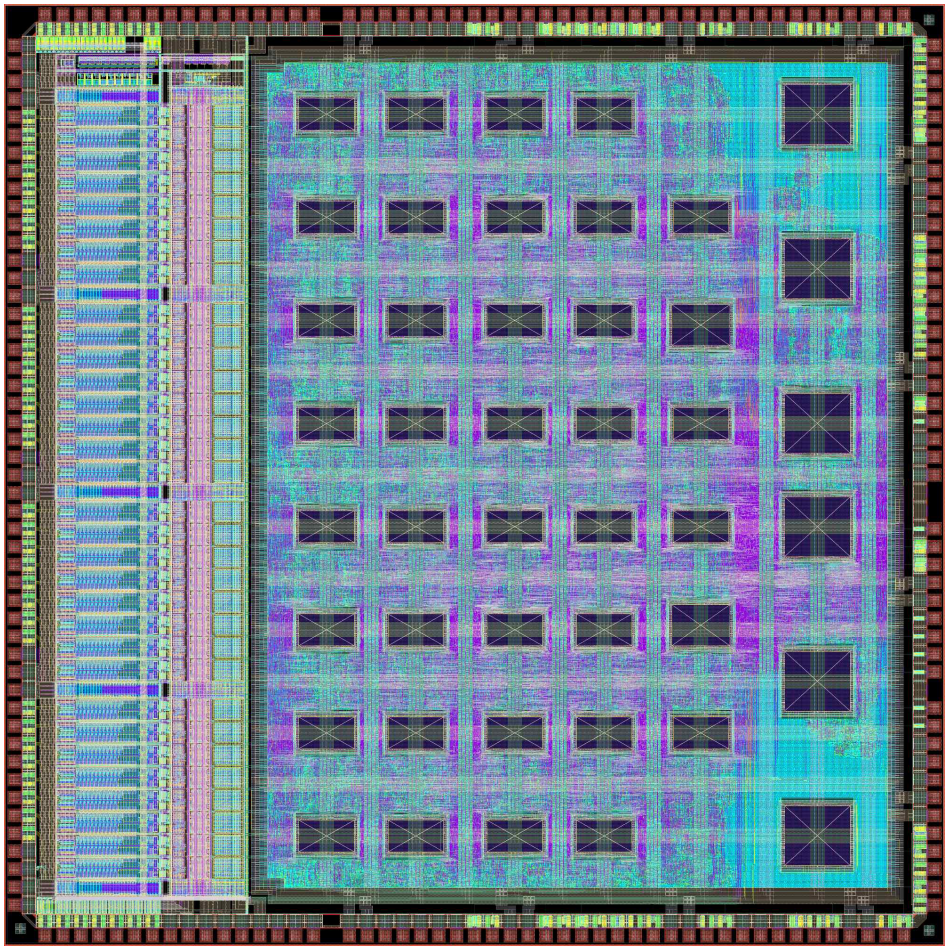


DAQ interface (CBMnet)



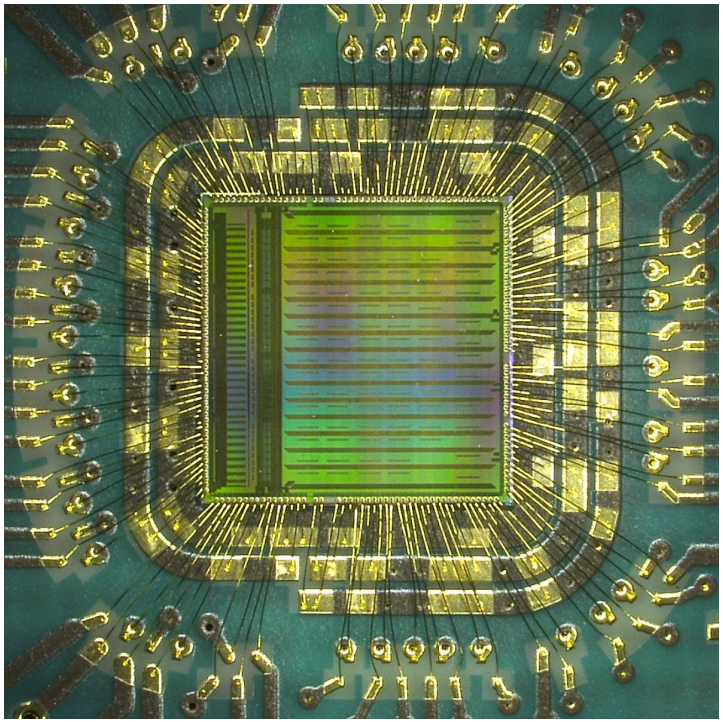
- error checking, retransmission
- *deterministic latency messages (DLM)*
- different traffic classes share single serial link
- 500 Mbit/s (DDR), 8b/10b encoded, LVDS (1 input, 2 outputs)

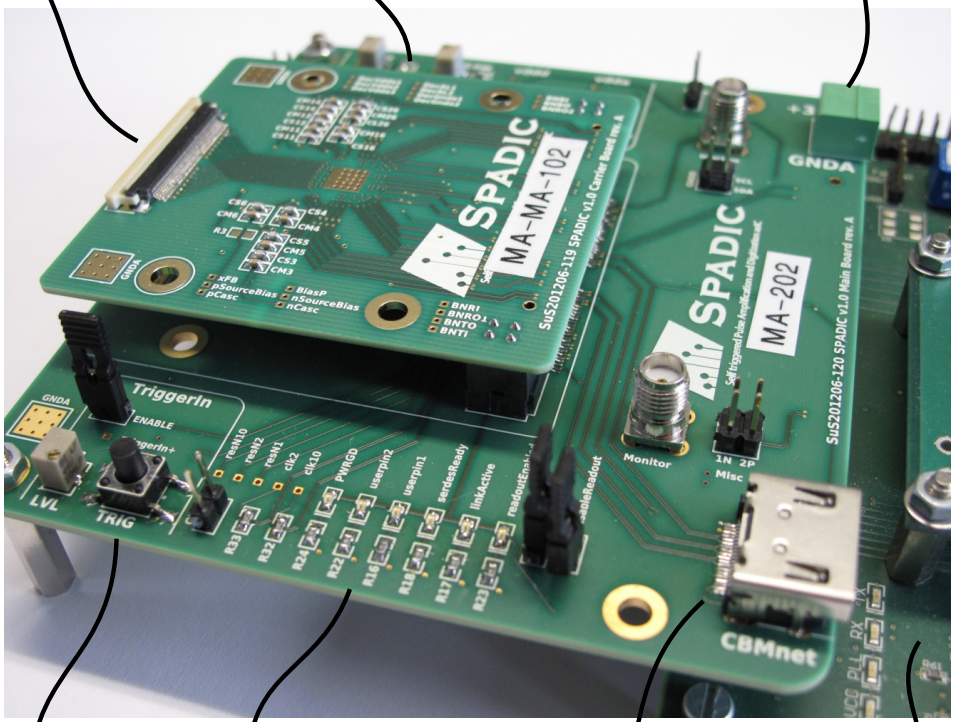
Layout view



- UMC 180 nm
- overall size: $5 \times 5\,\mathrm{mm}^2$
- digital part:
  - $3.5 \times 4.5\,\mathrm{mm}^2$
  - home-made standard cell library
  - 2.5 million transistors, 23k FF, 81k gates
  - 44 Faraday SRAMs
  - total wire length: 14.4 m
  - Power (200 MHz): 600 mW

Test setup





detector

voltage regulators

power

test pulse injection

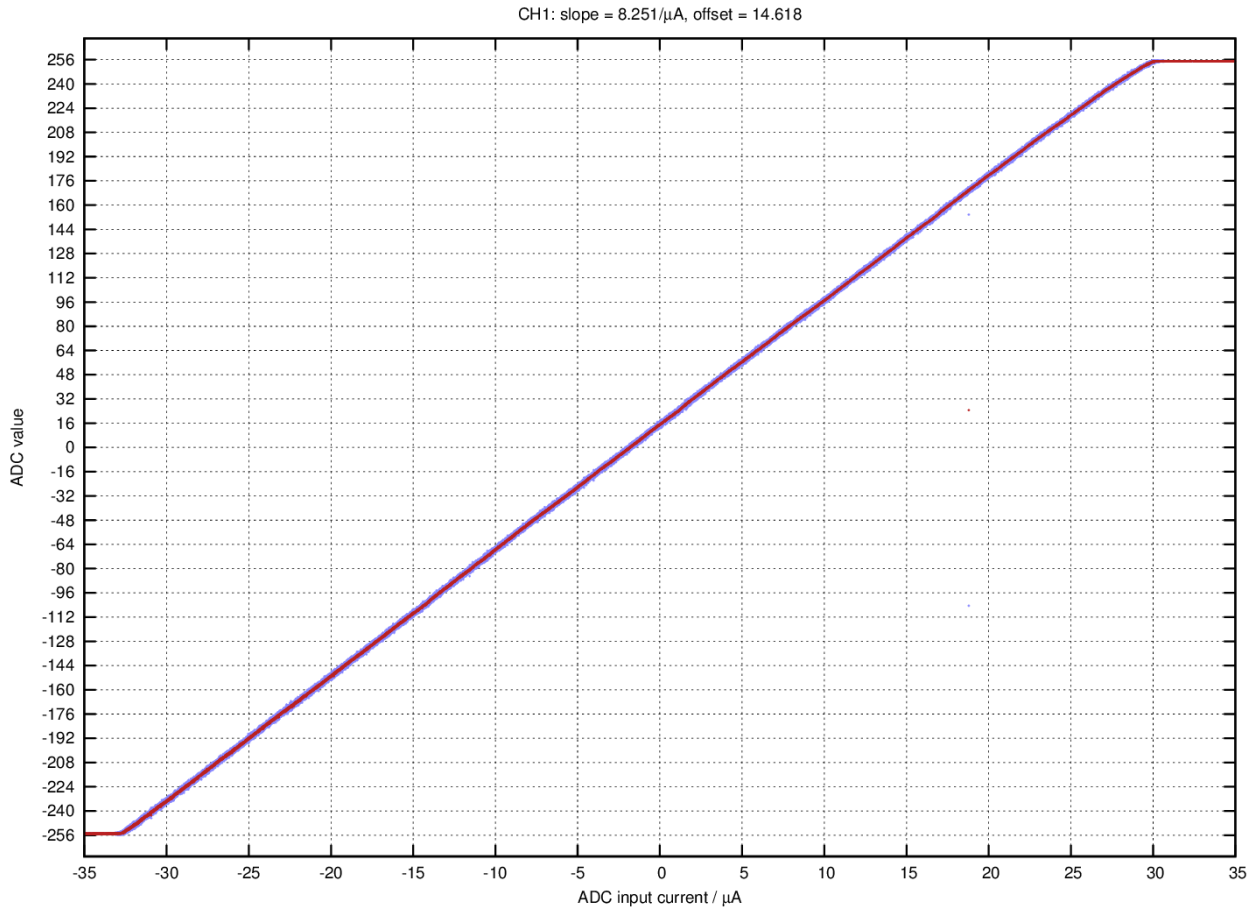
status LEDs

CBMnet (HDMI)

FPGA board *Susibo* → USB

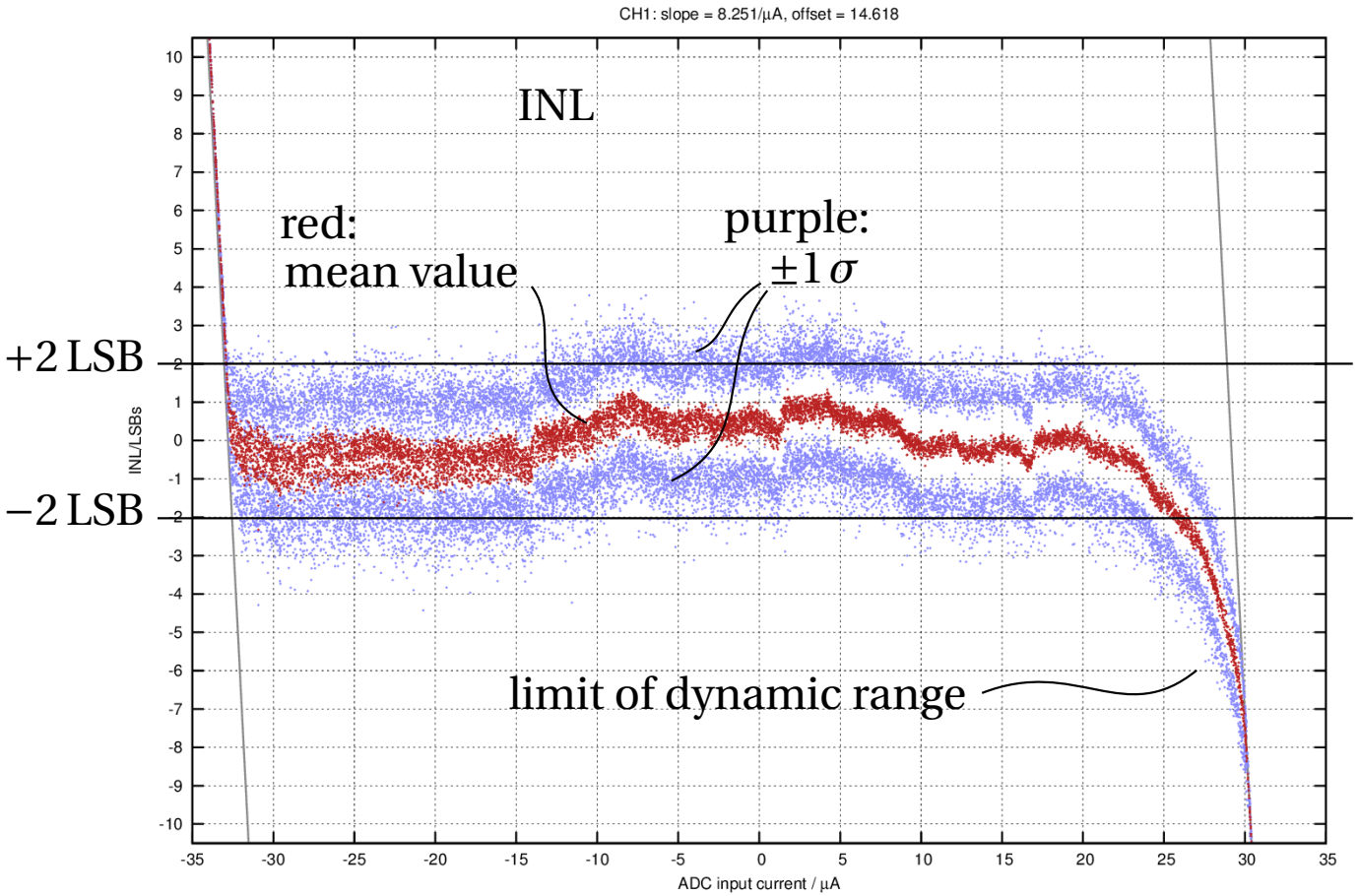
First results

ADC curve: taken at 20 MHz sample rate, preliminary bias settings



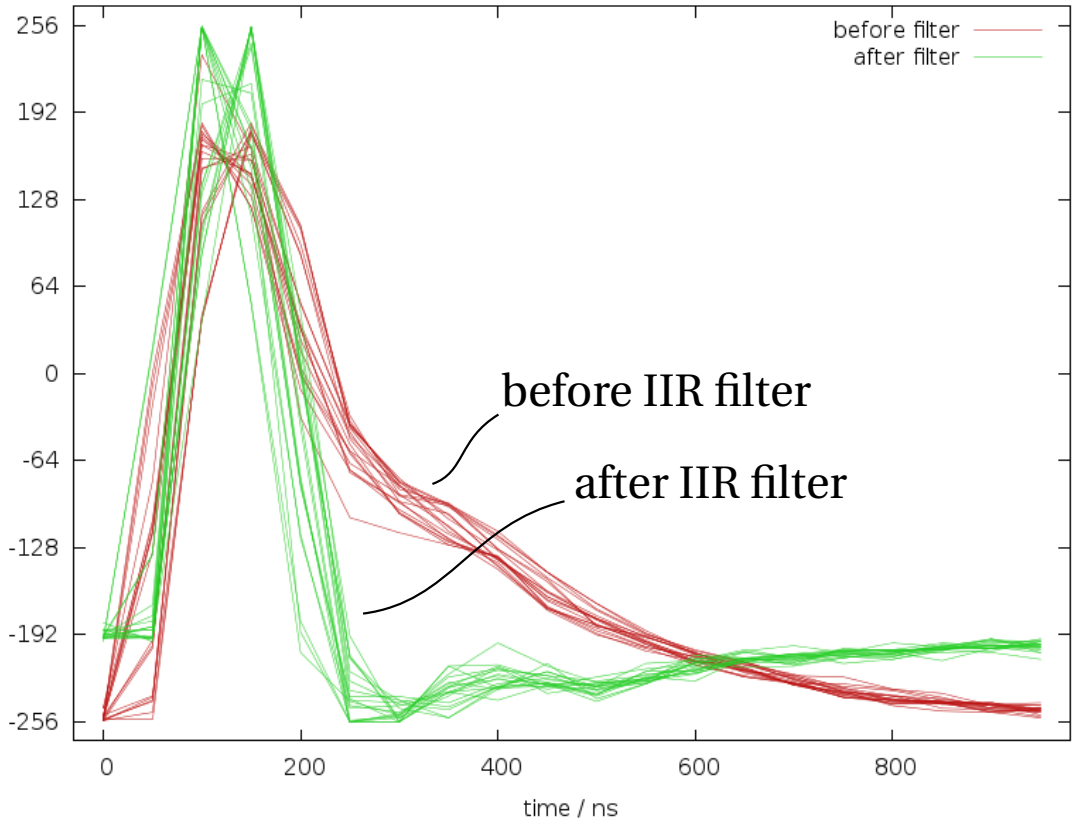
First results

ADC curve: taken at 20 MHz sample rate, preliminary bias settings



First results

measured pulses (20 MHz sample rate)

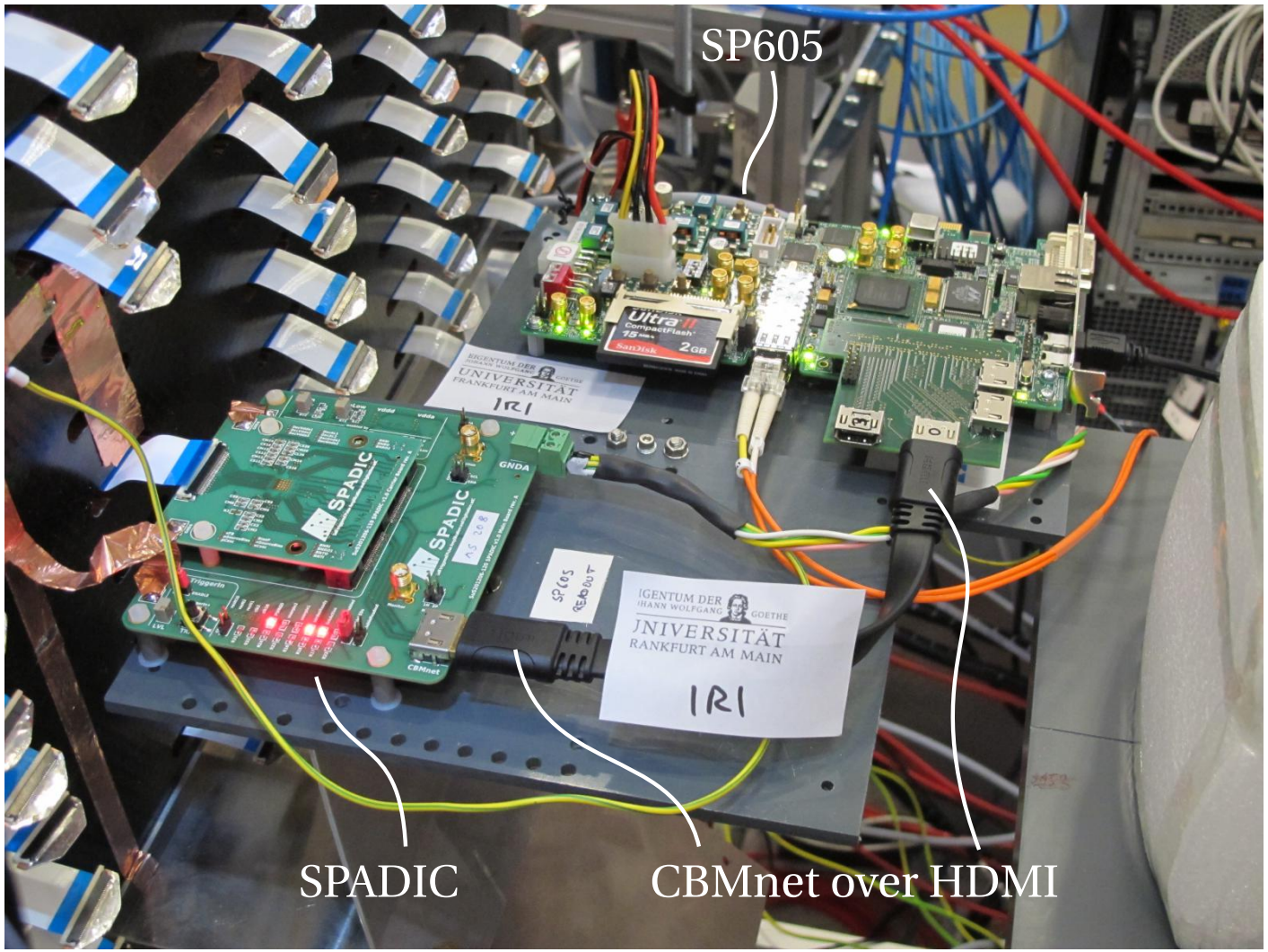


CSA → ADC → IIR Filter → hit logic → message building ✓

First results

CBM beamtime October 2012 @ CERN: first time CBMnet readout

TRD prototype



Development status & lookout

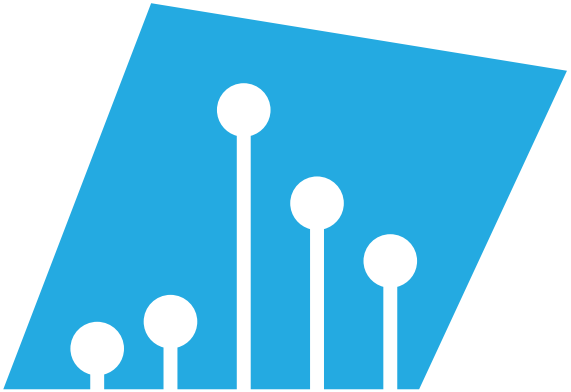
- shown measurements done using auxiliary readout (bypassing CBMnet, limited capabilities)
- no major bugs discovered, everything so far tested works
- lab setup not yet CBMnet compatible → in progress
- full characterization (CSA, ADC) to be done, optimal settings to be found

Summary

SPADIC

complete system for charge pulse readout

- 32 channels
- self-triggered recording of whole pulse shapes (programmable selection mask)
- neighbor trigger, global trigger
- flexible digital signal processing
- time-sorted output message stream with notification of error conditions
- CBMnet: built-in DAQ connection with reliable data transmission and synchronization features using 4 LVDS pairs



SPADIC

Self triggered Pulse Amplification and Digitization asIC

http://spadic.uni-hd.de