Status and Future of the Transient Recorder Chip

Development of the HitDetection ASIC @ GSI

Bonn – 28.02.2013

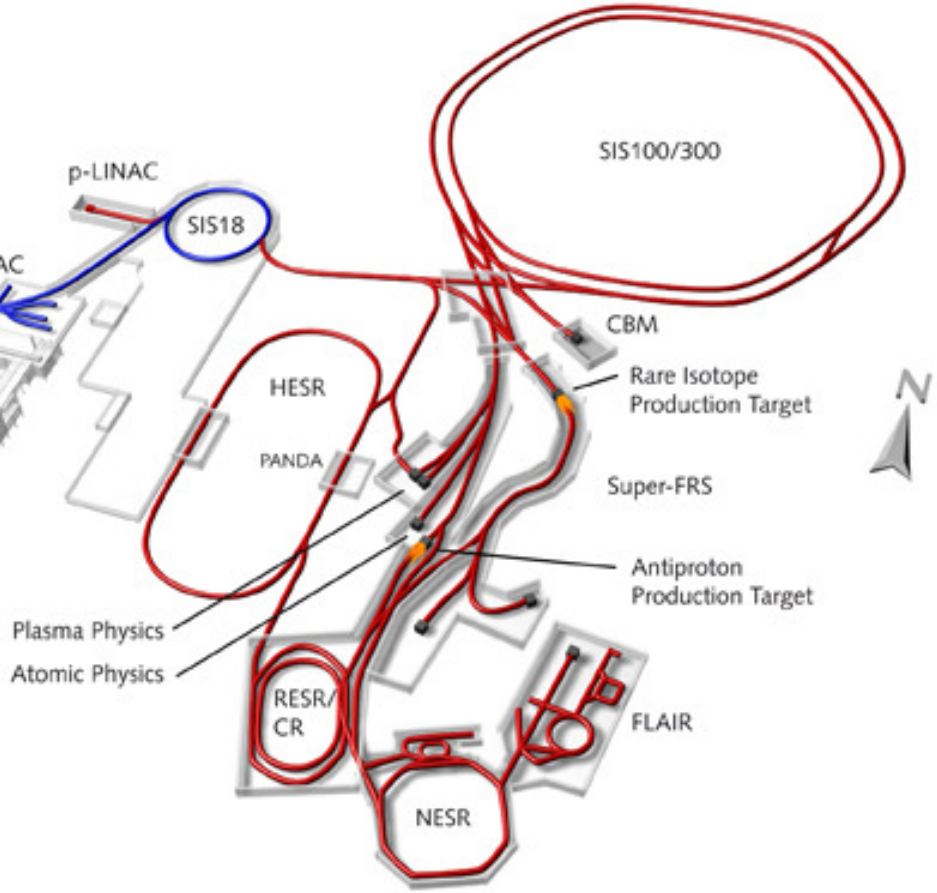
Peter Wieczorek, GSI

Overview

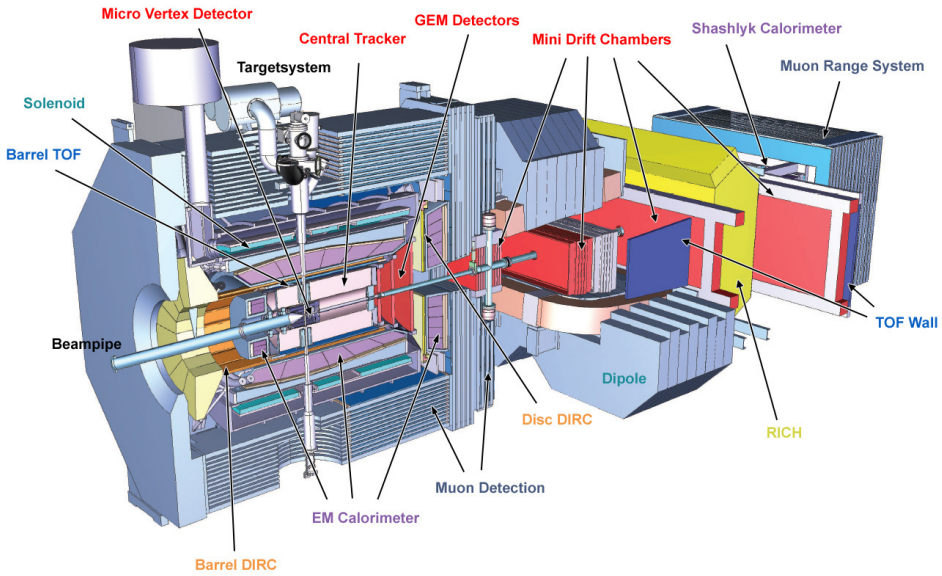
- FAIR @ GSI
- Motivation for the HitDetection ASIC
- ASIC Architecture
- Crucial Design Points
- First Results
- Summary and Outlook

FAIR Facility

Projected Facility



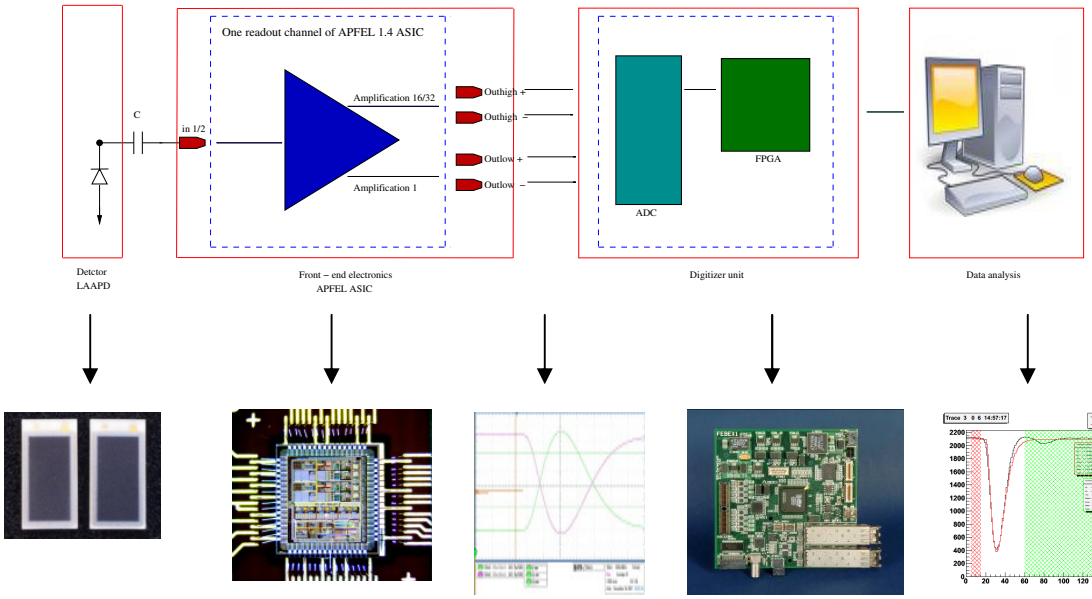
PANDA Experiment



- Several sub detector systems in a very compact design
- PANDA experiment: Trigger – less data taking

- PANDA EMC:
  - 11000 lead tungstate crystals
  - Event rate up to 300 kHz/per crystal
  - Operation temperature T = – 25 ℃

DAQ PANDA EMC



APFEL ASIC:
- 60 mW/ch
- Pulse width: 1 µs

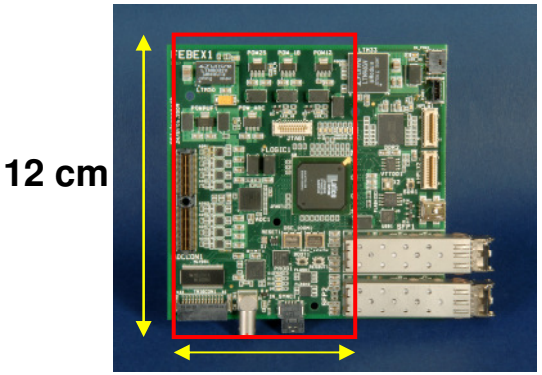
Digitiser unit:
- 1 W/ch @ 60 MS/s

Analysis

- **Readout chain**
  - **Detector**
  - **Front – end electronics**
  - **Digitiser unit**
  - **Analysis**

Motivation

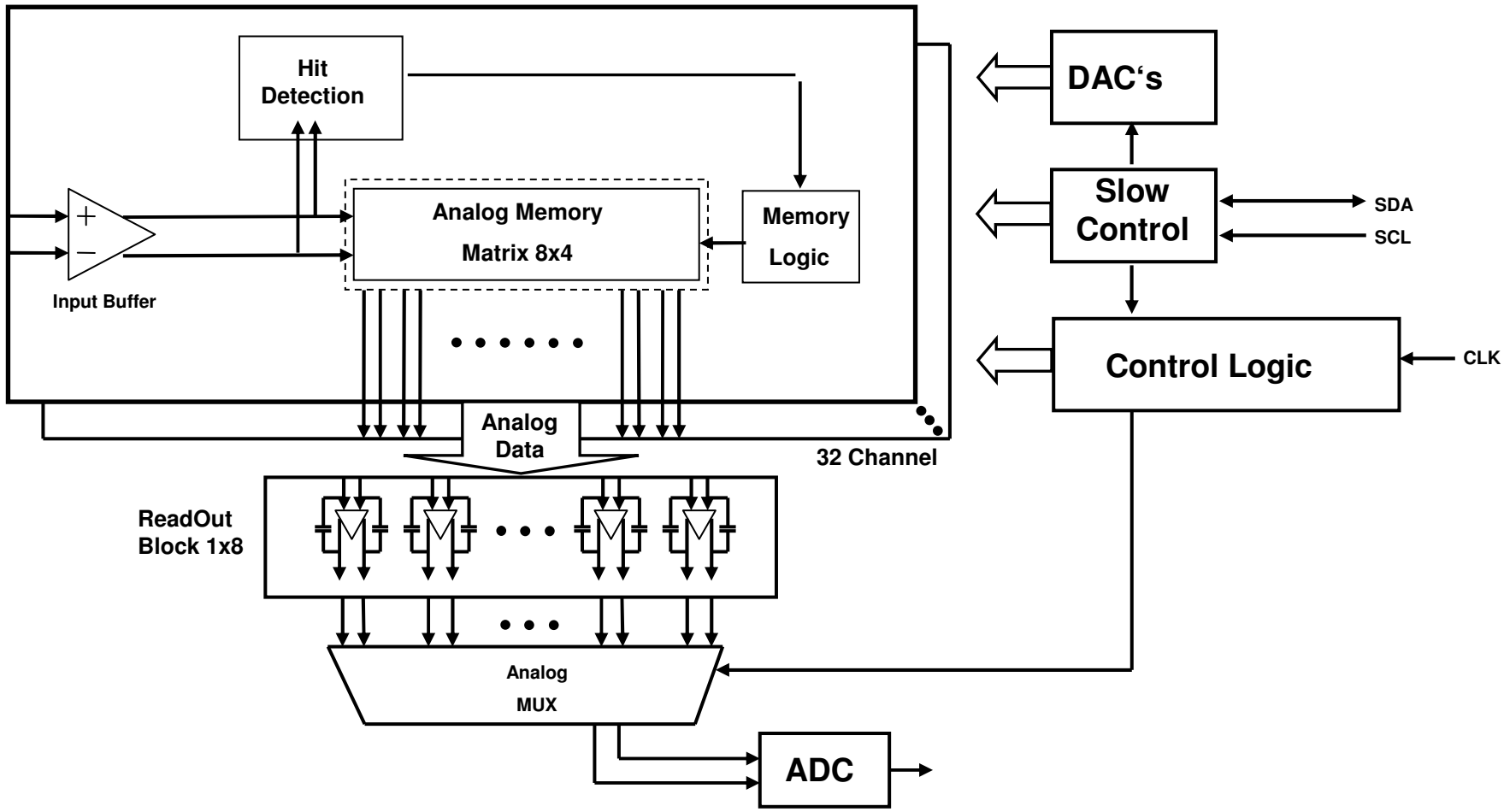
- Concept of HitDetection ASIC by Igor Konorov
- Multi purpose transient recorder ASIC
- Less external components
  - Higher reliability (limited access to sub detector volume)
  - Lower power consumption (100 mW/ch?)
  - Lower number of supply voltages (1 or 2)
  - Cost reduction
- Radiation tolerance
  - SEUs in FPGA configuration SRAM



Features of the HitDetection ASIC

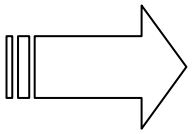
- Self – triggered transient recorder
- Configurable sampling rate (Detector specific configurable)
- Analogue signal storage and derandomisation
- On – chip ADC
- Time – stamping

Block Schematic HitDetection ASIC



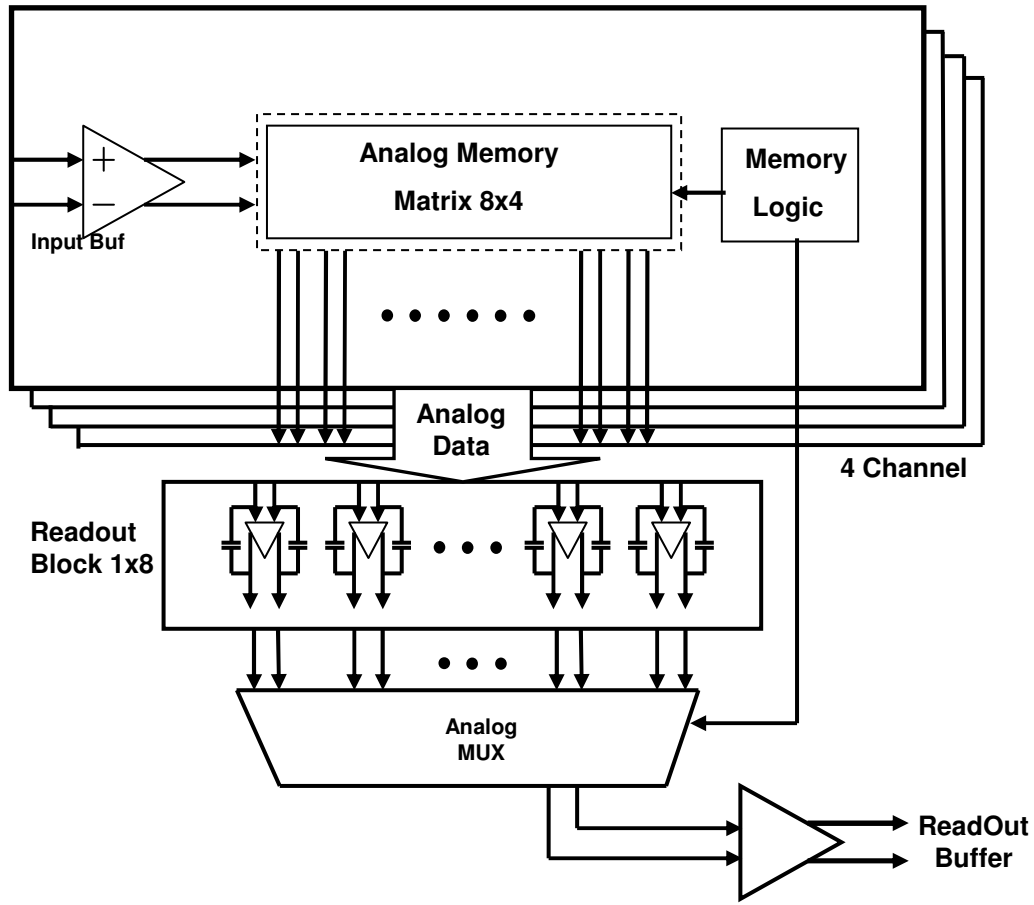
HitDetection ASIC Integration Level

- Number of input pads (differential = 2 pads/channel)
  - Proposal 32 channels:
    - Pad pitch 140 µm — chip width: 4500 µm + 500 µm (max. chip size 5000 µm (MPW run))
  - Proposal 64 channels:
    - Pad pitch 100 µm — chip width: 6400 µm + 500 µm
    - Pad pitch 80 µm — chip width: 5120 µm + 500 µm
- Space limitation from block size (analogue memory differential)
  - MIM – cap option @ 1 pF: Cell size : 20 µm x 100 µm
  - Channel width 4 x 20 µm + routing: 100 µm
- Data rate assuming 200 kHz/channel, 8 samples/event, 12 bit ADC, 20 bit timestamp
  - 32 channels: 3.2 mm; Data rate: 768 Mbit/s
  - 64 channels: 6.4 mm; Data rate: 1.54 Gbit/s
- Which integration level is reasonable for the detector?



Final: 32 channel solution

Block Schematic HitDetMEM 1.0

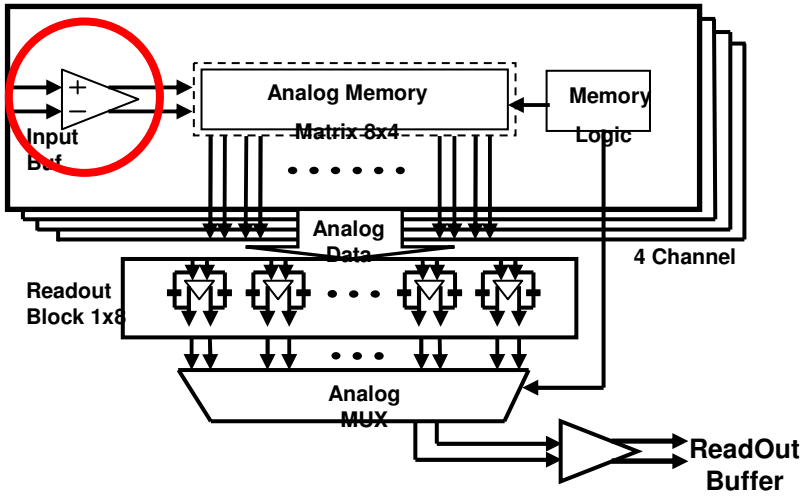


- HitDetMEM 1.0 includes:
  - Differential input buffer
  - External trigger for readout
  - Analogue memory with MIM – cap option
  - Differential integrator
  - Analogue multiplexer
- UMC 180 nm CMOS
- Chip size:

  3240 µm x 1525 µm

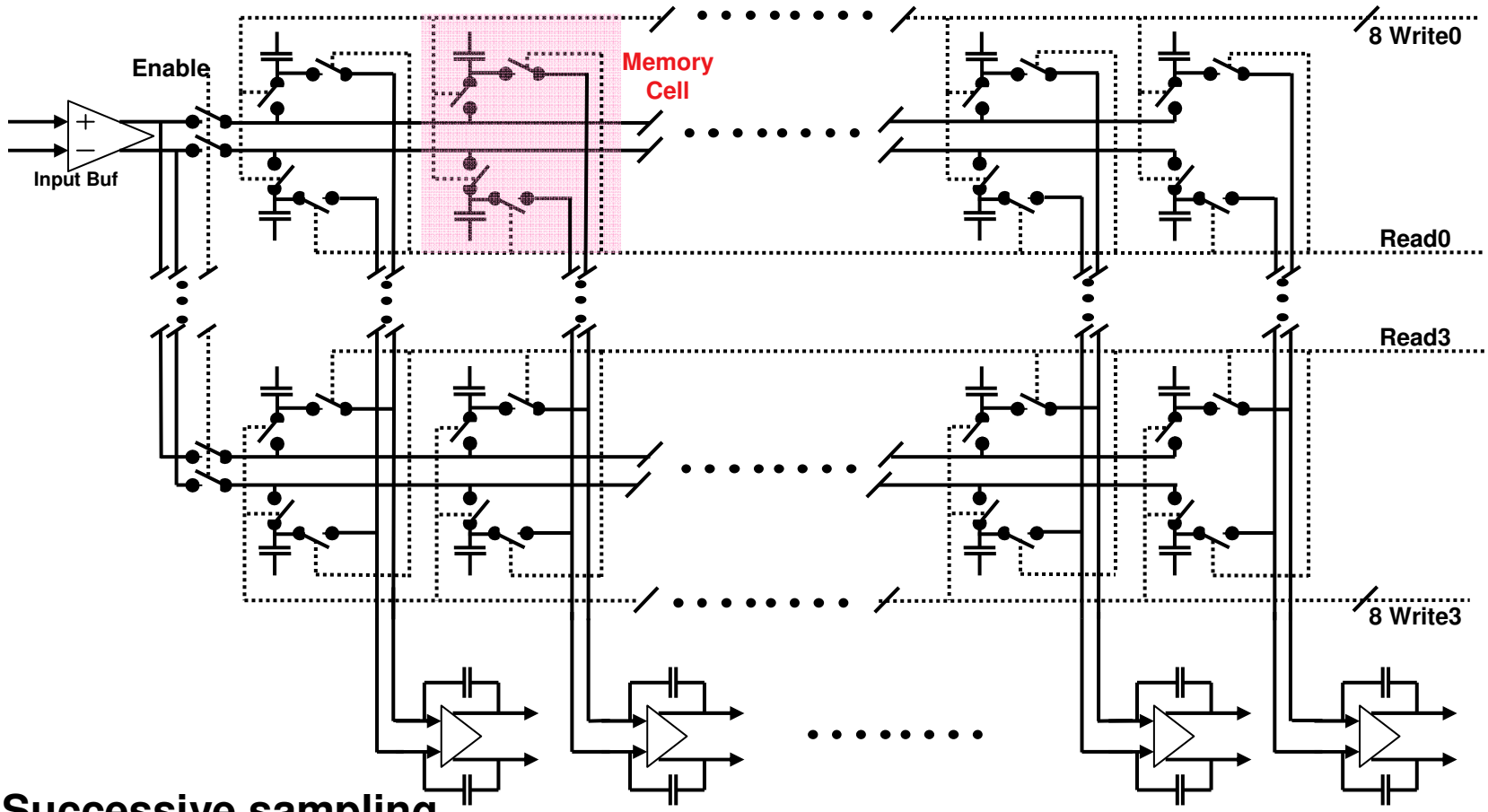
Differential Input Stage

- **Requirements for the input stage:**
  - **Fully differential operation**
  - **Input DC range: 0 – 3 V**
  - **Pulse heights: about ± 1 V**
  - **Output Vcm fix at 0.9 V**
  - **High linearity and slew rate (SR: 2 V / 5 ns)**
  - **Low noise / low power consumption**



- **Test different input stage based on a folded cascode architecture**

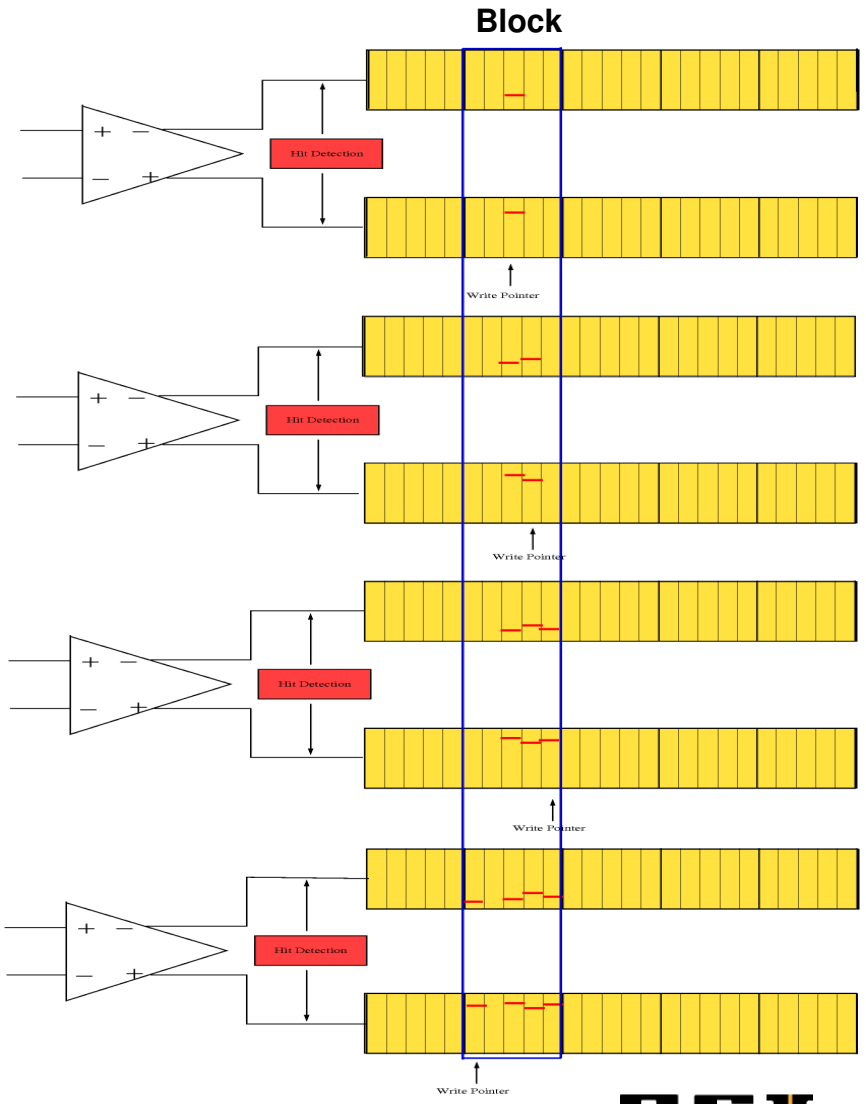
Channel Memory Matrix 8x4



- Successive sampling
- Parallel readout

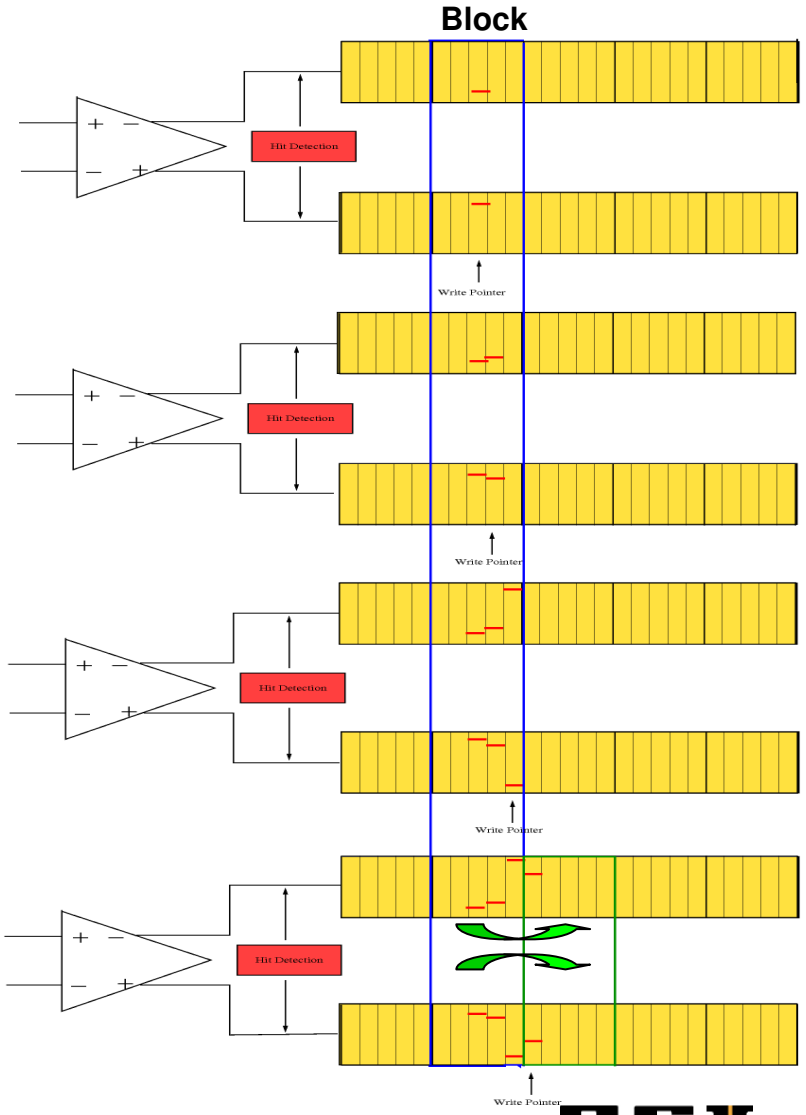
Analogue Signal Storage and Derandomisation

- Capacitor array used as analogue memory
- Analogue memory is divided into blocks with configurable size
- Signals from input receiver are sampled and stored at the position of write pointer
- Write pointer circles inside of one block



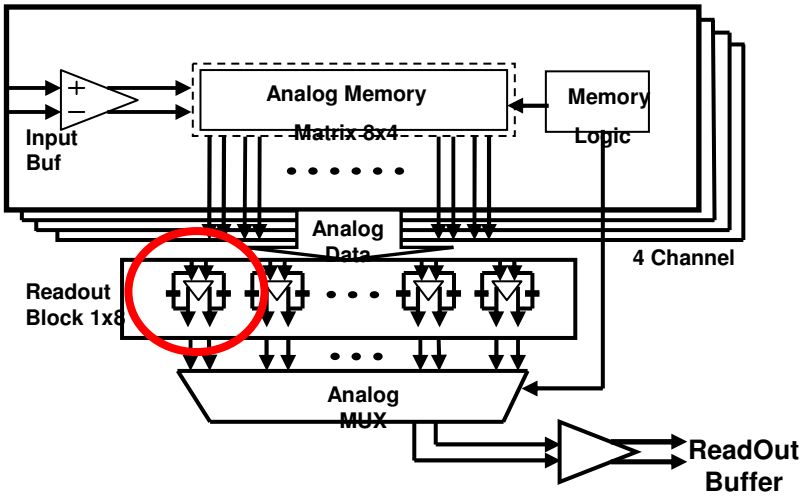
Analogue Signal Storage and Derandomisation

- Signals from particle energy deposits are detected by the hit detection unit
- Write pointer switches to the next memory block
- Signal transient is stored in previous block
- Analogue readout when shared ADC is available
- Block is available again for signal storage



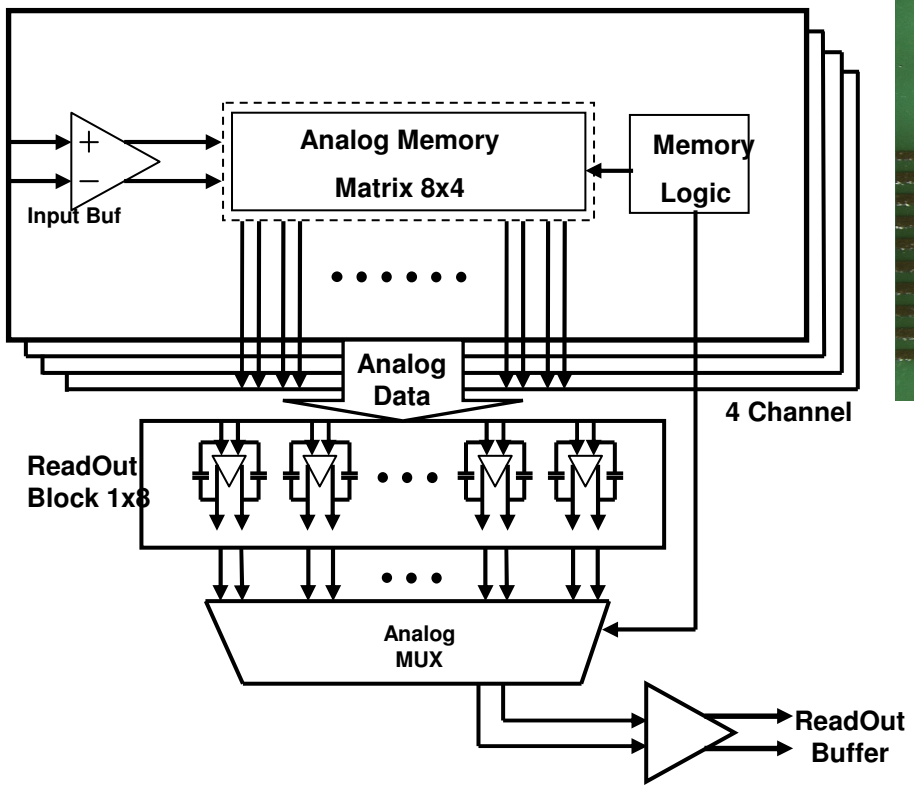
Differential Integrator

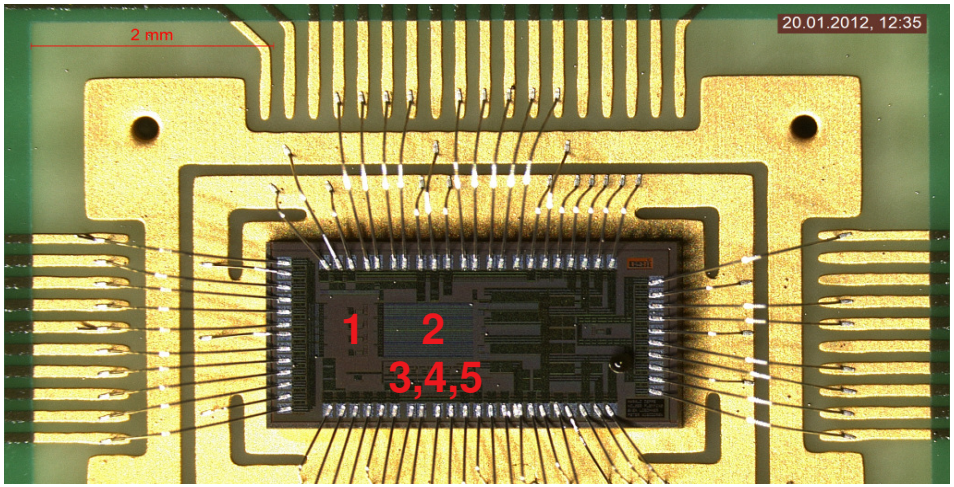
- Requirements for the integrator stage:
  - Fully differential operation
  - Input DC range: 0 – 1.5 V
  - Pulse heights: about ± 1 V
  - High linearity and slew rate
  - Low noise and low power



- Use a fast integrator architecture without CMFB:
  - Differential input (n – mos)
  - Auto zero circuit
  - Output buffer

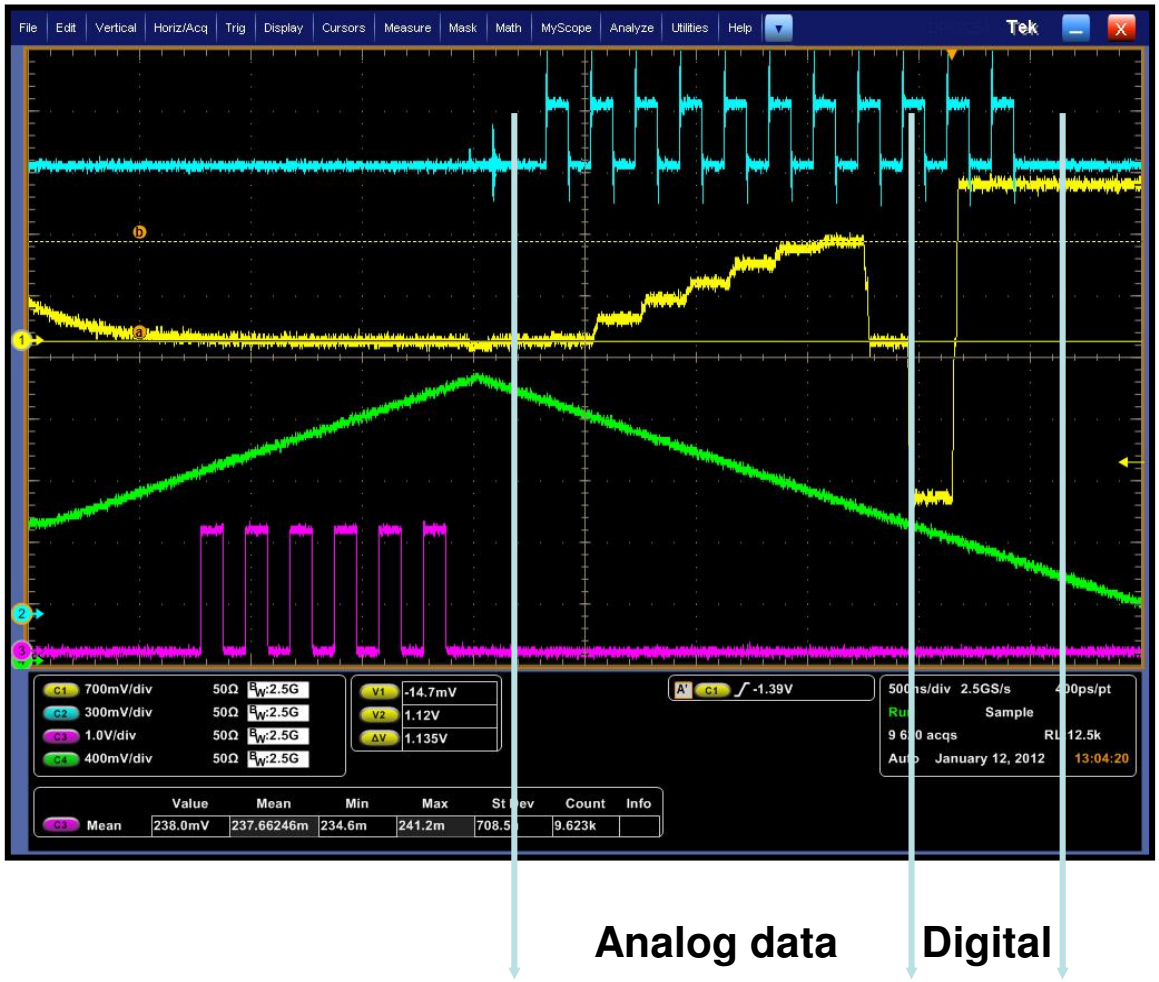
Functional Tests on HitDetMEM 1.0 (1)





1	Differential input buffer	=>	works
2	Analog MIM- cap memory	=>	works
3	Differential integrator	=>	works
4	Analogue multiplexer	=>	works
5	Output buffer	=>	works

Functional Test of HitDetMEM 1.0 (2)



MuxClk (blue)

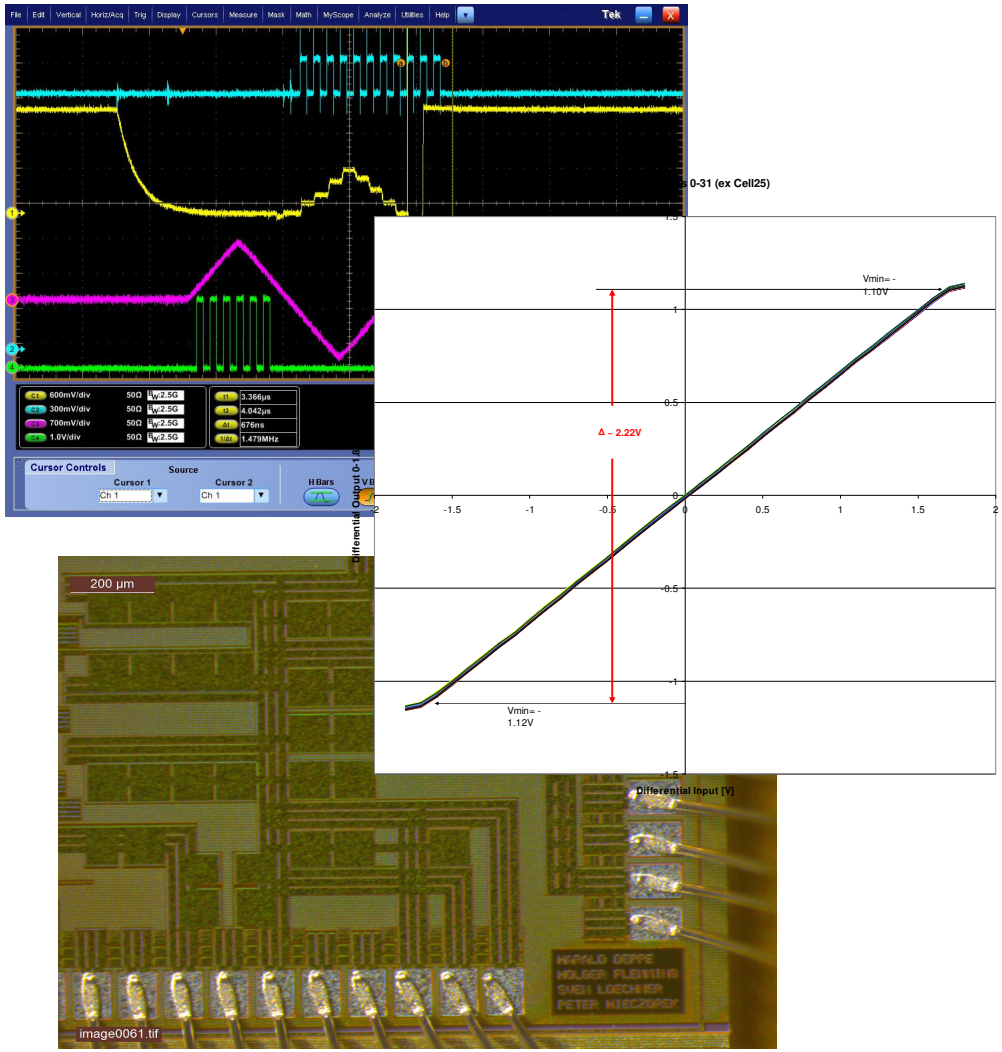
Analog out (yellow)

Input (+) ramp (green)

S – Clk (violet)

Analog data **Digital**

Results: HitDetMEM 1.0



- **Input stage: to slow for our application**
- **Memory cell: reach the range: ± 1 V**
- **Sampling frequency: up to 100 MHz**
- **Integrator stage: fulfill the design requirements**

HitDetMEM 1.0 vs HitDetMEM 2.0

- **HitDetMEM 1.0:**
  - **Input stage (rail to rail design):**
    - Works in the expected range
    - ***But:*** to slow for our application
  - **Memory cell:**
    - Reach the expected range of ± 1 V
  - **Integrator:**
    - Works as expected
  - **Multiplexer:**
    - Not connected to power
    - ***But***: function test was possible
- **HitDetMEM 2.0:**
  - **Input stage:**
    - 4 new different input stage concepts are implemented
  - **Memory cell:**
    - Same as in preversion
  - **Integrator:**
    - Same as in preversion
  - **Multiplexer:**
    - Same multiplexer with power connection

Status HitDetMEM 2.0: Delivered at GSI end of January

Summary

- **Measurements of the first HitDetMEM 1.0 ASIC are finished**
- **A 2nd test ASIC HitDetMEM 2.0 was submitted with several test structures**
- **Preliminary results of second submission are expected in march 2013**

Outlook

- Hit Detection unit (Filter)
  - In the proposal of Igor Konorov: FIR filter (Fine Impulse Respond)
    - A continuous level, discrete time filter
  - FIR filter should be able to detect hits in a pile – up situation
  - Open question:
    - FIR filter necessary?
    - Which order of this filter?
    - A free configurable filter coefficient or fixed one?
- Slow control and control logic
- ADC development
  - 12 bit
  - ADC speed?
- First full HitDetection ASIC submission (maybe 2013/2014)