MTCA.4 based LLRF system using direct sampling method

Maciej Grzegrzółka

Warsaw University of Technology

Institute of Electronic Systems

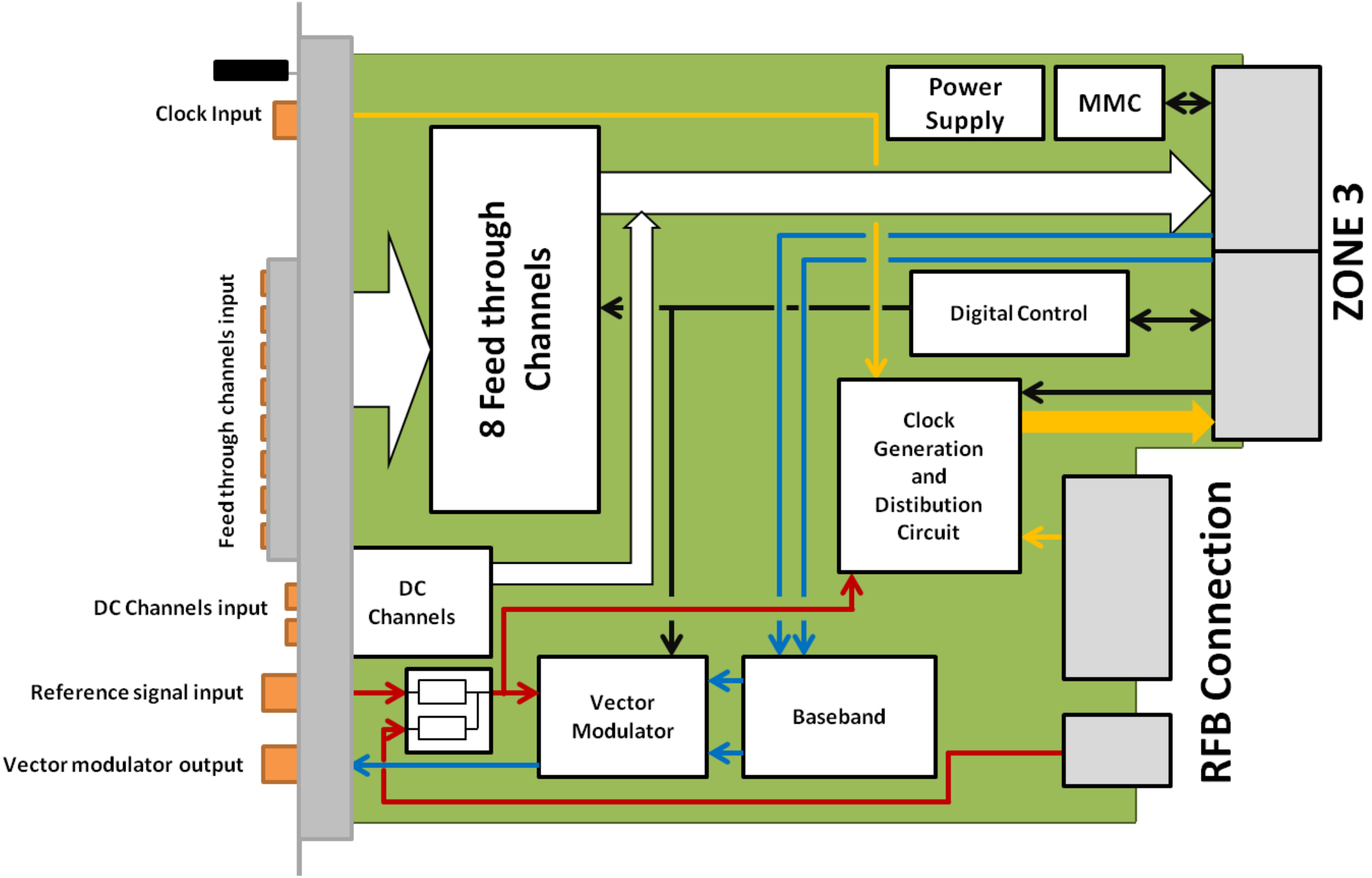
Maciej.grzegrzolka@desy.de

Igor Rutkowski, Radosław Rybaniec – Warsaw University of Technology, ISE, Warsaw
Michael Kuntzsch, Harmut Büttig, Rico Schurig - HZDR, Dresden
Hoffmann, Matthias, Schmidt, Christian – DESY, Hamburg

MTCA Workshop
DESY, 11.12.2014

HELMHOLTZ
ASSOCIATION

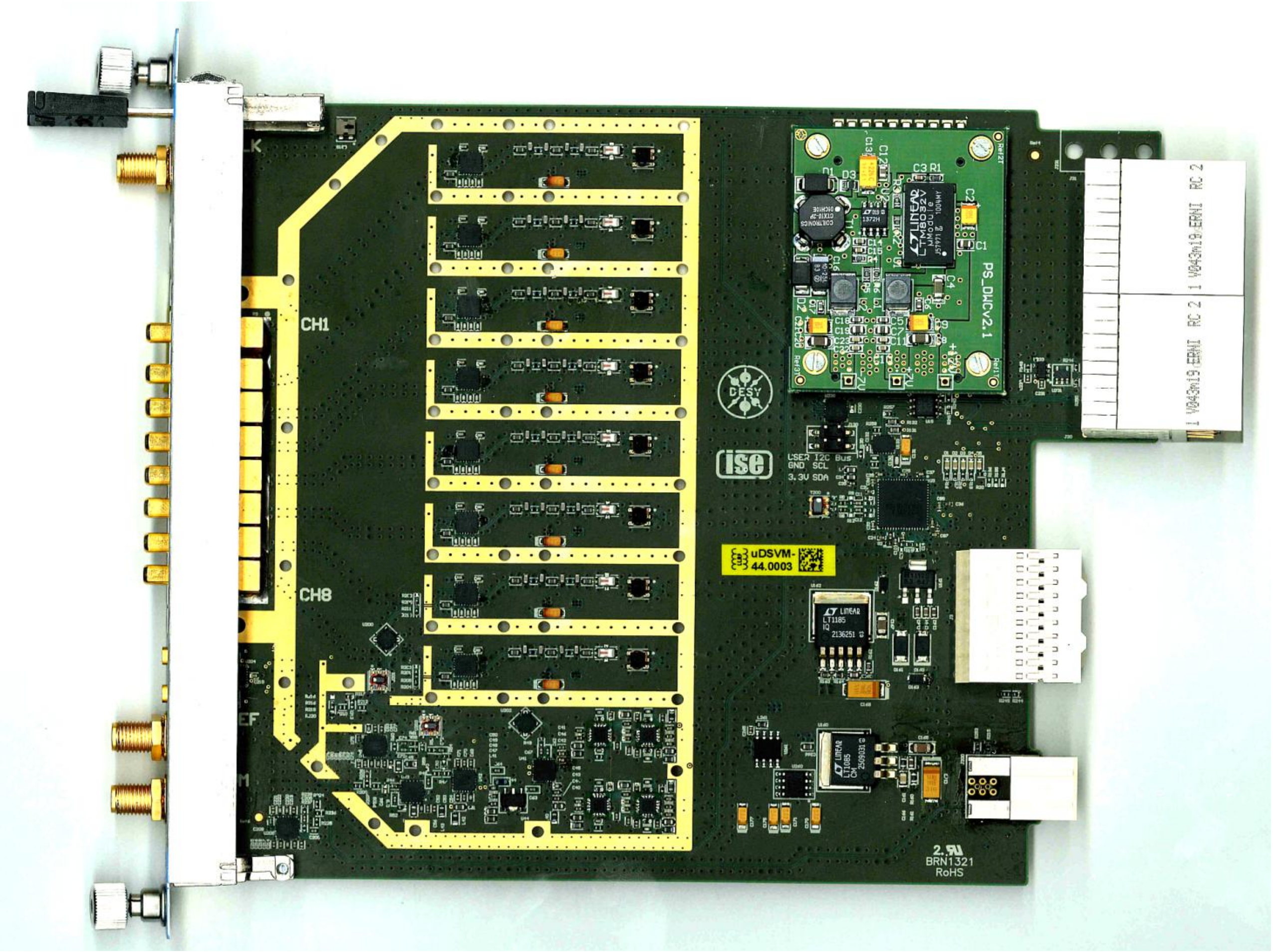
DS8VM1 Block Diagram



DS8VM1 Overview

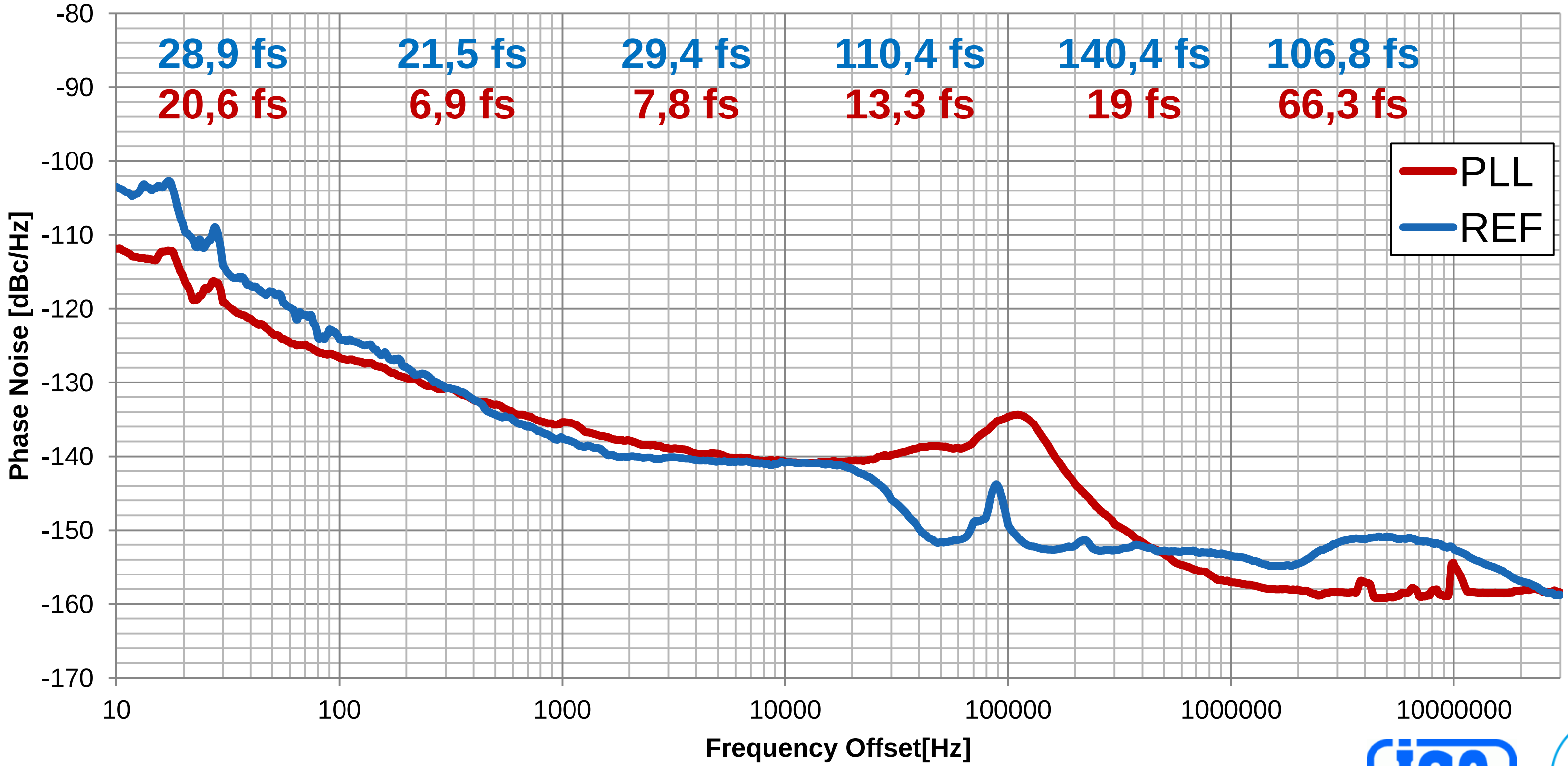
- Operation Bandwidth: 5-700 MHz
- 8 Feed through Channels
- 2 Additional DC Channels
- 1 Vector Modulator Channel
- Low-noise clock generation and distribution circuit
- DESY Analog Class Recommendation A1.1 compliant
- Compatible with RTM backplane
- Compatible with SIS8300L

DS8VM1



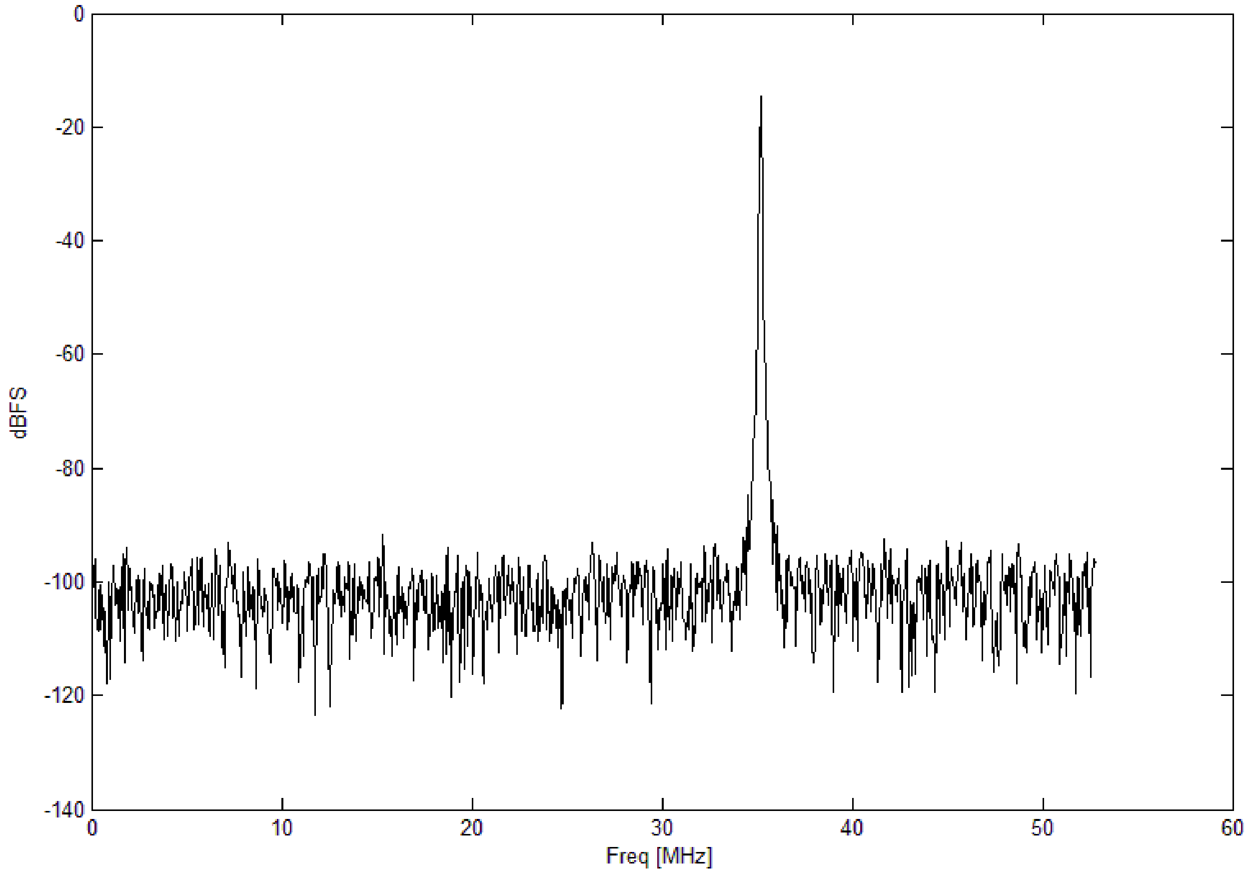
Clock generation phase noise

78 MHz clock signal generated from 260 MHz reference signal
Jitter (10 Hz – 30 MHz):
Reference: 95,8 fs
PLL: 266,9 fs



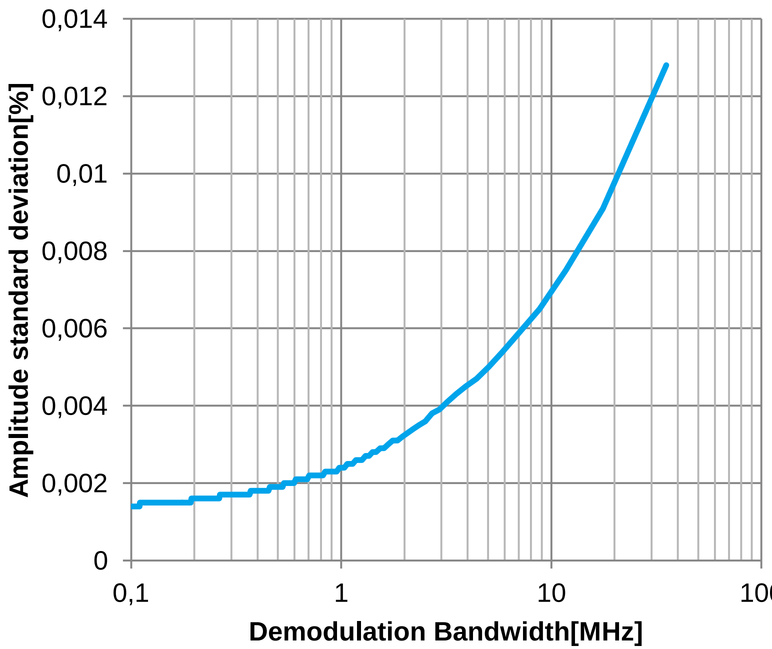
FFT

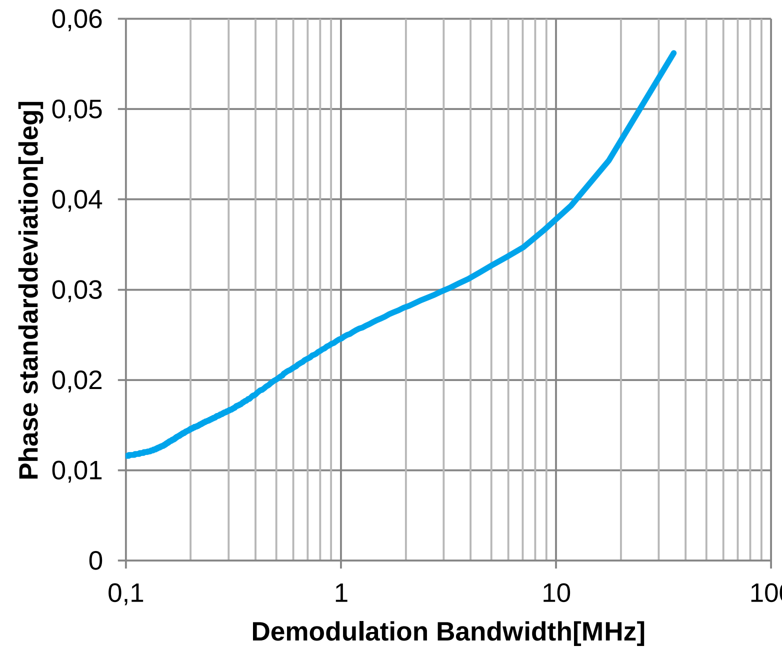
- 352MHz signal sampled with 105.6 MHz clock



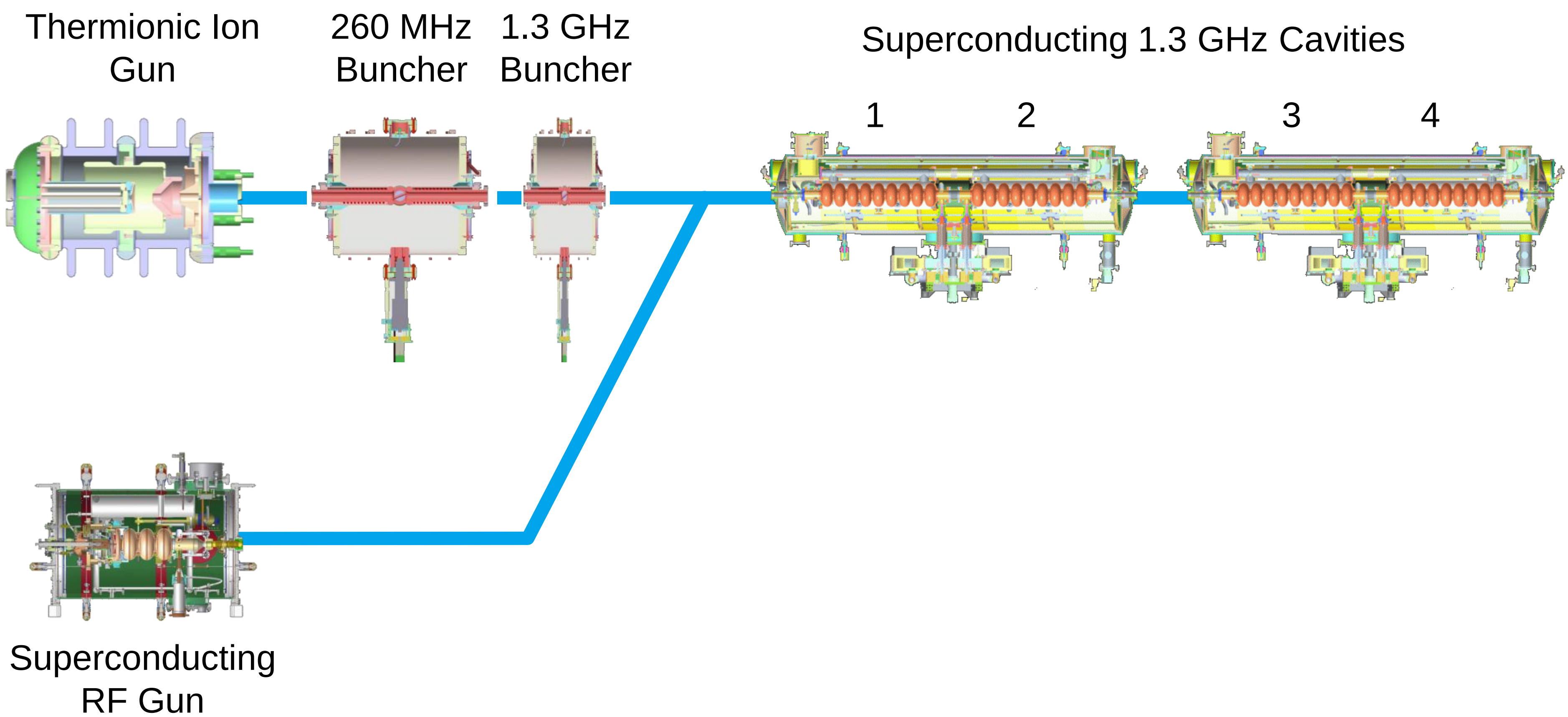
Phase and Amplitude stabilty

Demodulation bandwidth	Phase standard deviation	Amplitude standard deviation
8,8 MHz	0.0362^0(391 fs)	0.0066 %
1 MHz	0.0237^0(262 fs)	0.0022 %
100 kHz	0.0116^0(123 fs)	0.0014 %

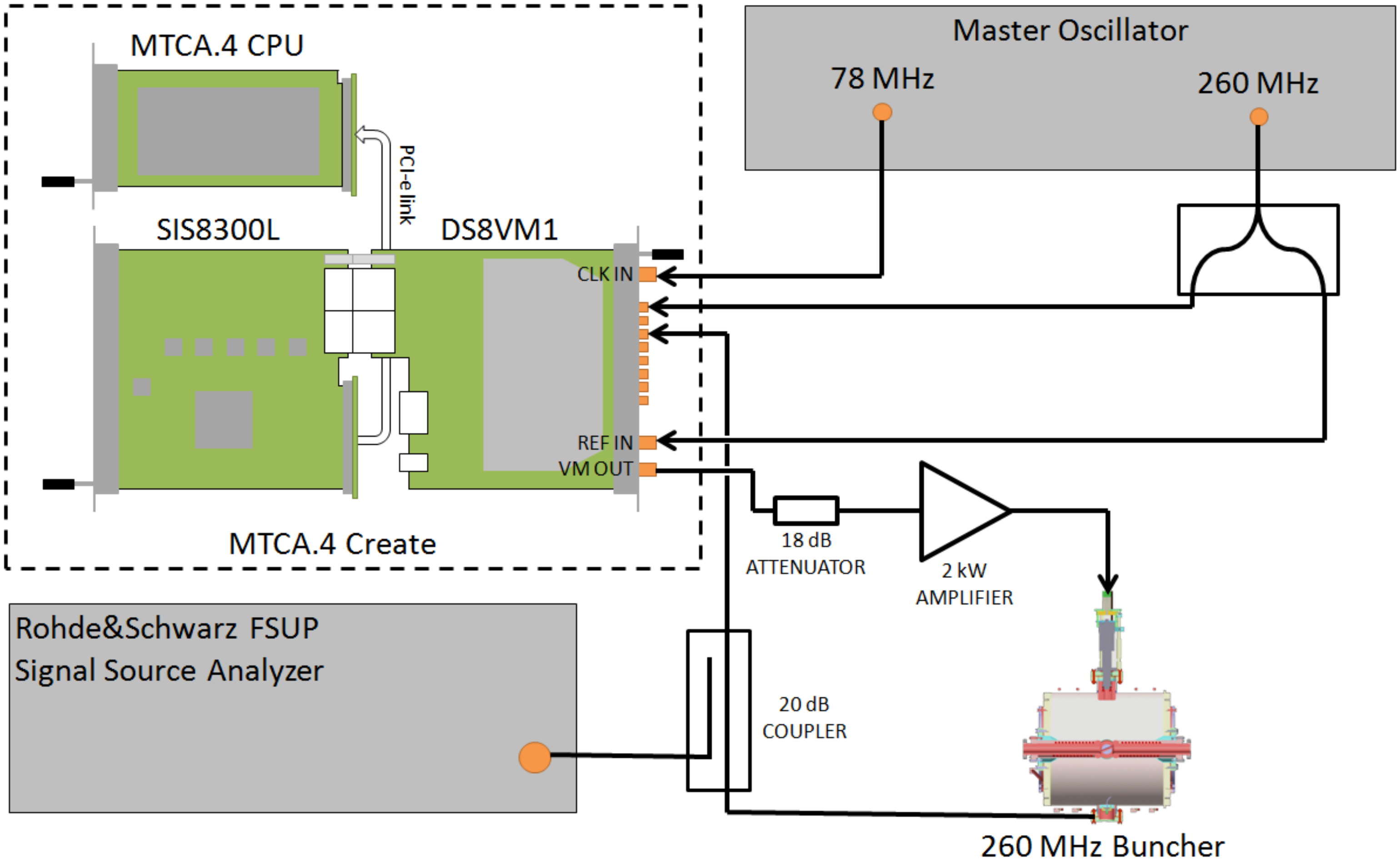


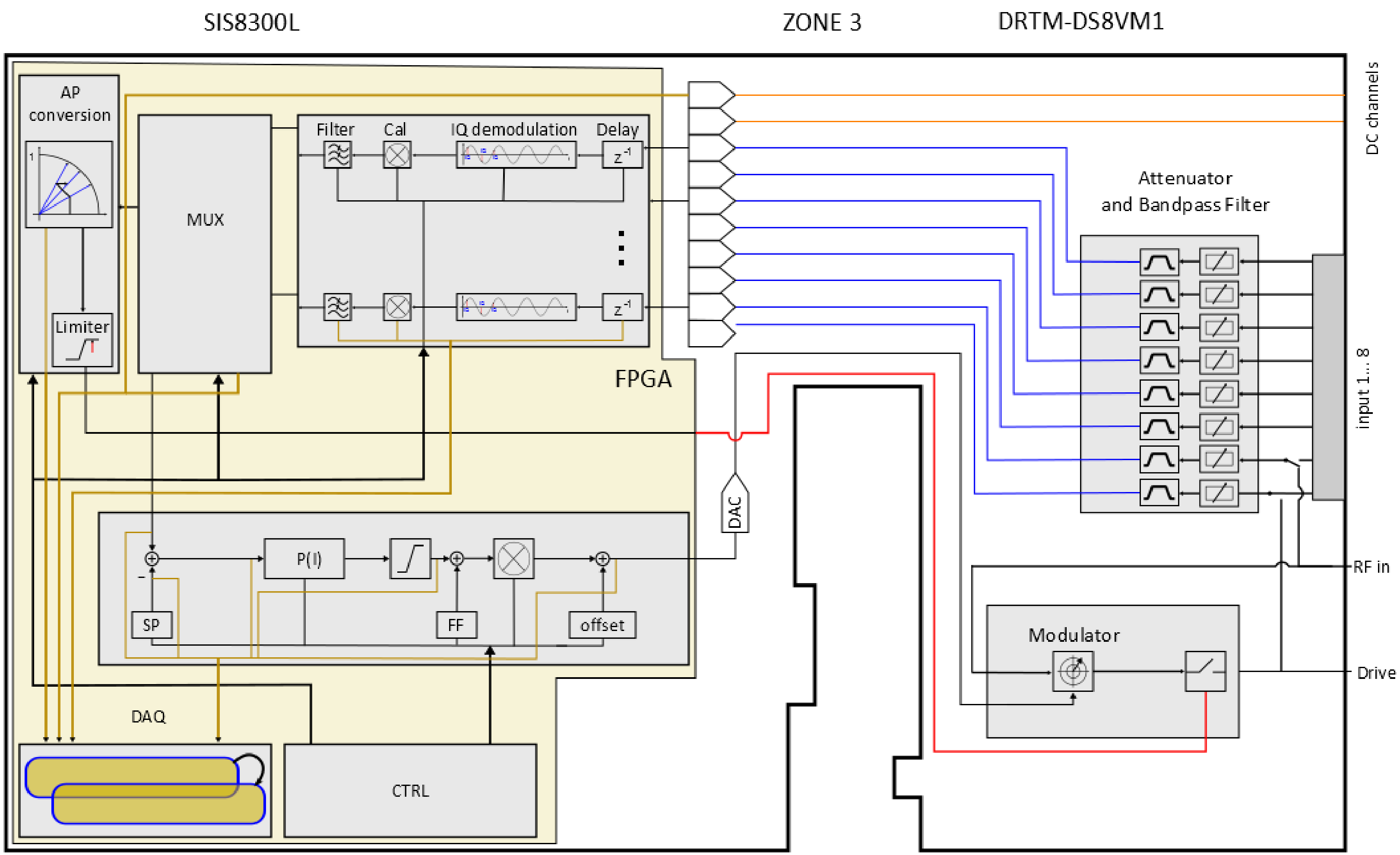


Elbe Accelerator



Test Setup

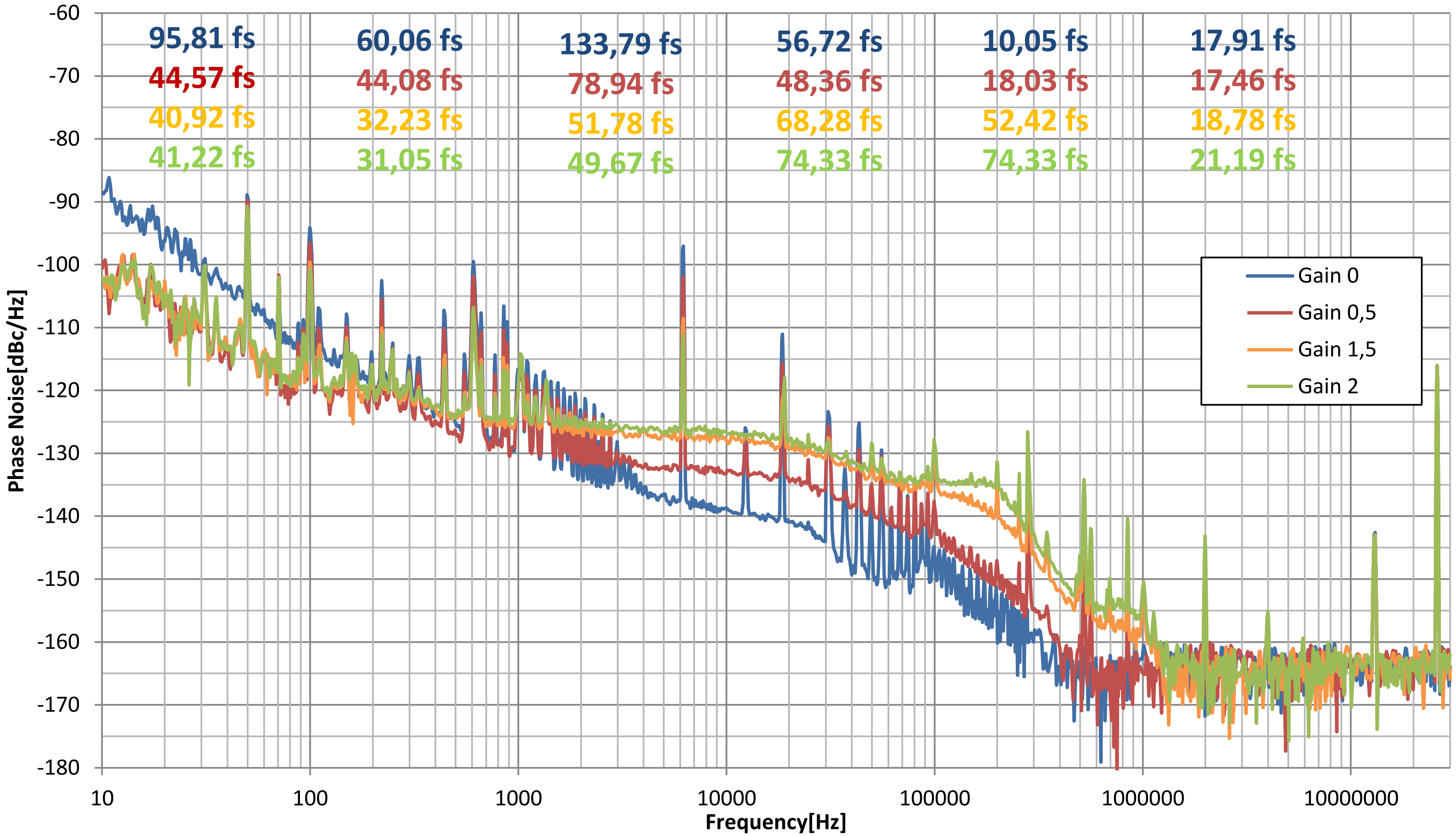

MTCA.4 CPU
PCI-e link
SIS8300L
DS8VM1
CLK IN
REF IN
VM OUT
MTCA.4 Create
Master Oscillator
78 MHz
260 MHz
18 dB
ATTENUATOR
2 kW
AMPLIFIER
Rohde&Schwarz FSUP
Signal Source Analyzer
20 dB
COUPLER
260 MHz Buncher



SIS8300L
ZONE 3
DRTM-DS8VM1
AP conversion
MUX
Filter
Cal
IQ demodulation
Delay
Limiter
FPGA
DC channels
Attenuator and Bandpass Filter
input 1… 8
DAC
P(I)
SP
FF
offset
RF in
Modulator
Drive
DAQ
CTRL

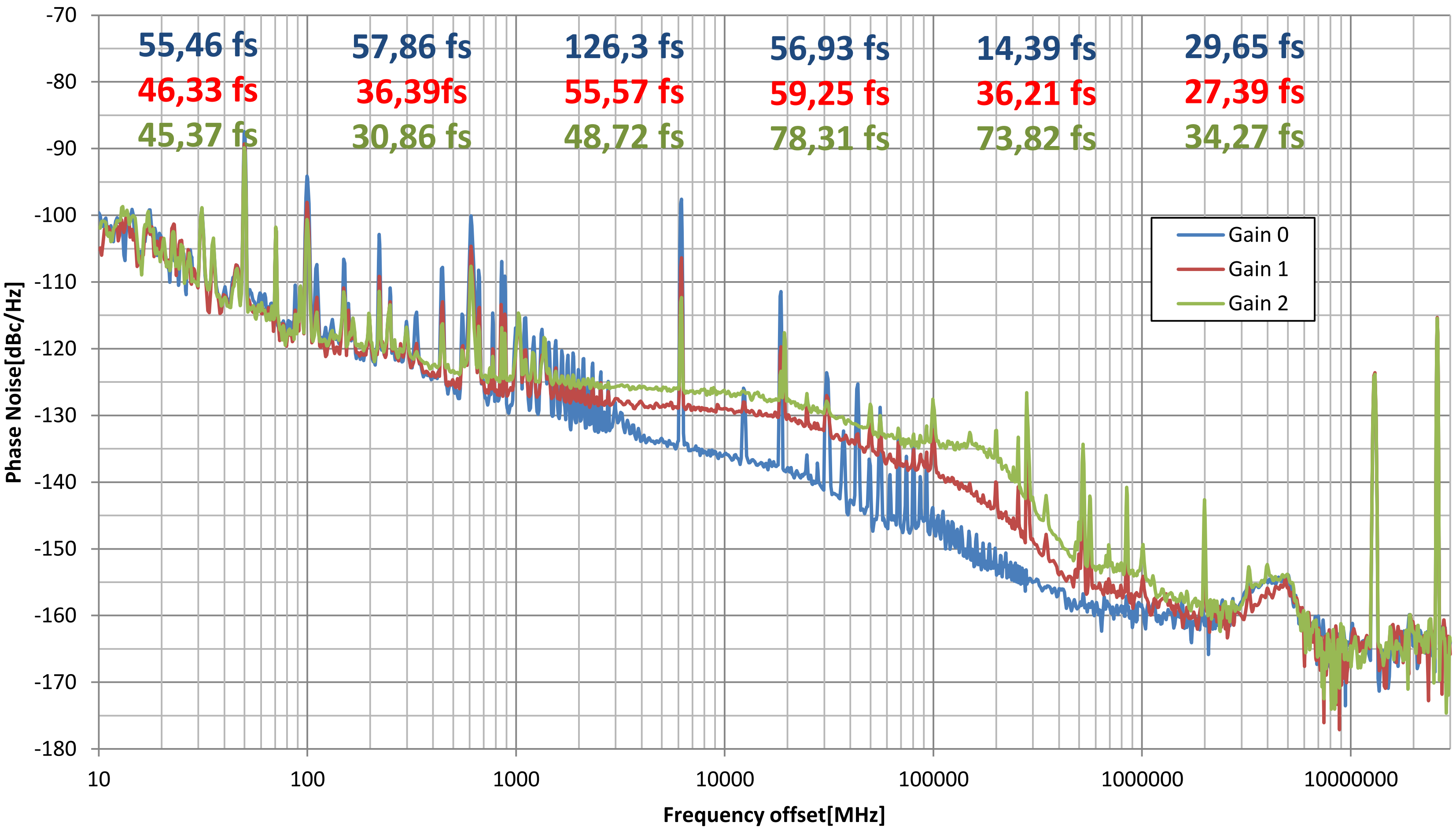
LLRF system photo

Test Results – beam off



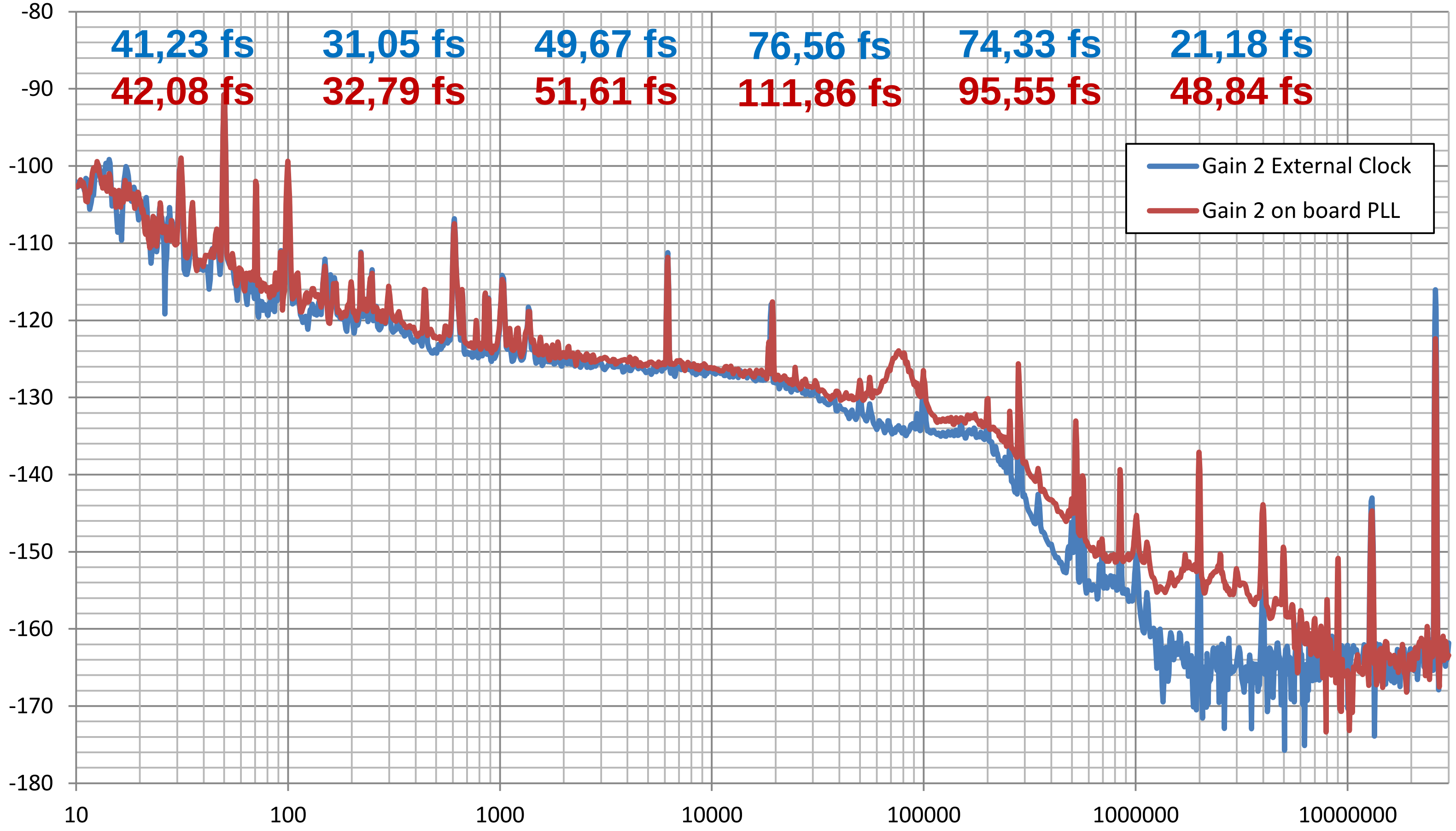
Jitter(10Hz-10 MHz): **185,3 fs 114,6 fs 114,7fs 130,25 fs**

Test Results – beam on



Jitter(10Hz-10 MHz): **163,42 fs** **110,14 fs** **134,68 fs**

External Clock and Onboard PLL Comparison



Summary

- DS8VM1 is module designed for LLRF systems using direct sampling method
- First revision was successfully tested at ELBE facility at HZDR
- Second revision should be ready soon
- New features added in second revision:
  - DC coupling option on all channels,
  - Second VCO for lower PLL jitter,
  - VM modulator bypass for 5 MHz to 50 MHz output,
  - Two precise temperature sensors (10 mK).

Thank you for attention!