

# MO components performance measurement

Stanisław Hanasz

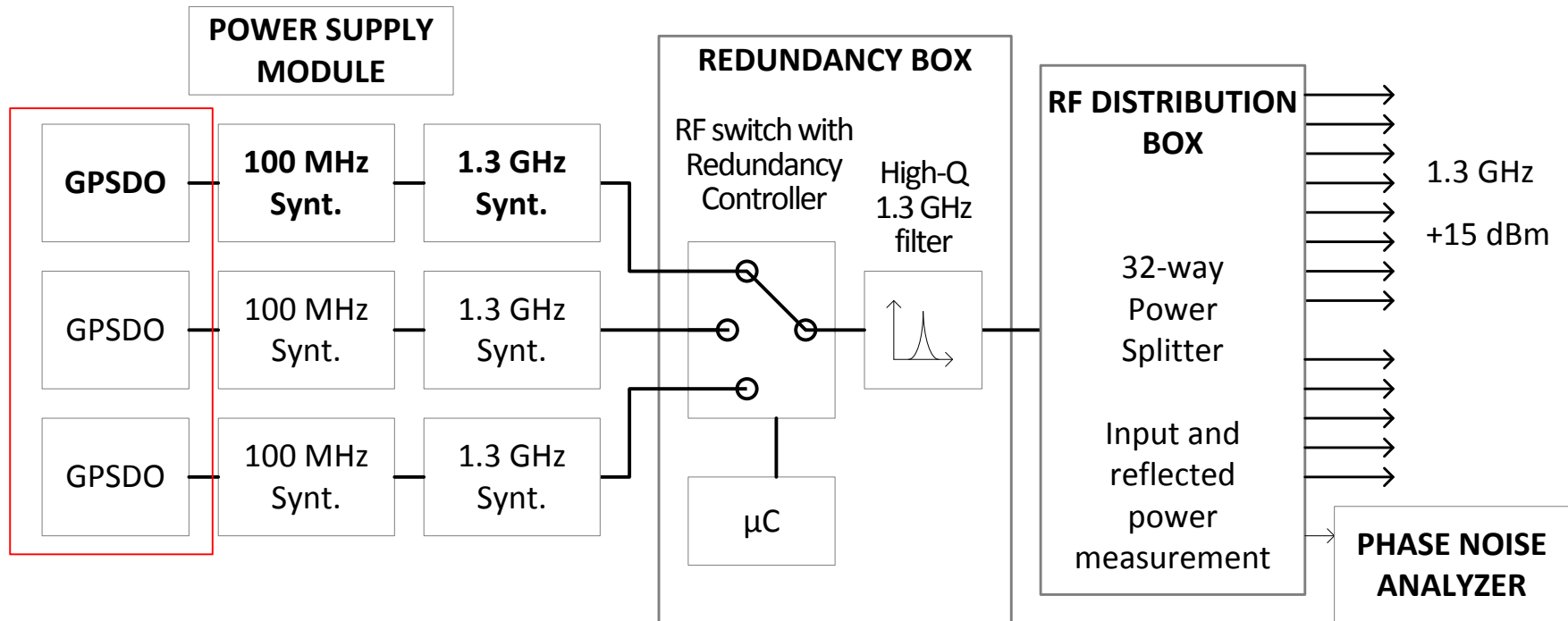
Warsaw University of Technology

Institute of Electronic Systems

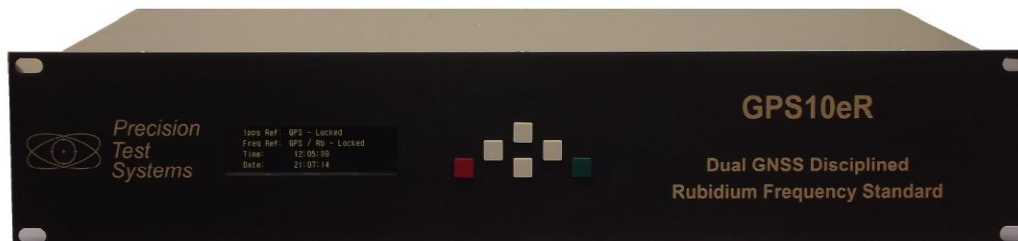
MSK Collaboration Workshop 2015

Warszawa 11.06.2015

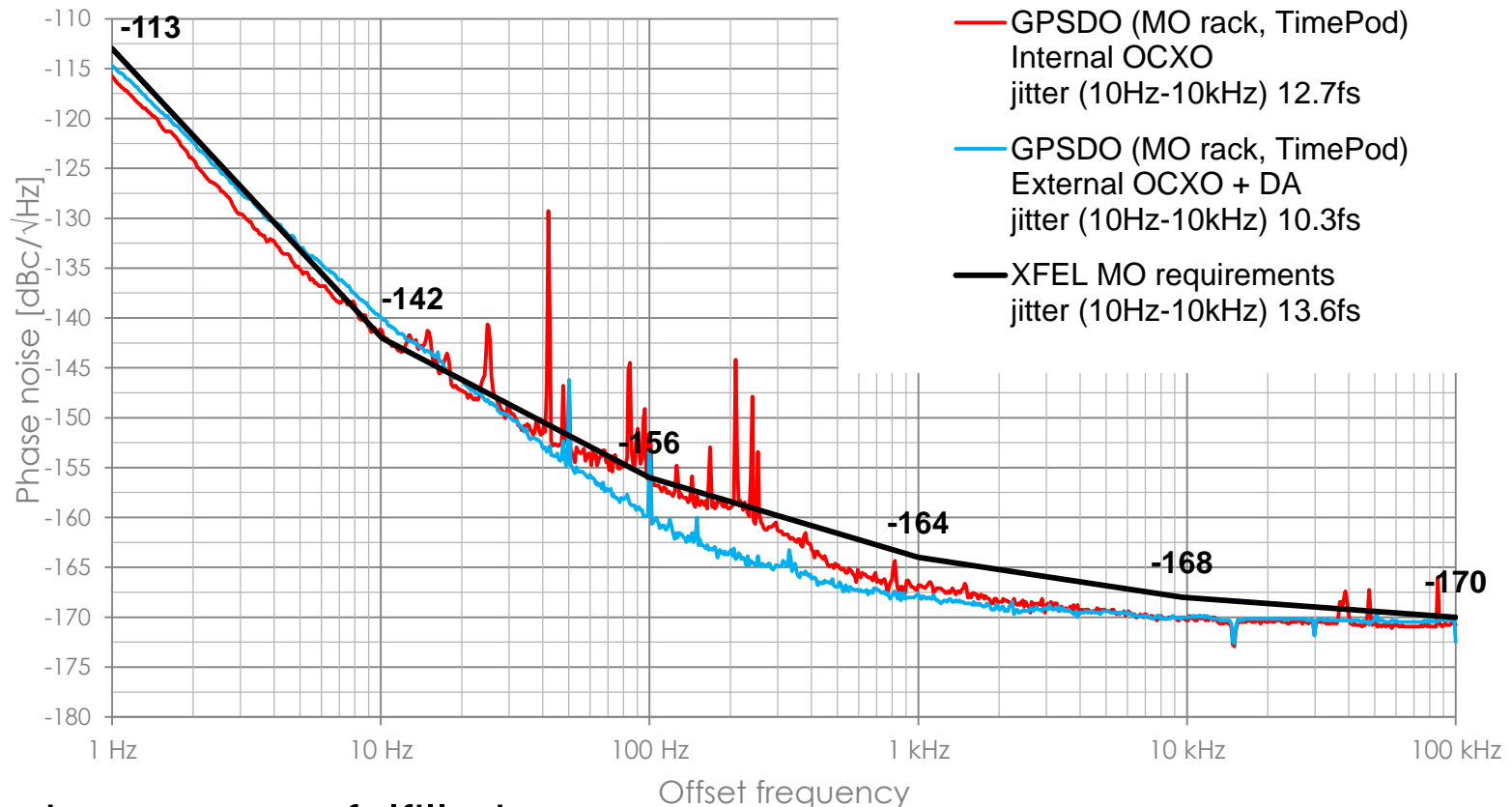
# PTSystems GPS Disciplined Oscillator



Łukasz Zembala – MO Design and Status Review – Slides, 11.06.2015

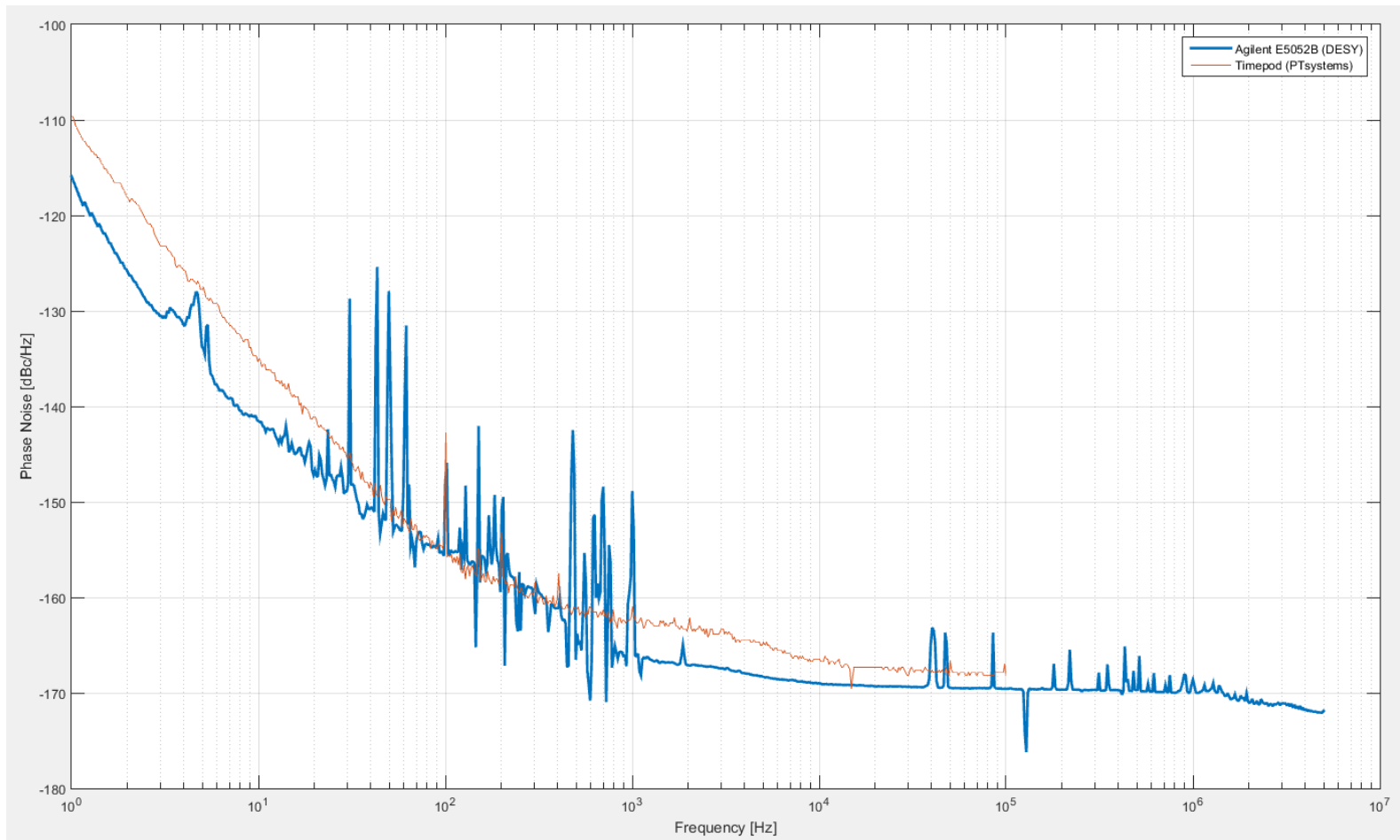


# PTSystems GPS Disciplined Oscillator



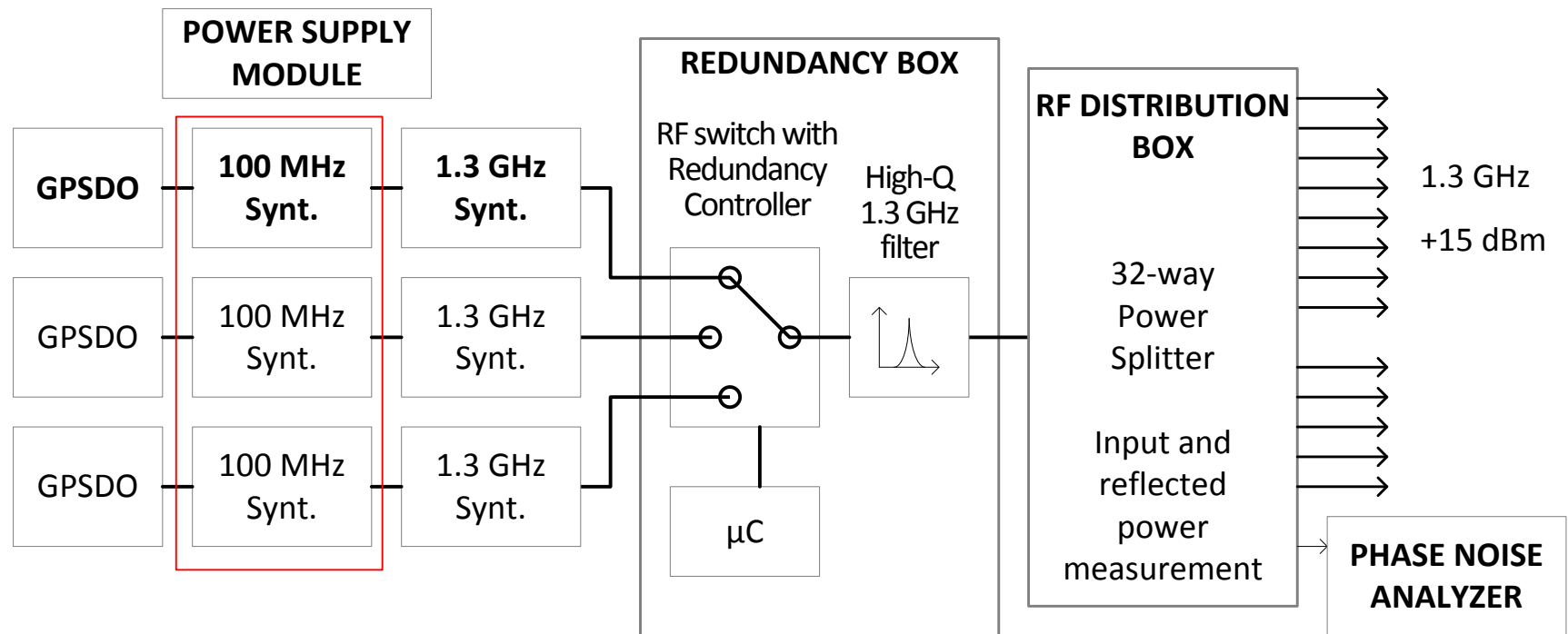
- Requirements are fulfilled.
- GPSDO phase noise will be monitored (environment impact on PN)
- External OCXO and distribution amp. increases Phase Noise performance.

# Spurious measurement problem

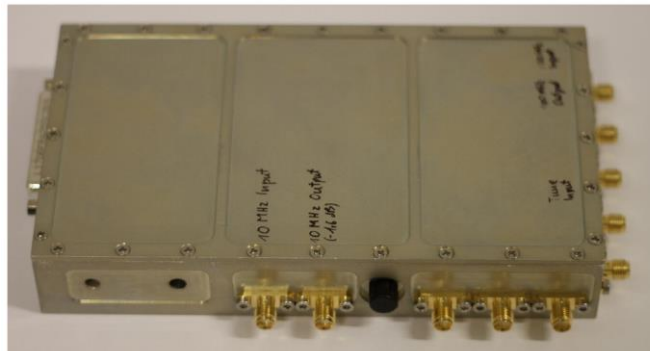


- Just 2 devices checked – Anapico and Holtzworth analyzers will be tested soon.

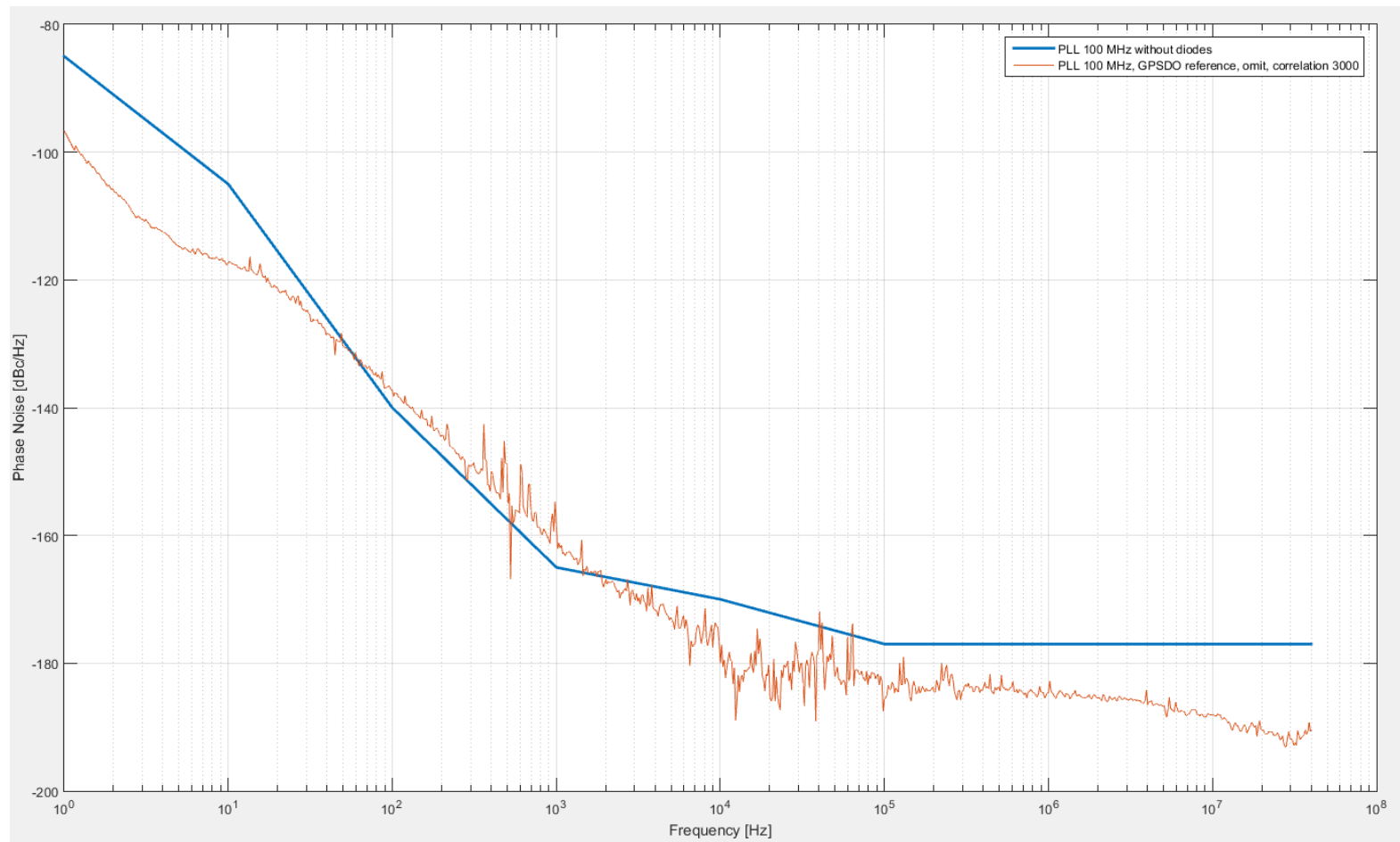
# 100 MHz Synthesiser



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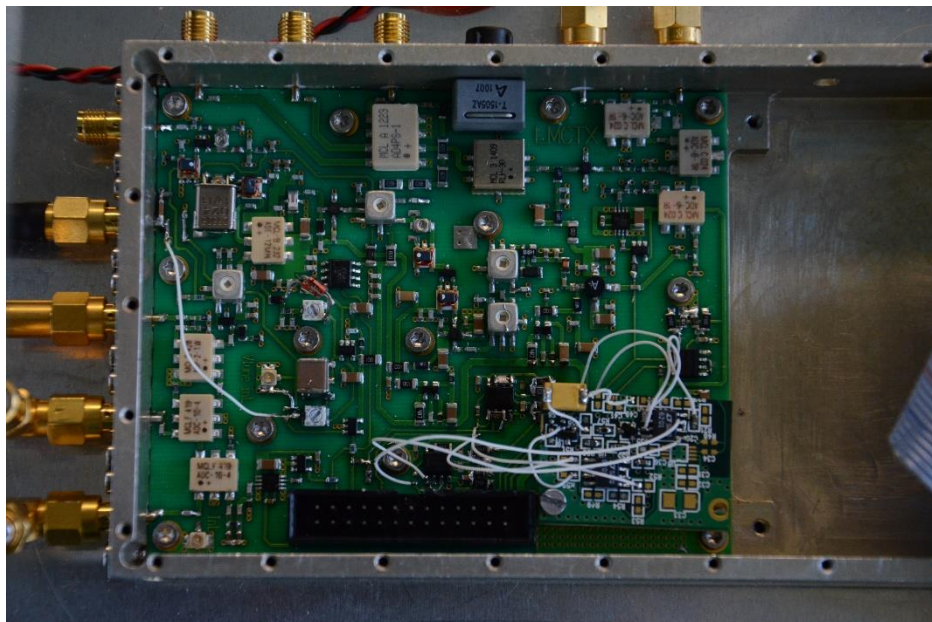
# 100 MHz Synthesiser – phase noise



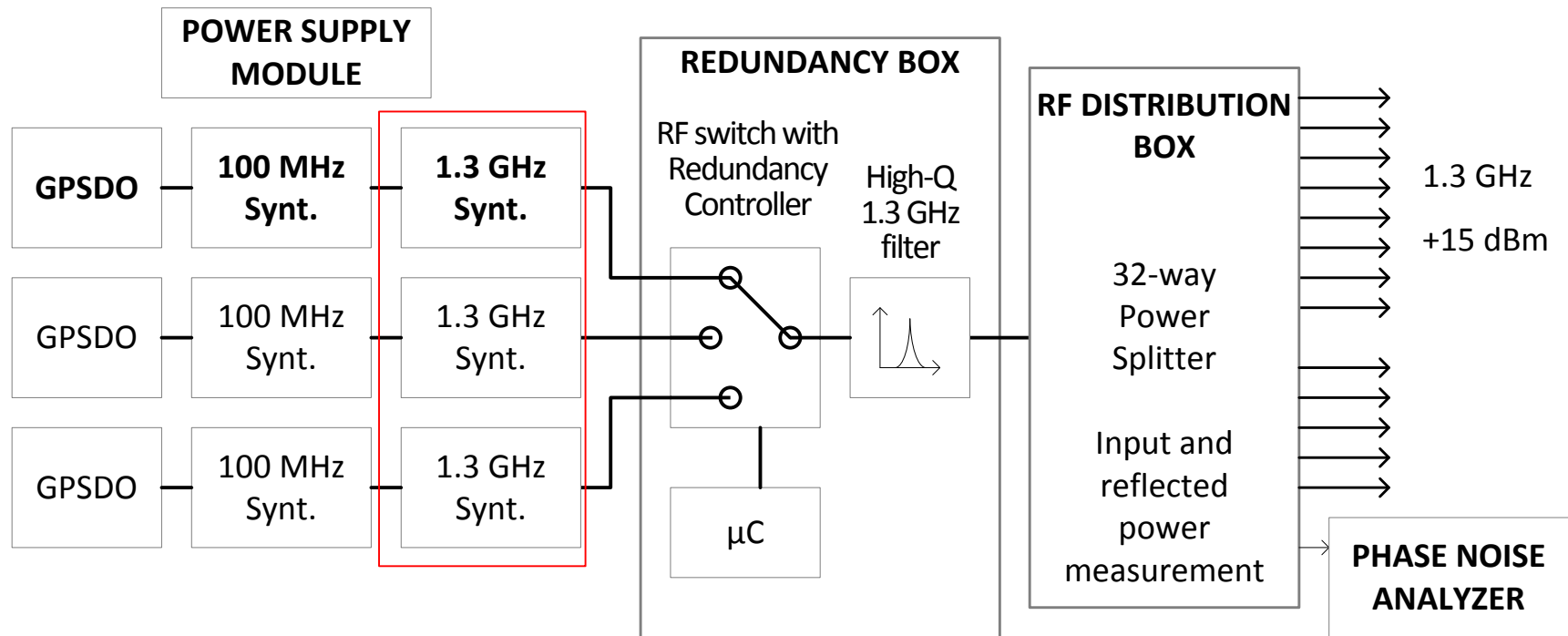
- Jitter: 11.3 fs ( 10 Hz – 1 MHz )
- Accurate loop bandwidth tuning and OCXO comparison need better SSA

# 100 MHz Synthesiser – diagnostics

- Device does not fulfill the specification:
  - RF power measurement, lock detector, TTL outputs
- Strong crosstalks were found.
- PCB is corrected and works properly.
- All errors will be corrected in 2nd revision.



# 1.3 GHz Synthesiser

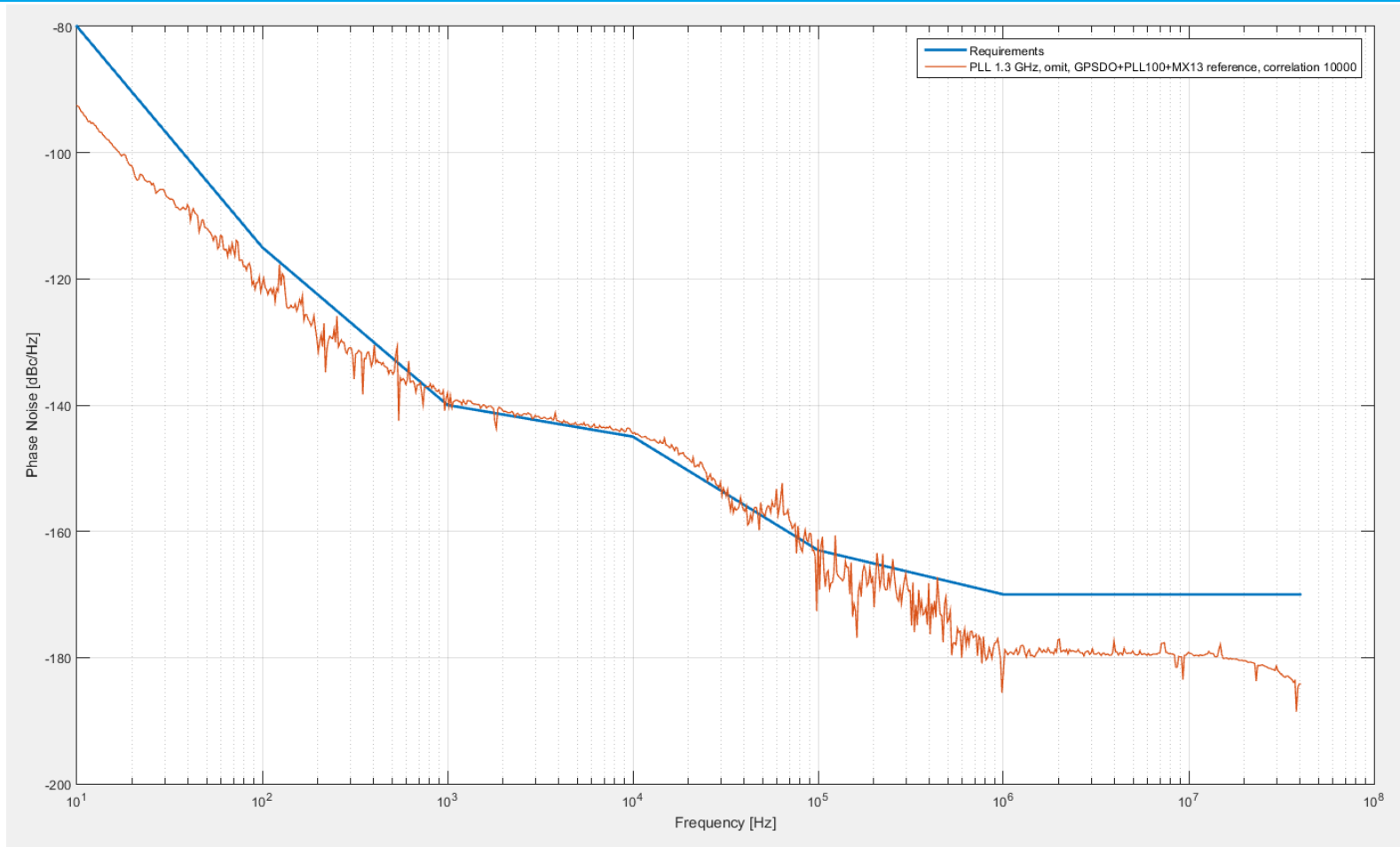


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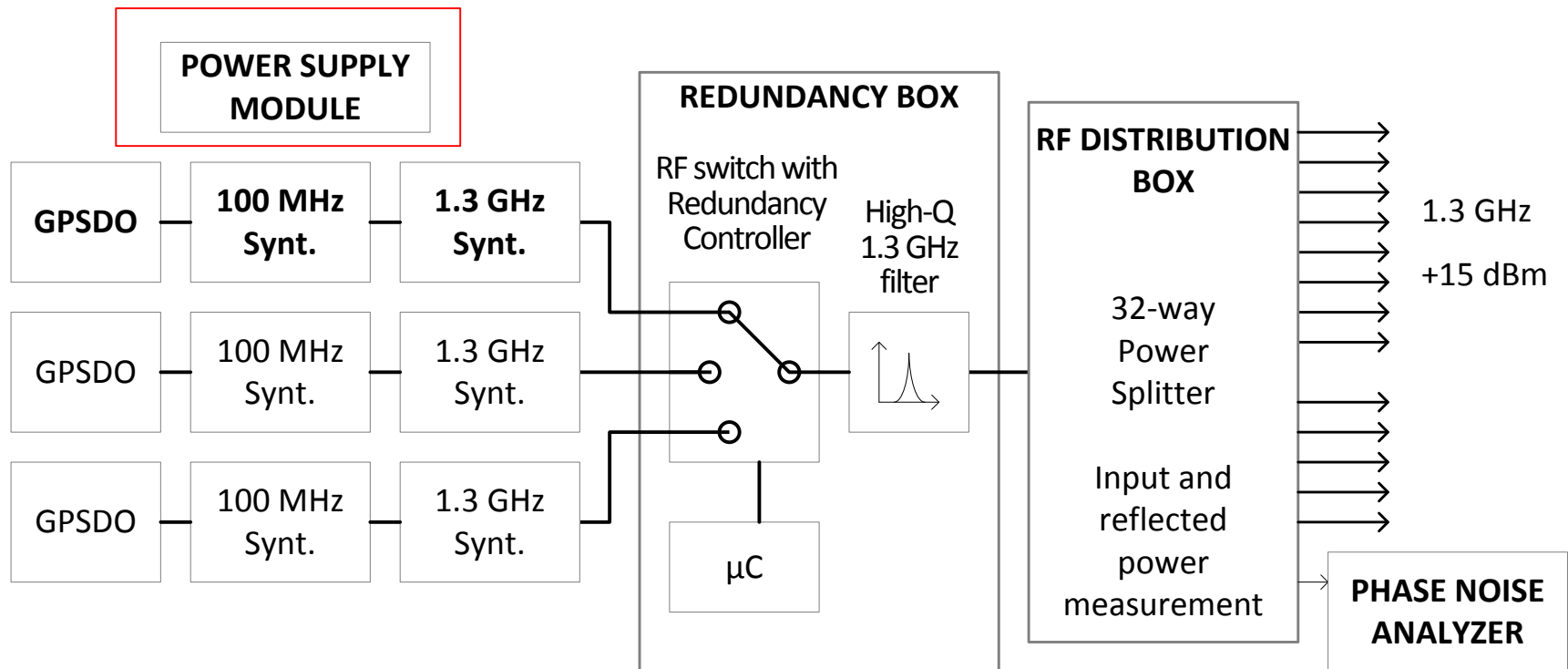


# 1.3 GHz Synthesiser

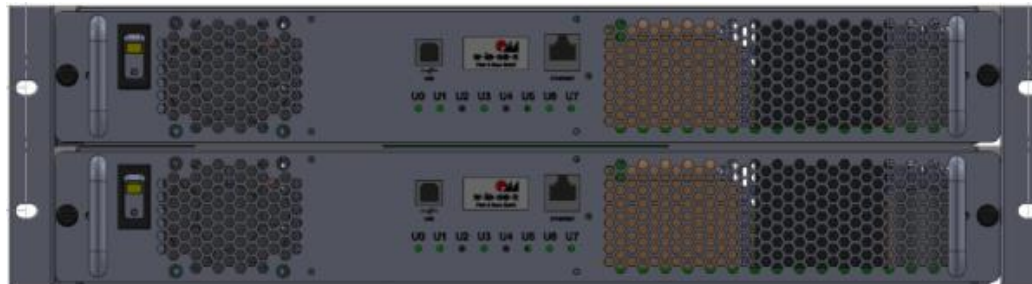


- > Jitter = 9.2fs (10Hz–1MHz)
- > Device is fully functional.

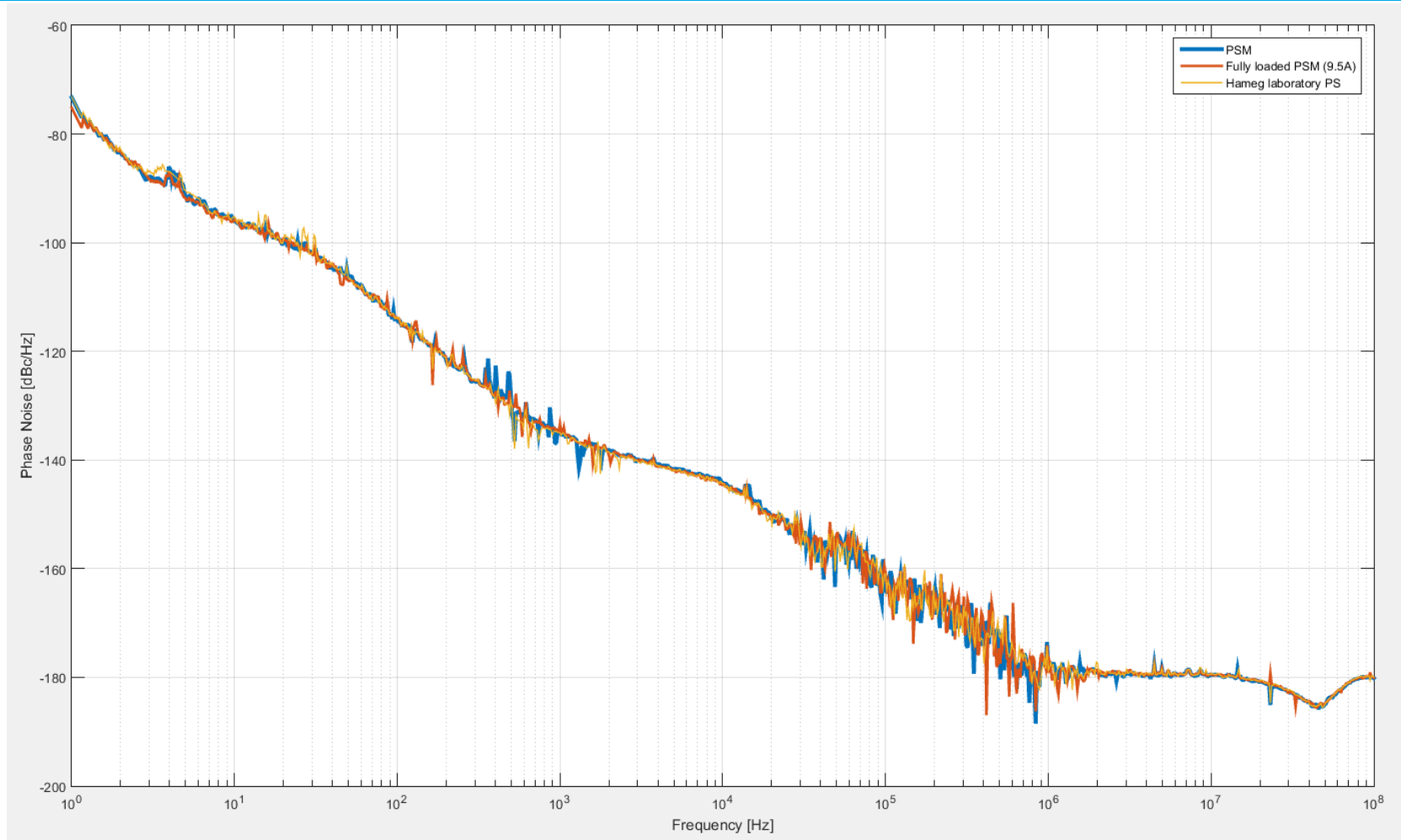
# Power Supply Module



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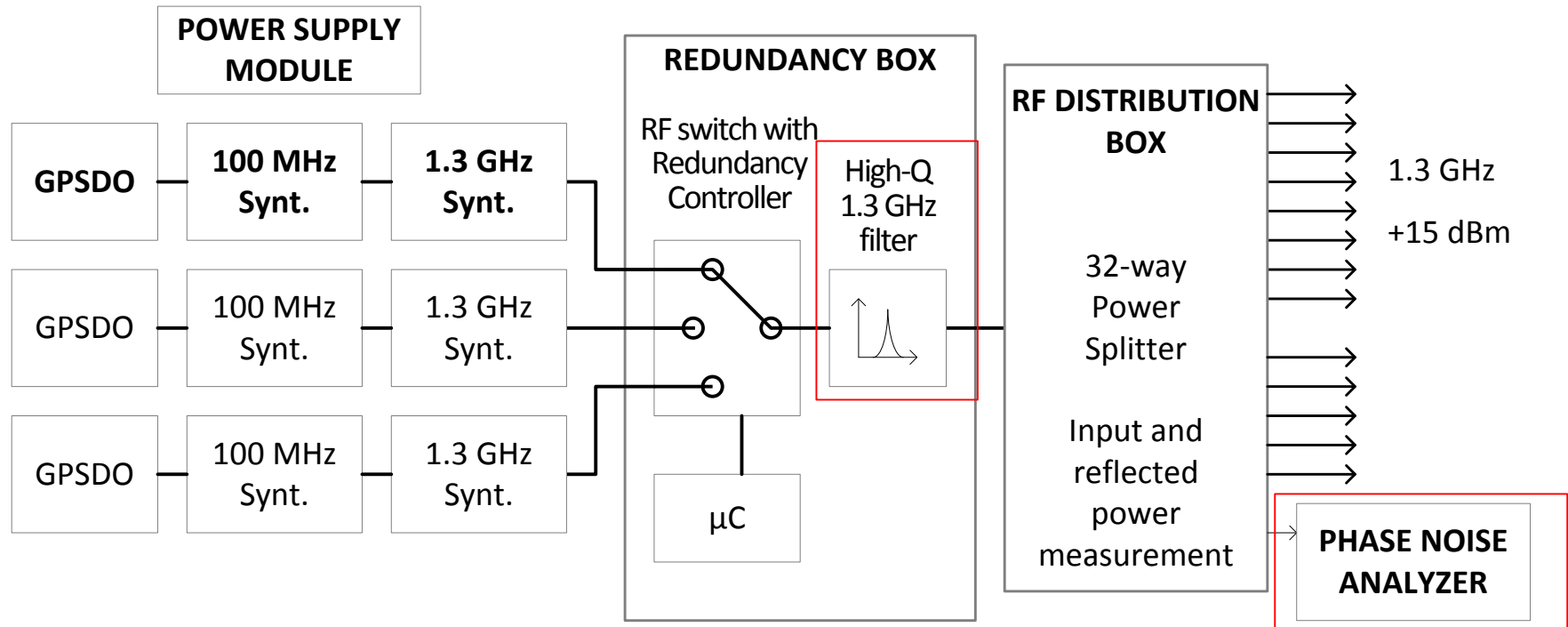


# Power Supply Module



- Better SSA is needed to check if no additional spur lines are visible using this power supply (in this plot spurs are omitted)

# Other devices



## > High Q filter:

- First module was not able to work with 50dBm power.
- Corrected module was tested for few weeks with 50 dBm input power, and no change of parameters were observed.

## > Anapico APPH6040 is actually tested for the phase noise performance.

# Future tests and measurements

- > Various SSA tests: Anapico APPH6040, Holtzworth HA7062C ~ 1 week
- > Measurements of Pascall and NEL 100 MHz OCXO's ~ 0.5 week
- > PSM impact on MO phase noise spurious ~ 0.5 week
- > Full 2nd revision PLL 100 MHz tests and phase noise optimisation ~ 2 weeks
- > High Power Amplifier measurements. ~ 1 week
- > Check of all chassis mechanical compatibility. ~ 1 week
- > Redundancy tests ~ 2 weeks
- > Assembly and tests of all 2nd and 3rd channel devices ~ 3 weeks

Estimated finish: end of september

# Thank You for Your attention.