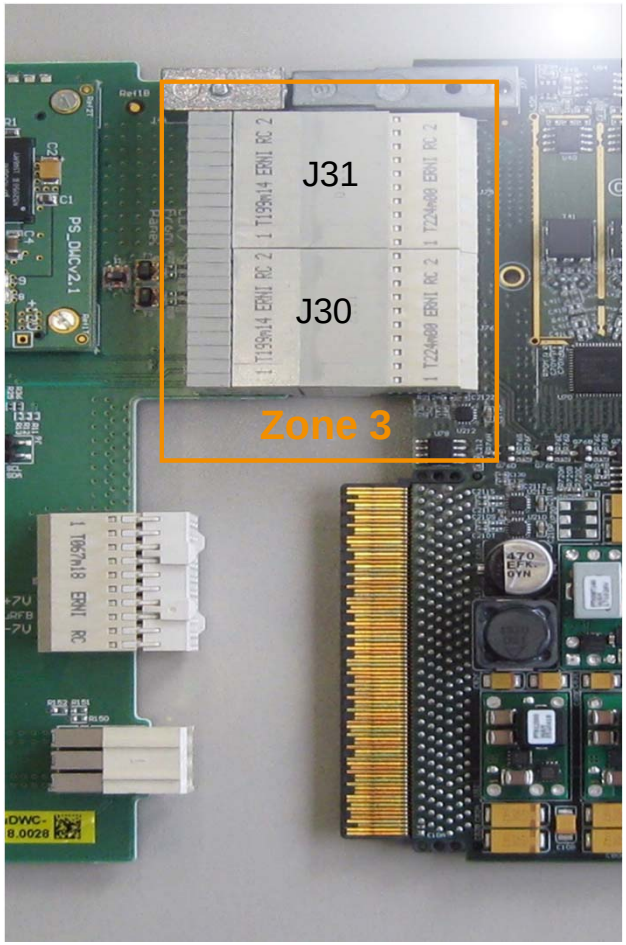
MTCA Workshop for Industry and Research



Recommendation for Zone 3 classes to achieve enhanced AMC – RTM modularity

Dr. Frank Ludwig
for the LLRF Team
Hamburg, 11.12.2012

HELMHOLTZ GEMEINSCHAFT

DESY

How can we improve the AMC – RTM compatibility ?

FIL

> Most of the existing AMC and RTM boards are not compatible :

AMCs:

Zone 3 Signal Types

RTMs:

Mainly analog signal transmission

- SIS8300_V2, SIS8300L (Struck)
- AMC520 (Vadatech)
- DAMC-DS800 (DESY MSK)
- SISxxxx 2Gsps (Struck)

Analog Signals:
Digital Signals:
(bi-directional, single, differential ended)
Low-jitter clocks
High speed links
Special signals:
(Interlock, Reset, ps-stable Timing)

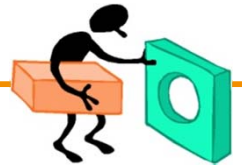
- DRTM-DWC10 (DESY MSK)
- DRTM-DWC8VM2 (DESY MSK)
- DRTM-DS800 (DESY MSK)
- BPM (DESY MDI)
- SIS8900 (Struck)
- SISxxxx 2Gsps (Struck)

Digital signal transmission

- DAMC-TC5, DRTM-TC7 (DESY MSK)
- DAMC-FMC25 (DESY MSK)
- DAMC2 (DESY FEB)
- TAMC 632 (TEWS)

Digital Signals:
(bi-directional, single, differential ended)
Low-jitter clocks
High speed links
Special signals:
(Interlock, Reset, ps-stable Timing)

- DRTM-VM2 (DESY MSK)
- DRTM-AD104 (DESY MSK)
- MPS (DESY MIN)
- DRTM-PZT4 (DESY MSK)



> . . . and approx. 10 new boards are in the HVF design pipeline . . .

Examples of incompatible AMCs and RTMs

FIL

uTC, uFMC25 (before classification) :

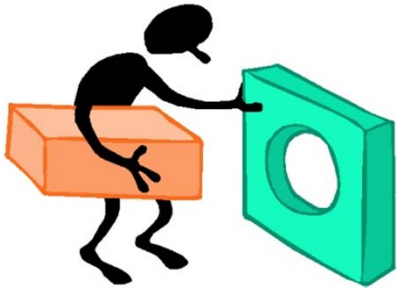
	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3	SFP1-TX+	SFP1-TX-	SFP1-RX+	SFP1-RX-	INTERLOCK 1	INTTERLOCK 2
4	SFP2-TX+	SFP2-TX-	SFP2-RX+	SFP2-RX-	RTM_D5+	RTM_D5-
5	RTM_D6+	RTM_D6-	RTM_D7+	RTM_D7-	RTM_D8+	RTM_D8-
6	RTM_D9+	RTM_D9-	RTM_D10+	RTM_D10-	RTM_D11+	RTM_D11-
7	gnd	gnd	81MHz+_O	81MHz-_O	gnd	gnd
8	gnd	gnd	RTM_CLK2+_I	RTM_CLK2-_I	MGT_CLK+_O	MGT_CLK-_O
9	URTM_CLK0+_O	URTM_CLK0-_O	gnd	gnd	SP6_CLK1+_O	SP6_CLK1-_O
10	RTM_main+_I	RTM_main-_I	gnd	gnd	gnd	gnd
1	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
2	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
3	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
4	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
5	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
6	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
7	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
8	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
9	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-
10	RTM2+	RTM2-	gnd	gnd	RTM2+	RTM2-

DAMC2:

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3	CLK_EC_RTM+_O	CLK_EC_RTM-_O	RTM1+	RTM1-	RTM1+	RTM1-
4	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
5	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
6	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
7	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
8	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
9	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
10	RTM1+	RTM1-	RTM1+	RTM1-	RTM1+	RTM1-
1	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
2	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
3	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
4	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
5	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
6	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
7	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
8	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
9	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-
10	RTM2+	RTM2-	RTM2+	RTM2-	RTM2+	RTM2-

TAM651:

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS
3	RTM_CLK0+_O	RTM_CLK0-_O	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
4	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
5	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
6	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
7	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
8	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
9	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
10	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-	RTM_30+	RTM2_30-
1	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
2	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
3	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
4	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
5	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
6	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
7	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_31+	RTM_31-
8	RTM_31+	RTM_31-	RTM_31+	RTM_31-	RTM_CLK1+_O	RTM_CLK1-_O
9	GTP1_CLK0+_I	GTP1_CLK0-_I	GTP0_Rx+	GTP0_Rx-	GTP0_Tx+	GTP0_Tx-
10	GTP1_CLK1+_I	GTP1_CLK1-_I	GTP1_Rx+	GTP1_Rx-	GTP1_Tx+	GTP1_Tx-

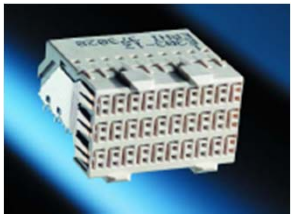


Proposal: Introduce Classes

FIL

- Recommendation – no standardization to be open for future signal types
- Class A1.1 mainly for analog signal transmission over Zone 3
- Class D1.x for digital signal transmission over Zone 3

- Requires
  - AMC FPGA module based,
  - 2 ADF 30 pair (Mid-size) connectors
  - Class A1.x and D1.x needs not to be compatible



- Supports
  - LVDS, LVCMOS, OC, CML, analog differential
  - Digital signals (single-, diff.-ended, bi-directional)
  - Analog signals
  - High-speed links
  - non-FPGA low-jitter clock signals
  - non-FPGA signals with fixed direction
  - ps-stable timing on RTMs

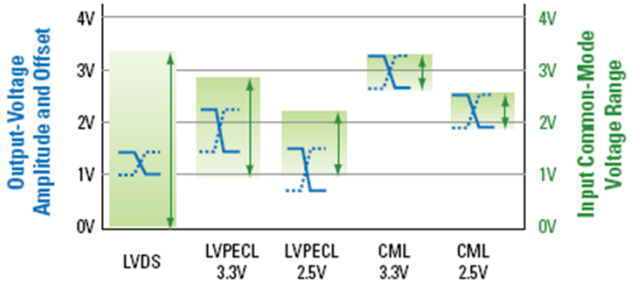


Figure 4-8. Differential Technologies

Class A1.1 (Analog signal transmission)

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> Zone 3 Pin Assignment (AMC side, Rev.A.2.):

Class A1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		3	SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
Digital fixed I/O		6	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5+
		9	RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	CH9_PA+	CH9_PA-	DAC0+	DAC0-	CH9_TF+	CH9_TF-
		2	CH8_TF+	CH8_TF-	gnd	gnd	CH8_PA+	CH8_PA-
		3	CH7_PA+	CH7_PA-	DAC1+	DAC1-	CH7_TF+	CH7_TF-
		4	CH6_TF+	CH6_TF-	gnd	gnd	CH6_PA+	CH6_PA-
		5	CH5_PA+	CH5_PA-	DAC2+	DAC2-	CH5_TF+	CH5_TF-
		6	CH4_TF+	CH4_TF-	gnd	gnd	CH4_PA+	CH4_PA-
		7	CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
		8	CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
		9	CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
		10	CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-

- MTCA.4 management
- 10 analog AC-coupled differential inputs
- 10 analog DC-coupled differential inputs
- 5 analog DC-coupled differential outputs
- 6 LVDS inputs for low-jitter clock signals
- 6 LVDS inputs / outputs
- 3 LDVS outputs
- Dual high-speed link support

Class A1.1 (Analog signal transmission)

FIL

> Zone 3 Electrical Specification (AMC side, Rev.A.2.):

Class A1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		3	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
User-configuration		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
Digital fixed I/O		6	LDVS - O	LDVS - O	LDVS - O	LDVS - O	LDVS - O	LDVS - O
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	LDVS - I	LDVS - I	LDVS - I *	LDVS - I *	LDVS - I	LDVS - I
		9	LDVS - I *	LDVS - I *	LDVS - I *	LDVS - I *	LDVS - I *	LDVS - I *
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		2	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		3	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		4	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		5	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		6	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		7	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		8	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		9	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		10	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	

- Logic levels : LVDS, LVCMOS, OC, CML, *= CW signals (TBD)
- Signal direction : „I“=input (RTM to AMC) „O“=output (AMC to RTM)
- Fixed output direction : DACx outputs, AMC_TCLK, OUT1, OUT2, SFP

Quiescent Condition

Class A1.1 (Analog signal transmission)

FIL

> Zone 3 Quiescent condition (AMC side, Rev.A.2.):

Class A1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Standard Gbit-Link		3			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
User-configuration		4	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
Digital fixed I/O		6	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
Shielding		7						
Digital clock inputs		8						
		9						
Shielding		10						
Analog signals	J31	1			DAC quiescent condition	DAC quiescent condition		
		2						
		3			DAC quiescent condition	DAC quiescent condition		
		4						
		5			DAC quiescent condition	DAC quiescent condition		
		6						
		7			DAC quiescent condition	DAC quiescent condition		
		8						
		9			DAC quiescent condition	DAC quiescent condition		
		10						

- Idle-state, AC-coupled : Idle-stated by FPGA, AC-coupled transceivers on AMC and RTM
- Disabling via FPGA : Tri-stated initiated by MMC
- Disbaling via buffer : Disabling via buffer controlled by MMC
- DACx quiesence : Output to zero current or voltage, power down mode

Class D1.0 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.2.):

Class D1.0 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
User -configuration		3	P30_IO+ / CC	P30_IO- / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		4	P30_IO+ / CC	P30_IO- / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		5	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		8	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		9	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User -configuration	J31	1	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		6	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		7	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		9	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		10	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-

D1.0 Subclass :

- MTCA.4 management
- 54 LVDS inputs / outputs

(+) High compatibility, also to existing boards

(-) No High-speed link support
(-) No support of low-jitter clocks
(-) No support of non-FPGA output signals

Class D1.1 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.2.):

Class D1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	RTM_CLK1+	RTM_CLK1-	AMC_TCLK+	AMC_TCLK-	OUT2+	OUT2-
		4	AMC_CLK1+	AMC_CLK1-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		8	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		9	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		6	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		7	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		9	GTP0-1_CLK_IN+	GTP0-1_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-1_CLK_OUT+	GTP0-1_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.1 Subclass :

- MTCA.4 management — ( ) Moderate compatibility
- 42 LVDS inputs / outputs
- 2 High-speed links — (+) High-speed link support
- 2 LVDS signals for low-jitter clocks — (+) Support of low-jitter clocks
- 4 LVDS outputs — (+) Support of non-FPGA output signals

Class D1.2 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.2.):

Class D1.2 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	RTM_CLK1+	RTM_CLK1-	AMC_TCLK+	AMC_TCLK-	OUT2+	OUT2-
		4	AMC_CLK1+	AMC_CLK1-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		8	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		9	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		6	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		7	P31_IO+	P31_IO-	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+	P31_IO-	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.2 Subclass :

- MTCA.4 management
- 38 LVDS inputs / outputs
- 4 High-speed links
- 2 LVDS signals for low-jitter clocks
- 4 LVDS outputs

( ) Moderate compatibility

(+) High-speed link support
(+) Support of low-jitter clocks
(+) Support of non-FPGA output signals

Class D1.3 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.2.):

Class D1.3 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	RTM_CLK1+	RTM_CLK1-	AMC_TCLK+	AMC_TCLK-	OUT2+	OUT2-
		4	AMC_CLK1+	AMC_CLK1-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		8	P30_IO+ / CC	P30_IO+ / CC	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		9	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		3	P31_IO+	P31_IO-	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4	P31_IO+	P31_IO-	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5	GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6	GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7	P31_IO+	P31_IO-	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+	P31_IO-	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.3 Subclass :

- MTCA.4 management
- 28 LVDS inputs / outputs
- 8 High-speed links
- 2 LVDS signals for low-jitter clocks
- 4 LVDS outputs

( ) Moderate compatibility

(+) High-speed link support
(+) Support of low-jitter clocks
(+) Support of non-FPGA output signals

Class D1.4 (Digital signal transmission)

FIL

> Zone 3 Pin Assignment (AMC side, Rev.A.2.):

Class D1.4 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	RTM_CLK1+	RTM_CLK1-	AMC_TCLK+	AMC_TCLK-	OUT2+	OUT2-
		4	AMC_CLK1+	AMC_CLK1-	OUT0+	OUT0-	OUT1+	OUT1-
Standard Gbit-Links		5	P30_IO+	P30_IO-	GTP15_RX+	GTP15_RX-	GTP15_TX+	GTP15_TX-
		6	P30_IO+	P30_IO-	GTP14_RX+	GTP14_RX-	GTP14_TX+	GTP14_TX-
		7	GTP12-15_CLK_IN+	GTP12-15_CLK_IN-	GTP13_RX+	GTP13_RX-	GTP13_TX+	GTP13_TX-
		8	GTP12-15_CLK_OUT+	GTP12-15_CLK_OUT-	GTP12_RX+	GTP12_RX-	GTP12_TX+	GTP12_TX-
		9	P30_IO+	P30_IO-	GTP11_RX+	GTP11_RX-	GTP11_TX+	GTP11_TX-
		10	P30_IO+	P30_IO-	GTP10_RX+	GTP10_RX-	GTP10_TX+	GTP10_TX-
Standard Gbit-Links	J31	1	GTP8-11_CLK_IN+	GTP8-11_CLK_IN-	GTP9_RX+	GTP9_RX-	GTP9_TX+	GTP9_TX-
		2	GTP8-11_CLK_OUT+	GTP8-11_CLK_OUT-	GTP8_RX+	GTP8_RX-	GTP8_TX+	GTP8_TX-
		3	P31_IO+	P31_IO-	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4	P31_IO+	P31_IO-	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5	GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6	GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7	P31_IO+	P31_IO-	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+	P31_IO-	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.4 Subclass :

- MTCA.4 management — ( ) Moderate compatibility
- 16 LVDS inputs / outputs
- 8 High-speed links — (+) High-speed link support
- 2 LVDS signals for low-jitter clocks — (+) Support of low-jitter clocks
- 4 LVDS outputs — (+) Support of non-FPGA output signals

Zone 3 Grounding and Signal Isolation

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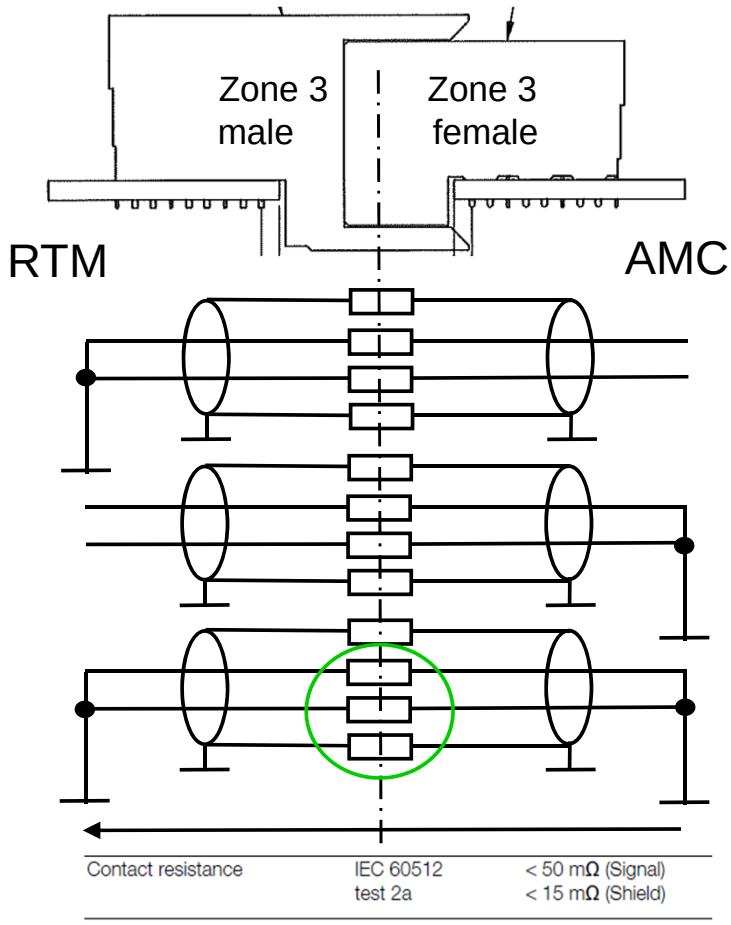
> Class A1.1: Grouding is essential !

- Improves signal isolation
- Improves signal isolation
- Improves signal isolation and robustness to EMI currents crossing Zone 3



> Class D1.x: To achieve a high compatibility

- Unused AMC FPGA pins should be not connected (NC) on the RTM side

Todo List . . .

FIL

- D1.x: - Subclasses cross compatibility has to checked
  - Remove D1.1 ? , Change filling sequence in D1.0 ?
- A1.1: Grounding for not used AMC functions to improve GND-GND, e.g.
  - DACx -> voltage outputs allowed ?
  - AC, DC-inputs, mixed mode -> power down, zero output, (isolation) or functional comparison
  - RTM_CLKx -> power down, disabling or functional comparison

  RTM disable options have to be investigated.
- Class comparison or simplified E-keying implementation
- Other classes, X2Timer, CPU, MCH, eRTMs . . .
- Misusage of digital ADF in A1.1: -> „Analog“ ADF connector for A1.1.

- A1.1 except minor things is in a pretty good state
- Continue process with a working group of experts (ASAP) . . .

Thanks for your attention!

MTCA.4 Standard: Zone 3 Connector

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MTCA.4 uses ADF connector:

- ADF 20 Pair (Mid-size)
- **ADF 30 Pair (Mid-size)**
- ADF 40 Pair (Full-size)

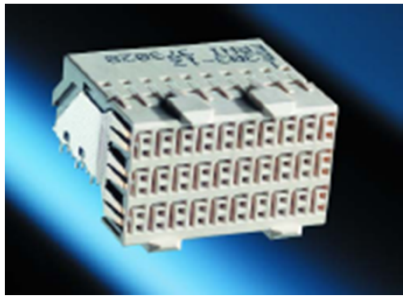

Table 2-5: J30/RP30 Pin Assignments

Col→ Row↓	GndH	H	G	GndF	F	E	GndD	D	C	GndB	B	A
10	GNDH10	H10	G10	GNDF10	F10	E10	GNDD10	D10	C10	GNDB10	B10	A10
9	GNDH9	H9	G9	GNDF9	F9	E9	GNDD9	D9	C9	GNDB9	B9	A9
8	GNDH8	H8	G8	GNDF8	F8	E8	GNDD8	D8	C8	GNDB8	B8	A8
7	GNDH7	H7	G7	GNDF7	F7	E7	GNDD7	D7	C7	GNDB7	B7	A7
6	GNDH6	H6	G6	GNDF6	F6	E6	GNDD6	D6	C6	GNDB6	B6	A6
5	GNDH5	H5	G5	GNDF5	F5	E5	GNDD5	D5	C5	GNDB5	B5	A5
4	GNDH4	H4	G4	GNDF4	F4	E4	GNDD4	D4	C4	GNDB4	B4	A4
3	GNDH3	H3	G3	GNDF3	F3	E3	GNDD3	D3	C3	GNDB3	B3	A3
2	GNDH2	H2	G2	GNDF2	TMS	TDI	GNDD2	SCL	MP	GNDB2	PWRB2	PWRA2
1	GNDH1	H1	G1	GNDF1	TDO	TCK	GNDD1	SDA	PS#	GNDB1	PWRB1	PWRA1
							20 Pair ADF Connector					
							30 Pair ADF Connector					
							40 Pair ADF Connector					

Table 2-6: J31/RP31 Pin Assignments

Col→ Row↓	GndH	H	G	GndF	F	E	GndD	D	C	GndB	B	A
10	GNDH10	H10	G10	GNDF10	F10	E10	GNDD10	D10	C10	GNDB10	B10	A10
9	GNDH9	H9	G9	GNDF9	F9	E9	GNDD9	D9	C9	GNDB9	B9	A9
8	GNDH8	H8	G8	GNDF8	F8	E8	GNDD8	D8	C8	GNDB8	B8	A8
7	GNDH7	H7	G7	GNDF7	F7	E7	GNDD7	D7	C7	GNDB7	B7	A7
6	GNDH6	H6	G6	GNDF6	F6	E6	GNDD6	D6	C6	GNDB6	B6	A6
5	GNDH5	H5	G5	GNDF5	F5	E5	GNDD5	D5	C5	GNDB5	B5	A5
4	GNDH4	H4	G4	GNDF4	F4	E4	GNDD4	D4	C4	GNDB4	B4	A4
3	GNDH3	H3	G3	GNDF3	F3	E3	GNDD3	D3	C3	GNDB3	B3	A3
2	GNDH2	H2	G2	GNDF2	F2	E2	GNDD2	D2	C2	GNDB2	B2	A2
1	GNDH1	H1	G1	GNDF1	F1	E1	GNDD1	D1	C1	GNDB1	B1	A1
							20 Pair ADF Connector					
							30 Pair ADF Connector					
							40 Pair ADF Connector					

> MTCA.4 Management

	a	b	c	d	e	f
1	PWR+12V	PWR+12V	PS#	SDA	RTM_TCK	RTM_TDO
2	PWR+12V	PWR+12V	MP+3.3V	SCL	RTM_TDI	RTM_TMS

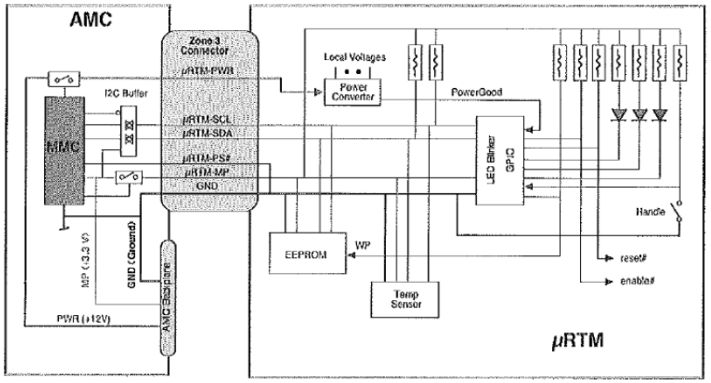

Figure 3-1: Example AMC/µRTM Management Block Diagram

- MTCA.4 inventors assumed allways having complete AMC – RTM pairs.

MTCA.4 : Electrical Protection during RTM Insertion

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> Quiesce Actions:

MicroTCA®

PICMG® Specification MTCA.4

Revision 1.0

3.5.7 Quiesce Actions

¶ 79 Because the Zone 3 Interface is mostly user defined pins, the actions needed to quiesce the Zone 3 Interface can vary greatly from one design to another. In the simplest cases, there might not be any action required. In other cases some or all of the user defined pins may need to be isolated, and in some cases, all or part of the Front AMC might even need to be powered off under MMC control. The specific actions needed are design specific and are beyond the scope of this specification.

→ - AMC isolation
- AMC power off

> RTM insertion process :