Development of a data compressor for the CMS phase II pixel detector

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* Supported by the EU FP7-PEOPLE-2012-ITN project nr 317446, INFIERI, "Intelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry"

About CMS

The Compact Muon Solenoid (CMS) is a general-purpose detector at the Large Hadron Collider (LHC). It has a broad physics programme ranging from studying the Standard Model (including the Higgs boson) to searching for extra dimensions and particles that could make up dark matter.

The CMS detector is built around a huge solenoid magnet. This takes the form of a cylindrical coil of superconducting cable that generates a field of 4 tesla, about 100,000 times the magnetic field of the Earth. The field is confined by a steel "yoke" that forms the bulk of the detector's 14,000-tonne weight.

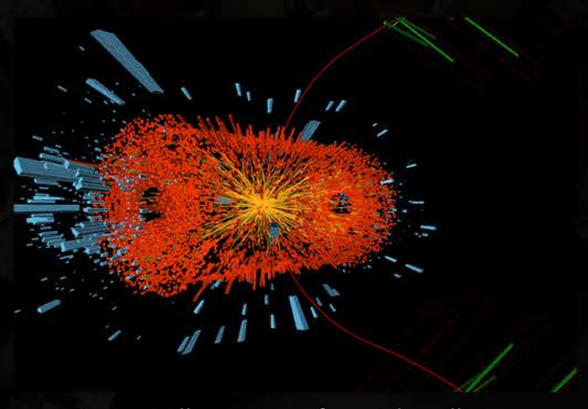

Figure 1. Illustration of particle collisions

Pixel module

- Hit rate estimation for inner barrel layer at 140 Pile-Up is about 2 GHz/cm^2
- Expected high readout rate (~4.8 Gbits/s per chip for 1 MHz trigger rate)
- 2.4 Gbits/s max bandwidth per chip (2 e-links)

It is essential to develop an efficient transfer protocol to collect all measurements and ensure good detector performance. A lossless compression is needed in order to reduce the usage of electrical links without losing any information for every event.

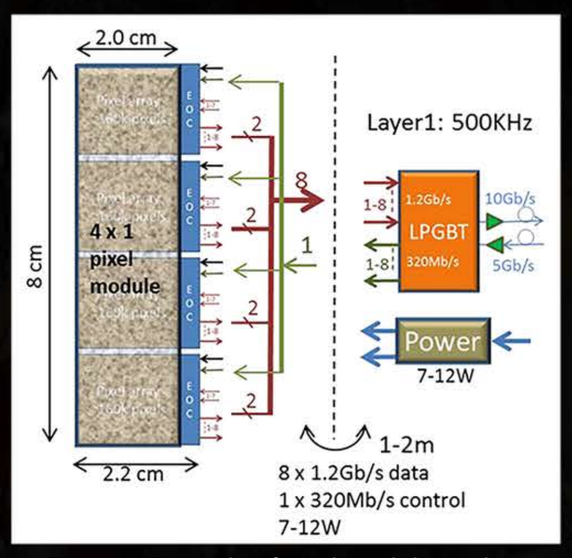

Figure 2. Example of pixel module readout

Arithmetic compression

Arithmetic compression is a form of entropy encoding used in lossless data compression. With this method the more frequently used symbols are stored with less bits, resulting in an overall reduced bitstream in the output. This method was selected because it gives good compression ratios and it has a quite simple implementation.

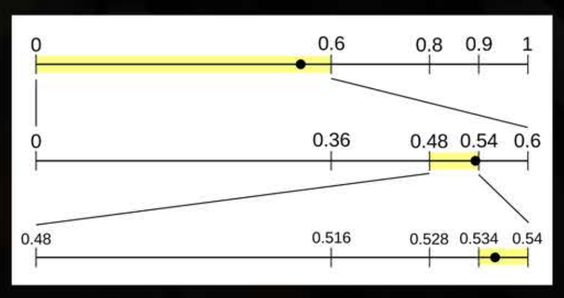

Figure 3. Example of the arithmetic compression algorithm

Objectives

• Development of the data compressor module

- The compressor is developed and tested in VHDL and SystemVerilog
- Simulations in Modelsim verify the functionality of the module

Architecture key points
- Arithmetic compressor
  - Core
  - Memory manager
- Controller
- Input/Output FIFOs

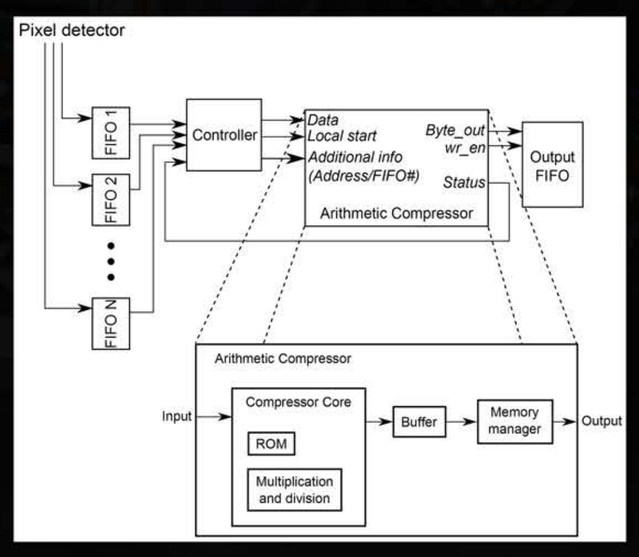

Figure 4. Compressor module architecture

• Investigation of data representation schemes

The efficiency of the compressor is related to the representation method

Delta representation :
- for every active pixel use only the information about the previous active pixels in X and Y directions, instead of the actual coordinates of the active pixel
- with this method we need to compress in parallel three sequences of data for each active pixel:
  * dx
  * dy
  * adc value
- compression ration ~2.1

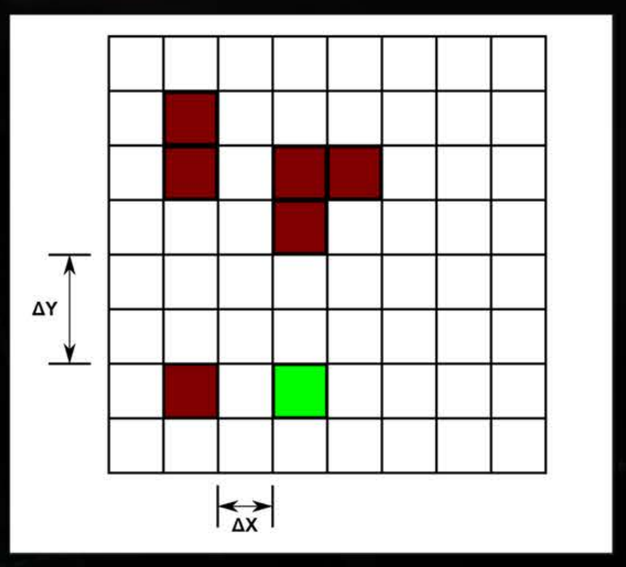

Figure 5. Delta representation

Future work

- Import the compressor to the VEPIX53 simulation and verification framework.
- Calculate power consumption.
- Timing analysis.
- Investigate simpler compression methods as backup.

2012-FP7-ITN-317446 INFIERI

*The research leading to these results has received funding from the People Programme (Marie Curie Actions) of the European Union's Seventh Framework Programme FP7/2007-2013/ under REA grant agreement n° [317446] INFIERI "INtelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry"

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