Development of Coincidence Sorter and Communication Protocol between the Boards on PET System

Eleftheria Kostara[1,3,*], Giancarlo Sportelli[2,3], Emanuele Zaccaro[2], Maria-Giuseppina Bisogni[2,3], Fabrizio Palla[3]

[1] University of Siena, Italy
[2] University of Pisa, Italy
[3] INFN, Sezione di Pisa, Italy

[*] Supported by the EU FP7-PEOPLE-2012-ITN project nr 317446, INFIERI, "Intelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry"

Introduction

Positron Emission Tomography (PET) is a functional imaging technique in nuclear medicine that produces a 3D image of functional processes in the body.

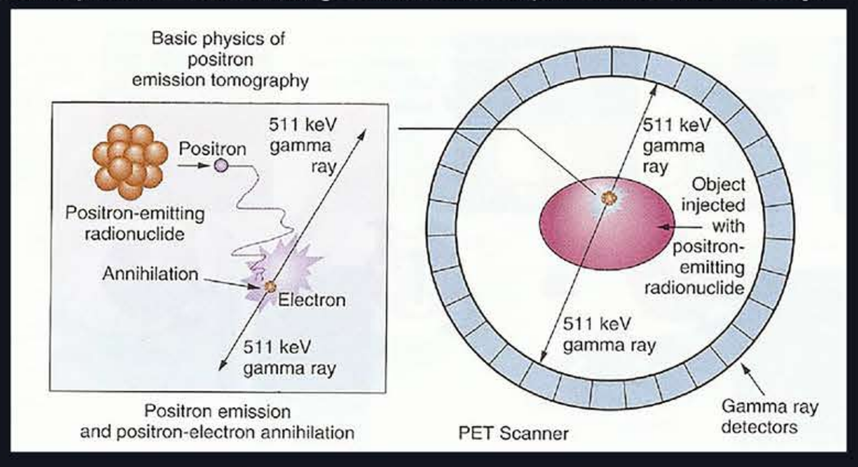


Figure 1. Basics physics on PET.

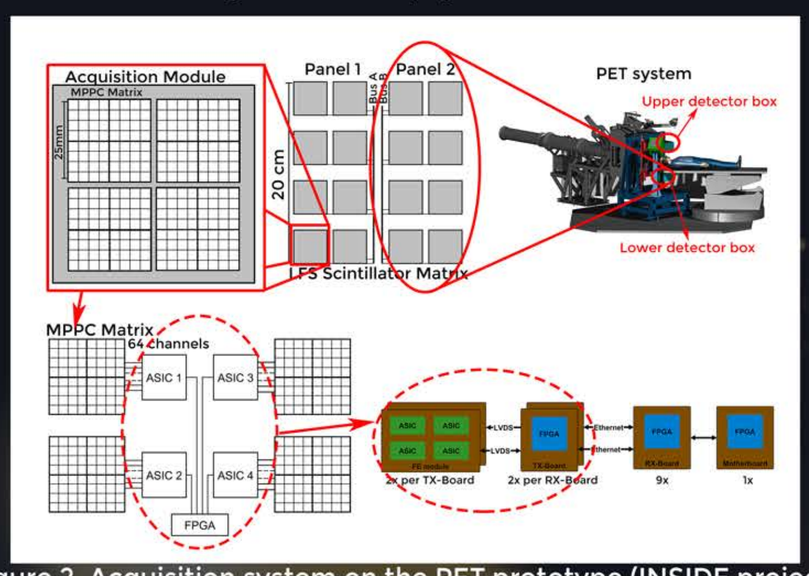


Figure 2. Acquisition system on the PET prototype (INSIDE project).

Objectives:

1 Sorter implementation for real time coincidence detection.

Specifications of the sorter:

- Cyclone V
- 20MHZ minimum throughput rate (system clock 200MHz)
- implementation on the DAQ board of an in-beam PET system for the INSIDE project

2 Communication protocol between the Host PC and the TX-Boards in order to configure the ASICs that are connected to the TX-Boards.

- 8 bytes of data for the ASIC configuration
- 2 bytes of data for the target RX-Board and the target TX-Board

Sorter Implementation

The proposed solution for the sorter is a pipelined architecture. The sorter compares the timestamps of the events and outputs the earliest one. The data packet with the earliest timestamp is stored to an output FIFO through a multiplexer.

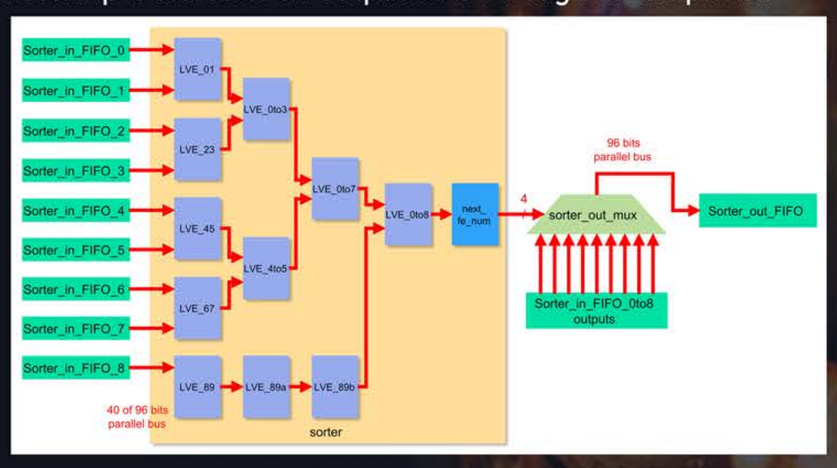


Figure 3. Architecture of the event sorter.

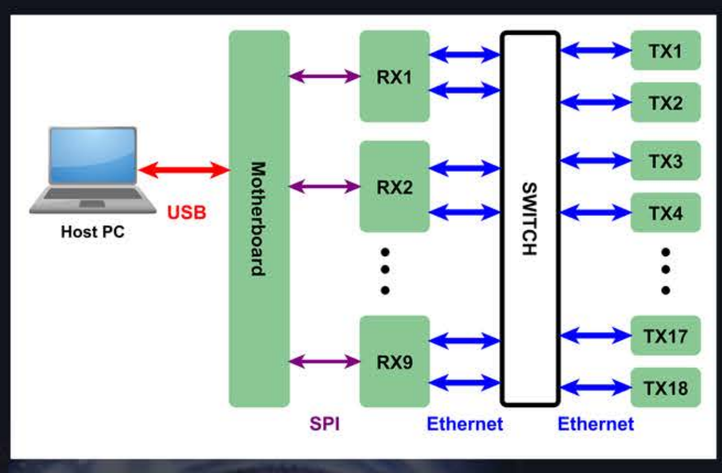
Table I. Data packet coming from the FE-Boards.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W0	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
W1	Detector ID						Crystal ID									
W2	E3	E2	E1	E0	Energy											
W3	Timestamp MSB															
W4	Timestamp LSB															
W5	Energy ID										Timestamp Fraction					

Table II. Proposed form of the input bits of the sorter.

1 bit	4 bits	40 bits
Valid Data	FE number	Timestamp

Communication protocol from Host PC to TX-Boards



Communication paths:

Host PC ⟷ MB: *USB*

MB ⟷ RX-Boards: *SPI*

RX ⟷ TX: *Ethernet*

Figure 4. Communication schematic from Host PC to the TX-Boards.

The data, coming from the Host PC, goes to the Configuration Parallel Access Memory Bank (pambank) (64-registers x 16-bits). The USB controller triggers the Dispatcher, which takes as input 6 registers from the pambank. The data transfer starts. The data stored in the pambank thus go from the motherboard to the RX-Boards through the SPI interface. Once the data are in the RX-Boards, they are routed to the proper TX-Board according to the address stored in the packet itself.

Once the ASIC configuration is completed, each TX-board sends the packet back to the motherboard through the proper RX-board. The data packet then goes through the SPI interface to the Dispatcher and the Dispatcher sends the data packet to 6 registers of the Status pambank. The Host PC through the USB can request these data.

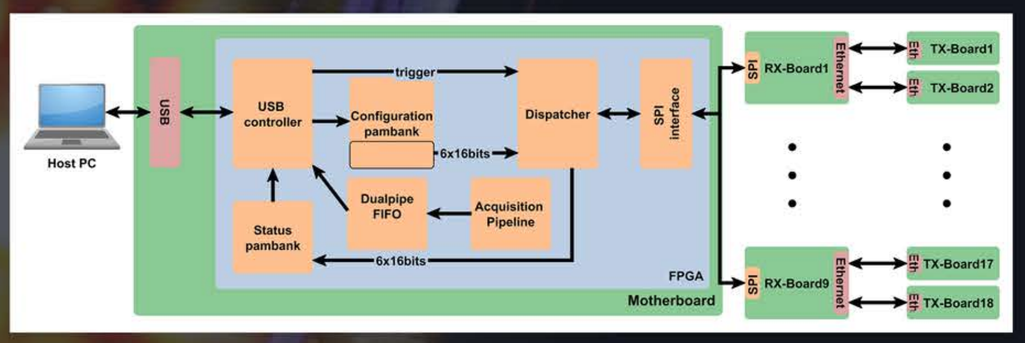


Figure 5. Host PC and motherboard communication using USB.

Table III. Words of the communication protocol for the ASIC configuration.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W0	RX_ID								TX_ID							
W1-4	DATA															
W5	T_ID															

Results

Sorter:

- The testbench was implemented and tested using ModelSim
- 28MHz throughput rate

Communication protocol:

Communication between:

- Host PC and MB through USB ✓
- MB and a prototype of the RX-Board ✓
- Host PC and a prototype of the RX-Board ✓

* The research leading to these results has received funding from the People Programme (Marie Curie Actions) of the European Union's Seventh Framework Programme FP7/2007-2013/ under REA grant agreement n° [317446] INFIERI, "Intelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry"