Advances in high-speed data converters

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The world yesterday

Historical radar

Aerospace & defense

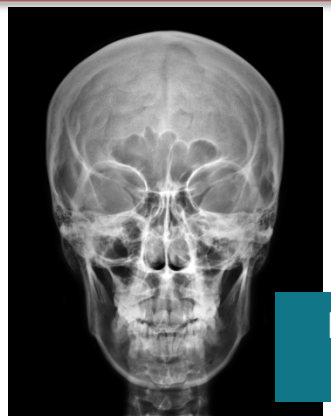
Test equipment (prior to 1990)

Wireless communications

Test & measurement

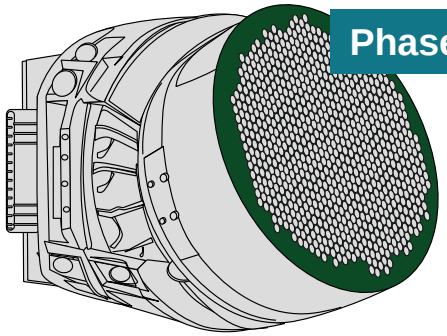
Mobile phone (1990s)

Medical instruments



Karl Dussik's apparatus for scanning the head (1940)

The world today



Phased array radar

Wireless broadband

Portable test equipment

Aerospace & defense

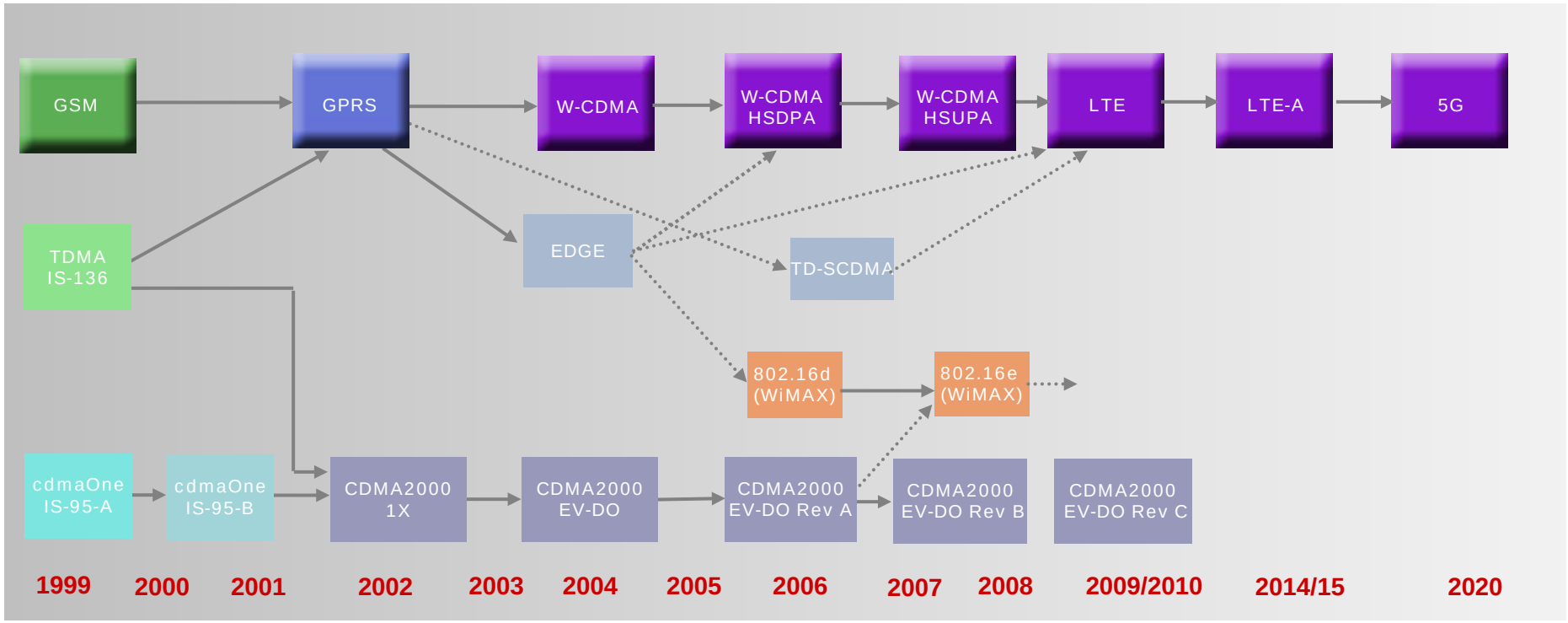
Wireless communications

Test & measurement

Medical instruments

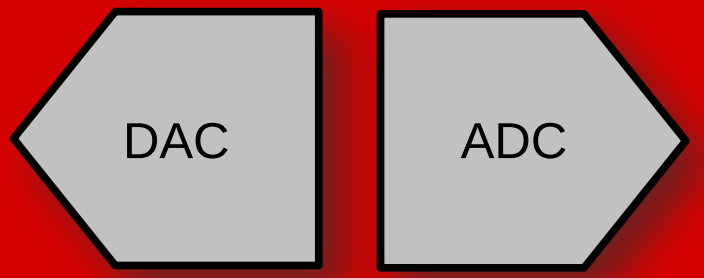
Portable ultrasound scanners

The wireless broadband revolution



Carrier bandwidth	200kHz	n*200kHz	3.84MHz	n*3.84MHz	20MHz	n*20MHz	n*250MHz
Peak Data rates	9.6kbps	384kbps	2Mbps	21Mbps	84Mbps	150Mbps	>1Gbps

What would the ideal data converter be like

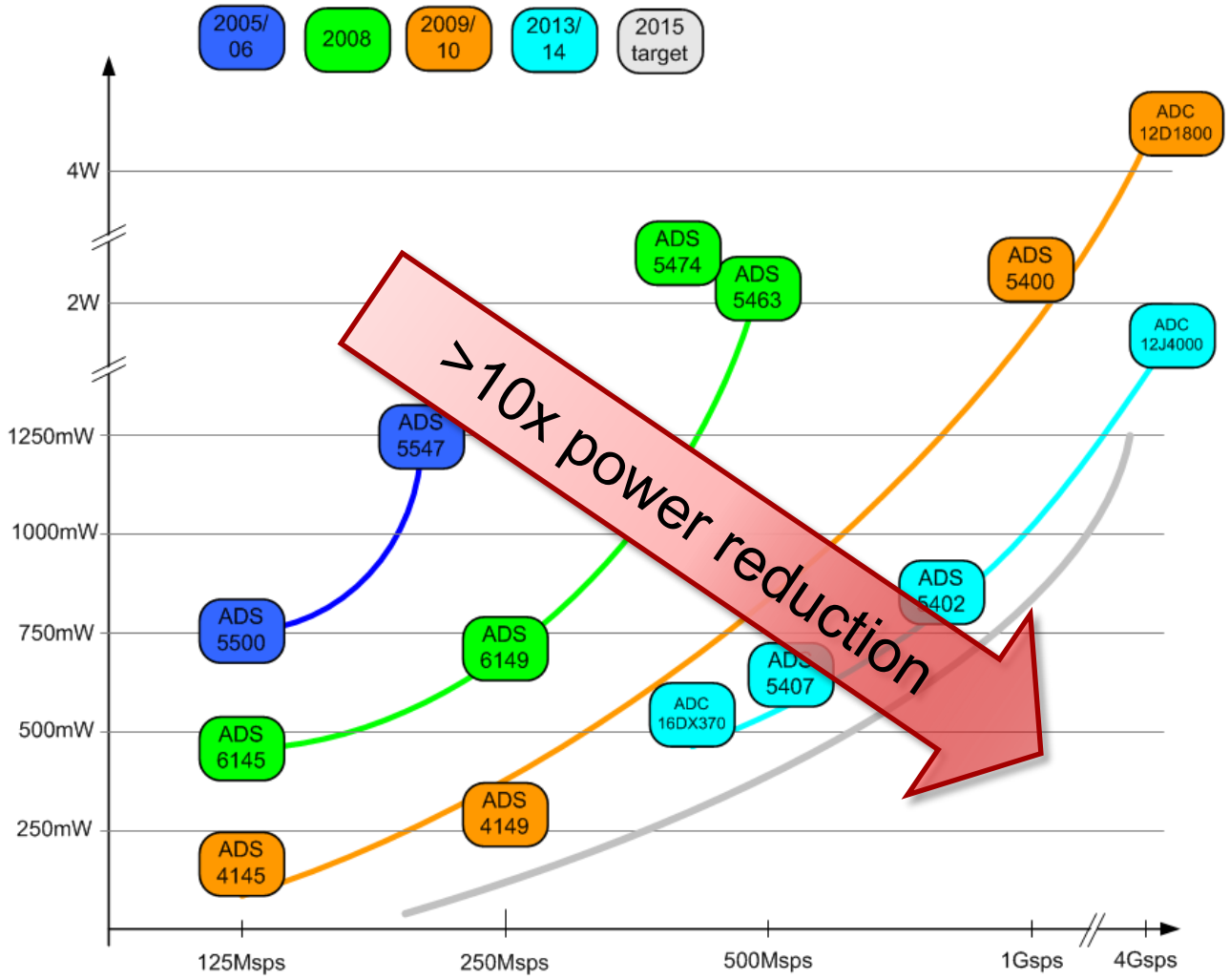


- Infinite analog bandwidth
- Infinite sample rate
- Unlimited dynamic range
- Unlimited interface throughput
- Zero power
- Zero footprint

----> Will we get it any time soon?

The last decade

Radical improvement in ADC power consumption

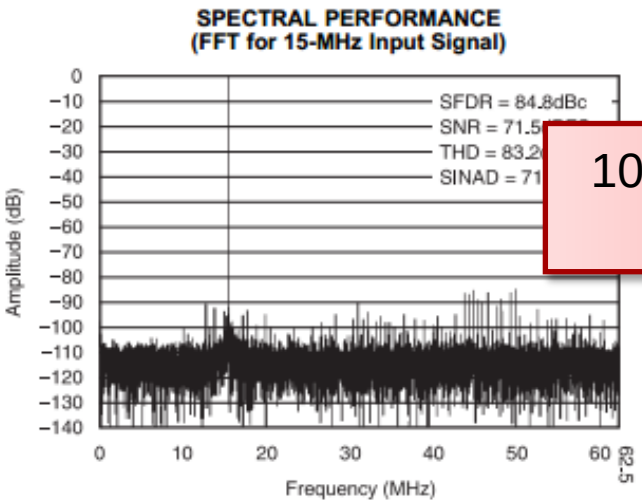


The last decade

Radical improvement in ADC dynamic performance

ADS5500 in 2003

14-bit, 125-MSPS ADC



10 .. 20dB improved dynamic range

ADS42JB49 in 2013

14-bit, 250-MSPS ADC

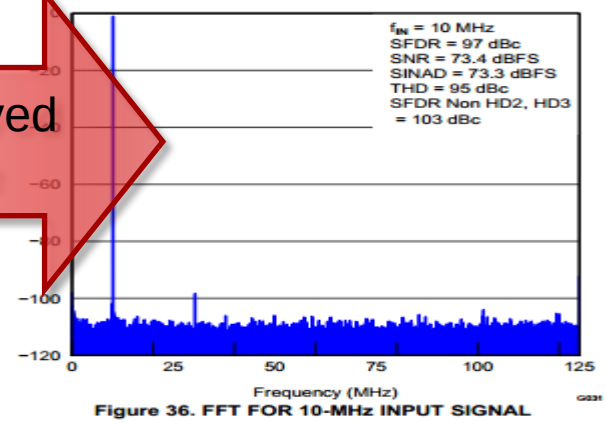
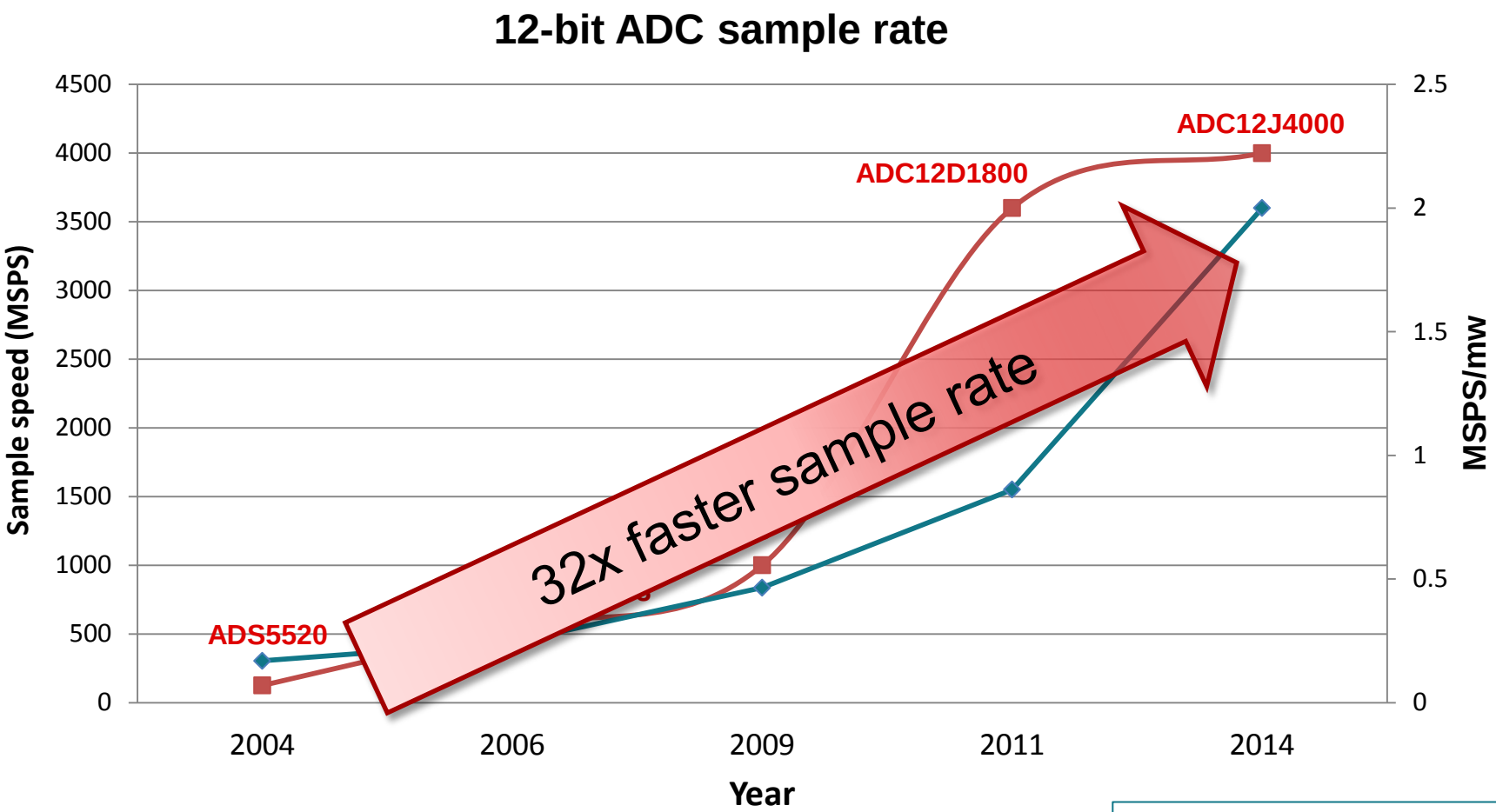


Figure 36. FFT FOR 10-MHz INPUT SIGNAL

The last decade

Radical improvement in ADC sample rate

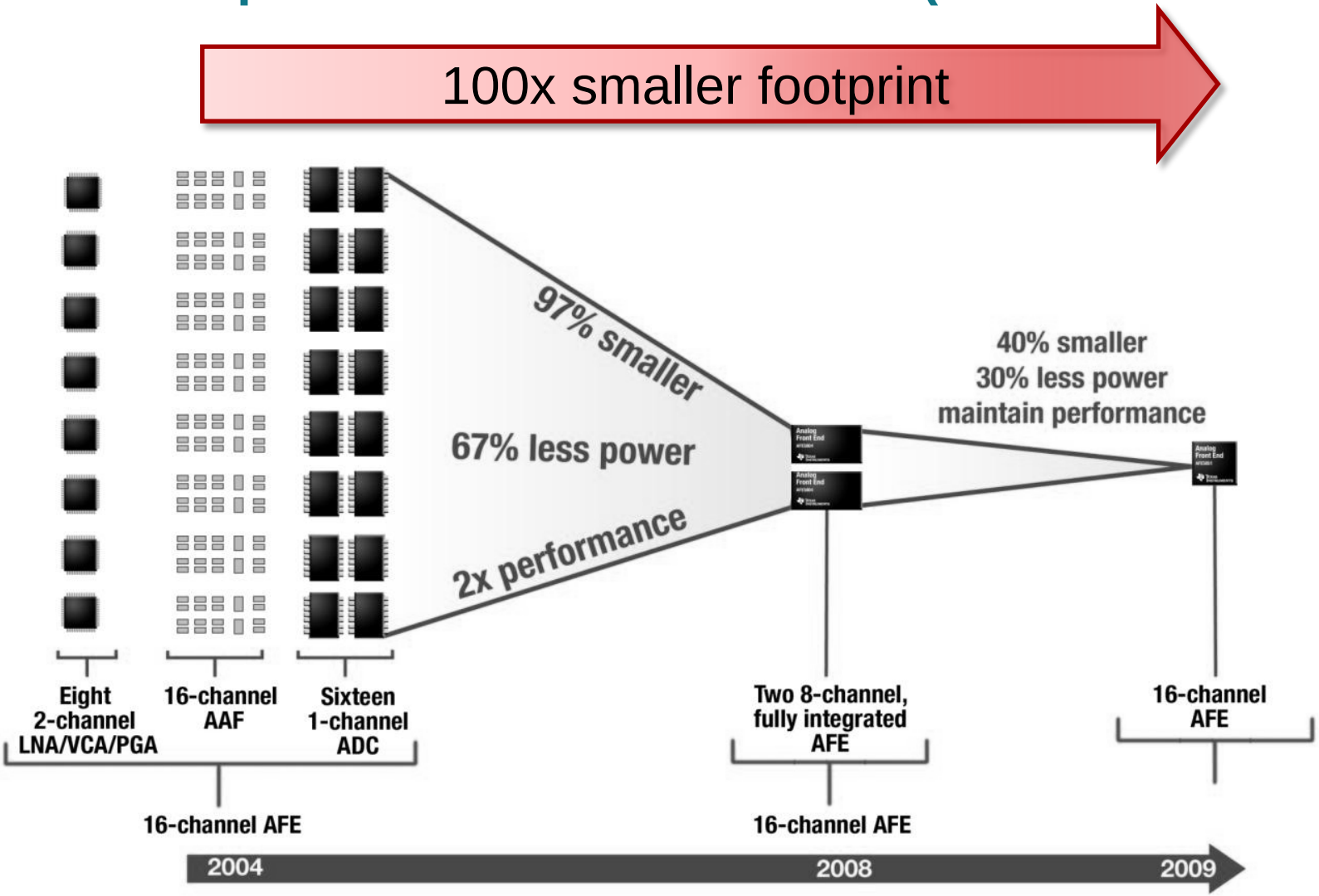


Bandwidth = 32x increase
Power[1] = 13x reduction

Note 1: MSPS/mw

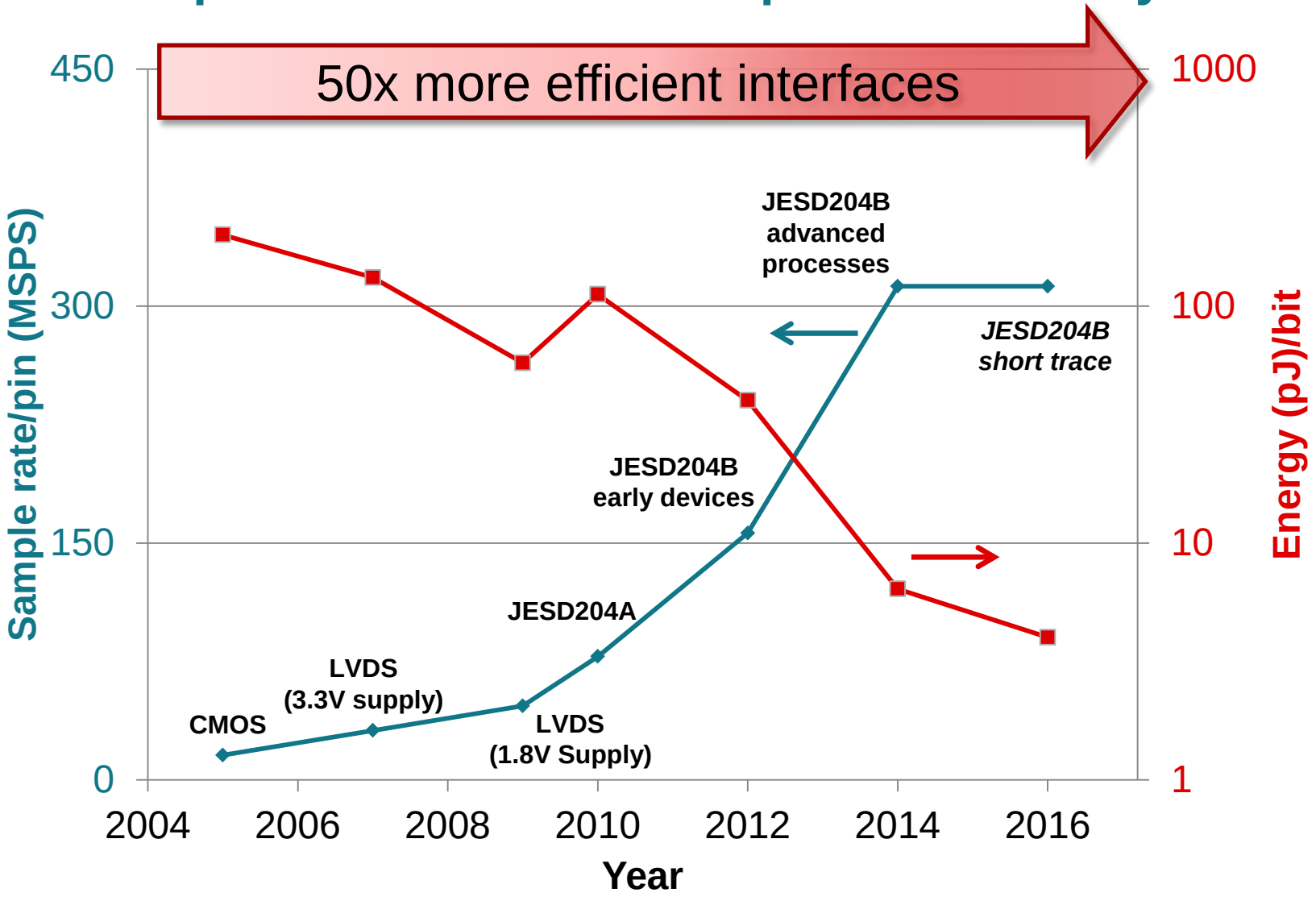
The last decade

Radical improvement in solution size (ultrasound frontend)



The last decade

Radical improvement in interface power efficiency



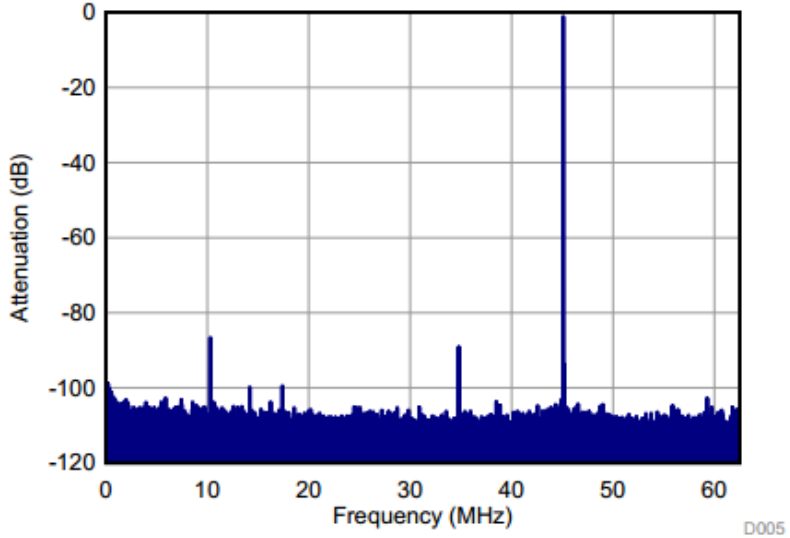
The last decade in summary

	HS ADC: 14 bit	HS ADC: 12 bit	HS DAC
Size, 1 channel equivalent	7x	3x	5x
Power (MSPS/mw), 1 channel equivalent (reduction)	5x[1]	13x	6x
Bandwidth	8x	32x	16x
Interface pins/channel (reduction)	6x	7x	8x

Note 1: Comparison between ADS5500 and ADS4125

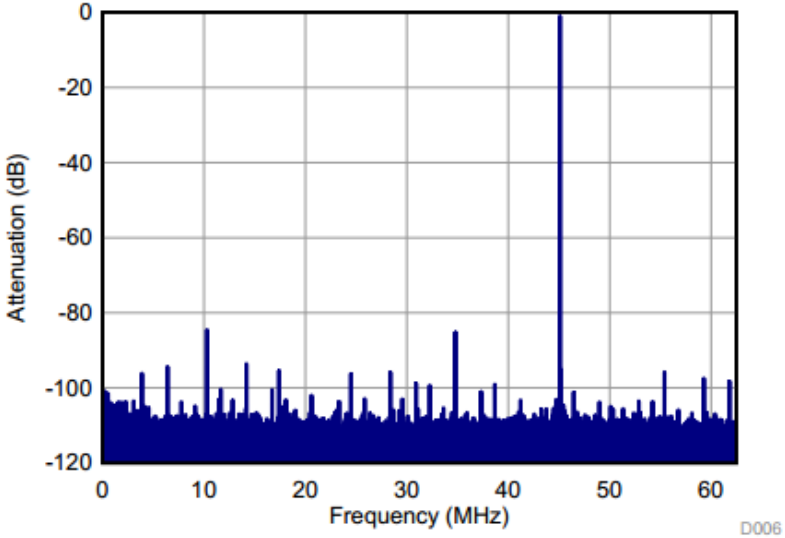
Enabling technologies
Dither removes harmonic distortion

ADC3244 with programmable dither



f_S = 125 MSPS SNR = 71.3 dBFS
f_{IN} = 170 MHz SFDR = 85 dBc

Figure 5. FFT with Dither On

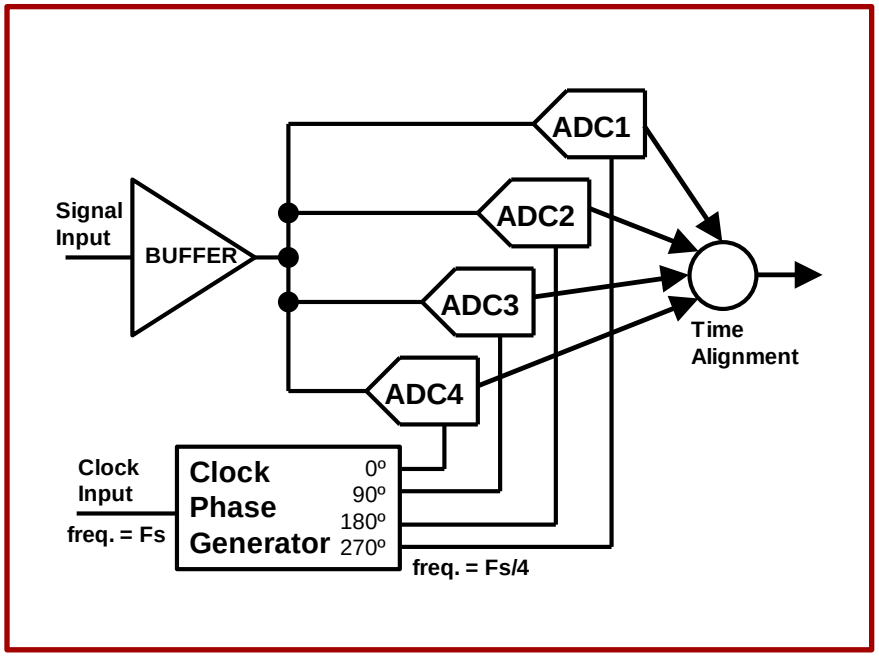


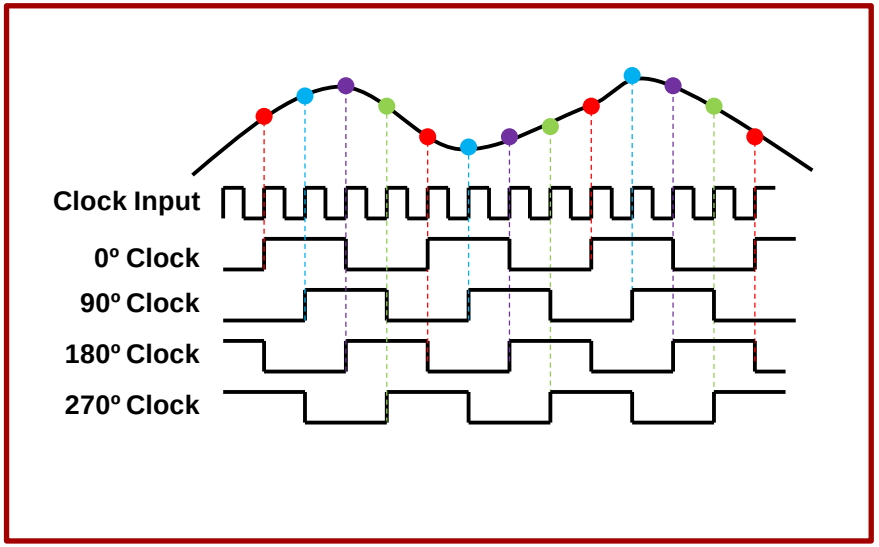
f_S = 125 MSPS SNR = 71.9 dBFS
f_{IN} = 170 MHz SFDR = 84 dBc

Figure 6. FFT with Dither Off

Enabling technologies

Interleaving extends maximum sample rate





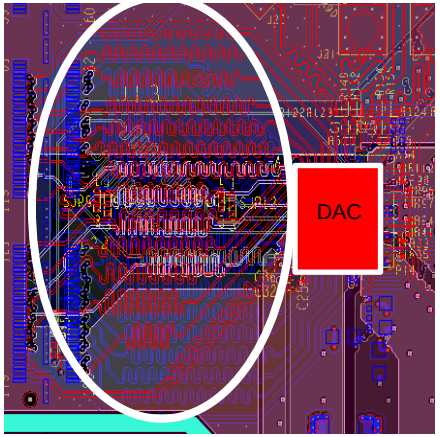
Enabling technologies

JESD204B SerDes interface

DAC34SH84
(LVDS Interface)
2011

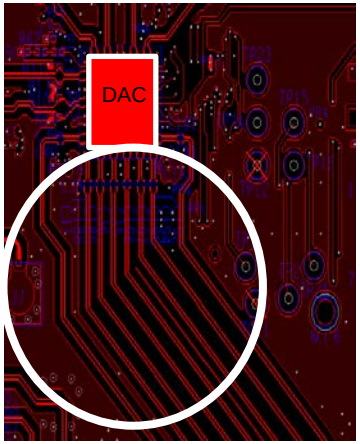
4ch
750 MSPS
input

32 lanes
aggregate
48Gbps
input data



'Squiggles' to match timing of LVDS bus lines

DAC38J84
(JESD204B Interface)
2014



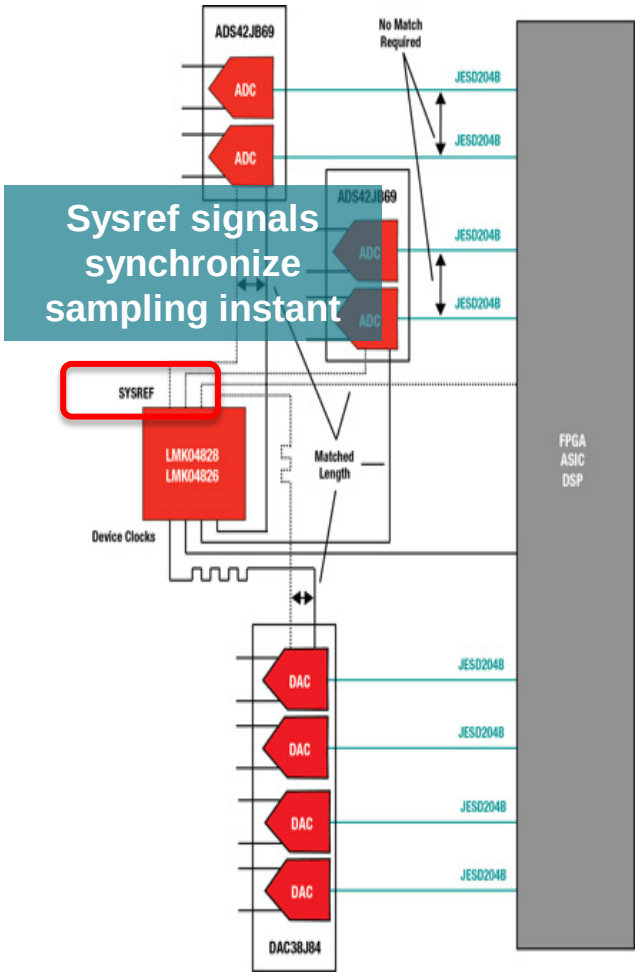
4ch
1.25 GSPS
input

8 lanes
Aggregate
100Gbps
input data

JESD204B bus lines with uncritical timing requirements

Embedded JESD204B synchronization

Latency deterministic, but need to manage overall latency



Sysref signals synchronize sampling instant

Elastic buffers ensure deterministic latency across lanes

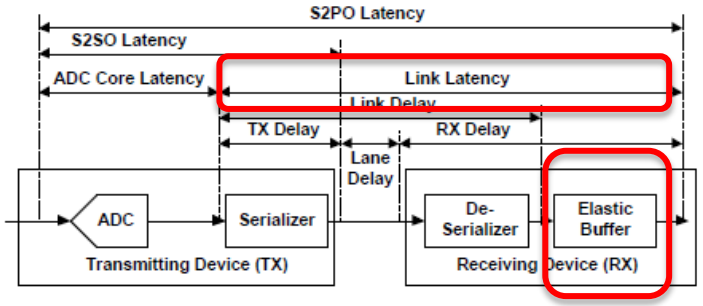


Figure 2. Block Diagram of Simplified Latencies in a System Using the LM97937

Where do we go from here?

Predictions for the next decade

Yr 2003 -> Yr 2013	HS ADC: 14 bit	HS ADC: 12 bit	HS DAC
Size	7x	3x	5x
Power	5x[1]	13x	6x
Bandwidth	8x	32x	16x

Yr = 2023

- 16 bit, 40 GSPS
- BW = 16G BW
- 20mW DAC cores

Yr = 2023

- 14 bit, 8 GSPS
- 350 mW ADC cores

Yr = 2023

- 12 bit, 128 GSPS
- 138 mW ADC cores

Will it happen?

What new applications will this enable?