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An MTCA White Rabbit Timing Receiver for FAIR

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Abstract content

The FAIR facility involves a long chain of accelerators which need to be tightly synchronized. This is achieved by using by using a timing system based on White Rabbit (WR). FAIR Timing Receiver Nodes (FTRNs) are part of the FAIR General Machine Timing System. FTRNs receive and decode broadcasted network messages in real time.

One of the form factors to be used in the facility will be the MTCA platform, therefore a WR timing receiver module had to be developed for it. The card format is a Single-Width Mid- Height AMC, and it is based on the Altera ARRIA V FPGA for the main functionality. The MMC was implemented using a NXP LPC2136 microcontroller.

Since the FAIR facility will also use the i-Tech Libera Platform B, the White Rabbit timing receiver card was designed to be compliant with this platform. The MMC firmware development was based on the Open Source coreIPM management architecture and the FreeRTOS operating system. Besides the standard functionality defined by the PICMG specification, the MMC must support a series of custom commands that allow it to fit either into an MTCA.0 or a Libera B system.

Summary

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