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Progress on MMC V1.00
Management Controller for MTCA.4
Hamburg, 11.12.2014
Introduction

➢ Agenda:
  ▪ Repetition of MMC features
  ▪ Improvements in 2014
  ▪ Demonstration

➢ DESY MMC V1.0 is a set of hardware and software building blocks, created by DESY and its partners

➢ Management is the most difficult part, almost all interoperability issues are based on management

➢ Idea: Create one proven feature-rich standard solution and share it with the partners

➢ Bases on Atmel ATxmega128A1

➢ Over 5 man-years of design work put into it

➢ Great improvements during the last year
Overview of Building Blocks – Starter Kit

Commonly used Blocks

> IPMI Communication
  - Intensively tested with NAT and Vadatech

> Power Management
  - Sequencing and safety shutdown

> FPGA Management
  - DONE, INIT, PROG, RESET over IPMI

> HPM.1 MMC and FPGA upgrade
  - Redundant SPI Flashes

> RTM Management
  - RTM Inrush current control
  - Temperature, voltage and current monitoring

> CPLD for JTAG and Flash Control (optional!)
  - Allows to program “dead board”; Redundant Flash selection

> Debug UART

> PMBUS control
Progress

State of Last Year: “Basic” functionality (Development Version)

- IPMI Communication
- Power Management, Temperature Monitoring
- FPGA Management
- Static CPLD for JTAG and Flash Control
- AMC FRU generator

Great Improvements in 2014 (25.000 lines of code added)

- Architecture change: Full separation IPMI/user logic
- Vadatech compatibility: IW25, IW26
- HPM.1 Support (8KB Boot loader) → MMC, SPI
- MMC and CPLD register control with IPMItool
- Temperature Events (Fan speed increase)
- Automation tools (program.bat, bin2hpm)
Reference Customers

- DESY MMC V1.00 is running on DESY Boards
  - DAMC-FMC20, DAMC-FMC25, DAMC-TCK7
- In 2014 we won partners – very good feedback
  - CAENels
  - Michigan State University
  - NRF Korea
  - Micro-Research Finland
  - Interface Concept
  - In negotiation with SLAC
- Success story: Struck SIS8300L2
  - Spend two days together for MMC schematic change
  - Spend one day for Code-Porting
  - Full set of new features: Remote MMC and Flash Upgrade, redundant FPGA Flash Memories, RTM inrush current control, Temperature Alerts, FPGA and RTM supervision
Demonstration

- Sensor Information
- HPM file generation
- IPMI Upgrade
- Production Programming
Bin2hpm – in Bitfile mode

D:bin2hpm llrf_ctrl_sis8300l_acc1_r908.bit /bit /compress
BIN-to-HPM file converter. Version: 1.0
Written by Michael Fenner (C) DESY 2014;
with compression based on UPackBits (C) Michael Dipperstein (LGPL) and
with MD5 algorithm from Alexander Peslyak (public domain)

Reading file : llrf_ctrl_sis8300l_acc1_r908.bit
File Length is : 5465076 bytes
Bit File mode. Header check ok.
a-Section detected. Design info : ENT_SIS8300L_TOP.ncd;UserID=0xFFFFFFFF
b-Section detected. Part name : 6v1x130tff1156
c-Section detected. File date : 2014/11/27
d-Section detected. File time : 01:58:26
e-Section detected. Image size : 0x0053638C (5336KB)
BIT header sucessfully parsed.
Generating HPM header...
Device ID : 0x00
Manufacturer ID : 0x000000
Product ID : 0x0000
Time value : 0x54886D64
Component ID : 0x01
Firmware revision : 0x0000
Firmware revision auxiliary information : 0x00000000
Generating header checksum : 0xF0
Generating upgrade action checksum (prepare) : 0xFE
Generating upgrade action checksum (upload) : 0xFD
Information: Output will be compressed with RLE
Reading 5464972 Bytes from file...
Largest RLE block is : 128 bytes
Compression Ratio is : 32.9%
16-bit Checksum of data is : 0xBD03.
Begin of data stream is : 9EFFB10004BB1122004486FF04AA995566208100...
End of data stream is : 0020810002200000020810000208100022000000.
Testing MD5 checksum : E5546C065678FBBF39EC2CC5FC2F8F32A
Output data length is : 1796463 bytes
Overhead {header+MD5} size is : 99 bytes
Writing file : llrf_ctrl_sis8300l_acc1_r908.rle.hpm
Bytes actually written : 1796463
All done.
Demonstration

PICMG HPM.1 Upgrade agent 1.0.2:

-------Target Information-------
Device Id : 0x0
Device Revision : 0x50
Product Id : 0x0002
Manufacturer Id : 0x053f (Unknown (0x53F))

<table>
<thead>
<tr>
<th>ID</th>
<th>Name</th>
<th>Versions</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>NMCV100 HPM</td>
<td>2.00</td>
<td></td>
</tr>
</tbody>
</table>

mskcpuhvfi@mskcpuhvfi:~$ ipmitool -H mskmchhvf1 -P "" -t 0x76 hpm upgrade SIS8300L2.hpm

PICMG HPM.1 Upgrade agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...OK

Performing upgrade stage:

<table>
<thead>
<tr>
<th>ID</th>
<th>Name</th>
<th>Versions</th>
<th>Upload Progress</th>
<th>Upload</th>
<th>Image</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>NMCV100 HPM</td>
<td>2.00</td>
<td>0%</td>
<td>50%</td>
<td>100%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:01</td>
<td>...........</td>
<td>00:33</td>
</tr>
</tbody>
</table>

Firmware upgrade procedure successful
<table>
<thead>
<tr>
<th>#</th>
<th>SDRTy</th>
<th>Sensor Entity</th>
<th>Inst</th>
<th>Value</th>
<th>State</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>MDevLoc</td>
<td>0xc1 0x65</td>
<td></td>
<td></td>
<td></td>
<td>SIS8300L2 AMC</td>
</tr>
<tr>
<td>0</td>
<td>Full</td>
<td>0xf2 0xc1 0x65</td>
<td>0x01</td>
<td></td>
<td>Hot Swap</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Full</td>
<td>Voltage 0xc1 0x65</td>
<td>12.1 V</td>
<td>ok</td>
<td>12V PP</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Full</td>
<td>Voltage 0xc1 0x65</td>
<td>3.30 V</td>
<td>ok</td>
<td>3.3V MP</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Full</td>
<td>Voltage 0xc1 0x65</td>
<td>0.97 V</td>
<td>ok</td>
<td>1.0V CORE</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Full</td>
<td>Voltage 0xc1 0x65</td>
<td>2.48 V</td>
<td>ok</td>
<td>2.5V</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Full</td>
<td>Voltage 0xc1 0x65</td>
<td>1.80 V</td>
<td>ok</td>
<td>1.8V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Full</td>
<td>Voltage 0xc1 0x65</td>
<td>1.49 V</td>
<td>ok</td>
<td>1.5V DDR3</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Full</td>
<td>Current 0xc1 0x65</td>
<td>0.240 A</td>
<td>ok</td>
<td>RTM PP Current</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Full</td>
<td>Current 0xc1 0x65</td>
<td>0.017 A</td>
<td>ok</td>
<td>RTM MP Current</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Full</td>
<td>Temp   0xc1 0x65</td>
<td>35.5 C</td>
<td>ok</td>
<td>Inlet</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Full</td>
<td>Temp   0xc1 0x65</td>
<td>39.5 C</td>
<td>ok</td>
<td>Outlet</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Full</td>
<td>Temp   0xc1 0x65</td>
<td>47.0 C</td>
<td>ok</td>
<td>Middle</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Full</td>
<td>Temp   0xc1 0x65</td>
<td>40.0 C</td>
<td>ok</td>
<td>FPGA PCB</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Full</td>
<td>Temp   0xc1 0x65</td>
<td>49.0 C</td>
<td>ok</td>
<td>FPGA DIE</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Compact</td>
<td>0x0b 0xc1 0x65</td>
<td>0x00</td>
<td>0x00</td>
<td>FPGA Done</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Compact</td>
<td>0x0b 0xc1 0x65</td>
<td>0x00</td>
<td>0x00</td>
<td>FPGA Init</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Compact</td>
<td>0x0b 0xc1 0x65</td>
<td>0x00</td>
<td>0x00</td>
<td>RTM OC Fault</td>
<td></td>
</tr>
</tbody>
</table>

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nat> SEL: 1970/01/01 01:40:00 alive
Licensing

- Licensor needs to sign an NDA and a Software License Agreement
- Free of Charge for collaboration projects
- Licensing Items
  - Altium Designer Files as Templates for AMC and RTM
  - C Source Code
  - AMC FRU Generator
  - Command-Line HPM Generator