Firmware design using RapidX

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Quick Refresher

- Simulink/System Generator-based toolset for firmware development
- Easy VHDL-less development for non-experts
- Simulink-powered simulation of designed algorithms
- Support for most commonly used MTCA boards
- Integration with existing VHDL framework
Hardware support

- Supported AMC boards
  - SIS8300
  - SIS8300L
  - FMC25

- Supported RTMs
  - DWC10
  - SIS8900
  - AD84 (partially)
  - PZT4

- Supported FMCs
  - MD22
  - AD16
  - LASIO
Software support

- Integration with automatic project creation / build tools used by the VHDL framework

- Automatic generation of initialization Matlab scripts

- Automatic generation of ‘mapp’-compatible map files

- Backup copies of RapidX project

- Automatic deployment to remote MTCA CPUs
Recent improvements

- Structures in place to support FMC/RTM modules
- More stable Low Latency Links
- Improved DAQ Module implementation
  - More channels for slower clock
- Function block
  - Read-only BRAM memory with function values
  - Calculated in Matlab and automatically initialized
- Trigger parameters
  - Change value only for one clock cycle
- Many smaller and bigger improvements
  - Over 60 Redmine tasks closed
Ongoing developments

➤ Michael Heuer – link locking firmware
➤ …
➤ …
➤ Tomasz Kozak – switched back to VHDL (traitor 😞)
➤ …
➤ …
➤ Ewa Janas – interested but overwhelmed 😊
What next?

➢ Continue support for RTM / FMC modules
➢ More users to help debug and improve the toolset
➢ Integrate more closely with the MTCA4U software
➢ Include SHAPI register support
➢ Improve the functionality, deal with ever-appearing bugs
➢ Finalize at least one project – link locking firmware + software

Thank you for your attention