HZDE LLRF status report

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10.06.2015
Outline

1. ELBE
2. Status
3. Recent developments
   - 260 MHz Buncher
   - Real-time BLC
4. Plans for future
   - Hardware
   - Software / Firmware
   - Installation
ELBE Status

Recent developments

Plans for future

Igor Rutkowski
HZDE LLRF status report
Layout of ELBE

Source: Peter Michel "ELBE Upgrade", ARD Workshop February 2013
(Almost) Done

System
- Closed loop operation verified

Hardware
- Power supply
- MCH / CPU
- SIS8300L2 (digitizer+controller)
- DRTM-DWC8VM1

Firmware
- DRTM-DWC8VM1 BSP
- SIS8300L2 BSP (minor changes expected)
- Controller application (minor changes expected)
1 ELBE

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   Real-time BLC

4 Plans for future
Results: phase noise

<table>
<thead>
<tr>
<th>Frequency Offset [Hz]</th>
<th>Phase Noise [dBc/Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10^1</td>
<td>-180</td>
</tr>
<tr>
<td>10^2</td>
<td>-160</td>
</tr>
<tr>
<td>10^3</td>
<td>-140</td>
</tr>
<tr>
<td>10^4</td>
<td>-120</td>
</tr>
<tr>
<td>10^5</td>
<td>-100</td>
</tr>
<tr>
<td>10^6</td>
<td>-80</td>
</tr>
<tr>
<td>10^7</td>
<td>-60</td>
</tr>
</tbody>
</table>

- **P gain: 0.5 I gain: 1024**
- **P gain: 0 I gain: 0**
- **260 MHz Reference**
260 MHz Buncher

Results: drifts

![Graph showing phase drifts over time](image-url)
Control loop react (with a delay) to sudden drop in the gradient. Proportional controller suppresses the error, but not perfectly. Integral controller cannot have doubling time short enough.
Real-time BLC

Idea

E. Vogel, et al. "Beam loading compensation using real time bunch charge information from toroid monitor at FLASH" (PAC 07)
Real-time BLC

Results: BLC (Gain = 30)
Real-time BLC

Results: BLC (Gain = 90)
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## ELBE Status

### Hardware

**Awaiting new revision**
- DRTM-DS8VM1

**Must be build**
- LO Generation Module (UNILOGM)
- Reference distribution box

**Needs implementation**
- Timing / Interlock module
## Firmware
- A BSP for the DRTM-DS8VM1 must be implemented.
- Access to the source code must granted by Holger Schlarb.

## Software
- API specification from Martin Killenberg.
- Adaptor to be developed for HZDR.
Rack occupation
A drawing should be prepared.

Cabling
To be done after the LO Generation and Reference distribution modules are build. Low drift cables prefered.

Training
HZDR’s stuff must be trained.
Questions
Thank You for attention!
**DRTM-DS8VM1**

Designed for direct sampling of low frequency signals
2nd revision (major changes)

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**Block diagram**

[Diagram of DRTM-DS8VM1 block diagram showing components such as Power Supply, MMC, Digital Control, Clock generation and distribution, Vector Modulator, and Baseband.]