

## **Introductory Tutorial To New Automata Processors**

Micron's introduction of the Automata Processor (AP) contributes a new hardware accelerator at a time when interest in hardware acceleration is on the rise, due to challenges in scaling performance with only conventional, general-purpose cores. Accelerators allow greater performance per watt, breaking through scaling and power constraints, at the cost of less generality. Many predict that heterogeneous systems will be necessary to maintain effective performance growth.

The AP chips per se provide native-hardware implementation of non-deterministic finite automata (NFAs), with 49K state elements per chip and a rich, reconfigurable activation network (one state can active over 2K successor states). This already provides substantial acceleration on complex regular expressions. The AP chips also add a large number of counters and Boolean elements, allowing them to accelerate tasks that do not map to NFAs. The resulting architecture has already shown speedups of 10X to more than 1000x on diverse applications.

This tutorial will cover the architecture, programming of the AP, and arouses research opportunities associated with the AP.